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Fully Digital Arrays of Silicon Photomultipliers (dSiPM) – a Scalable Alternative to Vacuum Photomultiplier Tubes (PMT)

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Abstract

Silicon Photomultipliers (SiPMs) have emerged as promising alternative to fast vacuum photomultiplier tubes (PMT). A fully digital implementation of the Silicon Photomultiplier (dSiPM) has been developed in order to overcome the deficiencies and limitations of the so far only analog SiPMs (aSiPMs). Our sensor is based on arrays of single photon avalanche photodiodes (SPADs) integrated in a standard CMOS process. Photons are detected directly by sensing the voltage at the SPAD anode using a dedicated cell electronics block next to each diode. This block also contains active quenching and recharge circuits as well as a one bit memory for the selective inhibit of detector cells. A balanced trigger network is used to propagate the trigger signal from all cells to the integrated time-to-digital converter. In consequence, photons are detected and counted as digital signals, thus making the sensor less susceptible to temperature variations and electronic noise. The integration with CMOS logic provides the added benefit of low power consumption and possible integration of data post-processing directly in the sensor.
In this overview paper, we discuss the sensor architecture together with its characteristics with a focus on scalability and practicability aspects for applications in medical imaging, high energy- and astrophysics.

Keywords: SiPM; digital SiPM (dSiPM); single photon detection, timing resolution, energy resolution, Čerenkov, scalability

1. Introduction

Recently, Silicon Photomultipliers (SiPMs) gained interest as a potential candidate to replace photomultiplier tubes (PMT) in several applications for reasons of ruggedness, compactness and insensitivity to magnetic fields [1]. Other advantages of solid state detectors in general are their relatively

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low operating voltage, low power consumption and large scale fabrication possibilities. Today, silicon photomultipliers almost exclusively operate in an analog way. The passively-quenched Geiger-mode cells of the SiPM are connected in parallel through long interconnects, and the resulting output signal is therefore the analog sum of the individual currents of all cells. Hereby, the good intrinsic performance of the SPAD is not fully utilized, as the generated signal is deteriorated by the parasitic capacitances of the on-chip interconnect, the bond wires and the external load. From a system perspective, large scale applications of analog silicon photomultipliers imply some design challenges: In systems comprising several tens of thousands of channels, dedicated readout chips are needed to condition and digitize the SiPM signals. As the single photon response is still in the mV range, the signals can be easily affected by electronic noise or unstable baseline due to high dark count levels, thus making single photon detection difficult. A typical single-channel sensor/readout system for the detection of scintillation light based on the analog silicon photomultiplier (aSiPM) is shown in fig. 1 (left).

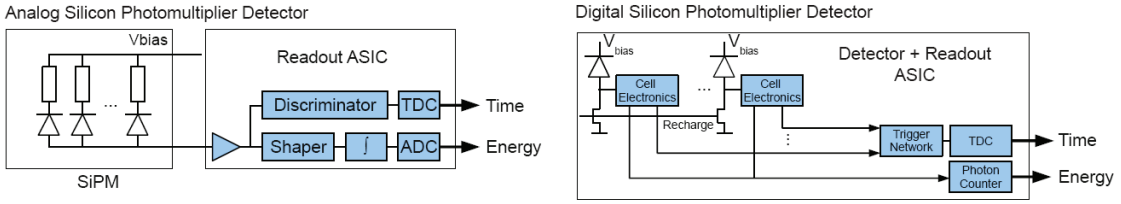


Figure 1: Scintillation light detector systems based on the analog (left) and digital silicon photomultipliers (right).

Similar functionality can be realized in a single chip according to the scheme shown in fig. 1 (right). Here, the SPADs are integrated with conventional CMOS circuits on the same substrate. Each SPAD has its own readout circuit, which also provides means for active quenching and recharging of the SPAD. A one bit memory cell integrated next to the SPAD can be used to selectively enable or disable the respective diode. Each cell, composed of the SPAD itself and the corresponding electronics block, is connected to the time-to-digital converter via a configurable, balanced trigger network. A separate synchronous bus is used to connect each cell to the photon counters to determine the number of detected photons. Eventually, correction look-up tables and other data post-processing could be implemented on the same chip.

Integration of additional logic next to the light sensing element can unlock the true potential of this new light detector in applications requiring very high time resolution while detecting only few photons per event. For example, the position of the photon can be detected and stored to the accuracy of the SPAD size, typically several tens of microns. Additionally, this information can be used to correct for the propagation delay non-uniformity of the trigger network and so to improve time resolution. The above figure illustrates also one characteristic of the new concept: by integrating part of the readout on-chip, the sensor becomes an application specific integrated circuit (ASIC). In this particular example, the digital Silicon Photomultiplier is intended to be used as a detector for scintillation light. A modified concept is needed to make the sensor also a good candidate for e.g. Čerenkov light detectors [2]. Extensions of the current digital Silicon Photomultiplier architecture to this effect will be presented below.

2. Digital Sensor Architecture & Operation (from [2])

Like in its analog counterparts, digital silicon photomultiplier pixels consist of arrays of Geiger-mode microcells (SPADs), each capable of detecting single photons. Contrary to the analog SiPM, however, each cell is capable of detecting and storing exactly one photon. Upon the detection of a photon, the

avalanche is actively quenched using a dedicated transistor, and a different transistor is used to quickly recharge the diode back to its sensitive state. SPAD breakdown results in an immediate voltage change of approximately the excess voltage at the anode. Upon reaching the inverter threshold, the anode voltage is

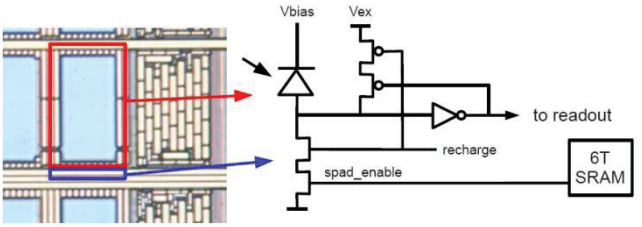
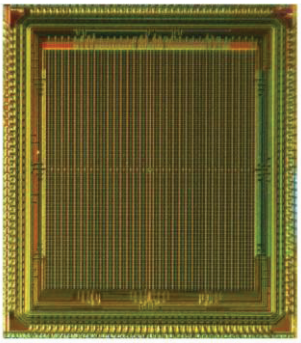


Figure 2: Close-up of a single cell (SPAD) and simplified schematics of electronics.

forced to the breakdown voltage level by closing the quenching transistor, thereby stopping the current flow through the diode. The combination of the diode capacitance and the quenching transistor feedback ensures proper storage of the information. The quenching transistor is disconnected and the diode is reset to sensitive state by a separate recharge transistor (fig. 2).

Each cell provides a fast asynchronous trigger signal and a slower synchronous data output signal. The trigger signal of each cell is connected to a balanced, low skew trigger network connected to the on-chip time-to-digital converter (TDC). The trigger network can be configured to start the TDC at the detection of the first photon or, alternatively, higher photon thresholds. In case of first photon trigger, the trigger network is equivalent to a balanced, distributed “all cells”-to-1 OR-gate. The discrimination of higher photon thresholds is described in [6]. The data output signals of all cells in a column are connected to the same data line and the data is applied to the data line using a row output enable signal. Then, the acquired data can be read out by selecting individual rows of the array one after the other and reading the data lines at the periphery of the pixel.

To simplify the design of the chip, a pixel is composed of four identical subpixels, each consisting of an array of 64 x 32 cells (demonstrator test chip). The cell size is 52 x 30 µm² each resulting in a 50% fill factor including the cell electronics. The total pixel size of 3840 x 3328 µm² therefore contains a sensitive area of 6403016 µm². One diode has been omitted in each subpixel to make space for the trigger logic at the center of the pixel, thus resulting in 2047 cells per subpixel. Each subpixel has its periphery logic on two adjacent sides to control the access to the cell inhibit memory and to provide the means to readout the



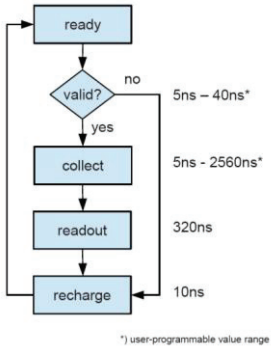


Figure 3: (a) Microphotograph of the demonstrator chip DLDK8. The size is 4.555x5.253 mm². (b) Acquisition sequence including typical timing values.

data and recharge the diodes. An integrated time-to-digital converter is connected to the trigger block at the pixel center via the master trigger line. A microphotograph of the technology demonstrator test chip is shown in Fig. 3a. The TDC is located on top of the SPAD array and has a block size of 96 x 3300 μm². All measurements presented in this paper were obtained using a sensor with 25 V breakdown voltage. The actual bias voltage of the sensor equals the breakdown voltage plus the 3.3 V excess voltage.

A typical data acquisition sequence is shown in Fig. 3b. This sequence is tailored to the acquisition of scintillation pulses [4] and has to be modified to reduce the sensor dead time when used for other applications with lower light fluxes (e.g. Čerenkov light detection). The timings shown in the figure are either defined by the sensor architecture and SPAD properties (readout and recharge phase) or programmable (validation and collection) to allow the user to adapt the acquisition sequence to the decay time of various scintillators.

The pixel state machine starts in the state READY with all diodes charged above their breakdown voltage and recharge transistors open. A trigger signal starts the acquisition sequence, forcing the pixel controller to change the state to VALIDATE. The pixel controller stays in this state for a user-defined time of 5 to 40 ns. After the validation hold-off timer expired, the validation signal is checked to determine if the event is indeed a real light pulse or dark count. In case of a dark count generated trigger, the pixel state machine changes to RESET to quickly reset the pixel and change back to the READY state in preparation for the next event.

In case of a real scintillator pulse, the validation threshold is reached and the state machine changes to the state COLLECT. While in this state, the pixel waits for the scintillator pulse to decay. The photons impinging on the sensor are detected and stored in the cells for later readout. After the expiration of the timer, the pixel state machine switches to the state READOUT. In this state, each line of the sensor is selected separately and the number of photons detected in the line is added to the photon accumulator. Finally, the pixel controller goes to the RESET state for global pixel recharge and TDC reset, and then back to the READY state. A more detailed description of the sensor can be found in [6].

3. Digital Sensor Performance of current sensor

A. Intrinsic Timing & Triggers (from [2])

The new sensor is designed to operate on 200 MHz reference clock, which can be supplied either via single-ended (LVCMOS) or differential (LVDS) inputs. Also, the electrical test input (SYNC) used to test and calibrate the TDCs can be supplied either in single-ended or differential configuration independent of selected clock configuration, to provide maximum flexibility for the system builder. When using differential inputs for clock and sync, the single-ended IO pads can be internally re-configured to provide additional external trigger input and internal trigger output. Using these signals, multiple sensors can be connected to trigger groups, so one sensor is capable to start acquisition in one or more of its neighbors. The acquired event data is transferred via two 100 MHz serial data links to the readout infrastructure. The transfer is independent of the acquisition and no additional dead time is introduced. Even for the minimum acquisition time, the sensor is capable of outputting data faster than acquiring new data.

The timings of the individual phases of the acquisition sequence (see figure 3b) can be programmed using the JTAG interface, which is also used to program the cell inhibit memory allowing to switch of cells with high dark count levels. The integrated time-to-digital converters have a typical bin width of 24 ps under nominal operating conditions. Fig. 4a shows the distribution of the bin width values for one particular sensor. Two time-to-digital converters running with complementary 100 MHz clock have been

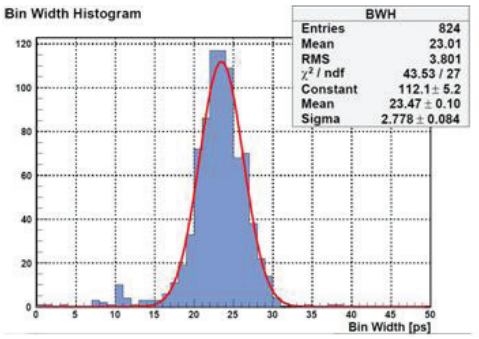
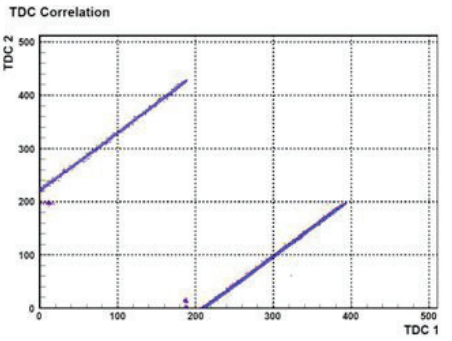


Figure 4: (a) Bin width histogram of the two time-to-digital converters.



(b) Cross-correlation histogram of the two complementary time-to-digital converter time stamps for randomly generated events.

integrated to provide at least one valid time stamp for every event. To counteract the meta-stability close to the reference clock edge, the TDC design has been modified and a 500 ps wide exclusion window has been added. As both TDCs are running 180° out of phase, both TDCs deliver a valid time stamp for 90% of all events, which can be used to further improve the timing accuracy.

The cross-correlation between the time stamps of the two TDCs is shown in Fig. 4b. This two-dimensional histogram is generated by using the time stamps of random events. The histogram can be used to generate the look-up table to correct for the TDC non-linearity.

The sensors employ a trigger network to provide a low-skew signal path from each micro-cell to the time-to-digital converters. It also provides some configuration options meant to increase the trigger threshold to higher photon levels to minimize system dead-time due to dark count related triggers. The basic function of the trigger network has been explained in [7] with the comment that the trigger thresholds except for the first photon are statistical thresholds. This behavior is now shown in the following figure 5. The graphs show the individual probability of the n-th photon to generate the trigger, based on an analytical model of the trigger network.

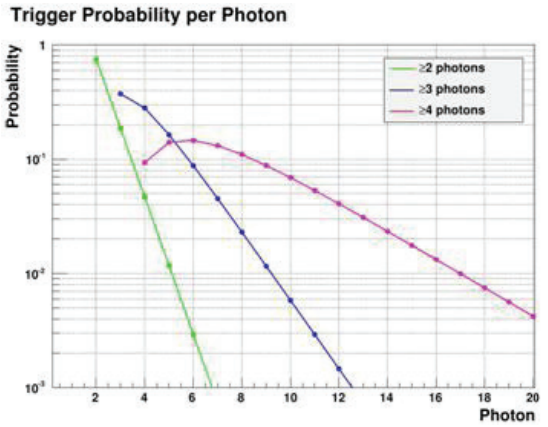
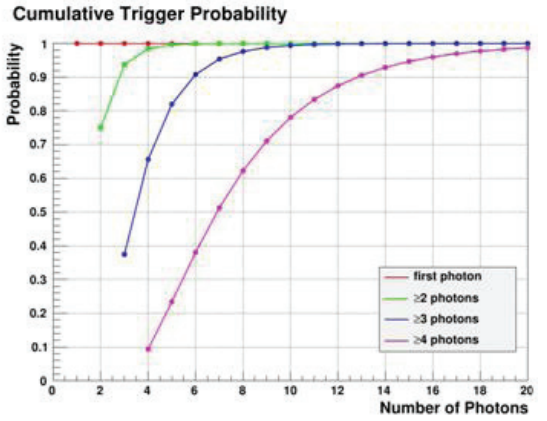


Figure 5: (a) The trigger generation probability for the n-th photon as a function of the selected trigger level.



(b) Total trigger generation probability for the number of detected photons as a function of the selected trigger level.

As shown in fig. 5a, for the ≥4 photon trigger network configuration, the 6th photon has the highest individual probability to generate the actual trigger signal. The actual trigger probability, as displayed in fig. 5b, is given by the sum of the individual probabilities over the number of detected photons. Fig. 5b indicates that for the ≥4 photon trigger configuration, at least 7 photons have to be detected in order to reach 50% trigger probability level.

The validation logic is based on the same principle. The only difference is the number of regions the pixel is partitioned to, namely 32 in the current sensor configuration. This, together with the variable validation interval, allows one to set a higher energy threshold to discriminate real events from dark count events to reduce the system dead-time [2].

An important goal of a sensor development aiming at high timing accuracy for e.g. Time-of-Flight Positron-Emission-Tomography (TOF-PET) applications is to achieve good timing resolution across larger sensor arrays. We have been testing the intrinsic timing resolution (jitter) of arrays with 8 x 8 pixels by means of electronic and picosecond laser pulses (24 ps FWHM), as depicted in fig. 6. The time stamp differences between the two sensors are shown in the graphs on the bottom. The full-width-half-max (FWHM) of the distribution indicates the timing jitter to be 44 ps for the electronic measurement, which is mainly due to the TDC's and the clock distribution network, and 59 ps for the laser pulses, which adds the contribution of the Geiger-mode cells. For these measurements the sensors were triggered on the first photon.

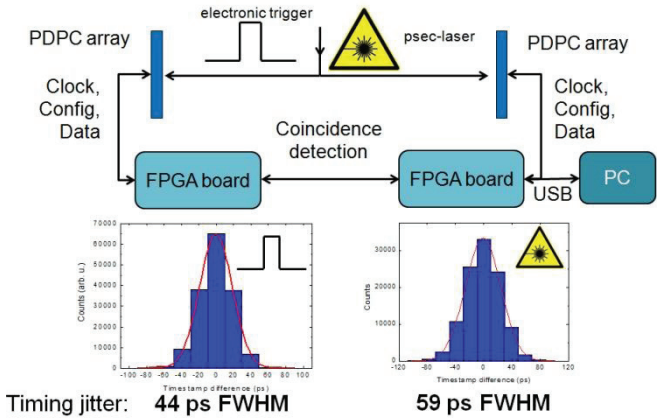


Figure 6: Timing jitter of dSiPM sensor arrays (8x8 pixel) as measured with electronic trigger (left) and picoseconds laser pulses (right). The measurement setup is shown on top.

B. Photon Detection Efficiency

In order to be able to trigger on the first photon arriving, a high Photon Detection Efficiency (PDE) is desirable. PDE is primarily influenced by the thickness of the active layer, the Quantum Efficiency (QE) of the diodes, the fill factor of the sensor surface and the reflectance of the surface layers.

Fig. 7 depicts the PDE of the DLDK8 demonstrator chip as shown in fig. 3 as a function of the incident wavelength emitted from a calibrated light source. The peak value of about 30% is achieved at 430 nm. The spectrum already points to a number of improvement possibilities as discussed later. The steep decline towards dark blue and UV on the left is attributable to surface reflection processes and could probably be shifted further to lower wavelengths for example by well designed anti-reflective coating (ARC).

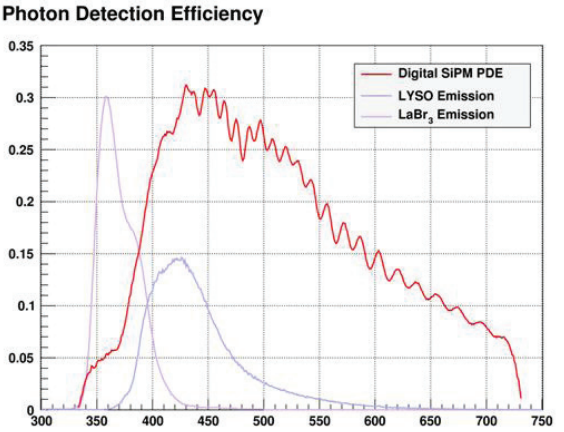


Figure 7: Photon Detection Efficiency of the demonstrator chip DLDK8 as shown in fig. 3 (red curve) as a function of the light wavelength. The measurement was performed on one cell at a time so that optical crosstalk is excluded. For comparison the emission spectra of 2 scinitillators for PET are shown (blue and violet curves).

C. Dark Count Measurements& Temperature Sensitivity

The design of the sensor as described in chapter 2 allows a control of the dark count rate (DCR) at the individual SPAD level. By subsequently switching on and off each individual SPAD cell in a completely dark environment, dark count maps and histograms like the one shown in fig. 8 (a) can be generated. As becomes clear from the histogram and the cumulative logarithmic plot in fig. 8 there is an over proportional contribution of a few cells to the DCR of the sensor. Since the digital architecture allows to

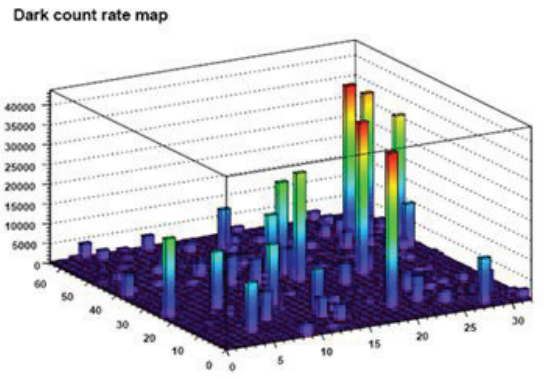
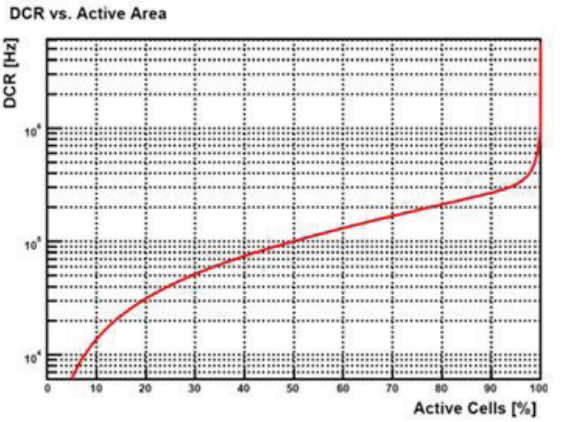


Figure 8: (a) Histogram of dark counts of cells of a subpixel taken at room temperature.



(b) DCR as a function of the number of active cells.

address each cell individually the DCR can be lowered by orders of magnitude by switching of the "bad" cells. This feature also contributes to the much reduced temperature sensitivity (compared to analog SiPMs) of the sensor as is shown in figure 9. Typical values of active cells are ranging between 90-98%. The measurement was carried out with a pulsed picosecond laser (24 ps FWHM). The photopeak changes

by 0.33%/°C, which is an order of magnitude lower than with analog SiPMs. The PDE drift can be compensated for by adapting the bias voltage. The TDC and trigger network drifts cause a change of the time of 15.3 ps/°C. TDC offsets can be periodically re-calibrated using the SYNC-input of the sensor.

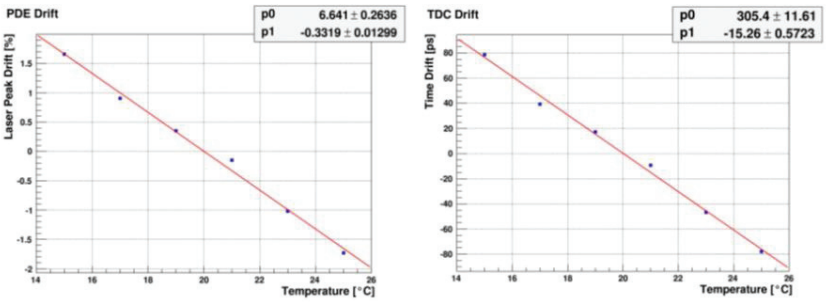


Figure 9: (a) PDE drift as function of the temperature and (b) TDC drift as function of temperature measured with picosecond laser pulses (24 ps FWHM) (no bias adjusted).

D. Performance with Scintillators (from [3])

Fig. 10 shows a schematic of the measurement setup that was used for coincidence measurements with scintillator crystals and arrays, similar to fig. 6. The dSiPM arrays are mounted on printed circuit boards containing an FPGA that provides the sensors with a 200 MHz reference clock and configures the sensors via their serial interface. One board contains a 200 MHz master oscillator that is distributed via an Ethernet cable to the second board. Scintillator arrays containing 8 x 8 LYSO crystals with 4 mm x 4 mm pitch and 22 mm length were optically coupled to the detector arrays, leading to a 1:1 coupling between the crystals and the dSiPMs. The individual scintillator crystals were separated by reflecting foil.

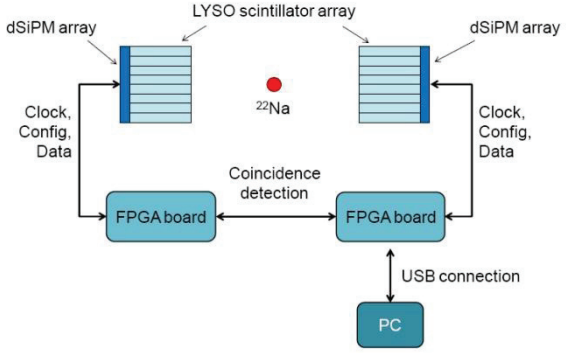


Figure 10: Schematic of the measurement setup. LYSO scintillator arrays are coupled to arrays of digital Silicon Photomultipliers. Readout boards with FPGAs are used to provide the dSiPMs with a 200 MHz reference clock and to configure and control the sensors. The data is transferred to a PC via a USB interface.

Recording all the timestamp differences using the above described LYSO scintillator arrays coupled to the dSiPM arrays generates a histogram presenting the sum of all individual timestamp differences recorded for the individual pixels. Fitting a Gaussian distribution to the data yields the coincidence timing resolution (CTR) of the setup, as shown in fig. 11b, of 283 ps (FWHM). In order to prove that the timing axis is calibrated correctly, two ^{22}Na sources, 8.3 cm apart, were put between the two arrays. Two peaks in the timestamp difference histogram were recorded, separated by 570 ps or 8.6 cm, which confirms the correct calibration of the timing axis. The measurements were performed at 10°C.

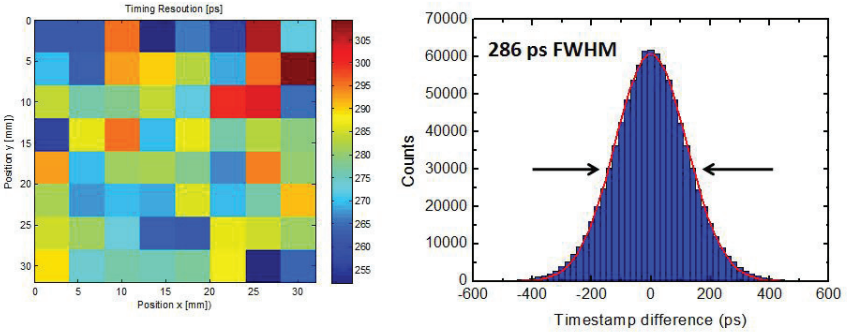


Figure 11: (a) Timing resolution as a function of the pixel position and (b) histogram of time stamps for the measurement as shown in fig. 10 using DPC3200-22-44 sensors with 8x8 pixels at 10°C.

Another important parameter of a scintillation detector is its energy resolution. The light detector as an important part of the detection chain adds to the intrinsic energy resolution of the scintillation crystal used [7, 8].

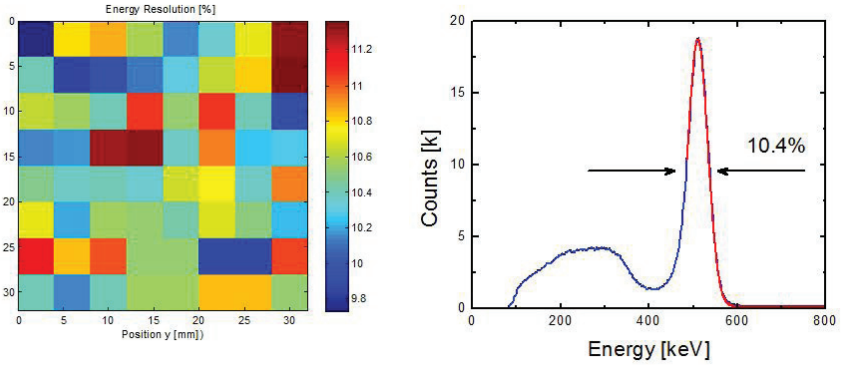


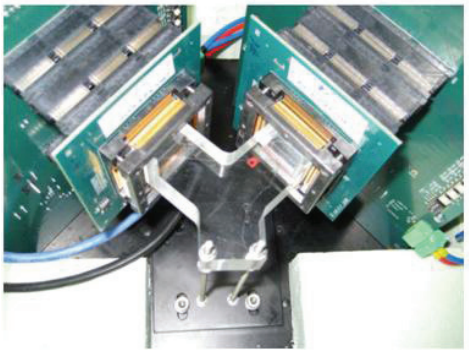
Figure 12: (a) Energy resolution as a function of the pixel position and (b) energy resolution summed over all pixels of the sensor for the setup according to fig. 10 using DPC3200-22-44 sensor arrays at 10°C.

Energy resolution is obtained by summing up the number of events in the photopeak per pixel. Prior to determining the FWHM of the photopeak, the spectrum is corrected for saturation. Since the number of active cells, N, and the number of triggered cells, k, is known, the number of photons, p, can be calculated according to $p = -N * \ln\left(1 - \frac{k}{N}\right)$. Fig. 12b shows the summed energy spectrum over all pixels and yields a global energy resolution for the configuration described above of 10.4% (FWHM).
Both the coincidence timing resolution (CTR) as well as the energy resolution are depending on the geometry of the scintillation crystals used which determines the light collection properties, light travel paths etc. Typically small and long crystals with high aspect ratio deliver worse results than shorter and larger ones. We have been measuring a CTR of 153 ps (FWHM) for LYSO crystals of 3x3x5 mm³, values of down to 120 ps (FWHM) for Calcium doped LSO of the same geometry have been reported using the digital sensor arrays [8,9]. The timing resolution is mainly affected by the aspect ratio of the crystals which determines the travel length of the light affecting the arrival time of the first photon.

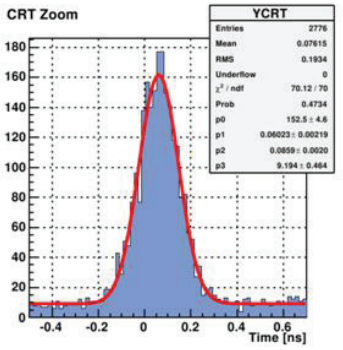
E. Čerenkov Light Detection (from [7])

We successfully tested the technology demonstrator as a sensor for Čerenkov light. The test setup shown in Fig. 13 was developed by the team of Prof. Dueren at Giessen University, Germany and tested at Philips Digital Photon Counting in Aachen using a picosecond-pulsed laser beam [4].

For the beam test, the Y-shaped Čerenkov radiator made of acrylic glass was coupled via approximately 1 mm air gap to two DLD8K demonstrator chips described in [6] connected in coincidence. The measurements were carried out using 120 GeV protons from the SPS test beam at CERN. The test setup was operated in first-photon trigger mode and all events have been validated. The setup temperature of 3°C was controlled by a thermoelectric cooler and 2% of the diodes with the highest dark counts have been disabled to further reduce the dark count rate of the sensors. The measured dark



(a)



(b)

Figure 13: (a) Čerenkov light detector setup. The Y-shaped radiator is coupled via a small air gap to two digital SiPMs connected in coincidence. (b) Coincidence time resolution of the Čerenkov light detector setup in (a).

count rates for both sensors were in the range of 500 kHz. Additionally, an external gate signal was used to reduce coincidences due to the low beam duty cycle of only 16%, to reduce the data file size. Measurement times ranged from few minutes to several hours. Coincidence resolving time of $\sigma = 86$ ps was measured for both sensors (fig. 13), resulting in $\sigma = 61$ ps per sensor. As the skew in the trigger network is currently the major contributor to the time resolution for single photons, re-balancing and fine-tuning of the trigger network will make it possible to improve the time resolution of the sensor to 30 ps - 40 ps at the single-photon level.

4. Optimization Possibilities towards Single Photon Detection (from [2])

The current versions of our digital Silicon Photomultiplier have been developed primarily for scintillation light detection. This resulted in an acquisition sequence which is not optimal for single photon detection where the dark count events cannot be separated from true events. As a consequence we observe a relatively large dead time of the sensor. The acquisition sequence could be optimized to reduce that dead time under the assumption that at most one photon is impinging on the sensor per event. The saving comes from skipping the readout phase of the sequence. This can be made optional to allow the same sensor to be used for both scintillation and Čerenkov light detection. Fig. 14 shows the difference in the state machine diagrams. Furthermore, reduction of the dark count rate further helps to reduce the dead time.

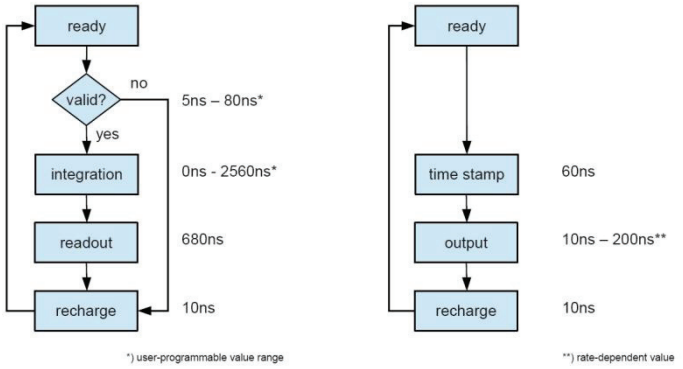
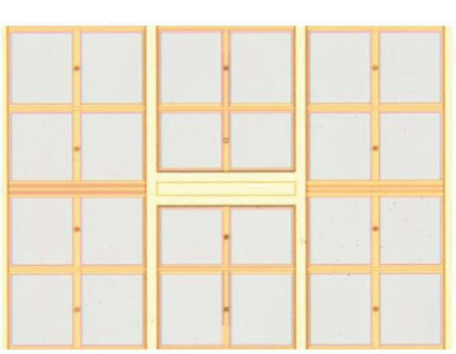


Figure 14: Original and modified acquisition sequence.

Second area of optimization is certainly the photon detection efficiency. A new improved version of the digital Silicon Photomultiplier has been developed and tested (fig. 15a). The new sensor has 59.4 µm x 64 µm cells with 78% fill factor. The peak photon detection efficiency (PDE) can reach more than 50% in single diodes but strong interferences due to the presence of nitride-oxide layers in the chip interconnect stack lead to a significantly lower average PDE (Fig. 15b). However, future optimizations of the optical interface will enable higher average PDE and improved sensitivity below 400 nm.



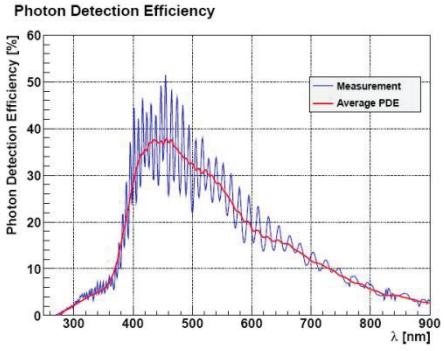


Figure 15: (a) Layout of new dSiPM with improved area efficiency. (b) Typical photon detection efficiency of the new sensor. The red line indicates the moving average over ± 20 nm.

Furthermore, the skew in the trigger network currently limits the single photon time resolution. To achieve optimal performance, the trigger network needs to be manually tuned to minimize its skew. This has already been done in simulation and needs to be verified in silicon. Nevertheless, even a perfectly balanced trigger network will suffer from process variations. Therefore, further improvement in the time resolution could be achieved if the position of the triggered diode was known. As there is at most one photon detected per pixel, this can be realized using a scheme shown in fig. 16.
Every cell is connected to a horizontal and a vertical data line. When a cell detects a photon, the position of the cell becomes visible at the periphery of the array as a signal on these two lines. The trigger signal can be used to latch-in the data lines into a register, which can be evaluated to calculate the diode position as a binary value. As this position is directly linked to the skew map, the skew map can be used to completely correct for the actual trigger network skew of the sensor.

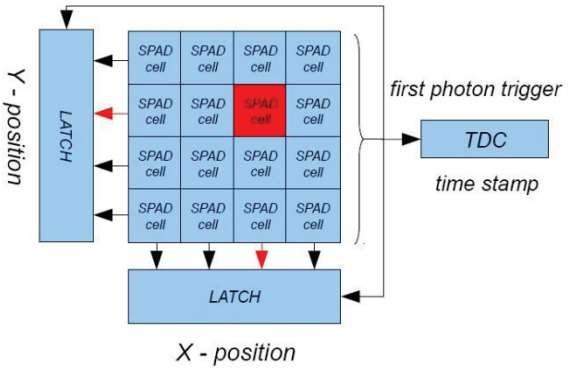


Figure 16: Potential future sensor architecture with position readout.

Optical crosstalk in the sensor and random coincidence of the photon with a dark count will make the position information ambiguous. Normally, this situation can be easily detected, as more than one line becomes active, and the event could be discarded. However, as optical crosstalk occurs most likely between neighboring cells the approximate position could still be estimated if two neighboring lines become active. This information could be used to reduce the loss of events due to optical crosstalk.

5. Scalability of Digital Light Sensors

From the beginning it has been our goal to develop not only a new kind of light sensor but a (disruptive) technology that could be scaled up to be useful in many applications such as medical imaging, high energy- or astrophysics detection or analytical instrumentation, basically everywhere today vacuum photomultiplier tubes (PMTs) are still used. In order to achieve this goal we went from one pixel to several 1000 pixels (Feb. 2012) within a relatively short time frame. The number of pixels operational

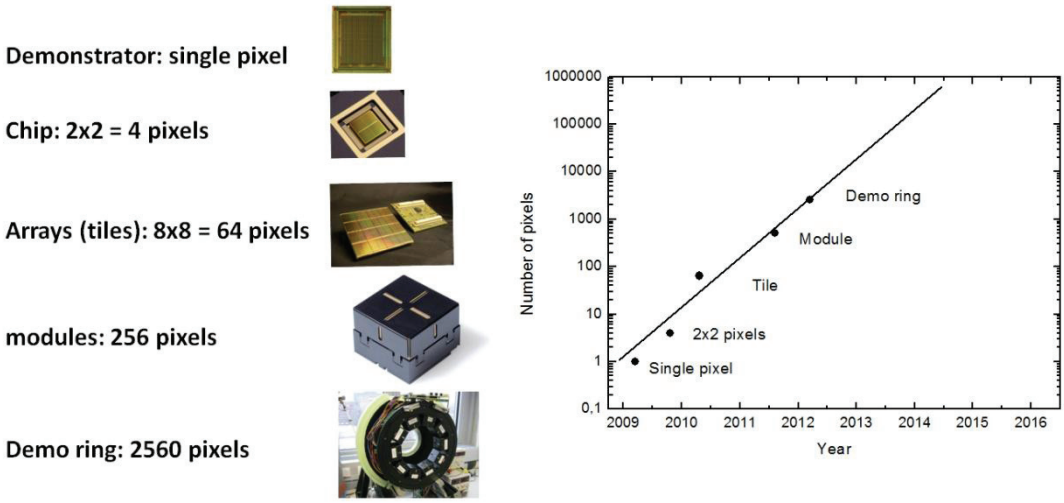


Figure 17: Evolution of the Philips dSiPM technology: the number of pixels doubled every 3 months.

basically doubled every 3 months, as can be seen in fig.17. This rapid increase is a direct consequence of the full utilization of the early signal digitization, the high level of integration and the complete absence of analog electronics. Pre-processing and configuration can be done at sensor level, sensors can be combined into larger units (modules) with intermittent data concentration and clean up steps and such modules can form larger detector areas such as planar cameras or rings. All the necessary electronics can be built from digital, off-the-shelf-components, thus reducing the overall costs of such detectors.

A very important feature of scalable technology is its energy consumption. A DPC digital sensor consumes on average 1.1 W of power whereas a detector module as shown in fig.17 consumes about 10 W at high rates, including electronics. Table 1 provides an overview of the digital light sensor arrays that are currently being produced and investigated. They fundamentally differ in the number of cells (SPADs) per pixel and cell size, thus in fill factor, PDE and dynamic range. However, they have the same "outer" geometry in terms of their size, the pixel matrix and pixel pitch. Also, they can be operated with the same interface boards, firmware and software.

Table 1: Digital Light Sensor Arrays produced and investigated

Feature	**DPC 3200-22-44**	**DPC 6400-22-44**
Sensor array size (mm²)	32.6 x 32.6	
Sensor Matrix	8 x 8 pixel	
Pixel size (mm²)	3.328 x 3.840	
Pixel pitch (mm), all directions	4	
Cells (SPADs) per pixel	3200	6396
Cell size (µm²)	59.4 x 64	59.4 x 32
Fill factor (%)	54	78
PDE (%) @ 430 nm	~ 50	~ 30

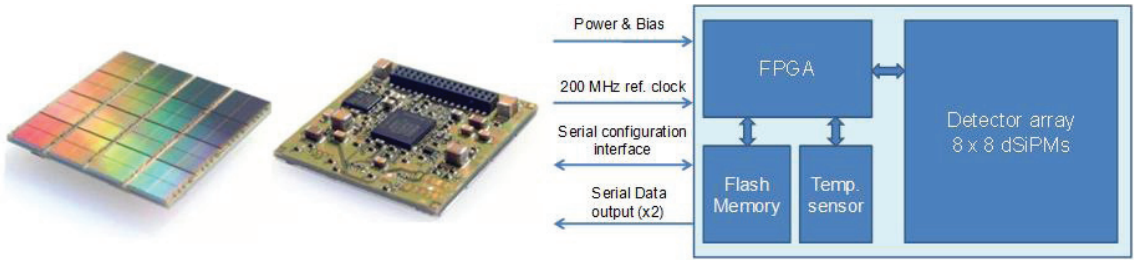


Figure 18: Philips DPC digital light sensors front- and back side (left) and integrated electronics and interface structure (right).

Fig. 18 illustrates the layout of the sensors with their electronic components on the back and the corresponding interface structure. The FPGA ensures the proper clock distribution, allows data collection and concentration, TDC linearization, saturation- and skew correction. The flash memory contains the FPGA firmware, the configuration files and inhibit-memory maps that allow to reduce the DCR or to generate patterns of active/inactive cells on the sensor. The built-on temperature sensor enables to record

the sensor temperature at all times. The sensors are four-side buttable so that larger areas of detector can be built with minimal gaps. MR compatible versions of these sensors are under development.

6. Summary

Fully integrated digital arrays of silicon photomultipliers (dSiPM) have been produced and characterized. Their physical performance parameters have been obtained and their functionality has been tested and optimized. Further optimization is possible in the direction of single photon counting by improving the timing and trigger networks and increasing the PDE. Respective developments are underway.

It has been shown that this technology is fully scalable, thus providing an elementary pre-requisite for its industrial application. The number of pixels could be doubled every 3 months and most recently a full system (a demonstrator ring) has been built and is currently being tested at the Philips DPC labs in Aachen, Germany.

Based on the results obtained so far the technology developed will have the potential to replace long-time used vacuum photomultiplier tubes in many applications, especially where accurate timing, very low light levels, low power consumption, compact size and magnetic fields are the challenges.

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