THÈSE

Pour obtenir le grade de

DOCTEUR DE L'UNIVERSITÉ GRENOBLE ALPES

Spécialité : Physique de la Matière Condensée et du Rayonnement

Arrêté ministériel : 25 mai 2016

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préparée au sein du **Laboratoire PHotonique, ELectronique et Ingéniérie QuantiqueS**
dans **l'École Doctorale Physique**

Couplage et dynamique de boîtes quantiques en technologie MOS silicium étudiés par réflectométrie radio-fréquence sur grille

Coupling and dynamics of quantum dots in silicon MOS nanowires studied with gate-coupled radio frequency reflectometry

Thèse soutenue publiquement le **10 décembre 2020**,
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Ce manuscrit est dédié à Marc Sanquer

Acknowledgements

Finalement, les remerciements ! Bon, ce n'était pas une partie de plaisir comme disait le philosophe. 4 ans et demi après avoir commencé cette thèse, il est temps de rendre à César ce qui est à César, de remercier chaleureusement toutes les personnes qui ont cru en moi et qui ont tout fait pour assurer la réussite de cette aventure.

First and foremost, I would like to warmly thank Georgios Katsaros, Francis Calmon, Maryline Bawedin and Laurent Saminadayar for accepting to be part of the jury, despite the sanitary conditions. Special thanks to my two reviewiers, Georgios Katsaros and Francis Calmon, for their commentaries about the manuscript. I want to tell that it was a real pleasure to present some of my work to the four of you. The asked questions led to interesting discussions.

Il est temps de remercier les deux personnes les plus importantes de ce projet, mes deux directeurs de thèse, Xavier et Louis.
Xavier, quoi dire à part que je n'aurais pas pu espérer meilleur encadrant au quotidien. Ce n'était pas facile tous les jours, loin s'en faut, mais tu as su garder patience, continuer à me motiver. Ton expertise en cryogénie et en électronique, entre autres, fut une aide précieuse pour mener à bien ce projet. Même après trois ans de travail avec toi, je reste impressionné du niveau de connaissances que tu as dans ces domaines en particulier. Merci encore pour tout ce que tu as fait.
Louis, le parfait co-encadrant. On ne se voyait pas aussi souvent qu'avec Xavier mais à chaque fois que l'on se voyait, c'était rafraichissant. Parler dispos, process, composés chimiques, stratégie d'amélioration des dispos, tout en faisant des jeux de mots un peu partout, un peu tout le temps, c'était super agréable. Et quelle expertise également ! J'avais l'impression que les MOSFET n'avaient pas de secrets pour toi. Quand on n'est pas de la microélectronique, ce domaine est assez déroutant. Tu incarnais à la perfection le pont entre la recherche fondamentale et l'industrie de la microélectronique. Merci à toi pour ta pédagogie, ta patience, ton humour.
A vous deux, je vous souhaite le meilleur pour la suite.

J'aimerais à présent rendre un hommage. Marc Sanquer, spécialiste de la physique mésoscopique, pilier de l'INAC et de la recherche sur les MOSFET à très basse température, s'en est allé le 15 février 2021. La soutenance de cette thèse est la dernière à laquelle il a assisté.
Lors de ma première année, Marc a été mon encadrant principal effectif, mon collègue de manip, un réel mentor. Les résultats présentés dans le chapitre 4 sont issus des dernières manip de Marc, ou presque. Il avait cette faculté à s'émerveiller de tout, y compris des choses semblant les plus simples. Je me suis fait la main sur *Diluette*, son cryostat wet. Il m'a initié à la physique des quantum dots comme personne n'aurait pu le faire.
Au delà de ses qualités de physicien, Marc était quelqu'un de très sympathique, aimé de ses collègues et de la communauté. Il méritait amplement la tranquillité attendue de la retraite. Puisse-t-il à présent reposer en paix. Merci pour ta contribution à la Science, merci pour ta contribution humaine au labo. J'ai une pensée pour tes proches. On ne t'oubliera jamais.

Place maintenant aux permanents du labo. Malgré l'état des locaux, il faisait bon vivre au C1, entre les équipes LaTEQS et IMAPEC. C'est en majeure partie dû à la bonne ambiance au sein des groupes. J'aimerais donc remercier François L., Vincent R., Claude C., Max H., Silvano D.F., Louis H., Christophe M., Etienne D. En particulier, je garde d'excellents souvenirs de ces GdRs à Aussois, des sorties skis, et d'un peu moins bons concernant les raclettes du labo. Mais bon, quelle idée aussi de ne pas aimer le fromage ! De plus, je tiens à vivement remercier François pour les discussions importantes lors de la fin doctorat. Merci enfin Etienne pour le template de ma présentation ! Je voudrais également remercier les membres de mon comité de suivi de thèse, Manuel H., Hermann S. et Jérôme P. Une pensée toute émue pour Jérôme qui nous a également quitté lors de ma thèse.
Je ne veux surtout pas oublier les techniciens permanents. Je tiens à remercier Fredéric G. & Fredéric P., Pierre P.B., Jean-Luc T. et Iulian M. En particulier j'adresse un grand merci à Iulian pour son aide ainsi que sa pédagogie concernant les cryostats. J'espère que tu es satisfait de ton protégé, que *Tritonito* tournes comme une horloge !

Entre les permanents (les trois-quarts) et les doctorants (les avants) il y a les post-docs (la charnière)[1]. Au début de ma thèse, ils étaient deux : Alessandro C. et Romain M. Depuis, Alessandro et parti et Romain est devenu permanent. Je veux vous adresser de sincères remerciements. Vous m'avez permis de m'initier à la physique des quantum dots, des MOSFET à basse température et, plus important encore, à la réflectométrie. Au delà des considérations de physique, merci Romain pour ton optimisme, ta bonne humeur et ton

[1] J'ai pas pu m'en empêcher, c'est le 6 nations

soutien du début de cette thèse à la fin.
Deux autres post-docs ont fait leur apparition dans le labo au cours de ma thèse. Florian V. et Simon Z. Je remercie le premier pour sa bonne humeur infaillible et le second pour son efficacité redoutable !

Venons-en maintenant aux thésards, aux collègues, aux amis. J'ai commencé ma thèse par m'installer dans le bureau de Salha et Anaïs. C'était le bon vieux temps de l'innocence de la première année. Merci à vous deux pour l'accueil que vous m'avez réservé. Je repense encore aux nombreuses façons d'offusquer sans méchanceté Salha, sans faire exprès des fois ! Comme je repense à nos débats pré-présidentiels de 2017 avec toi Anaïs (*rend l'argent !!*) ! Je vous souhaite le meilleur pour vous deux. A l'époque, Loic H. était encore présent. C'était très chouette de te rencontrer, de m'avoir initié à Dominion, entre autres ! J'ai repensé il y a pas longtemps à la mission de monter le canapé par le balcon chez vous, quelle histoire ! Je vous souhaite également le meilleur pour toi et Caroline.
En 2016, nous étions trois nouveaux thésards au sein du groupe. Estelle M. *Mozarella* et Romain A. *Râle-bert* complétait notre trio. Cela faisait quelques mois que Florian B. *the python master*, avait également commencé sa thèse. Nous avons été rejoint par Thomas J. *un dénommé José*, au cours de l'année 2017. Je pense ne pas me tromper si je vous dis que vous avez été sûrement les personnes les plus importantes au sein du labo. Je n'aurais jamais été au bout sans vous. Pour tout ce que nous avons partagé ensemble, de l'escalade à la bière, des jeux à la musique, des nuits en altitude aux journées ski, des GdRs aux K'Fée des jeux, de la virée en Angleterre à celle d'Helsinki, merci, merci pour tout. J'espère vous revoir un de ces quatre ! Et d'ici là, soyez heureux et portez-vous bien !

Je veux aussi remercier et encourager les derniers arrivants du groupe : Tom V., Rami E., Loïc L.G., Cécile Y., Agostino A., Florie M., Nicolas P., Estelle V., Gonzalo T., Chotivut T. En particulier, je veux remercier Tom qui me fait (entre autres choses) mourir de rire et Rami sans qui j'aurais mis beaucoup BEAUCOUP plus de temps à coder pour ma manip. Je vous souhaite à tous, y compris les nouveaux , de tenir le rythme et de prendre plaisir à ce que vous faîtes. Puisse le futur vous être favorable.
J'ai également une pensée chaleureuse pour les membres du groupe théorie et tous les thésards que j'ai rencontré lors des GdRs, ils se reconnaîtront (nom de code TipTop).

Comment parler de ces années Grenobloises sans parler des personnes que je voyais à côté du travail ? Je vous l'demande !
Je veux commencer par remercier Hugo D. et Jeannette R., Florian C., Jessy P. et Kilian M.

On se sera bien marré pendant ces années et sans vous tout aurait été plus compliqué depuis le début. Vous allez me manquer les gars, j'espère qu'on se reverra bientôt ! Bonne chance pour ta nouvelle petite famille le Hug, et profite de tout ce bonheur ! Je vous souhaite à tous les 5 de la réussite, que ce soit perso ou pro !
Je veux ensuite remercier Quentin F. et Palmerina G., Victor D., Alexis W. et Sophie C., le grand Nils, Paul et Marc M. Par où on commence ? Les blind tests au Metro ? Les tournois de coinche au Sub ? Les soirées billards au D'Enfer ? Les nuits drak' (ça manque tellement) ? Les soirées flims et séries ? Les fondues camembert ? C'était dingue, heureusement que vous étiez là au quotidien.
Je pense également à des amis de longues dates : Anthony L., tiens le coup mon pote la soutenance est en vue, Alexis T., Adrien G., Tobye X., Irina. On se reverra bien quelque part dans l'hexagone un de ces quatre !

Cette rédaction de thèse s'achève en plein contexte de pandémie du SARS-CoV 2. Drôle de façon de terminer son manuscrit que de vivre confiné du côté de sa ville natale. Mais indispensable. Je remercie donc infiniment tous mes potes de Brière (c'est mort je vous cite pas tous, c'est déjà bien assez long !) d'avoir été là dans la dernière ligne droite, en particulier Bastien G. (bon, 1 quand même), cette petite coloc de deux mois lors du premier confinement était idéale !
Je veux enfin remercier mes parents, mon frère et mon oncle d'avoir été un soutien sans faille durant ces longues années d'études. Merci de m'avoir laissé le choix. Merci d'avoir cru en moi.

Pour complètement terminer, je trouve que l'on ne remercie pas assez les professeurs, sûrement influents dans la vie d'un étudiant en doctorat, dans cette section. Alors j'ai une pensée sincère pour Mme Petit, Mme Villant, Mr Loncke, Mme Lefebvre, Mr Fournaise, Mr De Préville ainsi que la quasi-totalité de mes professeurs d'université et mes maîtres de stage. Je suis très fier d'avoir été l'un de vos élèves ou étudiants. Vous m'avez inspiré. Et vous continuerez.

Abstract

Abstract

We are measuring at low temperature silicon MOS nanowires transistors where quantum dots are created. We also built a radio frequency reflectometry setup allowing one to probe the charge and the spin states of a charge carrier trapped inside a quantum dot. One such apparatus could be used mainly for two things : electron pumps for the quantum metrology, the definition of the ampere and for spin quantum bits, called qubits.

In this PhD we focused on two important problematics of the qubits : the control of the coupling between quantum dots and state readout. More precisely we showed that i) the coupling between two quantum dots can be strongly influenced by the state of a third quantum dot placed in between and ii) the setup required for the energy selective spin readout, a new spin-to-charge conversion mechanism in our specific MOSFET based qubits community, works perfectly without magnetic field.

This work has been done in close collaboration with CEA-LETI for the design and the fabrication of the devices with their 300 mm CMOS SOI facilities.

Résumé

Nous mesurons à très basse température des transistors nanofils silicium en technologie MOS dans lesquels des boîtes quantiques se forment. Nous avons aussi construit un dispositif de réfléctométrie radio-fréquence qui permet de sonder l'état de charge et de spin d'un porteur de charge piégé dans une de ces boîtes. Une telle expérience peut servir principalement pour deux choses : les pompes à électrons pour la métrologie quantique de l'ampère et les bits quantiques, ou qubits, de spin.

Dans le cadre de cette thèse, nous nous sommes concentrés sur les problématiques liées aux qubits de spin. Plus précisément, nous nous sommes penchés sur deux points essentiels du fonctionnement d'un tel qubit : le contrôle du couplage entre les boîtes quantiques, principalement via une troisième boîte et la lecture du spin par sélectivité en énergie, un mécanisme de conversion spin-charge relativement nouveau dans notre communauté de qubits à base de MOSFET.

Ce travail a été mené en étroite collaboration avec le CEA-LETI, pour le design et la fabrication des échantillons sur leur plate-forme SOI (Silicon-On-Insulator) CMOS 300mm.

Contents

Chapter 1

Introduction

"Back in the 1940s, researchers were just discovering how to use vacuum tubes as simple switches. These switches could then form logic gates, which could be linked together to form the first logic circuits. That's where we're at now with quantum processors. We have verified that all the components work. The next step is to engineer the smallest, yet most interesting circuit possible"

-Jungsang Kim, 2016

1.1 The prospect of a quantum computer

For 60 years and following the so-called Moore's law [1] about the evolution of the number of transistors per chip, electrical engineering has evolved exponentially both on the theoretical and on the technical aspects . The first Metal-Oxide-Semiconductor-Field-Effect-Transistor, called MOSFET was developed in the early 1960s within Bell labs by Kahng and Atalla [2]. Today, a processor can unbelievably host almost 20 Billions of MOSFET transistors[1]. Still, even with the biggest processors and supercalculators, some problems cannot be simulated by a classical computer.

Back in 1982 already, the famous R. Feynman wondered about this specific question: is it possible to exactly simulate quantum systems, like chemical bounds and chemical reactions, with a standard, classical computer ? In this paper [3], collection of notes taken from a keynote speech, he is one of the first[2] to tell about a *universal quantum simulator*, the quantum computer. Altough the physical idea of a quantum computer was not clear yet, some

[1] The introduction of chapter 3 gives a more detailed story of the transistor.

[2] In 1980, the russian mathematician Yuri Manin also proposed the idea of a quantum computer in his book *Computable and Uncomputable*. In the early 1980s, the american Paul Benioff was one of the first to theoretically describe the quantum mechanical model of a computer.

(mostly theoretical) researchers started creating new algorithms and protocols based on laws of quantum mechanics in different specific fields (for instance a new protocol, called BB84, in quantum cryptography [4] already in 1984 or the Shor's algorithm [5] built for solving the prime number factorization problem in a polynomial time, 1997). The idea of considering hardware devices designed to process quantum mechanically has become serious in the late 1990s.

The analog of the classical digital bits are the quantum bits, called qubits. While the digital bit has only two available states, 0 or 1, the qubit is a quantum mechanical system characterized by its wavefunction $|\psi\rangle = c_0|0\rangle + c_1|1\rangle$, a superpostion of the two eigenstates $|0\rangle$ and $|1\rangle$. If one entangles N of such qubits, it represents 2^N values simultaneously. By processing each of these values at the same time, a quantum computer operates exponentially faster than its classical counterpart.

In early 1998, D. Loss & D.P. DiVincenzo published a well-known proposal for a scalable semiconductor-based quantum computer made of quantum dots [6]. In this case, the qubit states are the two spin states of coupled single-electron quantum dots hosted in semiconductor materials. The computation is achieved by varying the coupling between the dots, acting as logical gates.
Later in the year, B. Kane published another proposal for a scalabe quantum computer made of donors in a silicon matrix [7]. In that case, the nuclear spin states of the donor are the qubits. Again, the computation is done by acting on conducting gates, varying the coupling between the donors.
Finally in 1998 J. Preskill published a theoretical paper [8] about fault tolerant quantum computation, the ability to overcome the leak of quantum information due to uncontrolled interactions of the qubits with the environment. This 1998 year could be considered as the beginning of the race towards scalable quantum computers.

Following these pionnering works, D.P. DiVincenzo published another paper in 2000 [9] about the physical implementation of quantum computation. From that paper have emerged the *DiVincenzo Criteria*, a list of five technical requirements in order for a quantum computer to be reliable, which are discussed in the next section.

As a consequence, researchers have looked into many different kinds of hosting materials for the qubits. The two aforementionned proposals involved semiconducting materials. For the last 20 years, GaAs heterostructures, silicon and silicon-germanium quantum dots have

been deeply studied. As an exemple, in 2016 R. Maurand et al from our group achieved the first qubit in a PMOS silicon device [10]. For more details about silicon and silicon germanium baseds qubits, see [11]. In 2020, only a few coupled qubits have been achieved in semiconducting materials. Very recently, a four qubit device has been demonstrated [12].

Semiconducting materials are only one possibility. In fact, a lot of different systems have been invented and designed such that trapped ions [13], superconducting qubit and photonic systems [14]. The three of them have been deeply investigated and many qubits arrays have been experimentally realized. I can also tell a word about neutral atoms [15], carbon nanotubes [16], NV center in diamonds [17] which have only achieved a single or a coupled of connected qubits and, lastly, topological systems [18], being only developed at the theoretical level. As of now, the most advanced candidates for quantum computation are the superconducting qubits and the phtonic qubit. In 2019, 53 working connected superconducting qubits on a chip have been achieved mainly from Google AI Quantum lab [19]. In near future, they plan to work with a 72-qubits chip[3]. A recent review covering the state of the art of superconducting qubits from a quantum engineer perspective is presented in [20]. In 2020, 50 connected photonic qubits have been realized by a chinese group [21]. Being able to work with such a number of connected qubits paves the way for pionner experimentations involving the quantum algorithms.

It is clear that, for the moment, superconducting qubits are ahead in the race towards a solid-state quantum computer. However it is still hard to imagine a superconducting chip hosting thousands of functional qubits. The surface of the chip and the scalability of individual qubit control are strong experimental challenges[4]. In the next section I will briefly present what should be a good qubit and how MOSFET-based qubits are still viable candidates for large scale quantum computation.

1.2 What is a good qubit ?

As presented in the last section, the 1998-to-2000 era established the main technical necessities in order for a quantum computer to be reliable in the synthetic form of the five *DiVincenzo Criteria*:

[3] https://ai.googleblog.com/2018/03/a-preview-of-bristlecone-googles-new.html

[4] However, physicists are exploring a wide range of possible feasibility, for instance: https://singularityhub.com/2020/06/22/a-new-startup-intends-to-build-the-worlds-first-large-scale-quantum-computer/.

- Scalability with well-characterized qubits. Practically, it is possible to build a system with one well characterized qubit. However it is very challenging to build a system with an arbitrary number of qubits. Currently, one of the biggest issue being faced is that one requires exponentially larger experimental setups to accomodate a greater number of qubits.

- Initialising qubits to a simple, standard state. Quantum computation is based on performing operations on states maintained by qubits and reporting the result. This procedure is strongly dependent on the initial state. In many cases, initialisation is accomplished by letting the system relaxing to the ground state. Alternate approaches, like optical pumping [22] also exist.

- Long relevant coherence times. Coherence characterizes (superposed) quantum states which carry a well defined phase. Loosing coherence is called decoherence. Decoherence is an intrisic issue experienced in large, macroscopic, quantum systems. Moreover, the more the quantum system is coupled to its environment, the more it experiences decoherence.

- A "universal" set of quantum gates. In computer science, the algorithms that we can compute are restricted by the number of gates we can implement. It has been shown that a universal quantum computer can be constructed using a very small set of 1-and 2-qubit gates. Any experimental setup that manages to have well-characterised qubits, quick, faithful initialisation, and long decoherence times must also be capable of influencing the Hamiltonian (total energy) of the system, in order to bring coherent changes capable of implementing a universal set of gates.
  In practice, the most important figure of merit is the ratio between the coherence time (previous item) and the average gate time, giving the numbers of gate operations one can perform before loosing coherence, and, thus, quantum information. In the mean time, it is desired to have a system that can be manipulated quickly so that one can interact with it as quick as possible. All together, one needs to find a trade-off between ability to implement control and decoherence.

- A qubit specific measurement capability. For any process modifying the quantum states of qubits, the final measurement of those states is of fundamental importance when performing computations. The measurement capabilities are heavily studied in the community (for instance, radiofrequency refletometry in our group).

In the framework of this thesis, the first criterion concerning scalability is of prime interest. As opposed to single-fabricated device, with a low throughput, still studied in the superconducting and semiconducting community, our group focuses on quantum dots in MOSFET silicon nanowires produced at industrial scale on 300 mm silicon wafers. Thus, all the devices studied in this manuscript come from the LETI institute, located in CEA Grenoble. The motivation has always been to study quantum effects such that charge quantization, coherence, state manipulation, readout and so on in MOSFET-derived test devices. The long term prospect is to derive and design arrays of quantum dots based on what we are learning on MOSFET-based quantum dots. This point is one main goal of the 20 years of collaboration between our laboratory and LETI.

1.3 Outline of this thesis: scalability as a commom thread

Chapter 2 gives a theoretical basis on quantum transport through quantum dots. I will present the constant interaction model for the single and double quantum dots system, insisting on the double dot stability diagram, a crucial experimental tool. I will also discuss about the measurement techniques which have evolved throughout the story of quantum dots studies and, in particular, the gate radiofrequency reflectometry. This rather new and promising probing technique could be one of the answers to the first DiVincenzo criterion thanks to its sensitivity and potential scalability.

Chapter 3 deals moslty with device fabrication. After a brief story of the MOSFET and why it has great advantages as building blocks of classical computer science, I present the guideline of the industrial process developed at CEA LETI to create the MOSFET silicon nanowires. I also point out the specific needed variations from the routine process to our custom process in order for the devices to be as optimal as it is allowed by our knowledge. A presentation of each studied device is given. The reader shall be informed that i) I worked on two different double quantum dots geometries, namely the serial and parallel configurations and ii) I worked on the two possible dopings of the nanowires, namely N-doped devices with electrons as charge carriers and P-doped devices with holes as charge carriers. I complete the chapter with the presentation of the homemade cryogenic, dual channel reflectometry setup to study quantum transport in quantum dot systems. The particularity of the setup is that it also allows one to send pulses[5] through two channels onto the device, a feature which is necessary for the experiments that I will present in Chapter 5.

[5] between hundreds of nanoseconds to a few millisecond.

Chapter 4 is dedicated to the coupling between two quantum dots. As it is presentd in the Kane and DiVincenzo's proposals , one needs to carefully control the coupling between two quantum dots. Three different degrees of freedom are compared: the backgate approach being the historical approach; the metal line approach which is a new degree of freedom and the quantum mediator approach where a quantum object is placed in between two dots. The state of the inner dot will strongly influence the coupling between the two outer dots.

Finally, Chapter 5 presents the most ambitious experiment of the manuscript related to the fifth DiVincenzo criterion, the outcome measurement of the qubit. We decided to transpose the efficient energy selective spin readout, a pulse-required probing technique, from single-fabricated semiconducting devices to our industrial MOSFET silicon nanowire devices. I will first present the principle of the experiment and the practical needs for such experiment. Then I will show preliminary stationnary results, the stability diagrams and the Coulomb diamonds of the system. Going further, we decided to measure the stability diagrams while continuously pulsing on the device, hoping to gain information about the dynamics of the system. Finally, the energy-selective spin readout is attempted. I will present the main results both at zero magnetic field and finite magnetic field. The different codes used for that experiment are presented in the appendix.

At the very end, I will give my conclusion about these three years working on quantum dots in MOSFET silicon nanowires.

La perspective d'un ordinateur quantique

Depuis 60 ans et suivant la loi dite de Moore [1] sur l'évolution du nombre de transistors par puce, le génie électrique a évolué de manière exponentielle, tant sur le plan théorique que sur les aspects techniques. Le premier transistor à effet de champ métal-oxyde-semi-conducteur, appelé MOSFET a été développé au début des années 1960 dans les laboratoires Bell par Kahng et Atalla [2]. Aujourd'hui, un processeur peut accueillir près de 20 milliards de transistors MOSFET[6]. Pourtant, même avec les plus gros processeurs et supercalculateurs, certains problèmes ne peuvent être simulés par un ordinateur classique.

En 1982 déjà, le célèbre R. Feynman s'interrogeait : est-il possible de simuler exactement les systèmes quantiques, comme les liaisons chimiques ou les réactions chimiques, avec un ordinateur standard, classique ? Dans ce document [3], un recueil de notes prises lors d'un séminaire, il est l'un des premiers[7] à parler d'un simulateur quantique universel, l'ordinateur quantique. Bien que l'idée concrète d'un ordinateur quantique ne soit pas encore claire, certains chercheurs (surtout théoriques) ont commencé à créer de nouveaux algorithmes et protocoles basés sur les lois de la mécanique quantique dans différents domaines spécifiques (par exemple un nouveau protocole, appelé BB84, en cryptographie quantique [4] déjà en 1984 ou l'algorithme de Shor [5] élaboré pour résoudre les problèmes de factorisation en nombres premiers avec un temps de calcul polynomial, 1997). L'idée de considérer des dispositifs matériels conçus pour traiter l'information de manière quantique est devenue sérieuse à la fin des années 1990.

L'analogie des bits numériques classiques sont les bits quantiques, appelés qubits. Alors qu'un bit numérique n'a que deux états disponibles, 0 ou 1, le qubit est un système quantique à deux niveaux caractérisé par sa fonction d'onde $|\psi\rangle = c_0|0\rangle + c_1|1\rangle$, une superposition des deux états propres $0\rangle$ et $|1\rangle$. Si l'on intrique N de ces qubits, cela représente 2^N états propres et donc autant de coefficients. En traitant chacun de ces coefficients en même temps, un ordinateur quantique fonctionne de manière exponentiellement plus rapide que son homologue classique.

Au début de 1998, D. Loss & D.P. DiVincenzo ont publié une proposition bien connue d'un ordinateur quantique à base de semi-conducteurs, constitué de boîtes quantiques [6].

[6] L'introduction du chapitre 3 présente une histoire plus détaillée du transistor.

[7] En 1980, le mathématicien russe Yuri Manin proposait également l'idée d'un ordinateur quantique dans son livre *Computable and Uncomputable*. Au début des années 1980, l'américain Paul Benioff fut l'un des premiers à décrire théoriquement un ordinateur fonctionnant avec les principes de la mécanique quantique.

Dans ce cas, les deux états propres des qubits sont les deux états de spin d' électrons solitaires piégés dans des boîtes quantiques couplées, hébergées dans un matériau semi-conducteur. Le calcul est réalisé en faisant varier le couplage entre les boîtes, agissant comme des portes logiques.
Plus tard dans l'année, B. Kane a publié une autre proposition pour un ordinateur quantique intégrable à grande échelle, faite de donneurs dans une matrice de silicium [7]. Dans ce cas, les 2 états de spin nucléaire des donneurs sont les états propres des qubits. Là encore, le calcul est effectué en agissant sur des grilles conductrices, en faisant varier le couplage entre les donneurs.
Enfin, toujours en 1998, J. Preskill a publié un article théorique [8] sur la possibilité d'implémenter des codes de correction d'erreurs, la capacité de surmonter la fuite d'informations quantiques due aux interactions des qubits avec leur environnement. Cette année 1998 pourrait être considérée comme l'année de naissance de la course aux ordinateurs quantiques intégrables à grande échelle.

À la suite de ces travaux pionniers, D.P. DiVincenzo a publié un autre article en 2000 [9] sur la mise en œuvre pratique de l'informatique quantique. De ce papier sont nés les *critères de DiVincenzo*, une liste de cinq exigences techniques requises pour qu'un ordinateur quantique puisse être viable. Ces points sont abordés dans la section suivante.

En conséquence, les chercheurs ont examiné de nombreux types de matériel pouvant accueillir des qubits. Les deux propositions susmentionnées concernent les matériaux semi-conducteurs. Lors de ces 20 dernières années, les hétérostructures à base d'arsénure de gallium, les boîtes quantiques dans du silicium et du silicium-germanium ont été profondément étudiées. Par exemple, en 2016 dans notre groupe, R. Maurand et al ont réalisé le premier qubit dans un dispositif PMOS en silicium [10]. Pour plus de détails sur les qubits réalisés dans du silicium et du silinium-germanium, voir [11]. En 2020, seuls quelques qubits couplés ont été réalisé dans les matériaux semi-conducteurs. Très récemment, un dispositif de quatre qubits a été démontré [12].

Les matériaux semi-conducteurs ne sont qu'une possibilité. En fait, beaucoup de systèmes différents ont été inventés et conçus tels que les ions piégés [13], les qubits supraconducteurs et les systèmes photoniques [14]. Ces trois systèmes ont fait l'objet de recherches approfondies et de nombreux réseaux de qubits ont été réalisé de manière expérimentale. Je peux aussi dire un mot sur les atomes neutres [15], les nanotubes de carbone [16], les centres NV dans le diamant [17] qui n'ont atteint qu'un seul ou peu de qubits connectés et,

enfin, les systèmes topologiques [18], qui ont été développés au niveau théorique seulement. Aujourd'hui, les candidats les plus prometteurs pour réaliser un ordinateur quantique sont les qubits supraconducteurs et les qubits photoniques. En 2019, un puce de 53 qubits supraconducteurs connectés a été réalisé par Google AI Quantum labo [19]. Dans un avenir proche, ils prévoient de travailler avec une puce de 72 bits[8]. Une revue récente sur l'état de l'art des qubits supraconducteurs d'un point de vue d'ingénieur quantique est présenté dans [20]. En 2020, 50 qubits photoniques connectés ont été réalisé par un groupe chinois [21]. Pouvoir travailler avec un nombre élevé de qubits connectés entre eux ouvre la voie à des possibles expérimentations impliquant des algorithmes quantiques.

Il est clair que pour l'instant, les qubits supraconducteurs sont en avance dans la course à l'ordinateur quantique réalisé dans un solide. Cependant, il est encore difficile d'imaginer une puce supraconductrice pouvant accueillir des milliers de qubits fonctionnels. La surface de la puce et l'intégrabilité à grande échelle du contrôle individuel des qubits sont des défis expérimentaux importants[9]. Dans la prochaine section, je présenterai brièvement ce que devrait être un *bon qubit* et comment les qubits basés sur des MOSFET sont des candidats viables pour le calcul quantique à grande échelle.

Quelles différences entre le bon et le mauvais qubit ?

Comme présenté dans la dernière section, l'ère 1998-2000 a établi les principales nécessités techniques pour qu'un ordinateur quantique soit réalisable. Elles peuvent être écrites sous la forme synthétique des cinq *critères de DiVincenzo* :

- Intégrabilité à grande échelle avec des qubits bien définis. En pratique, il est possible de construire un système avec un seul qubit bien caractérisé. Cependant, il est très difficile de construire un système avec un nombre arbitrairement grand de qubits. Actuellement, l'un des plus grands problèmes rencontrés est qu'il est nécessaire de construire des installations expérimentales exponentiellement plus grandes et complexes pour accueillir un plus grand nombre de qubits.

- Initialisation des qubits à un état simple et standard. Le calcul quantique est basé sur l'exécution d'opérations sur des états de qubits et la communication du résultat. Cette procédure est fortement dépendante de l'état initial. Dans de nombreux cas,

[8] https://ai.googleblog.com/2018/03/a-preview-of-bristlecone-googles-new.html

[9] Cependant, les physiciens explorent un large éventail de réalisations possibles, par exemple : https://singularityhub.com/2020/06/22/a-new-startup-intends-to-build-the-worlds-first-large-scale-quantum-computer/.

l'initialisation est réalisée en laissant le système relaxer vers l'état fondamental. Il existe également d'autres approches, comme le pompage optique [22].

- Long temps de cohérence. La cohérence caractérise les états quantiques (superposés) qui portent une phase bien définie. La perte de la cohérence est appelée décohérence. La décohérence est un problème intrinsèque rencontré dans les grands systèmes quantiques macroscopiques. En outre, plus le système quantique est couplé à son environnement, plus il subit la décohérence.

- Un ensemble "universel" de portes logiques quantiques. En informatique, les algorithmes que nous pouvons coder sont limités par le nombre de portes logiques que nous pouvons mettre en œuvre. Il a été démontré qu'un ordinateur quantique universel peut être construit en utilisant un très petit ensemble de portes logiques à 1 et 2 qubits. Tout dispositif expérimental qui parvient à avoir des qubits bien caractérisés, une initialisation rapide et fidèle et de longs temps de cohérence doit également permettre d'influencer l'Hamiltonien (énergie totale) du système, afin d'apporter des changements cohérents capables de mettre en œuvre cet ensemble universel de portes logiques.
  En pratique, le chiffre le plus important est le rapport entre le temps de cohérence (point précédent) et le temps moyen des portes logiques, ce qui donne le nombre d'opérations que l'on peut effectuer sur les états du qubits avant de perdre la cohérence, et donc l'information. D'un autre côté, il est souhaitable de disposer d'un système qui puisse être manipulé rapidement afin que l'on puisse interagir avec lui le plus vite possible. Dans l'ensemble, il faut trouver un compromis entre la capacité à mettre en œuvre le contrôle pour les portes logiques et la décohérence.

- Une mesure spécifique au qubit. Pour tout processus modifiant les états quantiques des qubits, la mesure finale de ces états est d'une importance cruciale lors de l'exécution des calculs. Les diférentes possibilités de mesure des états quantiques sont énormément étudiées dans la communauté (par exemple, la réflectométrie radio-fréquence dans notre groupe).

Dans le cadre de cette thèse, le premier critère concernant l'intégrabilité à grande échelle est d'un intérêt primordial. Par opposition aux dispositifs fabriqués à l'unité, à faible débit, encore étudiés dans la communauté des supraconducteurs et des semi-conducteurs, notre groupe se concentre sur les boîtes quantiques dans des nanofils de silicium MOSFET produits à l'échelle industrielle sur des plaques de silicium de 300 mm de diamètre. Ainsi, tous les dispositifs étudiés dans ce manuscrit proviennent de l'institut LETI, situé au CEA Grenoble.

La motivation a toujours été d'étudier les effets quantiques tels que la quantification de la charge, la cohérence, la manipulation des états, la lecture des états, etc. dans les dispositifs de test dérivés des MOSFET. La perspective à long terme est de concevoir des réseaux de boîtes quantiques en se basant sur ce que nous apprenons sur les boîtes quantiques créés dans les MOSFET. Ce point est l'un des principaux objectifs des 20 années de collaboration entre notre laboratoire et le LETI.

Plan du manuscrit : l'intégrabilité comme préoccupation majeure

Le chapitre 2 donne une base théorique sur le transport quantique à travers les boîtes quantiques. Je présenterai le modèle d'interaction constante pour les systèmes de boîtes quantiques simple et double, en insistant sur le diagramme de stabilité de la double boîte, un outil expérimental crucial. Je parlerai également des techniques de mesure qui ont évolué tout au long de l'histoire des études sur les boîtes quantiques et, en particulier, de la réflectométrie radio-fréquence sur grille. Cette technique de mesure plutôt nouvelle et prometteuse pourrait être l'une des réponses au premier critère de DiVincenzo grâce à sa sensibilité et à son potentiel d'intégrabilité.

Le chapitre 3 traite principalement de la fabrication des dispositifs. Après une brève histoire du transistor MOSFET et des raisons pour lesquelles il présente de grands avantages en tant qu'élément central de l'informatique classique moderne, je présente la ligne directrice du processus industriel développé au CEA LETI pour créer les nanofils de silicium MOSFET. Je souligne également les variations spécifiques nécessaires entre le procédé standard et notre procédé personnalisé afin que les dispositifs soient aussi optimaux que le permettent nos connaissances. Une présentation de chaque dispositif étudié dans ce manuscrit est donnée. Le lecteur est informé que i) j'ai travaillé sur deux géométries différentes de boîtes quantiques doubles, à savoir les configurations en série et en parallèle et ii) j'ai travaillé sur les deux dopages possibles des nanofils, à savoir les dispositifs dopés N avec des électrons comme porteurs de charge et les dispositifs dopés P avec des trous comme porteurs de charge. Je complète le chapitre par la présentation d'une expérience cryogénique autorisant deux canaux pour la réflectométrie radio-fréquence dans le but d'étudier le transport quantique dans les systèmes de boîtes quantiques. La particularité de ce dispositif est qu'il permet également d'envoyer des impulsions (entre des centaines de nanosecondes et quelques millisecondes) électriques sur deux canaux, une caractéristique nécessaire aux expériences que je présenterai au chapitre 5.

Le chapitre 4 est consacré au couplage entre deux boîtes quantiques. Comme il a été présenté dans les propositions de Kane et DiVincenzo, il faut contrôler soigneusement le couplage entre deux boîtes quantiques. Trois différents degrés de liberté sont comparés : l'approche par la grille arrière, qui est l'approche historique ; l'approche par ligne métallique, qui est un nouveau degré de liberté ; l'approche par un médiateur quantique, qui consiste à placer un objet quantique entre deux boîtes. L'état de la boîte centrale influencera fortement le couplage entre les deux boîtes extérieures.

Enfin, le chapitre 5 présente l'expérience la plus ambitieuse du manuscrit, relative au cinquième critère de DiVincenzo, la mesure de l'état du qubit. Nous avons décidé de transposer la lecture sélective en énergie du spin, une technique de sondage par impulsions des dispositifs semi-conducteurs fabriqués en laboratoire, à nos dispositifs industriels en nanofils de silicium MOSFET. Je vais d'abord présenter le principe de l'expérience et les besoins pratiques de cette expérience. Ensuite, je montrerai les résultats statiques préliminaires : les diagrammes de stabilité et les diamants de Coulomb du système. Pour aller plus loin, nous avons décidé de mesurer les diagrammes de stabilité tout en pulsant continuellement sur le dispositif, dans l'espoir d'obtenir des informations sur la dynamique du système. Enfin, je tenterai de lire le spin par sélectivité en énergie. Je présenterai les principaux résultats à la fois à champ magnétique nul et à champ magnétique non nul. Les différentes codes informatiques nécessaires à la réalisation de l'expérience seront présentés en annexe

À la toute fin, je donnerai ma conclusion sur ces trois années de travail sur les boîtes quantiques dans les nanofils de silicium MOSFET.

Chapter 2

Basics of quantum transport through quantum dots

"We must be clear that when it comes to atoms, language can be used only as in poetry."
-Niels Bohr, 1920

Résumé

Ce premier chapitre consiste en une introduction à la théorie du transport quantique à travers des boîtes quantiques ainsi qu'aux techniques de mesure pour sonder de tels systèmes.

Dans une première section, je commencerai par définir ce qu'est une boîte quantique. Je me concentrerai ensuite sur le cas d'une seule boîte quantique piégeant un grand nombre de porteurs de charge, électrons ou trous. Grâce au modèle de l'interaction constante entre les porteurs de charge piégés dans la boîte, je définirai l'énergie d'addition, énergie nécessaire pour ajouter un porteur dans la boîte. Dans ce cadre, l'énergie d'addition est constante. Suite à ce résultat, je donnerai une représentation en potentiels chimiques séparés par l'énergie d'addition, une représentation qui sera très utile pour tous les cas abordés dans ce manuscrit. Les phénomènes de pics de Coulomb et diamants de Coulomb sont présentés.
Le cas d'une seule boîte quantique contenant un faible nombre de porteurs est ensuite introduit. Je montrerai que, dans cette situation et contrairement au cas précédent, l'énergie d'addition n'est plus constante et nous sommes sensibles aux états quantiques excités.

La deuxième section est dédiée au système contenant deux boîtes quantiques. Dans ce manuscrit, ce type de système sera majoritairement étudié. Je commencerai cette section

en présentant les deux géométries possibles, les deux boîtes en série ou en parallèle. La représentation en potentiels chimiques permettra de construire l'un des outils expérimentaux les plus importants de cette thèse, le diagramme de stabilité.
La suite de cette section concerne les systèmes de deux boîtes quantiques contenant un faible nombre de porteurs. Le diagramme de stabilité est présenté dans ce cas. En outre, un mécanisme de conversion spin-charge, la lecture de spin par sélectivité en énergie, est discuté. Le dernier chapitre de ce manuscrit tentera de mettre en oeuvre un tel mécanisme de conversion spin-charge en adaptant un cryostat du laboratoire.
Enfin, cette section présentera le cas où deux boîtes quantiques sont couplées *via* une autre boîte quantique. C'est le cas du médiateur quantique. Un modèle théorique sera présenté. Cette partie servira de support pour les expériences présentées dans le chapitre 4.

La dernière section traitera des techniques de mesures. Je discuterai surtout des détecteurs de charges locaux et de la réflectométrie radio-fréquence. En particulier, cette partie expliquera pourquoi, dans notre cas, nous avons préféré la réflectométrie aux détecteurs de charges.

As discussed in the introduction, the most important system we will work with in this thesis is the quantum dot or an ensemble of coupled quantum dots. In this chapter I am going to introduce a part of the theoretical background needed to properly understand the physics related to these systems. First, I will describe the single quantum dot system both in the many carriers and in the few carriers regime. Then I will present the double quantum dot system and the so-called stability diagram. Finally, I will say a few words about the measurement technics of such systems and in particular the introduction to the gate-coupled radiofrequency reflectometry.

2.1 The single quantum dot system

The single quantum dot is a canonical system and refers to a physical entity exhibiting charge quantization due to a three dimensional confinement potential. This entity might be a dopant, a region of the space where charge carriers are accumulated or a charge trap in the material. One must understand the physics behind it before going onto more complex systems. The simplest case is the many carriers regime that I will present first. Then I will move onto the few carriers regime.

2.1.1 The many carriers regime

The single quantum dot in the many carriers regime, often called the single electron transistor, has been widely studied in many different systems: metallic nanostructures [23], GaAs heterostructures [24], silicon nanowires [25], carbon nanotubes [26], superconducting materials [27]. While the host material is very different, the model can be the same because it is essentially an electrostatic effect. Most of this part is inspired by Mathieu Pierre [28] and Max Hofheinz's [29] thesises, former students of the group who studied the single quantum dot system in the many carriers regime as well as single dopants and charge traps.

A single quantum dot can be represented by the schematic system shown in the left panel of the next figure 2.1. It consists of a small-size conducting island[1] capacitively coupled to a source, a drain and a gate. The source (drain) is supposed to be metallic and is described by a Fermi-Dirac distribution with its inflexion point at $\mu_{s(d)}$. They are the carrier reservoirs. The charge carriers are able to flow between the source and the drain through the dot. The transport is allowed because of the presence of tunnel barriers between both leads and the dot. To sum up, the gate is only capacitively coupled to the dot and the tunnel barriers between the

[1] It should be clear hereafter why the island should be small.

leads and the dot can be modeled as a capacitance and a resistor in a *parallel configuration* and is schematized by the two rectangles in the electrical schematic shown in the right panel.

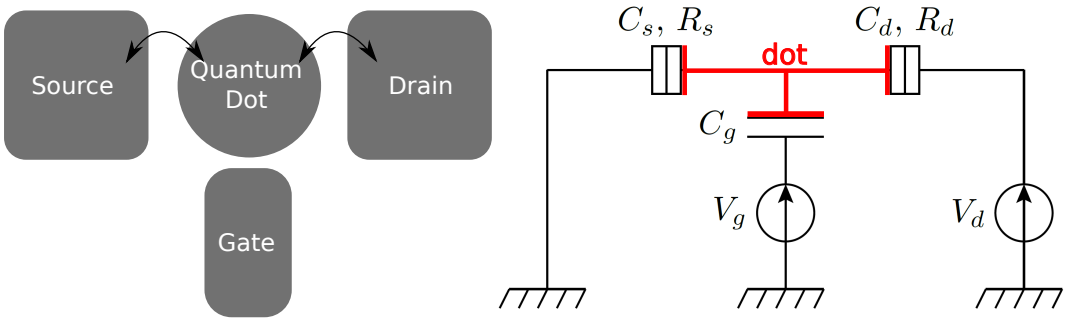


Figure 2.1 *Left panel: simple sketch of a single quantum dot tunnel coupled to the source and the drain and only capacitively coupled to the gate. Right panel: equivalent electronic schematic of that system. By applying a voltage between the source and the drain, charge carriers flow through the dot and the tunnel barriers, represented by the rectangle and characterized by a capacitance $C_{s(d)}$ and resistor $R_{s(d)}$ in parallel. By applying a voltage onto the gate, we will act on the dot only capacitively, characterized by the capacitance C_g. Eventually, we are going to modify the energy of the quantum dot. Adapted from [28].*

The simplest way to model the electrostatic of such many carriers system is the constant interaction model. It is based on the assumption that the Coulomb interactions among electrons in the dot, and between electrons in the dot and those in the environment, are parametrized by a single, constant capacitance C which is the sum of the three capacitances introduced in the right panel of the figure 2.1: $C = C_s + C_d + C_g$. Thus, the total energy $U(N)$ of a dot containing N carriers of charge q, with voltages V_s, V_d and V_g applied to the source, the drain and the gate, respectively, is given by:

$$U(N) = \frac{[qN + C_s.V_s + C_d.V_d + C_g.V_g]^2}{2C} = E_{elec}(N) \tag{2.1}$$

where q is either -|e| for electrons or |e| for holes with e the elementary charge[2]. This energy of the dot has only an electrostatic contribution. Playing with the different voltages will change the electrostatic potential of the dot.

[2]Since may 2019, the elementary charge e has been fixed in the SI and e=1.602176634e^{-19}*A.s*, exactly.

We define the electrochemical potential of the dot $\mu(N)$ as the difference in electrostatic energies of two consecutive carriers numbers, hence:

$$\begin{aligned}\mu(N) &\equiv U(N) - U(N-1) \\ &= (N - \frac{1}{2})E_C \\ &+ \frac{E_C}{q}(C_s.V_s + C_d.V_d + C_g.V_g) \\ &= \mu_{elec}(N)\end{aligned} \tag{2.2}$$

where $E_C = \frac{e^2}{C}$ is the so-called charging energy. This charging energy is inversely proportionnal to the dot size: the smaller the dot, the smaller the capacitance carried by the dot, the higher the electrostatic energy. In that many carriers regime, the contributions to the electrochemical potential is purely electrostatic. We go further and define the addition energy, the difference between two electrochemical potentials of successive occupation numbers $N+1$ and N or, equivalently, the energy needed to add 1 carrier when the dot is already occupied by N carriers:

$$E_{add}(N) = \mu(N+1) - \mu(N) = E_C \tag{2.3}$$

In the many carriers regimes, the addition energy is equal to the charging energy and does not depend on the occupation number N[3]. This energy corresponds to the energy one has to pay to put one more carrier in the dot. This characteristic energy E_C has to be compared with the temperature: if $k_BT >> E_C$, no electrostatic effect will occur since the temperature alone is able to overcome the tunnel barriers and charge the dot whereas in the opposite case $k_BT << E_C$, the energy has to be provided by the gate. This is the reason why we are working at very low temperature with small-size island, we want to be sensitive to Coulomb interactions between the carriers within the dot. In practice, a good condition is $E_C > 10k_BT$. E_C does depend on the dot capacitance. So one can associate a capacitance to a temperature: for instance, using the practical condition given earlier, a 1 fF capacitance corresponds to a temperature of T=0.185 K and a 50 aF capacitance corresponds to a temperature of T=3.7 K. The smaller the dot and the lower the temperature, the stronger the electrostatic effects will be on electrical transport.

Equation 2.3 gives a useful representation of a many carriers quantum dot and is presented in the following figure 2.2 where we consider 0K-Fermi-Dirac distributions for the source

[3]This is the reason why this model is called the constant interaction model.

and the drain. Carriers are allowed to flow through the quantum dot only when a dot chemical potential is aligned with μ_s and μ_d.

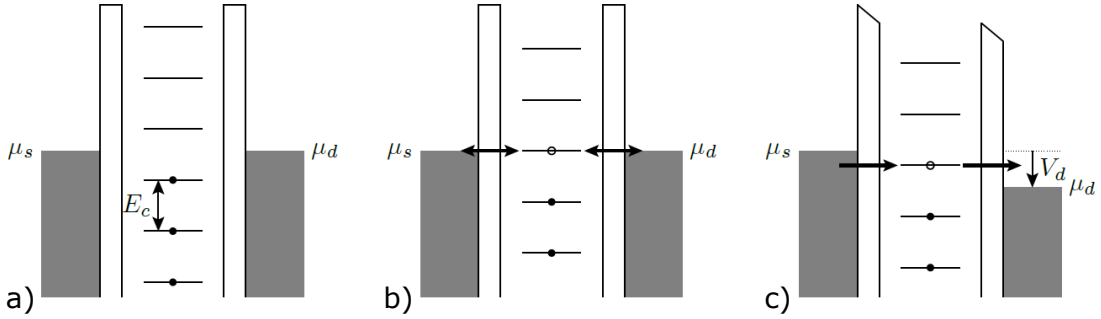


Figure 2.2 *Schematic model of the electrostatic behind the many carriers quantum dot. Three different regimes are presented. The two grey rectangles in each regime represent the 0K-Fermi-Dirac distribution of the carrier reservoirs characterized by their potential $\mu_{s(d)}$. In between is the quantum dot, represented by a regular ladder characterized by the charging energy E_c. It is connected to the leads thanks to two tunnel barriers. We basically act vertically on the ladder with the gate. In the case a), no chemical potential is aligned with the chemical potentials of the leads, no carriers flow, there is no current. In the case b), One chemical potential is aligned with the source and the gate potentials. Charges are able to flow through the dot, hence current is allowed. In the case c), we apply a voltage between the leads, opening a energetic window proportionnal to the bias voltage. Any levels, here only one, which lie in that window will contribute to the current.Taken from [28]*

This ladder of electrochemical potential can be moved up and down thanks to the gate voltage. In the case a) of figure 2.2 no electrochemical potentials of the dot is aligned with the source and drain chemical potentials, no carriers flow whereas in the case b), one chemical potential of the dot is aligned with the source-drain chemical potentials and hence, carriers flow. It is equivalent to say that the two energy levels E(N) and E(N+1) are degenerate. This is the reason why these kind of devices exhibits the so-called Coulomb Blockade regime. In the case a), the current is blocked until a potential of the dot is aligned with the source and drain thanks to the gate voltage or, equivalently, until the gate brings enough energy to counteract the Coulomb repulsion between carriers in the quantum dot. This Coulomb blockade regime can be easily revealed by the source-drain current versus gate voltage measurements and such a characteristics is presented in the following figure 2.3.

Each peak corresponds to one chemical potential aligned with the source and drain. Equivalently, the two energies corresponding to two consecutive Coulomb blockade areas are degenerate at the Coulomb peak. Between the peaks the occupation number is constant and

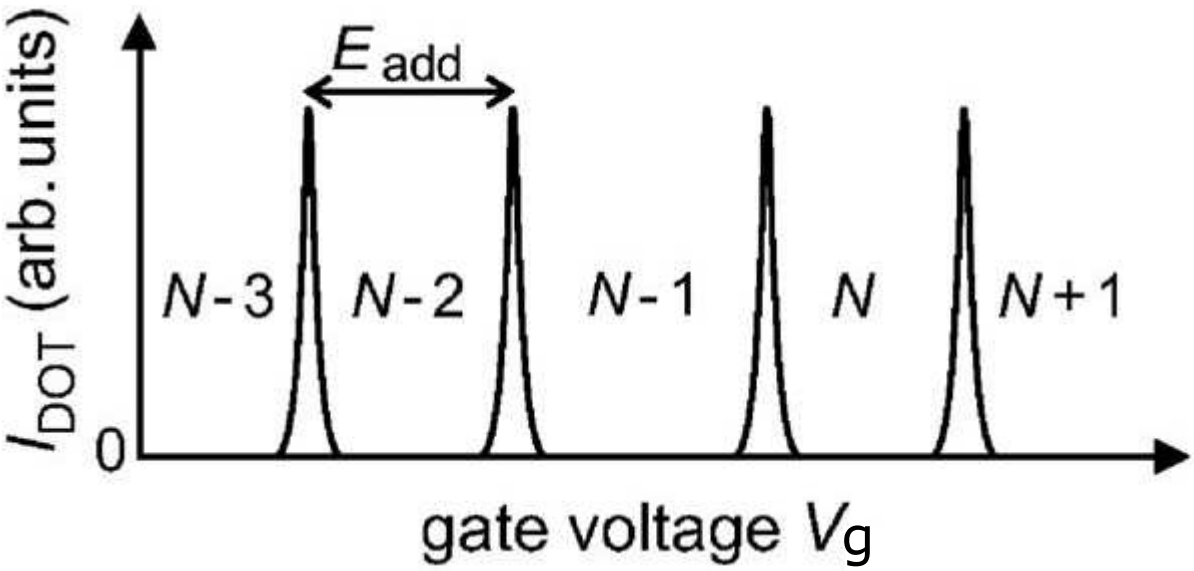


Figure 2.3 *Current between the source and the drain through the dot as a function of the gate voltage. Globally, there is no current flowing through the dot except for specific values of the gate voltage where current peaks appear, called the Coulomb peaks. Between these peaks, the current is blocked. This is called the Coulomb blockade phenomenom. In these regions, the number of carriers is constant. Practically, we can count the carriers inside the dot. Taken from [30]*

the peaks are intrisically separated by the addition energy E_{add}. However, on that graph, we do not directly extract the addition energy but rather the "addition gate voltage", ΔV_g, which is directly linked to the gate capacitance: $\Delta V_g = \frac{e}{C_g}$. In fact, in the limit scenario where the electrostatic control of the chemical potentials of the dot by the gate is maximum, 1 mV of addition gate voltage leads to 1 meV of addition energy. This is not true in realistic devices, the electrostatic control of the dot is partially done by the gate, by the source and by the drain and, thus, we define the lever-arm parameter α:

$$\alpha = \frac{C_g}{C} = \frac{C_g}{C_g + C_s + C_d} \tag{2.4}$$

This parameter gives the efficiency of the control of the dot potential by the gate.

The panels a) and b) of the figure 2.2 are representations of the system in the so-called linear regime where no (or very small) source-drain bias is applied. In the panel c), a source-drain bias $V_d = \mu_d - \mu_s$ is applied, opening what is called a bias window. This is the non-linear regime and we can now plot the source-drain current (or equivalently, the

transconductance) as a function of the gate voltage and the source-drain bias in a colormap. Such a characteristic 2D colormap is presented in the figure 2.4.

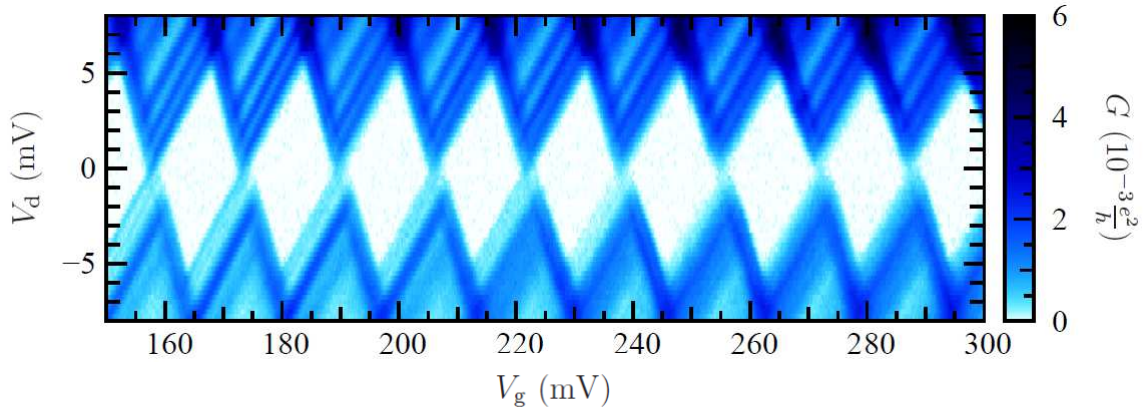


Figure 2.4 *2D-plot of the measured drain-source transconductance (equivalent to a current measurement) versus gate and drain voltages, presented in [29] showing regular so-called Coulomb diamonds. The carrier number is constant in the white region where no current flows. The half height of the diamond gives the addition energy in eV while the width between two consecutive diamond edges gives the equivalent of the addition energy but converted into gate voltage with the lever-arm parameter. In this presented case, the diamonds are pretty regular, showing a nice metallic dot in a clean region of the gate voltage paramater space.*

This 2D-plot is referred to as Coulomb Diamonds. White color indicates 0 conductance so no current flows. The darker is the blue, the higher is the conductance and the higher is the current value. The figure 2.3 can be seen as a cut along the $V_d = 0$ mV horizontal line of the figure 2.4. The reader shall wonder why we see lines out of the diamonds. This is due to the fact that in this experiment, the quantum dot is not alone but in fact, it is coupled to one or more fluctuating charges. This observation shows that a quantum dot in the metallic regime, a single electron transistor, is a very good charge sensor and, thus, it can be used as a charge detector. I will come back to this point at the end of this chapter and use this specific charge detector effect in the last chapter of the manuscript. These Coulomb diamonds are a very powerful tool for the experimentalist as it gives several informations about the system: the 2 slopes are related to the three capacitances of the systems while the half height of the diamonds gives the charging energy of the dot.

This introduction to many carriers regime/metallic quantum dots gave only the essential informations and parameters. However I coud have told much more about the theory. For instance one can calculate the current between two metallic leads through the quantum dots in different regimes. ([28], part 1.1.3-1.2, [29], chap. 2).

So far, I have considered charge states only. However, one can ask about the more interesting spin states. Theoretically, with the presence of a magnetic field, we should be able to see the spin states in the addition energy spectrum of the quantum dot because of Pauli exclusion principle. Once we pay the charging energy E_C, the next time we should pay $E_C + \Delta_{g\to e}$ with the second term being the energy splitting between two successive spin states.

This prediction of probing spin states in the many carriers regime has been seeked for a while with mitigate results. For instance the following paper [31] realized by our group measures the distribution of energy spacing in the addition energy spectrum. Although this many carriers regime has been extensively studied for the past decades, we have to go down to the few carriers regime if we really want to probe and effectively make use of spins states in such systems.

2.1.2 The few carriers regime: access to quantum states

A major advance for our group in the field of low carriers quantum dots has been done by B. Voisin and R. Maurand during their PhD and postdoc, respectively. I will present their main results inspired from Voisin's PhD manuscript and one of his papers [32].

We start from the same system presented in the figure 2.1. While in the many carriers regime the carriers lie in a continuum of orbital states within a single charge state (occupation number state), the few carriers regime offers the opportunity to populate orbital excited states. We then need to add the contribution of these excited states in the energy of the dot, equation 2.1:

$$U(N) = U_{elec}(N) + \sum_{n=1}^{N} E_n(B) \tag{2.5}$$

with the first term being the electrostatic term defined earlier and the second term taking into account the single-particle energy levels. This energy does depend on the magnetic field. The electrochemical potential of the dot will also have a contribution of this last term:

$$\mu(N) \equiv U(N) - U(N-1) \tag{2.6}$$

$$= \mu_{elec}(N) + E_N \tag{2.7}$$

with $\mu_{elec}(N)$ being the electrostatic contributions defined in equation 2.2. While we were only dealing with ground states in the many carriers regime, we now have access to single-particle excited states. To avoid confusion, we will adapt the notation of the electrochemical

potential: the electrochemical potential for a transition between the (N-1)-carrier state $|a\rangle$ and the N-carrier state $|b\rangle$ is then denoted $\mu_{a\to b} = U_b(N) - U_a(N-1)$. We can also define an addition energy:

$$E_{add}(N) = \mu(N+1) - \mu(N) = E_C + \Delta E \tag{2.8}$$

with E_c the purely electrostatic charging energy defined earlier and ΔE the energy spacing between two discrete quantum levels. ΔE can be zero when two consecutive carriers are added to the same degenerated level.

The first big difference between the many and the few carriers regimes is the value of that addition energy which is not a constant anymore and does depend on the single-particle excited states. When one introduces the first carriers into the dot, the space between the different Coulomb peaks is not constant anymore (it was the case in figure 2.3). This also means (and it is equivalent to) that the height of the Coulomb Diamond is not constant anymore too (different from 2.4). The following figure 2.5 shows experimental Coulomb diamonds in a P-type single dot realized by B. Voisin and presented in the paper [32]. The carriers are holes.

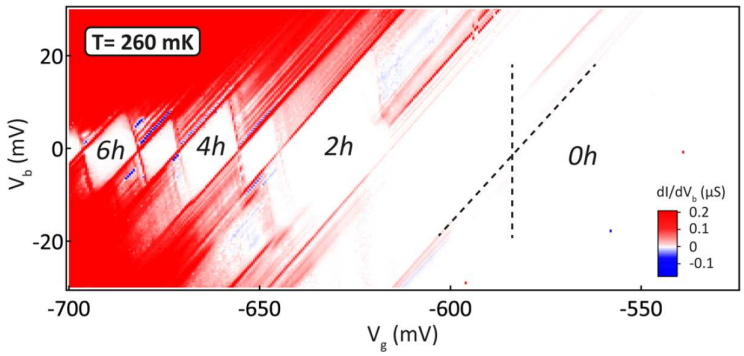


Figure 2.5 *Coulomb diamonds in the few carriers regime. Conductance as a function of gate and source-drain voltages. In that specific case, the carriers are holes. This is the reason why we increase the number of carriers carried by the dot by decreasing the gate voltage. Compare to the many carriers regime Coulomb diamonds of figure 2.4 which were regular and similar, we see that in the few carriers regime, the height of the diamonds as well as the width between two consecutive diamonds are not constant anymore. This is a strong experimental evidence that we are indeed dealing with a few carriers quantum dot. Taken from [32]*

A strong, if not a sufficient observation that we are dealing with a few carriers regime quantum dot system is the fact that for a large source-drain bias, here defined as V_b, the height

of the first diamond tend to infinity. There is no energy levels playing a role in the transport below. This is pretty clear in the figure 2.5: in the left part of the 2D plot, beyond $V_g = 600$ mV, we enter a region where the height of the Coulomb diamonds seems to be large. In fact, we could crank up the absolute value of the source-drain bias voltage and we would not see any current at all (this is also visible in [33] in a case of a double quantum dot system).

The following figure 2.6 shows on the left panel the device used during this study and the important results on the right panel. The device is a single quantum dot defined in a P-doped MOSFET device.

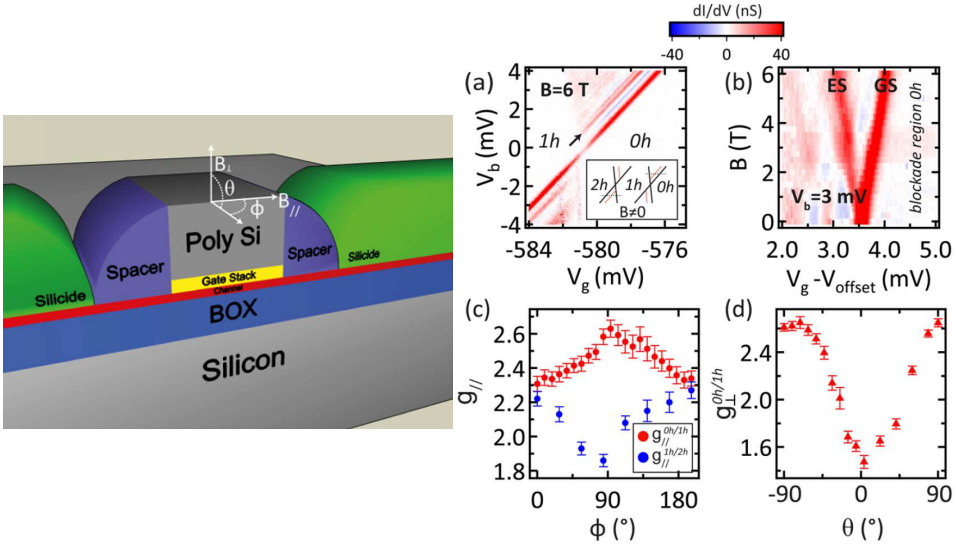


Figure 2.6 *Main results of [32]lead by B. Voisin. The paper is focused on the few holes regime. The device is shown in the left panel. It consists of a P-type MOSFET (*Metal Oxide Semiconductor Field Effet Transistor*) commonly used in electronic devices. The leads are in green, the gate in grey and the channel hosting the electrostatically defined quantum dot in red. The blue spacers ensure appropriate tunnel barriers between the leads and the dot. The whole paper discusses the asymetry of the first holes transitions g-factor involved in the Zeeman energy relation:* $\Delta E_Z = g.\mu_B.||\vec{B}||$ *with* μ_B *being the Bohr magneton.*

The main result of that paper is the measurement of the anisotropy of the g-factor g appearing in the Zeeman formula giving the splitting of spin states as a function of the magnetic field orientation $\Delta E = g.\mu_B.||\vec{B}||$. I am going to briefly present the result. They started looking at the evolution of the first Coulomb peaks, or equivalently the spacing between two transitions in the Coulomb diamonds 2D-plot, as a function of the magnitude of a magnetic field for a given direction of that field. This is presented in the figures a) and b) of the right panel of the figure 2.6. They also recorded that spacing for different orientations of

the magnetic field for a given amplitude. Thanks to the Zeeman formula, it is possible to plot the Zeeman g-factor as a function of the orientation of the magnetic field and they show that this g-factor is asymetric, figures c) and d) of the right panel of the figure 2.6. It does depend on the orientation of the magnetic field and on the occupation number of the dot, hence on V_g. For electrons, the g-factor is always close to 2. Here we see that, for different magnetic field orientations and occupation numbers, the g-factor spans between 1.5 and 2.5. For a 1T magnetic field and an electron g-factor equals to 2, the Zeeman energy spacing is roughly equal to $\Delta E \approx 110\ \mu$eV.
This work on a P-type single quantum dot in the few carriers regime has lead to the realization of the first silicon CMOS hole spin qubit presented in 2016 in R. Maurand's paper [34].

The single quantum dot device is the canonical system. I have presented what I consider to be the most important concepts for this system both in the many carriers and the few carriers regime, namely the charging energy, the addition energy, the Coulomb diamonds. In quantum transport through quantum dots, the next natural step is the study of the double quantum dot system, where two dots are involved in the charge transport. The next part is dedicated to the double quantum dot system.

2.2 The double quantum dot system

The double dot system offers a richer physics than the simple quantum dot. Lots of practical realizations are available. Beyond the materials involved, the elementary configurations are the serial or parallel ones. The theoretical description is basically the same. First, I will present the double quantum dot for spinless particles then I will introduce the spin in the system.

2.2.1 The many carriers regime and the stability diagram

As I said just before, the double quantum dot system gives rise to much more interesting physics. Most of this part is inspired by the Review of Van Der Wiel et al. [35] which gives the main ideas behind the many carriers double quantum dot system. I shall say that I will not talk about current modeling in quantum dots, the interesting reader can find a detailed study in [36].

I shall start first with the configurations. The following figure 2.7 presents the two main electronic networks studied in the double quantum dot system. The top panel represents the serial, also called the pump configuration, and the bottom panel represents the parallel, often called face-to-face in this manuscript, configuration. The two configurations will be discussed in this manuscript.

The two dots 1 and 2 are represented by the circles and denoted with their occupation number N_1 and N_2. Both are capacitively coupled to their own gate G_1 and G_2, respectively, characterized by the capacitances Cg_1 and Cg_2. I shall remark that for the sake of simplicity, I do not take into account the cross-capacitances between the gate 1 and the dot 2 and the opposite. As previously defined, the rectangles represent the tunnel barriers of the system modeled by a capacitance and a resistor in parallel, allowing carriers to flow. The source is grounded and the drain can be biased with the voltage V_{ds}. There are two kinds of tunnel barriers: the ones connecting the leads and the dots, responsible for dot-lead charge transitions and the one between the dots, responsible for interdot charge transitions.

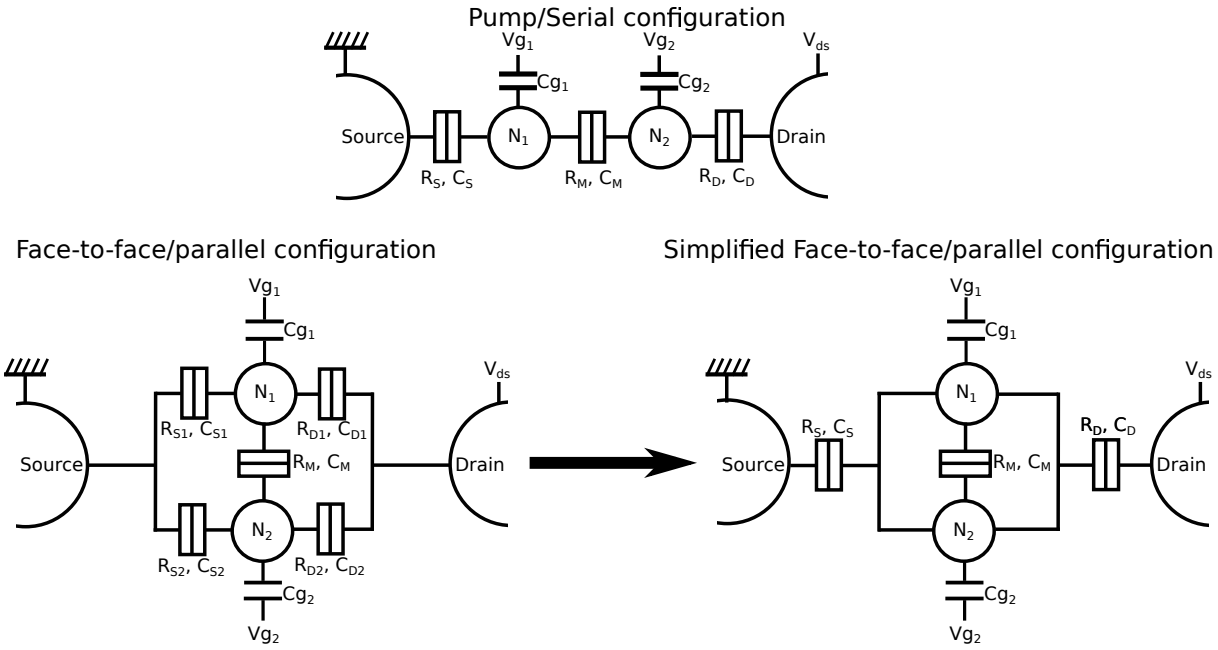


Figure 2.7 *Two main configurations of the double quantum dot system. The two circles represent the quantum dots, characterized by their occupation number N_1 et N_2. Each quantum dot is capacitively coupled to their own gate through the capacitances Cg_1 et Cg_2. The gates can be biased with Vg_1 et Vg_2, as well as the channel with V_{ds}. The rectangles indicate tunnel barriers, caracterized by a resistor and a capacitance in parallel. They appear between the leads and the dots and between the dot themselves. Top panel: pump configuration. The charge carriers have to flow trough both quantum dots in order to create current. Bottom panel: face-to-face configuration. the two dots are two channels in parallel. Current will flow if charge carriers pass either trough one dot or the other. The following theoretical model will be valid for the pump and for the simplified face-to-face configurations.*

We will model the double dot system in the same way we modeled the single dot system. For a zero voltage source-drain bias, the total electrostatic energy of the system is given by (the derivation of the formula is presented in the appendix of [35]):

$$U(N_1,N_2) = \frac{1}{2}N_1^2 Ec_1 + \frac{1}{2}N_2^2 Ec_2 + N_1 N_2 Ec_m + f(Vg_1,Vg_2) \tag{2.9}$$

with

$$\begin{aligned} f(Vg_1,Vg_2) = &\frac{1}{q}\{Cg_1 Vg_1(N_1 Ec_1 + N_2 Ec_m) + Cg_2 Vg_2(N_1 Ec_m + N_2 Ec_2)\} \\ &+\frac{1}{e^2}\{\frac{1}{2}Cg_1^2 Vg_1^2 Ec_1 + \frac{1}{2}Cg_2^2 Vg_2^2 Ec_2 + Cg_1 Vg_1 \frac{1}{2}Cg_2 Vg_2 Ec_m\} \end{aligned}$$

where $Ec_{1(2)}$ is the charging energy of each dot 1(2), Ec_m is the electrostatic coupling energy between the two dots, and q is -|e| for electrons or |e| for holes. The coupling energy Ec_m is the change in the energy of one dot when a charge carrier is added to the other dot. These energies depend of the capacitances of the system:

$$Ec_1 = \frac{e^2}{C_1}\left(\frac{1}{1-\frac{C_m^2}{C_1C_2}}\right) \tag{2.10}$$

$$Ec_2 = \frac{e^2}{C_2}\left(\frac{1}{1-\frac{C_m^2}{C_1C_2}}\right) \tag{2.11}$$

$$Ec_m = \frac{e^2}{C_m}\left(\frac{1}{\frac{C_1C_2}{C_m^2}-1}\right) \tag{2.12}$$

where $C_{1(2)}$ is defined as the total capacitance for dot 1(2): $C_{1(2)}= C_{S(D)}+Cg_{1(2)}+ C_m$.

These two charging energies Ec_1 and Ec_2 are very close to the one I defined in equation 2.2 for a single, uncoupled quantum dot. The difference is the multiplying correction factor which strongly depends on the coupling capacitance C_m. When C_m tends to 0, hence Ec_m also tends to 0, equation 2.9 simplifies and we recover the sum of the energies of two single independant quantum dots.

$$\begin{aligned} U(N_1,N_2) = &\frac{(N_1q+Cg_1Vg_1)^2}{2C_1} \\ &+\frac{(N_2q+Cg_2Vg_2)^2}{2C_2} \end{aligned} \tag{2.13}$$

In the opposite case where C_m becomes the dominant capacitance, $\frac{C_m}{C_{1(2)}} \to 1$, the electrostatic energy is expressed as:

$$U(N_1,N_2) = \frac{\left[(N_1+N_2)q+Cg_1Vg_1+Cg_2Vg_2\right]^2}{2(C_{1,out}+C_{2,out})} \tag{2.14}$$

This is the energy of a single quantum dot occupied by N_1+N_2 charge carriers and a capacitance of $C_{1,out}+C_{2,out}$ defined as the capacitances of each dot to the outside world: $C_{1(2),out}=C_{1(2)}-C_m$. Thus we see that a large interdot capacitance C_m effectively leads to one big dot.

We just expressed the electrostatic energy of the double dot system. As we did for the single quantum dot system, we will now define the electrochemical potentials of each independant dot, $\mu_{1(2)} = (N_1, N_2)$ of the dot 1(2) as the energy needed to add the $N_{1(2)}$th carrier to the dot 1(2) while having $N_{2(1)}$ carriers on dot 2. Thanks to the equation 2.9, we calculate the two electrochemical potentials:

$$\begin{aligned}\mu_1(N_1,N_2) &\equiv U(N_1,N_2) - U(N_1-1,N_2) \\ &= (N_1 - \frac{1}{2})Ec_1 + N_2 Ec_m \\ &+ \frac{1}{q}(Cg_1 Vg_1 Ec_1 + Cg_2 Vg_2 Ec_m)\end{aligned} \tag{2.15}$$

and

$$\begin{aligned}\mu_2(N_1,N_2) &\equiv U(N_1,N_2) - U(N_1,N_2-1) \\ &= (N_2 - \frac{1}{2})Ec_2 + N_1 Ec_m \\ &+ \frac{1}{q}(Cg_2 Vg_2 Ec_2 + Cg_1 Vg_1 Ec_m)\end{aligned} \tag{2.16}$$

At fixed gate voltage, if N_1 is changed by 1,. We recover here the same results than in the many carriers regime single quantum dot case where the energy difference between two consecutives electrochemical potentials is equal to the charging energy of the dot. Similarly, the addition energy of the dot 2 is equal to Ec_2, the charging energy of the dot 2. Moreover, $\mu_1(N_1,N_2+1)$-$\mu_1(N_1,N_2)$ =$\mu_2(N_1+1,N_2)$-$\mu_2(N_1,N_2)$=Ec_m.
From these electrochemical potentials 2.15 and 2.16 we can build the so-called stability diagram.

The double dot charge stability diagram

The charge stability diagram is one of the most important experimental tools to study double quantum dot systems. Originally, it consists of a 2D-plot of the source-drain current, exhibiting equilibrium charge number regions, N_1 and N_2, as a function of the two topgate voltages Vg_1 and Vg_2. In the last section of that chapter, I am going to introduce another way to probe the double dot system by recording the stability diagram with gate-based radiofrequency reflectometry.

We want to construct a diagram showing constant number of carriers in the dots. We start by defining the electrochemical potentials of both source and drain, μ_S and μ_D. In the case

where V_{ds}=0 V, μ_S=μ_D=0, the equilibrium charges on the dots result on constraints: first, N_1 and N_2 must be integers. Second, both electrochemical potentials $\mu_1(N_1,N_2)$ and $\mu_2(N_1,N_2)$ must be less than 0. If either is larger than 0, charges escape from the dots to the leads. These two constraints create domains, mostly heaxagonal, in the Vg_1, Vg_2 2D-plot.
The next figure 2.8 presents standard cases of stability diagrams.

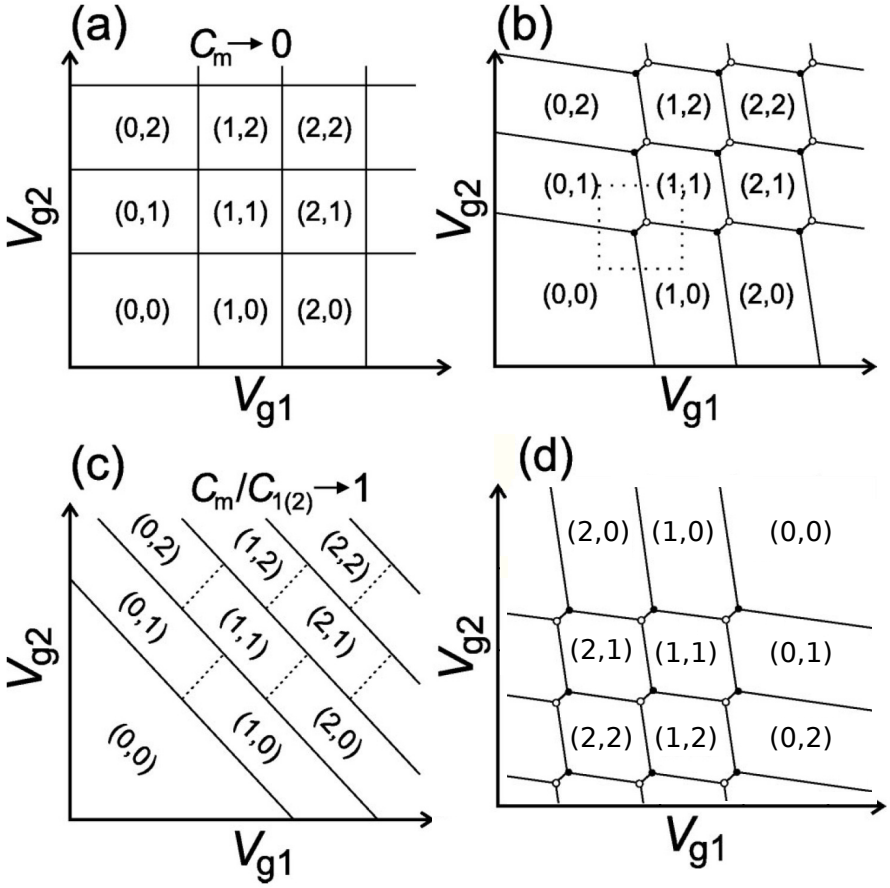


Figure 2.8 *Double quantum dots stability diagram. Domains of charge equilibrium in the (Vg_1,Vg_2) phase space. The panel a represents two uncoupled quantum dots: charging one dot has no effect on the other dot. The panel b shows a stability diagram for two coupled quantum dots. The corners of the former square domains have become pairs of points, called the triple points. In the panel c, the coupling is the dominant parameter, the two dots have merged in one single dot carrying N_1+N_2 carriers. These three diagrams are true for electrons. The last panel d shows a stability diagram for two coupled quantum dots populated with holes instead. Inspired by [35].*

The first case represented in figure 2.8.a occurs when the two dots are completely decoupled, C_m=0, associated to the equation 2.13. We change the number of charges in the dot

1(2) by changing the gate voltage $Vg_{1(2)}$, without affecting the charges on the other. This is characterized by square areas in the stability diagram. When the two dots start being coupled, the domains of equilibrium charges go from square to hexagonal. This is shown in figure 2.8.b. The corners of the domains becomes pairs of points called triple points. Such a pair of triple points is surrounded by a dashed square in the figure. If we continue to crank up the coupling till C_m becomes the dominant capacitance, $\frac{C_m}{C_{1(2)}} \rightarrow 1$, the maximum in the triple point separation is reached. This is shown in the figure 2.8.c where the double dots system behaves like one dot with the charge number N_1+N_2, associated to the equation 2.14 . This regime is characterized by antidiagonals in the stability diagram. These first three panels are true for negative charge carriers, the electrons. The last panel 2.8.d shows the stability diagrams of two coupled dots populated with holes instead. The full figure is reversed. Instead of increasing the number of electrons by increasing the gate voltage, here we increase the number of holes by decreasing the gate voltage.

The electrochemical potentials were also useful to represent a single quantum dot between two leads, see figure 2.2. We will also model the double quantum dot system in that manner and illustrates the stability diagram with this representation. The following figure 2.9 is a zoom of the dashed square in the figure 2.8b. so the carriers are electrons. The two coupled triple points are represented by the black and white points. The solid lines split the diagram in four regions of different charge configuration: either both dots contain no electrons and, thus (N_1, N_2) = (0,0) being the bottom left quadrant. Then, one dot can carry one electron while the other one is still empty. It corresponds to the top left and bottom right quadrant, (N_1, N_2) = (0,1) and (N_1, N_2) = (1,0), respectively. These two areas are separated by what is called the interdot transition line. On this particular line, both the electrochemical potentials of the dots and the ones of the leads are aligned $\mu_s = \mu_d = \mu_1(1,0) = \mu_2(0,1) = 0$. Finally there is the (N_1, N_2) = (1,1) region, top right quadrant, where both quantum dots carry an electron. All the solid lines but the interdot transition line are called the dot-lead transition lines. These dot-lead transition lines correspond to an alignement of one quantum dot electrochemical potential with its adjacent lead electrochemical potential.

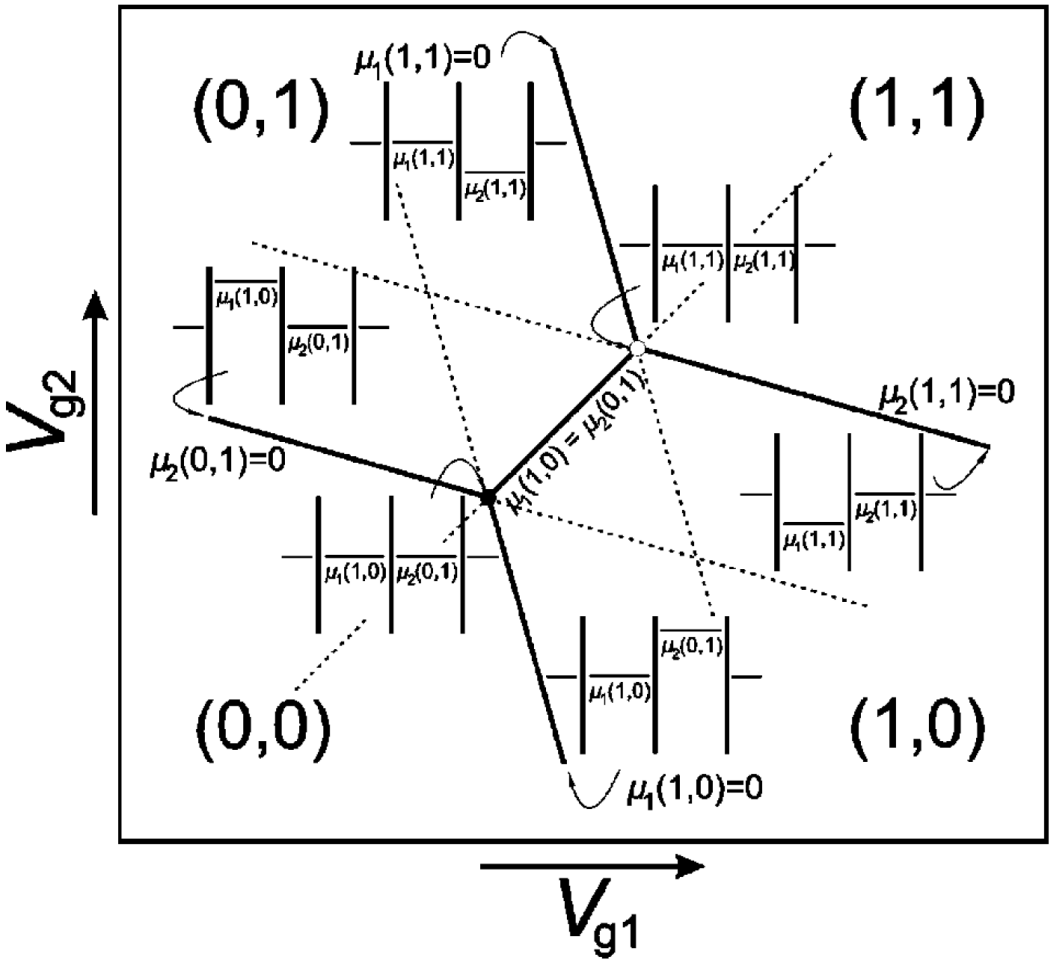


Figure 2.9 *Zoom in the dashed square of the figure 2.8b, showing 4 different domains corresponding to 4 different quantum dot configurations: (0,0), (1,0), (0,1) and (1,1). These domains are separated by the dot-lead-transition lines and the interdot transition line. The latter is located in between the two black and white points, the triple points. The dashed lines are the extensions of the solid lines. In that figure we do not only see the domains in the stability diagram but also the four electrochemical potentials of the system, represented in the same way we represented the single quantum dot (see figure 2.2), at different places in the diagram. In particular we see the alignment of the four electrochemical potentials, the two of the leads and the two of the dots, at the triple points. We can also see that, on a dot-lead transition line, the electrochemical potential of one of the dots is aligned with the one of the adjacent lead. Taken from [35].*

The reader shall wonder that we are in the many carriers regime section and I am presenting a portion of the stability diagram where the maximum number of electrons in a dot is 1. In fact, the electrochemical potentials represented in the previous figure 2.9 are *charge states*

and do not taking into account the spin. I could also say that we are only dealing with the ground states of the dots.

The stability diagram gives access to interesting parameters. In particular, we can relate the dimensions of the honeycomb cells appearing in the figure 2.8.b to capacitances of the system using the equations 2.15 and 2.16 and the following condition $\mu_1(N_1,N_2;Vg_1,Vg2) = \mu_1(N_1+1,N_2;Vg_1+\Delta Vg_1,Vg2)$: we end up with

$$\Delta Vg_1 = \frac{|e|}{Cg_1} \tag{2.17}$$

and, similarly we derive

$$\Delta Vg_2 = \frac{|e|}{Cg_2} \tag{2.18}$$

In the same spirit, we can derive others relations using a similar condition:$\mu_1(N_1,N_2;Vg_1,Vg2) = \mu_1(N_1,N_2+1;Vg_1+\Delta Vg_1^m,Vg2)$ and we can write

$$\Delta Vg_1^m = \frac{|e|C_m}{Cg_1C_2} = \Delta Vg_1\frac{C_m}{C_2} \tag{2.19}$$

and, similarly

$$\Delta Vg_2^m = \frac{|e|C_m}{Cg_2C_1} = \Delta Vg_2\frac{C_m}{C_1} \tag{2.20}$$

These four figures of merit are illustrated in the figure 2.10 showing a typical honeycomb lattice.

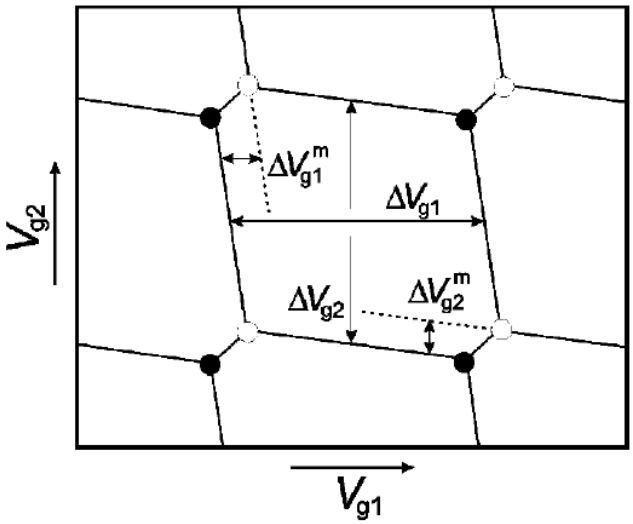


Figure 2.10 *Zoom on an elementary honeycomb cell, characteristic of a couple double dot system. The four figures of merit $\Delta V g_1$, $\Delta V g_2$, $\Delta V g_1^m$ and $\Delta V g_2^m$ are defined in the main text and are related to the capacitances of the system. Extracted from [35].*

I just presented what would be the most occuring case in this manuscript, the many carriers regime, coupled double dot system. During this PhD, I have measured different devices and have extracted a lot of different stability diagrams. The following figure 2.11 presents some examples of such diagrams.

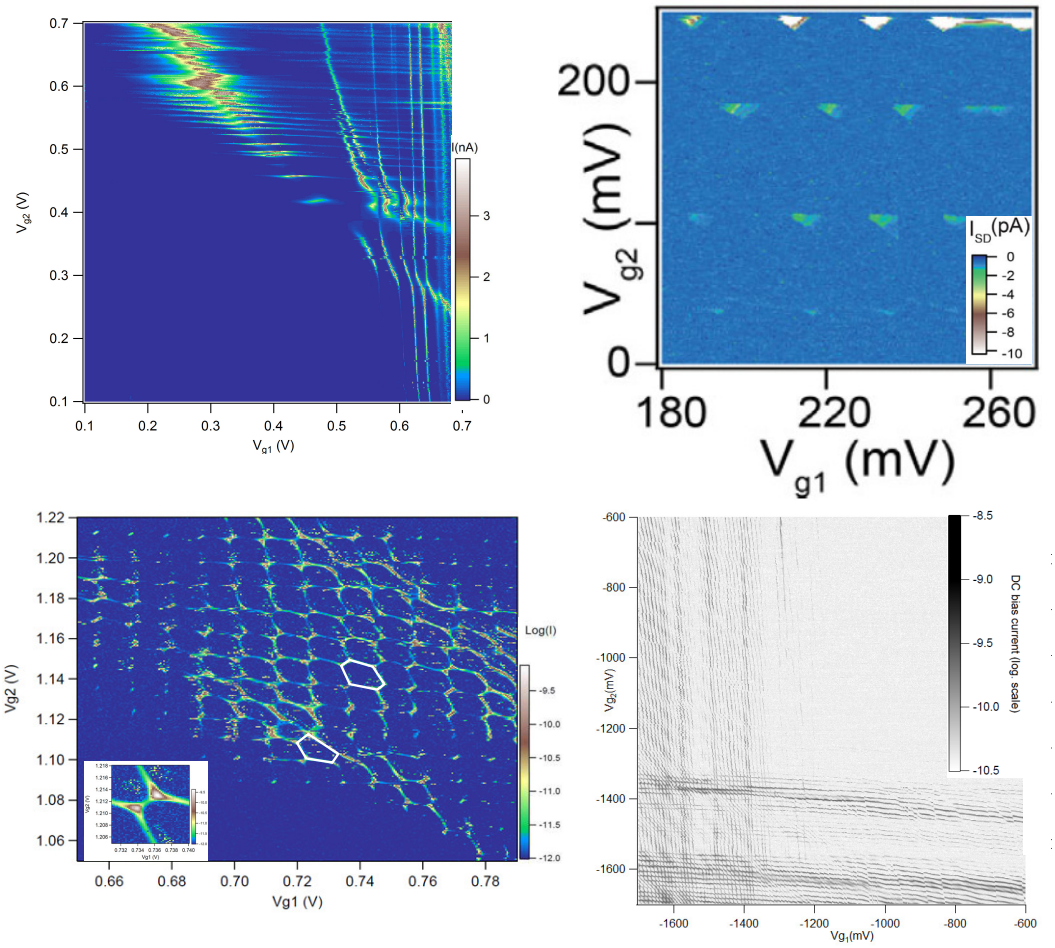


Figure 2.11 *4 different stability diagrams probed on 4 different devices. Top left panel: N-type face-to-face device like the one presented in figure 3.14. The transition lines appear when the topgate voltages increase as well and, moreover, they are fully visible, not only at the triple points like in the top right panel. This following stability diagram is taken from [37]. The device was a N-type pump with the gates in a serial configuration. In that configuration, we cannot access the full transition lines but only the triples points. Here they appears as triangles and I will explain why in the next section. The bottom left quadrant represents a beautiful honeycomb pattern, signature of strongly coupled double dot system. The N-type device associated to that measurement is shown in the figure 3.15. The two topgates are in series and, like in the previous example, we should have only access to the triple points. This is clearly not the case here. The results presented in the chapter 4 have revealed the presence of a third smaller quantum dot emerging from a small group of dopants located between the two gates. This third, different, quantum dot is very likely responsible for this huge coupling between the two dots. The last bottom right quadrant was measured on a P-type Face to face devive. The transition lines appears when one decreases the topgate voltages and these transition lines are fully visible.*

The top left diagram is presented in chapter 4, figure 4.2a and represents the DC source-drain current as a function of both topgate voltages. Blue corresponds to no current and yellow/brown to high current. There is no current in the bottom left diagram, when the gate voltages are low. Transition lines start appearing when we increase the gate voltage. For high gate voltages, above 0.5V the two families of lines, horizontal and vertical, start crossing each other. We are in the case of the figure 2.8, diagram a. The device is a N-type system. The carriers are electrons. At the crossing points, the two triple points are overlapped so the two dots are almost independant, $C_m \to 0$. I shall add another thing: in that diagram, we see the full transition line all across the diagram, when we see it. This is due to the fact that the device is a face-to-face. Both electrostatically defined quantum dots are a channel for a source-drain current. If an electrochemical potential of any dot is aligned with the source and drain electrochemical potentials, the charges will flow and we will measure a current.
On top of the 2D stability diagram we can also see two non straight lines interacting with the dot-lead transition lines showing high current. These lines seem to be related to a dopant or dopants. In that parameter space, the electronic system is then composed of two electrostatically defined quantum dots in parallel plus another quantum dot made of dopants.

The top right panel shows a zoom on a stability diagram presented in the paper [37]. The device is also a N-type device and the DC source-drain current is recorded as a function of the two topgate voltages. The major difference with an equivalent area in the previous diagram[4] is the absence of dot-lead transition lines. Here, the device is clearly a pump device with the topgates in a serial configuration. It means that the two dots form one unique channel, both dots must have an electrochemical potential aligned with the ones of the leads. The consequence is that we only see current at triple points. In that specific case the triple points are in fact triangles, this will be explained in the next section.

The bottom left quadrant correponds to the figure 4.8 in chapter 4. The DC source-drain current is recorded as a function of two topgate voltages. This measurement shows a pretty nice double dot stability diagram like we saw in the figure 2.11, diagram b. The two dots are strongly coupled and, even though the two dots are in serie, we see the dot-leads transition line, the edges of the honeycomb pattern. This was a very surprising measurement. The point is that the device is not a perfect double dot in serie. Between the two dots, there is a third, way smaller dot formed with a group of dopants. This particular device is at the heart of the last part of the chapter 4.

[4] Which would be located in the top right quadrant.

Finally, the bottom right quadrant is presented in chapter 5, figure 5.2. The DC current is one more time recorded. White means no current and black represents current. While in the three last diagrams the carriers were electrons, here the carriers are in fact holes. A big clue is the absence of charge transition lines in the upper right quadrant. It means that we need to decrease the topgate voltages in order to find such transition lines, characteristic of hole devices. We recover here the diagram d of the figure 2.8.

The double quantum dot system can be achieved in quite a lot of configurations. However, if we want to study spin physics in such system, we need to go down to the few carriers regime. Indeed, this regime allows to probe the quantum states as we saw in the single quantum dot section. Now I am going to tell a few words about this regime.

2.2.2 The few carriers regime and energy selective spin readout

The few carriers regime has already been described in the case of a single quantum dot. I will follow what has been done for the single quantum dot and extend the model for the double quantum dot system.

We just saw that, in the many carriers regime, the addition energy is always equal to the charging energy, which is a pure electrostatic contribution, for both single and double quantum dot systems. However, we also saw that, in a few carriers regime single quantum dot system, the addition energy differs from the charging energy, see equation 2.8. Indeed, in the latter situation this addition energy is the sum of the charging energy plus the energy spacing between two consecutive levels. We can do the same kind of calculus to find the addition energy of the dot 1:

$$E_{add,1}(N_1,N_2) = \mu_{1,m}(N_1+1,N_2) - \mu_{1,n}(N_1,N_2) = E_{C1} + (E_m - E_n) = E_{C1} + \Delta E \quad (2.21)$$

and, similarly we find $E_{add,2}(N_1,N_2) = E_{C2} + \Delta E$ with ΔE being the energy difference between two consecutives quantum levels. When the energy levels are spin-degenerate, ΔE is zero. In that few carriers regime, the four figure of merits illustrated in the figure 2.10 evolve as follow:

$$\Delta V g_{1(2)} = \frac{|e|}{C g_{1(2)}} \left(1 + \frac{\Delta E}{E_{C1(2)}}\right) \quad (2.22)$$

$$\Delta V g^m_{1(2)} = \frac{|e| C_m}{C g_{1(2)} C_{2(1)}} \left(1 + \frac{\Delta E}{E c_m}\right) \quad (2.23)$$

The equation 2.21 coupled to the previous figure 2.3 presenting the Coulomb peaks shows that a strong characterisitic of the few carriers regime is the unregular spacing between the Coulomb peaks.

As explained in the single quantum dot section, a simple way to experimentally access the quantum states is referred to as the non-linear regime. In that regime, the excited states start playing a role in the charge transport. The next figure 2.12 illustrates that regime. We assume that the drain lead is grounded ans we apply the bias V to the source lead. Thus the chemical potential of the source is given by $\mu_s = -|e|V$. This is basically the same diagram as the one presented in the figure 2.9 except that we apply a source-drain bias voltage. The consequences of such applied source-drain bias in the stability diagram in the canonic case of only one ground state and one excited state per quantum dot are quite clear. It opens what is called the bias triangles, regions in the stability diagram where not only ground states but also excited states can contribute to the transport. In the electrochemical potential representation, the ground states are in black while the excited states are in grey. Such bias triangles have been measured during this PhD. Some of them are presented in chapter 4, figure 4.10.

Spin states are a specific kind of quantum states. They are reavealed with an applied magnetic field through the Zeeman effect. In the following, I will not detail all the spin physics in quantum dots. If the reader wants to know more about coherent manipulation of spin states, magnetospectroscopy, spin orbit interaction, state relaxation through phonons, spin states in two-electron quantum dots or Pauli spin blockade, the review [30] for instance gives a solid background. I am just going to present one way for the spin readout of the system or, equivalently, how can we probe the spin of a charge in such system ?

So far we were considering recording the stability diagram and, thus, the transition lines with a DC current measurement. However, even though we could probe the excited states in the non-linear regime, we are not sensitive to the spin states. We have to proceed to what is called a *spin-to-charge conversion* and this point is a cornerstone. In the quantum dot community, some solutions have been found such that Pauli spin blockade readout used in the first CMOS hole spin qubit realized within the group [34] or latched charge sensing mechanism [38], for instance. Other readout fashions have been exploited. I am going to present the so-called *energy selective spin readout*.
Indeed, the chapter 5 is dedicated to this readout method which has never been set up in our CMOS devices. In particular, this kind of spin readout is very powerful as it allows for *single-shot* spin readout[39], [40]. Instead of doing a sufficient number of independent

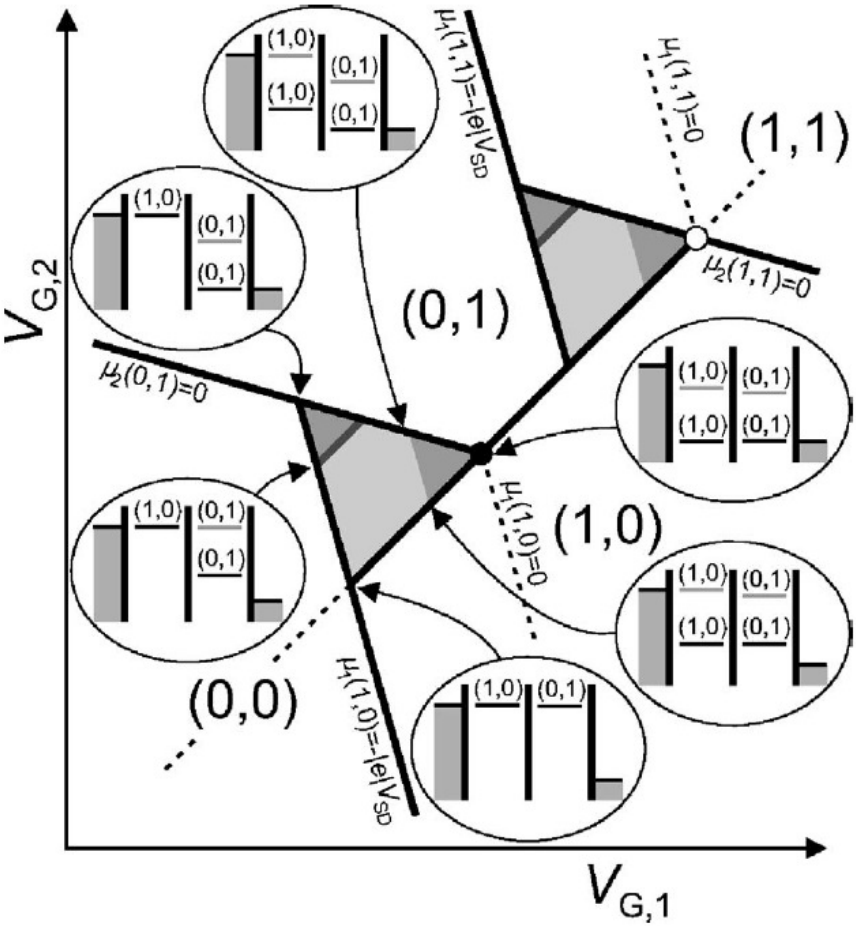


Figure 2.12 *Same region of the stability diagram than the one presented in the figure 2.9 except that we are applying a source-drain bias voltage V. This bias opens a window of energy between the source chemical potential $\mu_s = -|e|V$ and the lead chemical potential $\mu_d = 0$ as shown in the multiple chemical potentials representation where ground states are in black and excited states in grey. This window allows transport over a wide range of topgate voltages. This is clearly visible on a stability diagram where triangle areas, often called bias triangles arise near the triple points. The lines appearing inside the triangles correspond to charge transport through at least one excited states. Taken from [30].*

measurements to be averaged in order to be able to yield a result, in contrast a single-shot measurement does not need the repetition of the experiment.

Energy selective spin readout

The principle of the energy selective spin readout is presented in figure 2.13 and more in details in [30], section VI, B. It is also detailed in [41] or [39]. It consists of a dynamical experiment where one has to pulse (typically over microseconds time scale) onto a topgate.

The canonical system is a single quantum dot connected to only one carrier reservoir probed with a charge detector like a QPC (standing for *Quantum Point Contact*) or a SET (standing for *single electron transistor*)[5]. The device is submitted to a magnetic field in order to split the spin states. The top left panel a) shows the full pulse sequence and the middle left panel b) presents the typical result when one probes a nearby charge detector [6]. The last bottom left panel c) gives a representation in terms of chemical potentials of the charge displacement under such pulse conditions. The right panel shows a typical 2D-plot of that measurement [39]. In that plot, the current of the SET, the charge detector in that setup, is plotted as a function of time in x and as a function of the read-level voltage in y. I am now going to detail each step, the empty state, the inject & and wait stage and the readout stage.

The aim of this dynamical manipulation is to proceed to a spin-to-charge conversion. We are going to cleverly use the Zeeman splitting between two spin states.
The first (and last) pulse stage is the *empty stage*, simply pulling up the two chemical potentials of the two spin states above the lead chemical potential in order to empty the quantum dot. At this stage, the quantum dot occupation number is 0 and the detector gives a reference current value corresponding to N=0.
The next stage is the *inject & wait stage* where one fills the quantum dot by pushing down the chemical potentials for a certain duration t_{wait} by increasing the gate voltage. The panel b) shows a sharp increase at the beginning of the inject & wait stage. This is not the signal we have to look at. In fact, this is a direct consequence of the capacitive coupling between the QPC and the gate (more informations in [42]). After a certain amount of time, the tunneling time, one carrier has come into the quantum dot, either in the spin up state or in the spin down state. At this point, indicated by the vertical arrow, ΔI_{QPC} decreases instantly for a small amount and the detector gives its reference current value corresponding to N=1, giving the information about the carrier occupation of the quantum dot.
The next and most important stage is the *readout stage* during the time t_{read} where one has to push up the chemical potentials until the core configuration where the spin down state is above the chemical potential of the reservoir and the spin down state is below the chemical potential of the reservoir. This configuration allows only for a the spin down carrier to tunnel out of the quantum dot[7] whereas a spin up carrier will stay in the quantum dot. This is the spin-to-charge conversion step. If the spin is down, the detector will probe a charge displacement between the dot and the reservoir. In the other case, if the spin is up, no charge

[5] the next section 2.3 is dedicated to measurement techniques

[6] which I will present later. As of now, the reader only has to know that a charge detector is very sensitive to charge displacement, with or without a net DC source-drain current.

[7] followed by another carrier tunneling in the quantum dot.

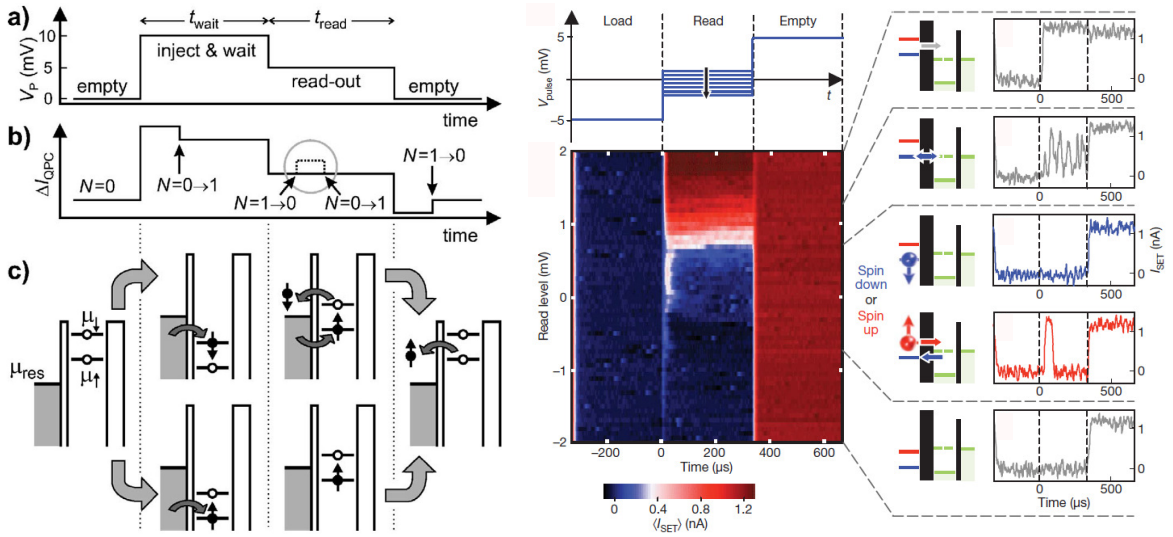


Figure 2.13 *Left panel: Energy selective spin readout principle. The two spin states must be splitted by a magnetic field, for instance. This readout scheme requires pulse sequences. The panel a) presents such typical sequence consisting of a succession of three stages, the emtpy stage, the inject & wait stage and the readout stage. The panel b) shows a typical measurement result for the different stages. Here, the system is probed by a charge detector. The last panel c) gives a representation of the system in terms of chemical potentials for each stage. Details are in the main text. Taken from [30]. Right panel: Experimental results where one wants to know where the critical point in the read level voltage is reached, i.e. where the two spin states are on each side of the reservoir. This step is crucial because the read level must be set at the right voltage if one wants to achieve spin-to-charge conversion. To know that, we one plots the 2D colormap of the current (here, of an SET detector) as a function of time in x and read level voltage in y. This is the typical experiment I have reproduced during my PhD. Results are presented in the last chaper. "Load" in the right panel is equivalent to "inject & wait" of the left panel. Taken from [39].*

displacement occurs in the system and the detector sees nothing. The key signature of this energy selective spin-to-charge conversion method is the circled little bump in the probed signal on the readout stage, panel b) of the figure 2.13. The position and the length of the bump is strongly correlated to the two tunneling times, from the dot to the reservoir and the opposite. At the end of the readout stage, we simply initialize the sytem by emptying the quantum dot. Again, we can see the effect of the capacitive coupling between the QPC and the gate, responsible for the sharp decrease of the signal. After a certain amount of time, the tunneling time, it is followed by a little increase corresponding to N=0.

This 3-step sequence allows one to detect whether the charge carries a spin up or a spin down with a spin-to-charge conversion scheme. Moreover, one can access another core

parameter, the relaxation time T_1 for an excited state to decay down to the ground state. Indeed, if t_{wait} is much longer than the relaxation time, the charge will always be in the ground state at the end of the inject & wait stage. In that case, no charge will flow out of the quantum dot. An example of such T_1 study as a function of the magnetic field is presented in [39].

The single-shot spin readout is a natural goal in the context of quantum computing. We just saw that, besides not being straightforward, it is possible to perform it on quantum dots. However, the method is quite challenging and requires a very good control over a wide range of parameters, the cleanliness of the device, the opacity of the tunnel barriers, the sensitivity of the nearby charge detector and so on. Even though it is duable, the presence of the nearby QPC will not be a good point in the race of scalability.
In the same fashion, it is also possible to proceed to an average measurement over lots of pulse sequences. Although it cannot be called a single-shot measurement, this approach is less challenging in terms of detection.

This "averaged energy selective spin readout" is presented in the paper [43] with the main results presented below in figure 2.14. The studied device is a single quantum dot probed by a charge detector. In the top panel, we recover the 3-step pulse sequence presented earlier in figure 2.13. We also recover the bump in the read stage, corresponding to a spin down state.

In the last chapter of the manuscript, I will try to reproduce this 'averaged' experiment in our MOSFET devices. More generally, most of the results presented in this manuscript deal with double dot systems either in the many carriers or in the low carrier regime. All the most important situations and parameters, such that the stability diagram, needed to understand the double quantum dot system in the context of that manuscript have been described in that section. However in chapter 4, I will work with another system, a triple quantum dot system. I am going to briefly talk about that system.

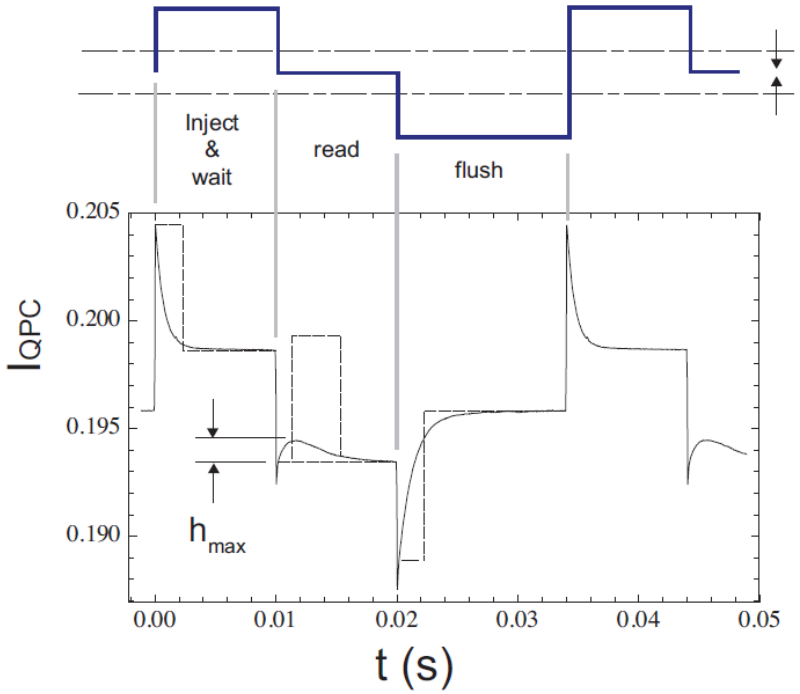


Figure 2.14 *'Averaged' energy selective spin readout. The principle of the experiment is exactly the same than the one presented in the figure 2.13 except that, here, we average the result over a large number of single pulse sequence which is presented in the top panel. The bottom panel shows a typical result where the charge displacements are probed by a charge detector. Like in the previous experiment, the most important thing in the bottom panel is the little bump emerging in the readout stage. This little bump represents a distribution of single counts over time. The shape of the distribution is strongly correlated to the opacity of the tunnel barriers. Taken from [43].*

2.2.3 Coupled quantum dots via a quantum mediator

In the former section, I presented the double quantum dot system which will be the most frequent case in that manuscript. The last occuring case is presented in the last section of the chapter 4 and deals with the concept of quantum mediator. In contrast of having two quantum dots directly coupled to each other, another quantum dot is placed in between the two outer dots such that the two outer dots are indirectly coupled to each other through the inner quantum dot. The whole system is a triple quantum dot system in series. These triple quantum dot systems are of prime interest for some specific protocols. Indeed, these system have already been studied for a while, see for example [44] for a theoretical description of a triple quantum dot system, [45], [46] about the stability diagram of a triple quantum dot, [47] about coherent transport in a three quantum dot linear array, [48] and [49] about spin

transfer and spin manipulation in triple quantum dot, [50], [51] about exchange only spin qubits and finally [52] about coupling two spin qubits via an intermetiate quantum state.

The following figure 2.15 presents the electrostatic model of such linear triple quantum dot array.

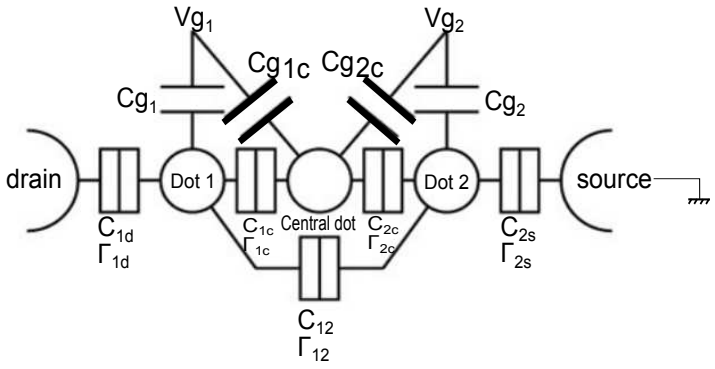


Figure 2.15 *Electrostatic scheme showing (almost) the whole capacitive couplings of the system. The three dots are supposed to be in serie but each dot can exchange carriers to the two others thanks to the tunnel bariers, characterized by the tunnel rates* Γ_{xy} *between x and y and represented by the rectangles, as always in this manuscript. To control the energy of the dots, two topgates are capacitively coupled to each dot with* Cg_1 *and* Cg_2*. The scheme shows also the cross-capacitances, highlighted in bold black, between the topgates denoted by* V_{g1} *and* V_{g2} *and the central dot, both allowing the control of the inner quantum dot energy. Finally, the dots are also capacitively coupled to their neighbours, characterized by the capacitances* C_{xy} *between x and y. x and y can be leads or quantum dots.*

I will not give too much details about this system. I just want to emphasize one last thing. In general, a triple quantum dot system is made of three quantum dots of the same nature and roughly the same size. In my case, the two outer dots are bigger than the inner dot. The intrisic nature is not the same neither. This leads to peculiar and interesting effects which I will describe in the last section of the chapter.
Indeed, the simulations, ran with python codes, of the system presented in 2.15 showed that depending of the nature of the central quantum dot, whether it is a big or small dot, a metallic or a few carriers quantum dot, the stability diagram will not be the same. As an example, the following figure 2.16 presents two different stability diagrams, DC source-drain bias current as a function of both topgate voltages, the only difference between them being the nature of the inner quantum dot. The left panel shows the simulation for a metallic, many carrier regime inner quantum dot whereas the right panel shows the simulation for a few carriers

inner quantum dot. The outer dots are defined as metallic. All the parameters including capacitances, resistors, temperature and DC biases are realistic, see figure 2.16.

I will start with the common features of both simulations. Blue represents high DC current while white represents no current. The device is a N-type, the carriers are electrons. These two stability diagrams can be seen as a composition of two (sub-)stability diagrams. The first thing we see are the antidiagonals transition lines in blue. Each line corresponds to the addition of one electron in the inner quantum dot. This diagram is the diagram of a single quantum dot coupled equivalently to the two topgates. On top of these antidiagonals, we recover a standard stability diagram of a double quantum dot made of faint blue bias triangles. Basically, the two outer dots can exchange electrons directly and on top of that the inner quantum dot will be filled thanks to the topgate coupling to the inner quantum dot. However, the left panel where every dot is metallic tends to be more regular than the right panel where the inner dot is in the few carriers regime. Indeed, the antidiagonals are wider in the right panel and the bias triangles almost vanished in between the antidiagonals.

These simulations will help us understanding the nature of the inner quantum dot and the overall transport in that triple quantum dot system, which is presented in the last section of the chapter 4. I will show that, depending on the state of the inner quantum dot, the two outer dots are either weakly coupled or strongly coupled to each other. This peculiar way of varying the interdot coupling may be interesting in some protocols.

To finish this preliminary part, I want to tell a few words about the different measurements technics used in the field of quantum transport and more specifically I will introduce what is called the gate radiofrequency reflectometry.

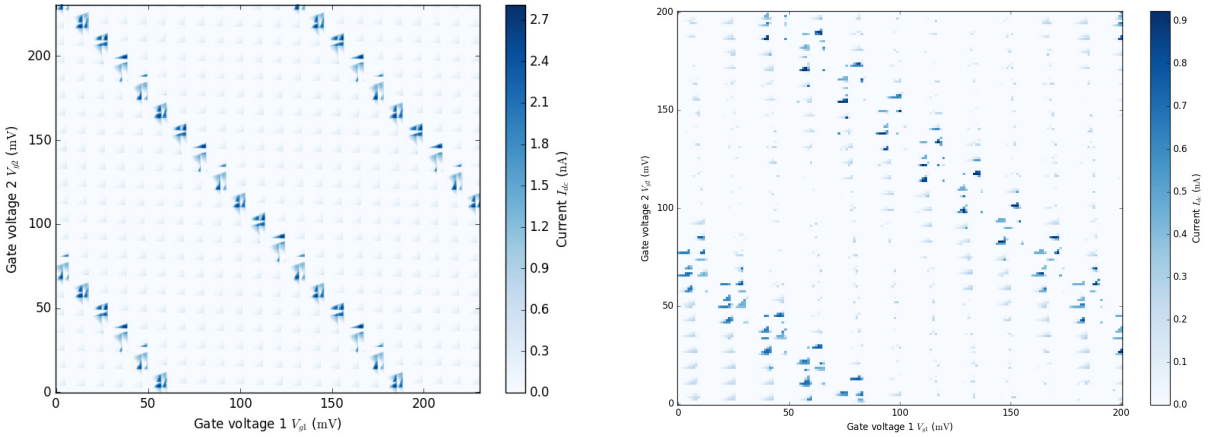


Figure 2.16 *Two python simulations of the triple quantum dot system presented in the figure 2.15 (instead on setting the tunnel rates, we set the conductances in units of conductance quantum $G_0 = \frac{2e^2}{h} \approx 7.75.10^{-5}\,S$ for the metallic (left) case and we directly set DC currents in Ampère for the few carrier case (right)-this is fully related to conception of the code) giving the stability diagram of the system, DC source-drain bias current as a function of both topgate voltages. The device is a N-type, the carriers are electrons. For both simulations: $V_{bias} = 1\,mV$, $g_{12} = 0.01\,G_0$, $C_{12} = 1\,aF$, $C_{1c} = C_{2c} = 5\,aF$, $g_{1d} = g_{2s} = G_0$, $C_{1d} = C_{2s} = 70\,aF$, $Cg_1 = Cg_2 = 15\,aF$, $Cg_{1c} = 1\,aF$, $Cg_{2c} = 1.25\,aF$. We also allow tunnel and capacitive couplings between the leads and the central dot: $C_{dc} = C_{sc} = 0.5\,aF$ Left panel: the inner quantum dot is supposed to be metallic. $g_{1c} = g_{2c} = G_0$, $g_{dc} = g_{sc} = 0.1\,G_0$. Right panel: the inner quantum dot is supposed to be in the few carriers regime. $I_{1c} = I_{2c} = 1\,nA$, $I_{dc} = I_{sc} = 1\,pA$. The antidiagonal blue lines represents charge transitions of the inner quantum dot. On top of that, we recover a weakly coupled double dot (sub-)stability diagram with the faint blue bias triangles. This double dot system is in fact the two outer dots. They can exchange carriers directly. There are a couple of differences between these two stability diagrams. First, the antidiagonals are wider in the right panel. Second, the double dot (sub-)stability diagram is less regular in the right panel. Indeed, the bias triangles vanish in between the antidiagonals. These two differences will help us to discriminate the nature of the inner quantum dot and to understand the underlying transport in that triple quantum dot system.*

2.3 The measurements techniques

So far we have considered mainly source-drain DC current measurements[8] which consists in just probing the number of flowing charges from one lead to the other one. I also introduced the AC conductance measurement (see figure 2.5 for instance), which is basically a measure of the source-drain current but with a lock-in demodulator. It seems natural that these two technics are the most simple way to probe charge trasnsitions in the system. However,

[8]except for the presentation of the energy selective spin readout, originally made with a nearby charge detector

when the number of charges involded in the current flow is too low or when charges do not completely go from one lead to another, it is impossible to measure a current.

Since the early studies of quantum transport in the 80's, physicists have developed the charge detector technical solution, as presented in 2.13 or 2.14 using a QPC, to overcome the two aforementionned issues. I am going to briefly introduce that experimental approach.

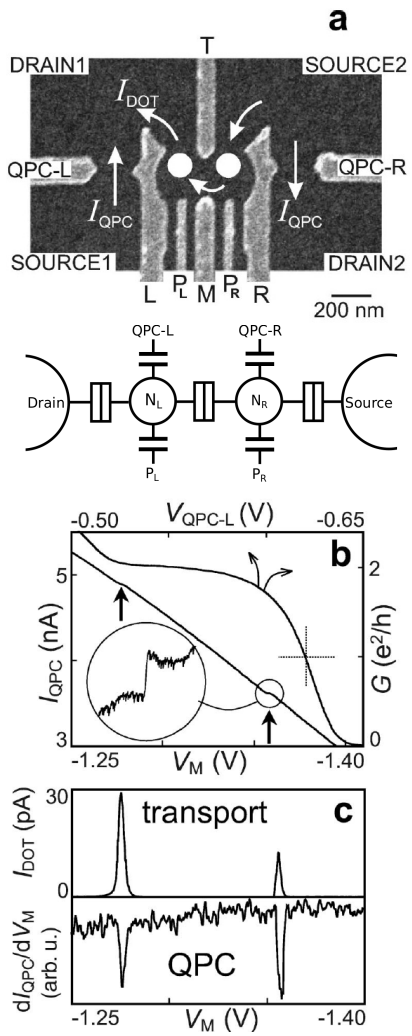
2.3.1 From charge detectors to radiofrequency (RF) reflectometry

A charge detector is an electrometer which is able to probe motion of charges thanks to a capacitive coupling, not through a current flow of charges whithin the device. In the frame of GaAs heterostructure quantum dots, the most common one is the Quantum Point Contact, often called QPC. However in our silicon nanowires, a quantum dot can be set in a SET configuration which also behaves as charge detector.

The Quantum Point Contact (QPC)

Instead of *simply* probing the current flowing from one lead to the other, physicists have developed a charge detector approach to probe charge transitions in quantum dots system. The most common charge detector is reffered to as a QPC. A QPC is a 1D conducting channel whose potential is controlled by a gate. If the reader is interesting in the physics of QPCs, [53] gives a theoretical description of the transport through QPCs and [54] presents a short review both on the experimental and the theoretical points of view.
The QPC is placed nearby the quantum dot of interest, to be capacitively coupled. Therefore it is a local charge detector. The following figure 2.17, extracted from [55], gives a good illustration of what is the principle of a QPC.

The top panel a) shows a SEM picture of a typical GaAs heterostructure serial double dot system represented by the white circles. The two lateral gates denoted as QPC-L and QPC-R control the electrostatic potentials of the two QPCs, each being a 1D conducting channel. Each QPC does probe only one quantum dot at first order. The middle panel b) shows the characteristics of the left QPC. The top curve with the top and right axis is the conductance as a function of the gate voltage V_{QPC-L}, showing the last quantized plateau and the transition to complete pinch-off. The dashed lines indicate the point of highest sensitivity. The bottom curve with the bottom and left axis is the current flowing through the QPC as a function of the topgate voltage of the left dot. The two steps, pointed by arrows are the signatures of charge transitions in the left dot. Indeed, when a charge goes in or out of the quantum dot,



Top panel a) SEM picture and schematic of a GaAs serial double quantum dot system represented by the white circles. Nearby both dots are the two QPCs, each being made of a 1D conducting channel electrostatically controlled by two gates, QPC-L and QPC-R. The middle panel b) shows two curves. The top curve with the upper and right axis is the conductance of the QPC as a function of QPC gate voltage V_{QPC-L} showing the last quantized plateau and the transition to complete pinch-off. The dashed lines shows the most sensitive working point for the QPC. The bottom curve with the left and bottom axis shows the current as a function of dot gate voltage V_M. The steps pointed by arrows shows charge transitions in the quantum dot. The bottom panel c) shows a comparison between a classic DC source-drain current measurement and a QPC measurement.

Figure 2.17 *Typical QPC device and characteristics. Extracted from [55].*

the overall electrostatic potential will change in the quantum dot vicinity. Therefore, when one sets the QPC in good conditions, for instance at the highest sensitivity point (top curve), it will be sensitive to charge displacements in the quantum dot. The bottom panel c) shows a comparison between a *traditionnal* DC source-drain current measurement and the QPC measurement.

The charge sensitivity is a central figure of merit of an electrometer. A typical sensitivity for a QPC is around $10^{-4}e/\sqrt{Hz}$ [42]. This basically means that the motion of a charge of about 10^{-4}e can be detected in a measurement time of 1 second.
Earlier in the presentation of the single quantum dot, I said that a SET can be an electrometer too and is characterized by a similar sensitivity, about $10^{-4}e/\sqrt{Hz}$ [56]. Besides being very sensitive, these two electrometers have their own limitations. First, the operational bandwidth

is limited to a few kHz due tot the electronic environment of the electrometer. Second, the performance of the electrometer are lower at low frequency due to background charge motion inside the QPC or the SET, which is responsible for a 1/f noise.

The QPC as well as the SET are powerful ways of probing the charge number in quantum dots. It is even possible to probe the first charges in a dot. For instance, this is the case in [55] or in [45]. However, physicists were very interesting in increasing the sensitivity of their charge detectors and overcome their own limitations. In 1998 in [57], a new device working as a charge detector was presented, the radiofrequency single electron transistor, called the RF-SET, increasing the sensitivity up to $10^{-5}e/\sqrt{Hz}$.

This RF-SET is the first presented device using a resonant tank circuit in the community of quantum dot. Among the RF-SET, physicists have also developed the RF-QPC with the same goal of increasing the sensitivity of the charge detectors. For instance, in [58], they reached $10^{-6}e/\sqrt{Hz}$.

The radiofrequency Single Electron Transistor (RF-SET)

I have already presented the SET in the single quantum dot section. An RF-SET is the association of a SET and a resonant tank circuit made of an inductance and a capacitance. The tank circuit is a resonant circuit meaning that if one sends a signal at the resonance frequency $\omega = \frac{1}{\sqrt{LC_{pad}}}$, one will be sensitive to any change in capacitance or inductance of the total circuit including the SET. The next figure 2.18 adapted from [57] shows an electrical scheme of such RF-SET. For a more complete work on the sensitivity of such charge detector, see [56].

However on the one hand, I have never used any local charge detector during this PhD, simply because of design constraints. As I have worked on SOI MOSFET quantum dots processed with industrial protocols, it is very complicated to strongly modify standard processes and designs. Only small changes at a time can be implemented. On the other hand, in the context of quantum computing, it is known that one would need thousands of connected quantum dots in array (see [59] for instance). Therefore it is tough to imagine a local charge detector nearby each quantum dots in such complex network. So, even though it would be possible to design charge detectors nearby the SOI MOSFET quantum dots, we decided to probe charge transitions in quantum dots without any local charge detectors. In the next section, I am going to present the RF reflectometry, a charge detection method which does not require local charge detectors. Instead, we directly send the RF signal on

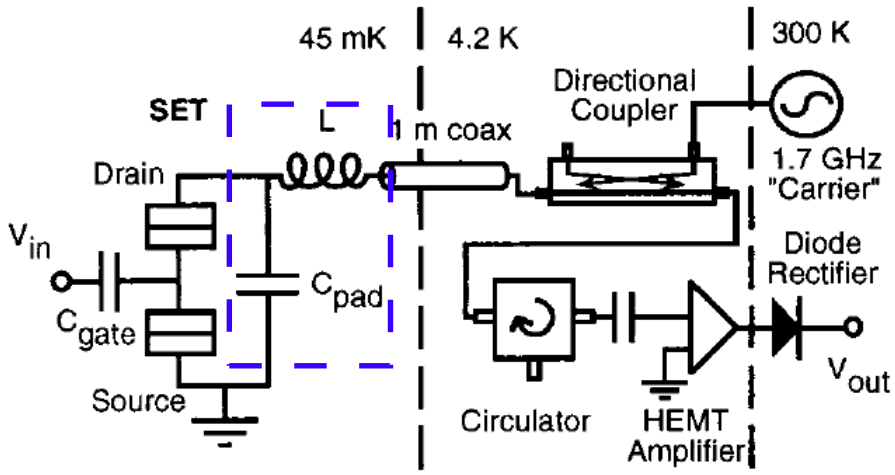


Figure 2.18 *Electronic schematic of a RF-SET. The SET is represented on the right in the lowest temperature stage, simply a single quantum dot in the many carriers regime. The SET in embedded in a tank circuit resonating at* $\omega = \frac{1}{\sqrt{LC_{pad}}}$*, highlighted with the dashed blue rectangle. One sends a carrier signal at the resonance frequency, here at 1.07 GHz. A directionnal coupler splits the incoming and reflected signal. If the SET gains or looses an electron, the whole capacitance of the circuit will change. By analysing the reflected signal, one is sensitive to tiny changes of the capacitance of the SET which is detected as a change in the renonance frequency. Adapted from [57].*

the device, either on one of the leads or on the topgate. For instance, the following paper [59] gives a proposal for a specific quantum computer architecture made of a 2D arrays of CMOS quantum dots. In that proposal, the detection is done with direct gate-coupled RF reflectometry.

2.3.2 The gate-coupled RF reflectometry

The previous section was dedicated to local charge detectors, either with or without the help of a tank circuit and a RF signal. Today, we know that it is possible to directly probe the charge state of a quantum dot by sending a RF tone on the device through a resonant LC circuit and by looking at the reflected signal, see for instance [60], [61]. This part is inspired by the chapter 4 of former postdoc A. Crippa's PhD manuscript [62] which gives a detailed theory of modeling a RF-SET and the direct reflectometry and by the chapter 3 of former student A.Corna's PhD manuscript [63].

The goal of the reflectometry detection, which is also called dispersive readout signal, is to be sensitive to small changes of the total capacitance of the circuit without the implication of a local charge detector. Let's call the bare capacitance of the tank circuit (labelled C_{pad}

in the figure 2.18) the geometric capacitance. In the following, this geometric capacitance will be labelled C_p. The tank circuit must contain an inductance L. The resulting resonant frequency is given by $\omega = \frac{1}{\sqrt{LC_p}}$.

The next figure 2.19 taken from [64] presents a serial double quantum dot system experiment realized earlier in the group. The device is a typical CMOS device realized here in CEA Grenoble and hosts the quantum dots system. The associated electronic scheme shows the dot tunnel barriers, and the capacitances between the gates and the dots. Two gate RF reflectometry channels are used to directly probe on the gates the states of both dots. The carrier signal is sent by an UHF lockin detector [9] which is also responsible for the reading of the reflected phase. We operate the device in a regime where $k_B T_e \leqslant 2t < \Delta$ with k_B is the Boltzmann constant, T_e the electron temperature in the range of a few hundreds of milliKelvin, t the interdot tunnel coupling and Δ the mean level spacing in each dot (typically, between ~ 0.1 to few meV (for instance, see [37], [32]).

Besides the geometric capacitance C_p presented figure in the 2.19, one can define the differencial capacitance C^j_{diff} seen by the tank circuit associated to the gate j. This differential capacitance is related to any carrier tunneling in or out of the dot associated to the gate j. It reads:

$$C^j_{diff} = q\alpha_j \frac{\partial \langle \nu \rangle}{\partial V_{Gj}} \tag{2.24}$$

where q is either $-|e|$ or $|e|$, depending on the nature of the carriers, electrons or holes, respectively. α_j is the lever-arm parameter associated to the gate voltage V_{Gj} and $\langle \nu \rangle$ is the average excess charge flowing through the dot. In the case where the charge dynamics is faster than the carrier frequency f_0^j associated to the gate j, the reflected signal experiences a phase variation $\delta\Theta_j \propto -C^j_{diff}$, hence nonzero in correspondance of the charge transitions. This result is derived in the more complete paper [65].

In order for the reader to better understand the physics underlying this differential capacitance, I will briefly derive the formalism of an isolated double quantum dot only populated with one electron. No electrons are given to or removed from the reservoirs and a single electron can be switched between the two dots, corresponding to an excess electron in either dot 1 or dot 2. Interdot dynamics between the localized states $|1\rangle$ and $|2\rangle$ is described by the Hamiltonian $H = \frac{\varepsilon}{2}\sigma_z + t\sigma_x$ with ε being the detuning parameter, the misalignment between chemical potentials of the two dots in the limit of vanishing interdot coupling t. $\sigma_{x,z}$ are Pauli

[9] I will briefly present the instrument in the electronic part of the chapter 3.

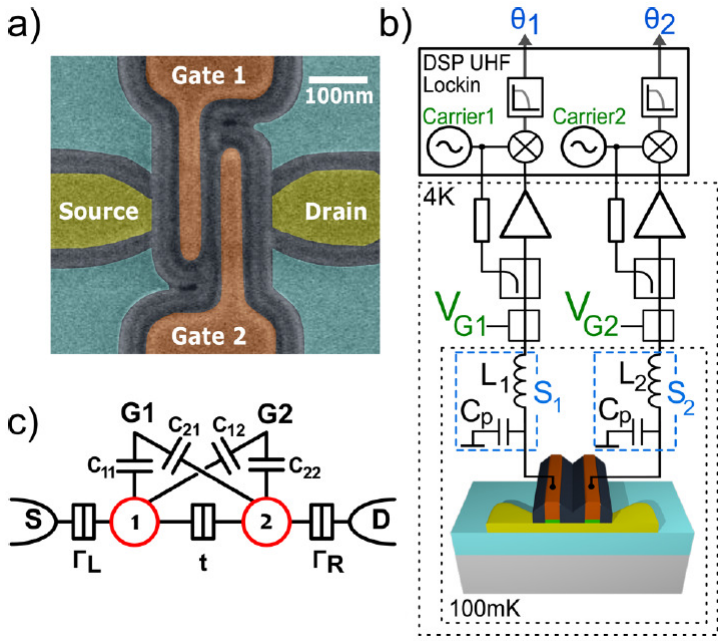


Figure 2.19 *Dual-channel gate RF reflectometry setup presented in [64] realized by former PhDs R. Maurand and A. Crippa. The panel a) is a false coloured scanning electron micrograph of a typical CMOS device hosting the double quantum dot, 1 and 2 underneath the gate 1 and the gate 2, respectively. The panel b) is a simplified electronic scheme of the gate RF reflectometry setup. In that case, two tank circuits, S_1 and S_2 made of an inductance $L_{1(2)}$ and the geometric capacitance C_p, are connected to the two topgates G1 and G2. The carrier signals are generated by an UHF Lockin which would also collect both reflected signals and read the phases θ_1 and θ_2. The panel c) shows an electronic picture of the two quantum dots in serie interconnected through the tunnel barrier t and connected to the leads through the tunnel barriers Γ_L and Γ_R. Both dots are capacitively coupled to each gate. C_{12} and C_{21} are the cross capacitances. In this experiment, the parameters of the LC circuits are L_1=270 nH, and L_2=390 nH, f_0^1= 421 MHz and f_0^2=335 MHz giving C_1= 21 pF and C_2=25 pF. These are the orders of magnitude.*

matrices. The eigenstates of such two level system read.

$$|\Psi_-\rangle = sin\left(\frac{\theta}{2}\right)|1\rangle - cos\left(\frac{\theta}{2}\right)|2\rangle \tag{2.25}$$

$$|\Psi_+\rangle = cos\left(\frac{\theta}{2}\right)|1\rangle + sin\left(\frac{\theta}{2}\right)|2\rangle \tag{2.26}$$

where $tan(\theta) = \frac{2t}{\varepsilon}$ and $|\Psi_-\rangle$, $|\Psi_+\rangle$ correspond to the bounding and antibounding molecular states expressed in terms of the localized states $|1\rangle$ and $|2\rangle$. These two eigenstates are associated to two eigenvalues, basically the states of a charge qubit, and are given by $E_\pm = \pm\sqrt{\varepsilon^2 + (2t)^2}/2$. In the limit of small excitations applied by gate j to the dot i, i.e.,

$\delta V_{Gj} \ll \frac{2t}{e\alpha_{ij}}$ (see [66]), the differential capacitance for the resonator associated to the gate j eventually reads:

$$C^j_{diff} = \frac{\beta_j^2}{2}\left(\frac{dP_d}{d\varepsilon}\frac{\varepsilon}{\sqrt{\varepsilon^2+(2t)^2}} + P_d\frac{(2t)^2}{[\varepsilon^2+(2t)^2]^{\frac{3}{2}}}\right) \tag{2.27}$$

with $P_D = P_- - P_+$ the difference between the occupation probabilities of $|\Psi_-\rangle$ and $|\Psi_+\rangle$ and $\beta_j \equiv -e(\alpha_{1j} - \alpha_{2j})$ is the detuning lever-arm factor for the gate j.
The first term of the equation 2.27 is called the *tunnel capacitance*. It depends on the variation of the occupation probability difference as a function of the detuning $\varepsilon = \mu_2 - \mu_1$. This contribution arises when the charge tunnels from one dot to the other. In such a case where a charge tunnels from one dot to the other, we will be able to detect a variation of the phase of the reflected signal.
The second term of the equation 2.27 is called the *quantum capacitance*, first mentionned in [67]. It is proportionnal to the difference between the occupation probabilities of the two molecular states. In fact, it is known (for instance, see [65]) that this second term is related to the band curvature $\frac{\partial^2 E_\pm}{\partial \varepsilon^2}$ of the energy states around the anticrossing point at $\varepsilon = 0$. In particular, the sign of the variation of the reflected phase signal will be related to the sign of the curvature. On top of that , if a charge transition is associated to a flat energy state (for instance a spin-triplet state, see [68]), the quantum capacitance term would vanish. Hence, in a case of a flat state transition, we would not get any phase variation of the refected signal.

This little insight on the differential capacitance, sum of the tunnel and the quantum capacitance, in the case of the isolated quantum dot system shows that, indeed we are able to detect charges tunneling between quantum dots through the tunnel capacitance with radiofrequency reflectometry. Moreover, we are also sensitive to the curvature of the states through the quantum capacitance. The interested reader shall find a deeper theoretical work in [69]. Although this direct reflectometry probing technic is quite new in the frame of semiconducting qubits, it has shown promising results in both cases of charge states and spin states bases [70] [71], [72] [64] [68], [73].

Throughout this first chapter, I wanted to introduce the reader to the basic of charge transport in quantum dot systems with a simple theoretical description of mainly the single and double quantum dot systems and a practical introduction to the newest way of probing charge transitions in quantum dots, the gate-RF reflectometry. In the next chapter, I am going

to present the experimental frame. First the studied devices and the associated process flow is discussed, then the electronic for a direct RF reflectometry.

Chapter 3

Device fabrication and electronic setup

"What we observe is not nature itself, but nature exposed to our method of questioning."
-Werner Heisenberg, 1956

Résumé

Ce chapitre est dédié à la création des dispositifs mesurés pendant cette thèse ainsi qu'à une présentation de l'installation électronique utilisée dans le dernier chapitre.

La première section introduit le lecteur à l'histoire du transistor, composant électronique inventé par des physiciens du solide à la fin des années 40.

La deuxième section commence par rappeler pourquoi le transistor est devenu indispensable dans le développement de l'électronique moderne. Le principe de son fonctionnement seul ainsi que le principe de logique complémentaire basé sur l'association de transistors est présenté.
Après cette introduction aux transistors, le procédé de fabrication standard de tels transistors développé au laboratoire LETI est présenté à travers les étapes les plus importantes. Je me concentrerai ensuite sur certaines étapes particulières qui doivent être modifiées dans le but d'obtenir des dispositifs utiles à des fins d'ingénierie quantique. Je finirai par présenter les trois dispositifs que j'ai étudiés durant cette thèse.

La dernière section est dédiée à l'électronique nécessaire à la réalisation de la dernière expérience présentée dans le chapitre 5. En particulier, j'insisterai sur les lignes dédiées à la réflectométrie radio-fréquence ainsi qu'à la création de deux lignes permettant d'envoyer des impulsions électriques sur le dispositif. L'ingénierie des bandes passantes nécessaires de ces

deux lignes est discutée. Cette section se termine par un diagramme électronique générale du cryostat.

3.1 A brief history of the transistor

Since its official discovery in 1948 by J. Bardeen, W. Shockley and W. Brattain at Bell labs [74], the transistor has been widely produced and used for a whole lot of purposes. Nowadays, every electronic component or setup which is more sophisticated than a simple electric switch relies on transistors. Logical circuits, amplifiers, voltage stabilizers, signal modulators among others are possible applications for transistors and this has been responsible for its development and its omnipresence for the last half of the of the XX^{th} century. The following website *www.computerhistory.org* gives a large overview of the history of silicon engines and computer science more generally.

The transistor in itself is an electronic device which makes use of characteristic physical effects occuring in semicondutors. It is not a surprise then that its Nobelized inventors cited above are not just engineers, but major solid-state physicists.

The following review [75] written in 1958 presents the story of semiconductor research from the end of the XIX^{th} century to its time and shows how transistor devices had been developed after World War II, in the years following the 1948 discovery.
During the whole first 40 years of the century, physicists as well as chemists and metallurgists had to work together in order to figure out the strange behaviors of some pieces of matter, semiconductors. Indeed, their properties have departed so much from ideal (ohmic) conductors that,in many cases, they have been mistaken with oxides.
Gradually, there was an improvement of the technical skills to make purer and purer crystals all along with a net advance in theoretical physics. From the experimental point of view, a couple of situations were crucial like the Hall effect or the rectification effect. The first allowing to probe mostly the body properties and the second to probe the surface properties. This lead to the future invention of the transistor.

The next crucial step in transistor development is the MOSFET, standing for *Metal-Oxide-Semiconductor Field Effet Transistor* invented in 1958 by D. Kahng and M. M. Atalla [2], again at Bell Labs. While the original transistor, made of germanium, was big and rather fragile, the MOSFET was more robust, very suitable for miniaturization and relied on a very cheap and abundant element on Earth, namely silicon. At the same time at the Fairchild

Semiconductor corporation, the first planar integrated circuit was fabricated. 10 years later, this lead to the creation of the first comercialized microprocessor by intel corporation in 1971, intel 4004, constituted with 2300 transistors working in harmony. Back in 1965 already, G. Moore did observe that the number of transistors in a dense integrated circuit doubled about every two years [1]. This empirical remark will become the Moore's law. For the next 40 years till today, this trend has been verified and the manufacturers has kept the technical progression of the miniaturization as close from this law as possible.

Today, billions of transistors[1] are built every day and the latest commercial processors can hold up to 20 billions of transistors on about a five square centimeters area. The typical length goes from 10 μm in 1971 with the intel 4004 down to 7 nm in 2019[2]. The following part presents how we go from conventional MOSFET and their characteristics to specific devices that are able to host a quantum dot. I will first present the basic of MOS transistor, the standard fabrication process flow of transistors designed here at CEA LETI, the specific steps quantum physicists need to custom and the devices studied in this manuscript. The last part of the chapter is dedicated to the measurement system involved.

3.2 From transistors to qubits

We just saw that transistors are nowadays everywhere thanks to the miniaturization. However one may wonder: how is it possible to keep at mesoscopic scale the good properties working at macroscopic scale, how can one scale the production at industrial level, what is a good transistor and finally, how the LETI's transistor can be a perfect host for the sake of the quantum computer ? I will start with an introduction of the properties of the transistor from the point of view of an electronical engineer, then I will present the general ideas of the standard process performed here at LETI and finally I will present the small differences at some specific steps of the process that one can make in order to optimize the device from a quantum computing perspective.

[1] 99.9% of worldwide production are MOSFETs, because they are the building blocks of logical circuits.

[2] Although the typical length of the first transistors was the real gate length, it is not true anymore. The gate length cannot go beyond tens of nanometers. However, the new technologies allow for a much more dense chip. Today, the typical length is just a name, a brand. When one talks about the 7 nm node as in 2019, it means that the reached density corresponds to a hypothetic chip full of 7 nm gate length transistors. In reality, the involved technologies have changed compared to earlier technologies. I could cite the FINFET for example.

3.2.1 The transistor: a crucial tool for digital logic

A transistor is usually a 3-terminal component constituted of a source and a drain together referred as the carrier reservoirs and a gate. In this manuscript[3], these reservoirs will be called *leads*. As discussed in the introduction, there are many practical realizations of the transistor and the following general properties can apply to any kind of field effect transistors (*FET*). However the technological answers corresponding to these properties will be the ones from the LETI laboratory and its technology, the Silicon On Insulator (*SOI*) MOSFET.

A MOSFET is basically an electron/hole tap, the gate being the valve. There are two types of MOSFET, the N-doped and the P-doped devices. N-doped are doped with donor elements like phosphorus, arsenic and thus have an excedent of electrons while the P-doped are doped with acceptors elements like boron and have a lack of electrons (equivalently, an excedent of holes). These two polarities are the central tool of the CMOS logic (standing for *Complementary Metal Oxide Semiconductor*). Both are presented in the following figure 3.1.

The following is true at 300 K. The two leads are either N-doped (left panel) or P-doped (right panel). As said earlier, they are the carriers reservoirs and ideally are metallic. Between these two leads is the semiconducting silicon channel. At equilibrium, when the gate voltage V_{GS} is equal to 0, no significative current flows since the natural barrier of the semiconductor is too high. The residual current is called I_{off} in that regime. When one starts biasing the gate, up to a point called the *threshold voltage* V_T, the drain-source current will increase exponentially. Beyond this threshold voltage, the current will increase linearly. Normally, the working point of the transistor in the conducting regime belongs to this linear regime. We define I_{on} as the drain source current when V_{GS}=V_{ds}=V_{DD}, with V_{ds} being the drain source voltage and V_{DD} a standard, non zero, voltage value. These figure of merits are presented on a typical FET characteristic in the figure 3.2 showing a typical source-drain current in log-scale as a function of the gate voltage in absolute value, making this curve valid for a nFET as well as for a pFET. The reader can clearly distinguish beween the *OFF* state and the *ON* state when carriers flow. These two regimes are separated by a linear regime (in log scale) characterized by the *Sub Threshold Slope* S_s parameter, the slope of this linear regime. We define the *Sub Threshold Swing* S_{ss}, as the inverse of the Sub Threshold slope. These figures of merit are intrisically limited by the temperature and, at T=300 K, $S_{ss} > 60$ mV/dec with *dec* standing for decades and corresponds to a 10 times increase of the drain-source current I_{DS}.

[3] and more generally in the MOSFET based qubit groups.

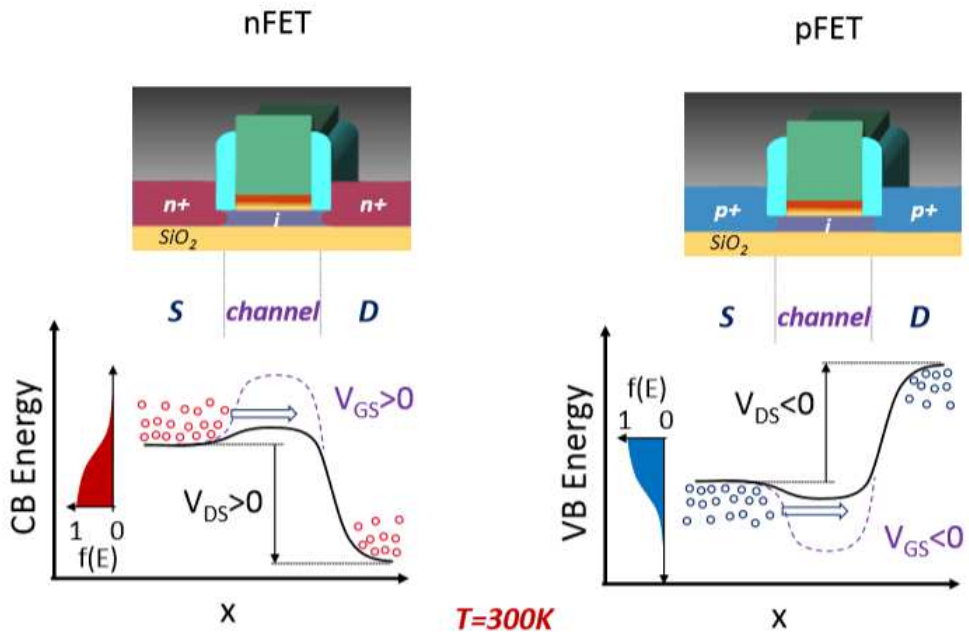


Figure 3.1 *Schematic of the FET principle. The nFET is presented on the left panel and involves the Conduction Band while the pFET on the right panel involves the Valence Band. The x-axis is the position along the channel from source to drain and the y-axis is the energy in the band. At 300 K, the gate acts as a valve. The current increases exponentially (linearly in log scale) with respect to the gate voltage until a point called the threshold voltage V_T. Beyond this point, the current increases linearly with the gate voltage. Finally, as a function of the drain source voltage, the current increases linearly up to a certain point and then saturates.*

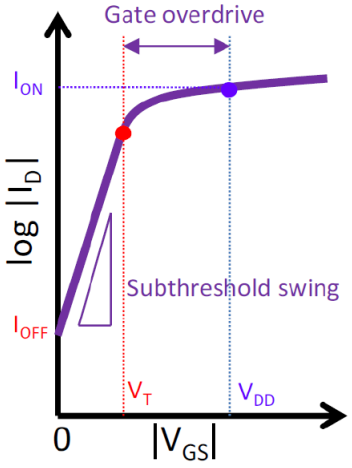


Figure 3.2 *Typical Current (log-scale) vs gate voltage characteristic. Thanks to the absolute value in x-axis, this curve is valid for a nFET as well as a pFET. Three regimes can be distinguished: The* OFF *regime characterized by the current I_{off}, the linear regime characterized by its slope S_s and the* ON *regime characterized by the current I_{on}.*

This ability to control the carrier flow and thus the current thanks to the gate additionned to the two possible polarities allow one to apply complementary logic in electronics. The figure 3.3 illustrates that point. The left picture is a schematic of the simplest combination of pFET (blue, topside) and nFET (red, downside). The gate is common, as well as the drain. The gate will serve as the "input" and the drain will serve as the "output", from a logic point of view. The source of the pFET is always polarized at V_{DD} and is analogous to the '1' logic state while the source of the nFET is grounded, equivalent to the '0' logic state. The right picture illustrates two conditions for two different "input" values in the previous configuration. Depending on the condition on the gate voltage value and thanks to the common drain of the two FETs, the two transistors will either block or allow the current to flow in a opposite way: when one is closed, the other is opened. This leads to an *Inverter* configuration of the system: '0' in input will lead to '1' in output and vice-versa.

I will only present the inverter logical gate however one can build all the boolean logic gates (such that the NAND or NOR gates, for instance) with the following basic principles: the drain voltage V_{out} is always connected to a pMOS pull-up block (connected to V_{DD}) and to a nMOS pull-down block (connected to the ground). The two blocks are complementary, mathematically speaking.[4]

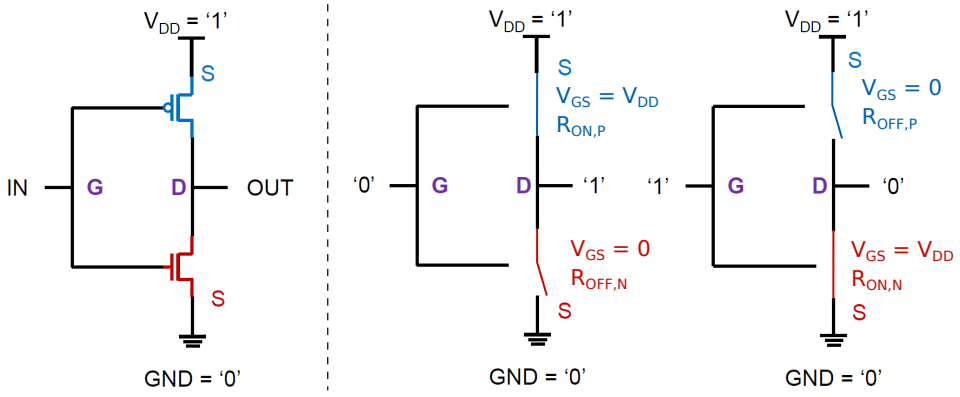


Figure 3.3 *Complementary logic. The left panel shows the schematic of an inverter. The p-FET is in blue while the n-FET is in red. Both gates gates and both drains are common. The p-FET is biased by V_{DD} at its source while the n-FET is grounded. The logical input is the gate voltage value and the logical output is the drain voltage value. '0' is equivalent to 'grounded' while '1' is equivalent to 'V_{DD}'. The right panel shows the equivalent electrical schematic in both the '0' and '1' input cases. The transistors are simply represented by either a close or an open switch, each of the 4 characterized by a R_{ON} and a R_{OFF} resistor values. Depending on the input value, the current will not flow through the same elements.*

[4]For example, in a NAND gate, the two nMOS are in serie giving A And B = 0 and the pMOS are in parallel leading to Not(A) And Not(B)=1=Not(A And B).

Both transistors have two regimes, *ON* when the channel is closed and the carriers flow and *OFF* when the channel is open and no current flows. Each regime has their own characteristics: the value of the channel resistivity R_{ON} and R_{OFF} and the gate voltage V_{GS}. By construction, $R_{ON} \ll R_{OFF}$. The full circuit can be seen as a voltage divider.

$$V_{OUT,'1'} = \frac{R_{OFF,N}}{R_{OFF,N} + R_{ON,P}}.V_{DD} \tag{3.1}$$

$$V_{OUT,'0'} = \frac{R_{OFF,P}}{R_{OFF,P} + R_{ON,N}}.V_{DD} \tag{3.2}$$

These simple formulaes highlight the central obsession of electronical enginners: getting the highest R_{OFF} and the lowest R_{ON} to be able to discriminate as mush as possible the two possible logical outputs. This is even more true when one has to cascade multiple stages of logical gates on a microship. This fact will act as a guide during the fabrication process that I am going to present. Of course, the $\frac{R_{ON}}{R_{OFF}}$ ratio is not the only important criterion for a transistor. For instance the sub threshold slope is also important. Eventually, each practical need is associated to a technological answers. As a simple example, minimizing R_{ON}, the access resistivity, can be reached by shortening the spacers that are presented in the future figure 3.6 and by a lighly doped source and drain below the latter. A last example of such correspondance is between the insulating layer in the gate stack and the gate control of the channel. The thinner the layer, the better the control and, in practice, the highest sub threshold slope. This is the reason why the standard process involves a high-K dielectric material layer in the gate stack, figure 3.5.

3.2.2 LETI's standard process flows and custom steps

Since its creation, the LETI laboratory has been one of the world's largest organizations for applied research in microelectronics and more specifically (and recently) in the Silicon On Insulator (*SOI*) technology. Since 2011 the LETI has been able to produce MOSFET on 300 mm diameter silicon wafers. One of the specificity of LETI's MOSFETs is the wrapping gate around a 3D silicon nanowire.

In this part I will describe the standard process flow conceived by the LETI to create a conventional MOSFET. Because of the very large number of steps involved during the process flow[5], I will focus on the most important steps. Following the standard process flow I will present what I called the custom steps or how to adapt LETI's technological route to our

[5] more than 150 !

quantum, cryogenic aims. The reader shall be aware that I will not go into technical details such that the gases and the machines used in practice.

Standard process flow for a conventional MOSFET

All the folllowing 3D schematics and cuts were realized with the *SEMulator3D* software.

We start from a trilayer made of a natural silicon substract, 145 nm of silicon dioxide called the buried oxide (*BOX*) and a last 16 nm layer of natural silicon, from bottom to top. This trilayer is shown in the first picture of the figure 3.4. The natural silicon is in blue while the oxide is in yellow. We will now design the nanowire with a combination of lithography and etching. First, we deposit a photoactive resist drawn in magenta in 3.4 at step 2. We expose the resist to UV light through a desired mask designed by the electronical enginner, here the active zone. We now develop the resist in 3 leaving only some resist which will protect the future active zone from the etching of the silicon in 4. Finally we strip the remaining resist and we get our silicon nanowire on insulator in 5, leading to the SOI designation for this kind of MOSFET.

During the whole process flow, the directionnal lithography/etching sequence (step 2 to 5 in the last figure 3.4) will be involded at many different steps. Even though the used mask will be different depending on the area one wants to define (active zone, gates etc), the sequence will always be the same. Thus, for the sake of clarity, I decided to not show the following lithography/etching sequences.

We have the nanowire lying on top of the BOX. We will now design the gate stack and this is presented in the figure 3.5. To do so we will proceed to a conformal deposition for the different layers. However, first, we expose the upper surface of silicon to a well controlled chemical oxidation, leading to a very thin 0.8 nm of silicon dioxide. We then deposit 1.9 nm of high-K dielectric material[6], here hafnium dioxide, allowing to reduce the thickness of this insulator layer and to get a higher electrostatic control of the channel. On top of the insulator we deposit the future metallic part of the gate made with 5 nm of titanium nitride. We complete the stacking with a layer of 50 nm of poly-silicon in red, 30 nm of silicon nitride in green and finally with a layer of silicon dioxide in yellow, step 1 in figure 3.5. The last bilayer of silicon nitride and silicon dioxide (green and yellow) is called the *Hard Mask*. We then have to etch the multilayer. At step 2 we deposit a layer of resist and we expose it to UV light. This will transfer the optical mask pattern into the hard mask. The step 3 consists

[6]It has a higher dielectric constant than silicon dioxide.

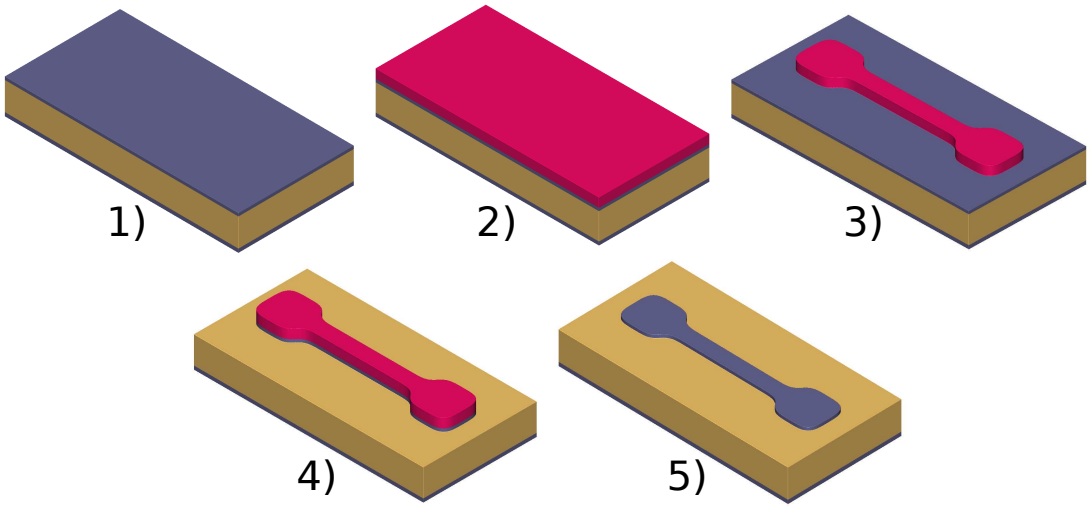


Figure 3.4 *Active zone design. The starting point of the process is a trilayer of natural silicon subsract, 145 nm of buried oxide (called the BOX) and 16 nm of natural silicon, from bottom to top. The four others shown steps are the lithography/directinonal etching of the silicon nanowire. Step 2) we deposit a photoactive resist (magenta) and expose this resist to UV lights through a mask, here the active zone mask. Step 3) we then develop the resist in order to keep some resist only on top of the future nanowire. Step 4) we etch the silicon layer. The remaining resist protects the nanowire. Step 5) we strip the remaining resist and we finally get our silicon nanowire on top of the BOX leading to the Silicon-On-Insulator (SOI) designation for this kind of device.*

in stripping the remaining resist following by an etching without any resist to transfer the hard mask pattern into the gate stack.

At this point we have the undoped silicon nanowire and the gate stack on top of it. We now need to dope the leads of the nanowire while keeping the channel undoped and this is presented in the figure 3.6. To do so we need to deposit a layer of insulating silicon nitride, drawn in green in this figure, step 1. We will etch this layer in step 2. All the silicon nitride but the part on the flanks of the gate stack is stripped. This will protect the channel and the gate from the source drain epitaxy and the LDD (standing for *Lightly Doped Drain*) implantation of the leads of the nanowire depicted in step 3. The schematics 4 and 5 are longitudinal cuts of steps 2 and 3, respectively. The resulting insulating nitride is called *Spacer 1* and is roughly 11 nm width. I will not go into details about this LDD implantation. The reader shall know that, in practice, the engineers have to make a compromise between access resistivity (the closest the reservoirs to the undoped channel, the lowest the access resistivity is) and the reliability of the transistor (if the reservoirs are too close to the channel, some side effects start taking an important role in the characteristics of the transistor).

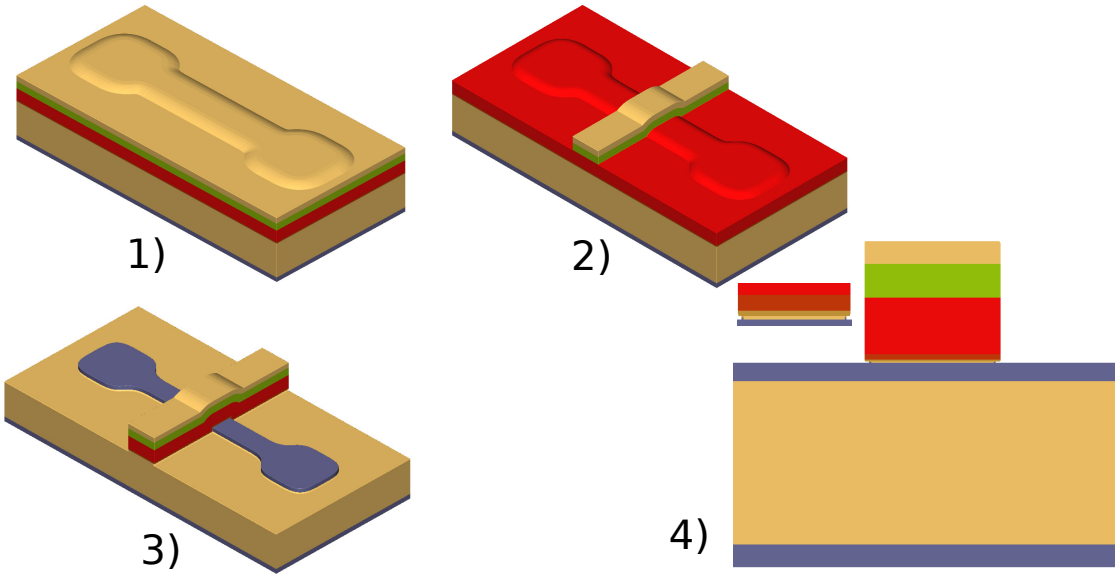


Figure 3.5 *Gate stack design. Step 1) multilayer conformal deposition. From first to last we got 0.8 nm of silicon dioxide (yellow) and 1.9 nm of high-K dielectric material (light brown), together being the insulating layer of the gate. We then deposit 5 nm of titanium nitride (dark brown) and 50 nm of poly silicon (red). The latter being heavily doped later on, both will become the metallic part of the gate. We finally complete the staking with the so clled hard mask, a bilayer of silicon nitride and silicon dioxide. Step 2) We directionaly etch the hard mask with a resist through an optical mask. Step 3) We finally etch without any resist the rest of the gate stack by transfering the hard mask pattern into the gate stack. Step 4) Longitudinal cut of the gate stack. The inset is a zoom of the first thin layers of the gate stack.*

The next steps presented in the figure 3.7 is also a spacer deposition. We will deposit what we called the *Spacer 2* or *sacrificial spacer*. Even though it is called a spacer and is insulating, this one is made with silicon dioxide, unlike the spacer 1 made with silicon nitride. This is shown in step 1 of the figure 3.7. We finally etch the silicon layer at step 2 and, like in the previous figure, we end up with a small portion of silicon dioxide on the flanks of the topgate. The schematic 3 is a longitudinal cut taken at step 2. The reader shall notice that during this process, the upper layer of the gate stack (in silicon dioxide, yellow) is also taken out. The usefulness of that spacer 2 will be seen later on when we want to take out the hard mask in order to be able to dope the gate without removing the spacer 1.

We now want to make the gate metallic. To do so, we need to heavily implant (HDD step, standing for *Heavily Doped Drain*) the poly-silicon (red). However there is still a layer of silicon nitride on top of the gate stack preventing the doping. We need to etch it and this is presented in the figure 3.8, step 1. Now we understand the utility of the sacrificial spacer,

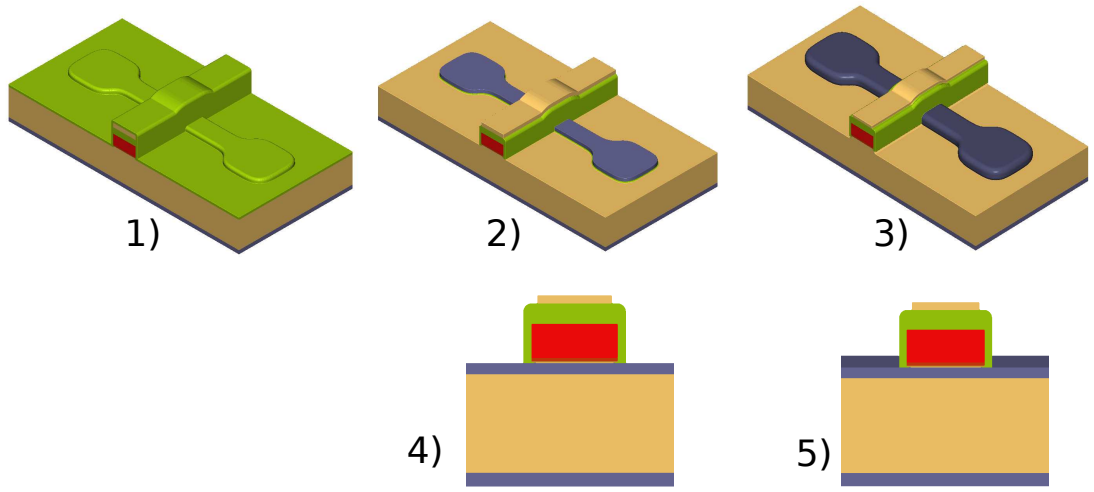


Figure 3.6 *First doping step for the leads of the nanowire. Lighly Doped Drain implantation (LDD). However we need first to protect the buried channel, the area below the gate stack. Step 1) In order to protect the buried channel, we deposit a layer of silicon nitride. Step 2) we directionnaly etch this layer with the gate mask. Only the two flanks of the gate stack are recovered by some silicon nitride. These insulating flanks are called spacers 1. Step 3) Finally we are ready to lighly dope the leads (dark blue). Schematics 4) and 5) are longitudinal cuts of the steps 2) and 3), respectively.*

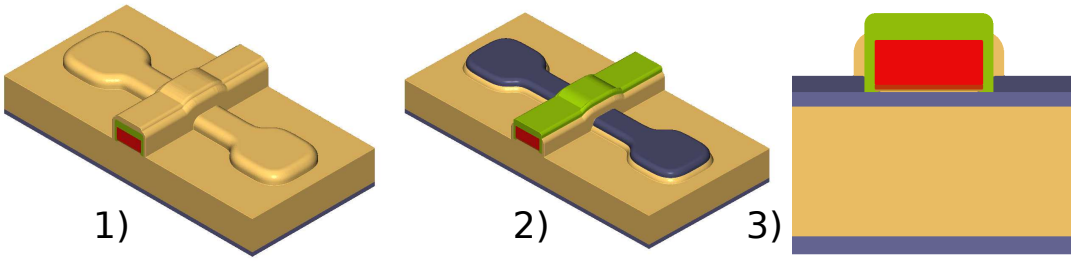


Figure 3.7 *Sacrificial spacer deposition. Step 1) We deposit a layer of silicon dioxide (yellow). Step 2) We directionnaly etch this layer with the gate mask. Again, only a bit of silicon oxide stays on the flanks of the gate stack. Schematic 3) is a longitudinal cut of the step 2). We also removed the last layer of the gate stack, the silicon dioxide layer. This spacer will be useful in the next few steps.*

protecting the underneath spacer 1 also made in silicon nitride[7]. We need to remove the silicon dioxide spacer and this is done at step 2 in the same figure. The schematic 3 is a longitudinal cut of step 2 showing the device after the so-called *hard mask removal* sequence.

[7] more generally, using two kinds of material, here silicon nitride and silicon dioxide, is completely related to material selectivity.

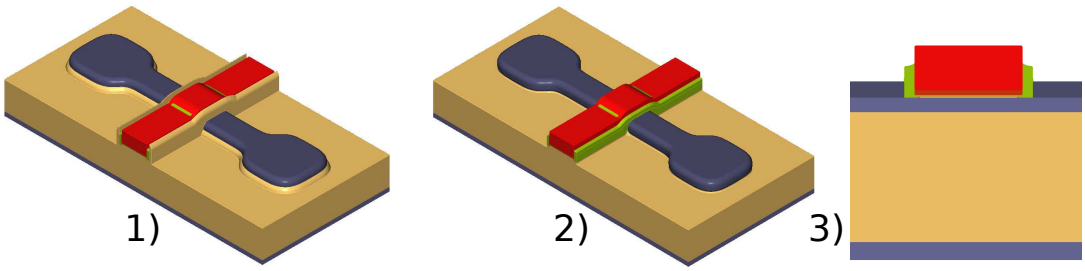


Figure 3.8 *Hard mask removal. In order to make the poly-silicon (red) metallic, we need to heavily implant (HDD) the gate during the HDD steps of the leads later. Step 1) We remove the silion nitride layer (green) of the gate stack. Step 2) We also remove the sacrificial spacer. The schematic 3) is a longitudinal cut of the step 2). The reader now understands the usefulness of this sacrificial spacer by protecting the underneath spacer 1 made with silicon nitride (green) during the hard mask removal, also made in silicon nitride.*

After removing the hard mask and before the metallization of the poly-silicon (and the HDD implantation of the leads), we must add further protection to the channel. Indeed, if one does not care enough, the heavily doped silicon region will be too close to the wanted undoped region underneath the gate and dopants will diffuse below the gate. This is presented in the following figure 3.9. The idea is to add another silicon nitride spacer without impacting the spacer 1. To do so we deposit a bilayer of first silicon dioxide and then silicon nitride, step 1 and 2 in figure 3.9, respectively. We now etch the silicon nitride (step 3) and the silicon dioxide (step 4). The schematics 5 and 6 are longitudinal cuts of step 3 and 4, respectively. In the schematic 6, we clearly see that the whole point of that sequence is to extend the protected area nearby the undoped region by adding some silicon nitride (green corner) a bit farther from the gate stack.

At this stage we removed the hard mask of the gate and we added the spacer 3. Now we can heavily dope the poly-silicon *and* the leads and this is presented in the following figure 3.10. First, in step 1, we procced to the HDD implantation of the leads and we deposit a layer of nickel platinium (light blue) . The step 2 is an annealing allowing the metallization of the leads[8] *and* the gate. This is clearly visible in the schematic 4, longitudinal cut of step 2. The hard blue represents the metal-Si alloy, NiPtSi. Finally we selectively take out the excedent of nickel platinium which did not react and made a shortcut between the leads and the gate at step 3 . The schematic 5 is a longitudinal cut of step 3. On both cuts, the reader can see the impact of the spacer 3 the dark blue regions on both sides of the gate vanishe before reaching the undoped channel, avoiding undesired dopants in that region.

[8]in practice, this annealing leads to the formation of metal-Si alloy which has a lower contact resistivity than low-doped silicon or poly-Si.

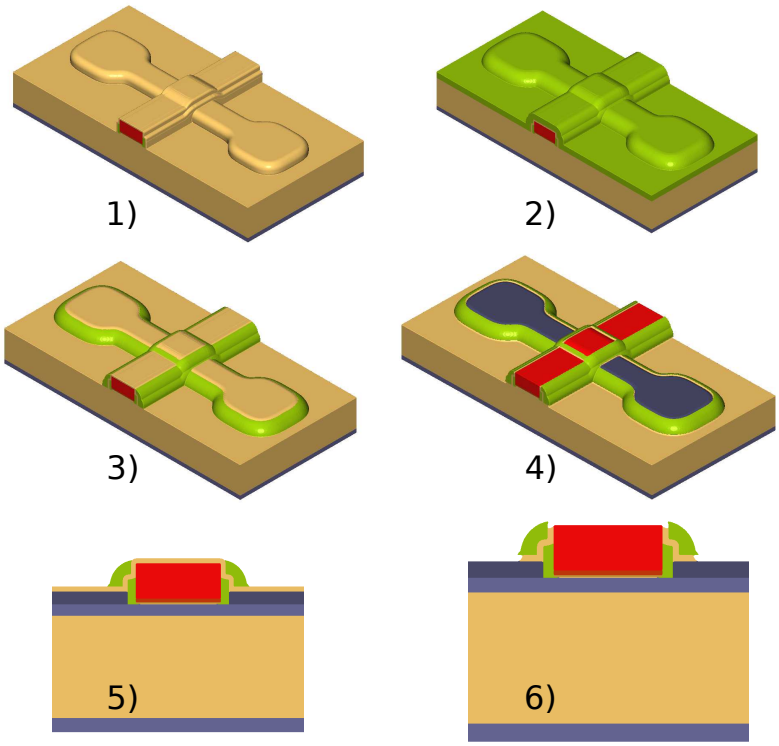


Figure 3.9 *Spacers 3 deposition. Before the HDD steps we must add further protection to the undoped silicon channel. Step 1) we deposit a layer of silicon dioxide (yellow) and step 2) we deposit a layer of silicon nitride (green). Step 3) we remove most of the part of the silicon nitride layer except around the gate stack and the nanowire. Step 4) we now remove the silicon dioxide layer, the poly-silicon layer of the gate and the nanowire are ready to be heavily doped. Schematics 4) and 5) are longitudinal cuts of the steps 3) and 4), respectively.*

At that stage, the device is ready to be used[9]. The last remaining steps are the encapsulation, the contact access and the metallic contacts. The figure 3.11 presents both the contact accesses and the metal line access. All accesses are done in the same way so I am going to detail the contact accesses only. First, we deposit a layer of silicon nitride (green) called the *contact etch stop layer* at step 1. Then at step 2, we deposit hundreds of nanometers of silicon dioxide (yellow) and flatten the top surface. The encapsulation is done. We now need to etch both the silicon dioxide and the silicon nitride in order to have contact accesses. This is shown in step 3 and the scematic 5 is a longitudinal cut. Finnaly we have to fill the accesses with a metal, here tungsten. In fact, there is a trilayer in the contact access, the tungsten one being the upper one. The other two layers made of titanium and titanium nitride (first and second layer, respectively) have their own utility: the titanium layer is an adhesion layer and the titanium nitride layer prevents fluorine diffusion during the subsequent tungsten hexafluorin

[9]If we could bound wires at nanometer scale !

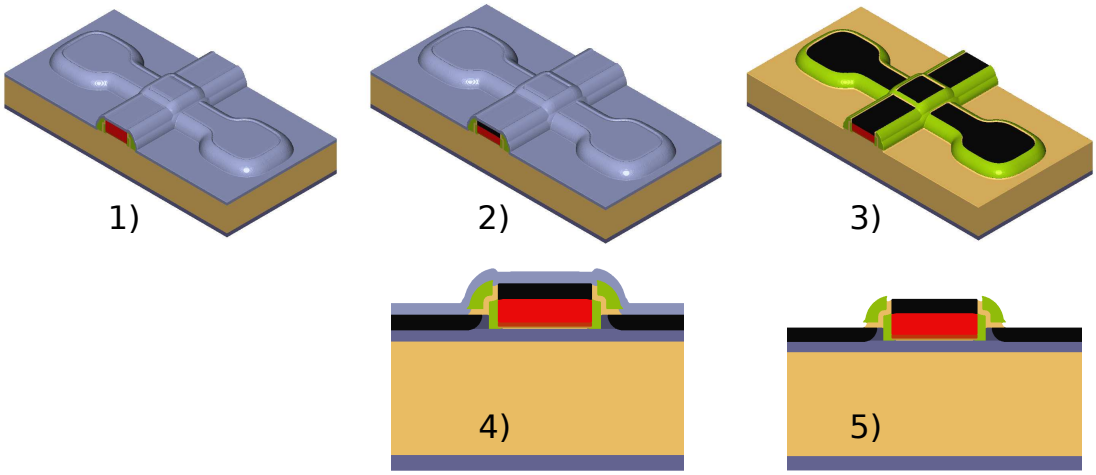


Figure 3.10 *We have to make the leads a metal-Si alloy and the gate metallic. To do so we deposit at step 1) a layer of platinium nitride and at step 2) we anneal. This will lead to the formation of an intermetallic (dark blue) which has a lower contact resistitvity than poly-silicon or low doped silicon. We remove the upper layer of platinium nitride at step 3). The schematics 4) and 5) are longitudinal cuts of steps 2) and 3), respectively.*

CVD[10] of tungsten. The filling of these accesses is shown in step 4. The longitudinal cuts 5 and 6 is taken at step 3 and 4, respectively. Step 7 is the device with the realization of the metal line access, acheived with the same routine as for the contact accesses and the panel 8 is its longitudinal cut.

I just presented the most important steps of a standard process flow developed here at LETI to realize 300 mm wafers of *standard* MOSFETs[11]. However, during years of collaboration between the LETI and the LaTEQS laboratories for the study of transistors at cryogenic temperature and the purpose of realizing quantum bits in such systems, it has appeared that the standard route is in fact not optimized for quantum, cryogenic purposes. In the next section I will point out some aspects of a standard MOSFET that need to be modify in order for the quantum physicists to realize quantum bits.

Custom steps for the quantum physicists

The standard process flow presented above is optimized for classical electronics. As I said before the presentation of that process, the $\frac{R_{ON}}{R_{OFF}}$ ratio of a transistor is one of the most crucial figure of merits for electronic purposes. A low gate voltage and the reliability of the transistors are also of prime importance in that context. However, depending on whether it is

[10] standing for Chemical Vapor Deposition.
[11] here, standard means optimized for the microelectronic market.

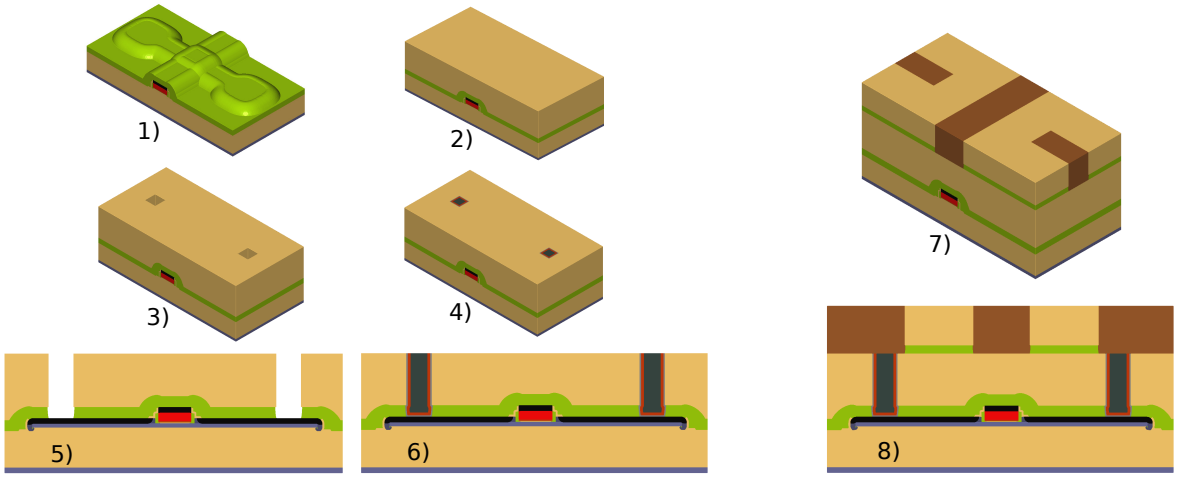


Figure 3.11 *The device is finally functional. The remaining steps consist of the encapsulation, the contact accesses and the metal line access. I will present the contacts acceesses because the metal line access follows the routine . Contact accesses: Step 1) we deposit a layer of silicon nitride (green) called the* contact etch stop layer. *Step 2) we deposit hundreds of nanometers of silicon dioxide (yellow) and we flatten the top surface. Step 3) We first etch the silicon dioxide until the contact etch stop layer and then we etch the latter. Both are done with the contact access mask. Step 4) we fill the contact access with a trilayer layer of first titanium, then titanium nitride and finally tungsten. Schematics 5) and 6) are longitudinal cuts of the steps 3) and 4), respectively. Step 7 shows the device after the metal line access and the panel 8 is its longitudinal cut.*

for a classical or a quantum aim, the required functionalities are not the same. On one hand, to satisfy their needs, electronical enginners have done technical choices such as a very thin gate oxide, shorts spacers or specfic junction engineering (relative to the LDD and the HDD processes). On the other hand, in the frame of quantum dots, the needs are different. For instance, a MOSFET at dilution temperature may host a quantum dot underneath the gate if and only if the channel is sufficiently isolated from the leads.
I am now going to present some key adjustments that can be done during the fabrication process. To do so, I will call back some of the last figures (started from 3.4 to 3.11) and discuss the possible changes.

In the figure 3.4, showing the design of the silicon nanowire, one can shrink down the width of the nanowire to get smaller quantum dots. For instance, the device used in chapter 4 and presented in the future section in the figure 3.15 gets a very agressive width of 18 nm instead of the standard 80 nm [12]. This is very interesting because the charging energy

[12] done with DUV etching.

of a quantum dot, the energy you need to add one charge, increases when the dimensions decrease allowing the scientists to go deeper in the quantum phenomena.

The figure 3.5 is dedicated to the gate stack. Important changes may occur here. I shall mention two things at that point. First, from a geometric point of view, it is now possible to design multigate devices. One just has to create a more complex gate mask. In fact, only devices with two gates will be studied in this manuscript. Two major families of devices can be produced: the *pump* geometry with the two gates in serie along the nanowire (see figure 3.15 for an example) and the *corner gates* or *face-to-face* geometry with the two gates being on top of the corner of the nanowire, facing each other (see figure 3.14 for an example). Second, from the gate stack point of view, electronic research enginners showed that the 1.9 nm high-K dielectric layer laying above the very first layer made of silicon dioxide of the gate stack is responsible for trapped charges and dipoles at the interface between the silicon dioxide and the dielectric, being very close to our channel. This leads to a disturbed electrostatical landscape very close to the quantum dot as well as more variability between two nominally identical devices (see for instance this study realized at CEA LETI [76]). We then decided to remove the high-K dielectric layer for the last batches and to come back to the original insulating layer full made with silicon dioxide. Furthermore, we decided to make insulating silicon dioxide layer thicker and, thus, the device is more robust against electric breakdown[13].

The figure 3.6 presents the spacer 1 deposition. From both the classic and the quantum electronic point of view this spacer is crucial but does not achieve the same purposes. For a quantum physicist, this spacer sould be large enough to ensure sufficiently high insulating tunnel barriers around the quantum dot[14] first and second to prevent as effective as possible any dopant implentations in the channel both below the spacers themselves and below the gate. This is the reason why most of the studied device get a longer spacer 1. We simply deposit 3 times the spacer 1. This can be shown in the next figure 3.14 and we eventually end up with an effective spacer 1 of 30 nm instead of the 11 nm in the standard process flow.

The two figures 3.7 and 3.8 present the sacrificial spacer deposition and the hard mask removal. Technically, no changes have been done at these stages but I shall mention the following: the hard mask removal step takes some time and is quite challenging to execute.

[13] which is, in fact, one of the most common and easiest way to destroy a MOSFET..

[14] in practice, the conductivity of these barriers has to be less or around the conductance quantum $\frac{2e^2}{h} \approx 7.75.10^{-5}\,S$.

The hard mask is a thick layer. We normally take it out to ensure the most efficient doping of the poly-silicon of the gate in order to end up with the lowest resistance between the future metallic contacts and the doped poly-silicon. During my PhD, one classic, standard MOSFET batch was designed with the hard mask still in place during the doping steps of the gate. I put one of these single gate transistor at dilution temperature and unfortunately these devices are useless. It appeared that the electric potential of the gate was fluctuating, drifting with time making these devices inoperative. That was due to a very high interface resistivity between the metallic contact and the poly-silicon. The conclusion is: in that process or processes very similar to that one, you have to take out the hard mask to have a metal/poly-silicon interface resistivity as low as possible. However, in different processes, other solutions can be found where the hard mask is not removed[15]

I just presented core modifications for the standard process flow to be adapted to quantum dot devices. Now I am going to present two of devices that I studied during this PhD, insisting on the geometry.

3.2.3 Presentation of the studied devices

During these three years I have characterized and measured many different devices coming from many different batches. Each batch has its own specificity. I will describe the devices that I am going to present in the two last chapters, ordered chronologically. On top of that I am going to give the full reference of the devices, the batch number, the wafer, the die, the type of the device and the device's numbers. I know that, in the frame of a thesis these informations are a bit superficial but I think they are quite important for future PhD students and even permanent researchers.

First, in the next chapter 4, I present some results about the impact of the backgate on the coupling between two quantum dots in the figure 4.2. These measurements have been done on a N-type face-to-face device coming out of the Carnot batch (*T14S0810B*) and more specifically from the wafer 5 (die 249, SHN4 device 4), lightly doped in arsenide below the long spacers. The figure 3.12 shows the two field effects for both gates at 300K. A typical face-to-face device is presented in the figure 3.14 The width of the channel is 105 nm, the gate length is 60 nm (along the channel) and the length between the gates is 30 nm. On top of these results on the backgate dependancy with transport measurements, the first

[15] for instance, one can deposit an *in situ* doped poly-silicon instead of undoped poly-silicon.

measurements involving reflectometry that I carried on were on devices coming out of this batch.

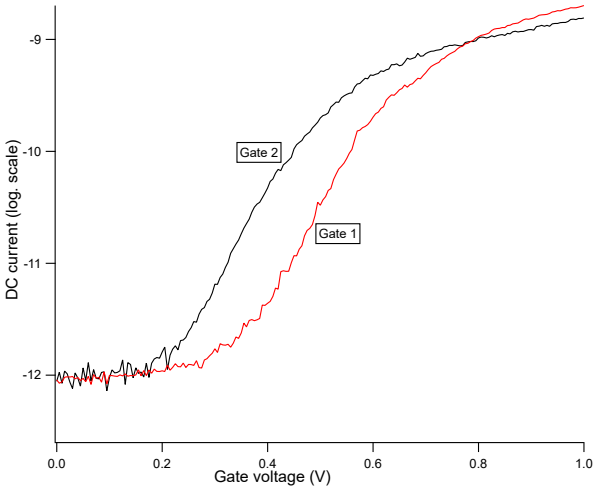


Figure 3.12 *Field effect characterization for both topgates of the N-type face-to-face device presented in chapter 4. T=300 K, Vdc=50 µV, the other topgate being set at -1 V.*

Second, following the backgate study we started to characterize the new metal line. The results are presented in the figures 4.3 and 4.4. This device was also a face-to-face (see the next figure 3.14) but doped with boron ensuring a P-type device. It comes out of the last batch I received, "MOSQUITO II" (*T18S0063*) from the wafer 16 (die 29, 1S25 device 3). The width of the channel is 70 nm, the length of both gates is 40 nm and the space between the gates is also 40 nm. This device is a bit smaller than the previous one but designed with long spacers as well. Pulse measurements and spin-related experiments have eventually been done on that device and are presented in chapter 5. The next figure3.13 presents both field effects of the two gates for that device at 300 K.

Finally, the last part of chapter 4 is dedicated to the notion of quantum mediator, experimented on the device presented in the figure 3.15. This is an N-type serial double gate device and it comes out of the first batch I studied, "SIAM 3" (*T14S0788*) from the wafer 23 doped in arsenide (die 259 SHN6 device 3). Its field effect characteristics are presented in the figure 3.16 for both gates, at 300K. This is the smallest device I ever studied with a width of roughly *18 nm* (to be compared to the previous mentionned witdh of 105 nm and 60 nm), a gate length of 35 nm and a space between the gates of 30 nm. This device is also the only one that I studied designed with *short spacers* and thus, has a pump configuration with two serial topgates and a central metallic island. I will show that the extreme small dimensions of

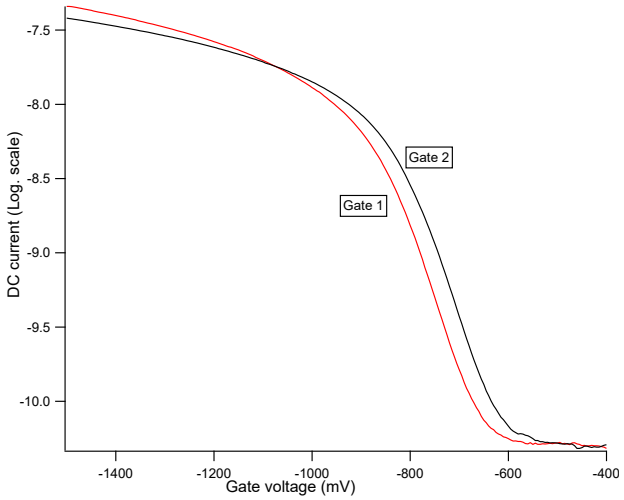


Figure 3.13 *Field effect characterization for both topgates of the P-type face-to-face device presented in chapter 5. T=300 K, Vdc=5 mV, the other topgate being set at +1 V.*

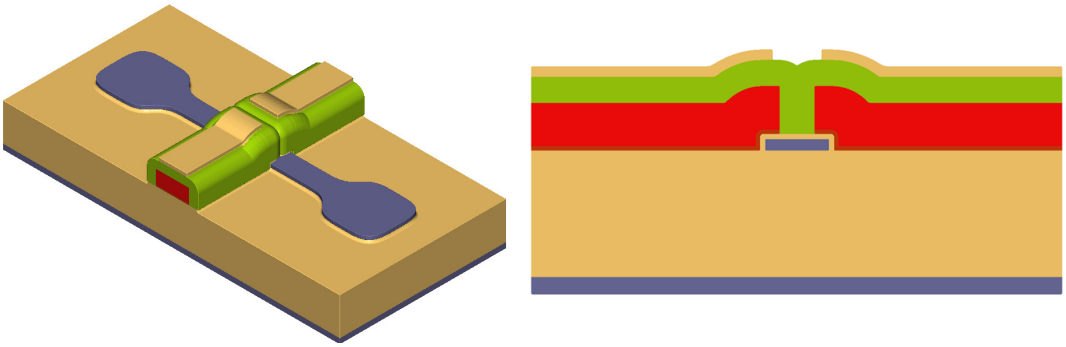


Figure 3.14 *Face-to-face geometry. Almost all the studied devices in this manuscript are Face-to-face except the last part of chapter 4. The left panel is a 3D schematic taken after spacer 0 deposition and the right panel is a cut along the red gates. Instead of having one wrapping gate all around the nanowire, we do an e-beam lythography to split the gate in two parts, preferentially at the middle of the nanowire. The length between the gate is aroud 35 nm. The reader shall notice that this in-between space is fully filled with the long spacer 0. If it were a short spacer, the inner area would not have been protected.*

the device allow for more exotic physics, yet to be understood, than the simplest case of an electron pump.

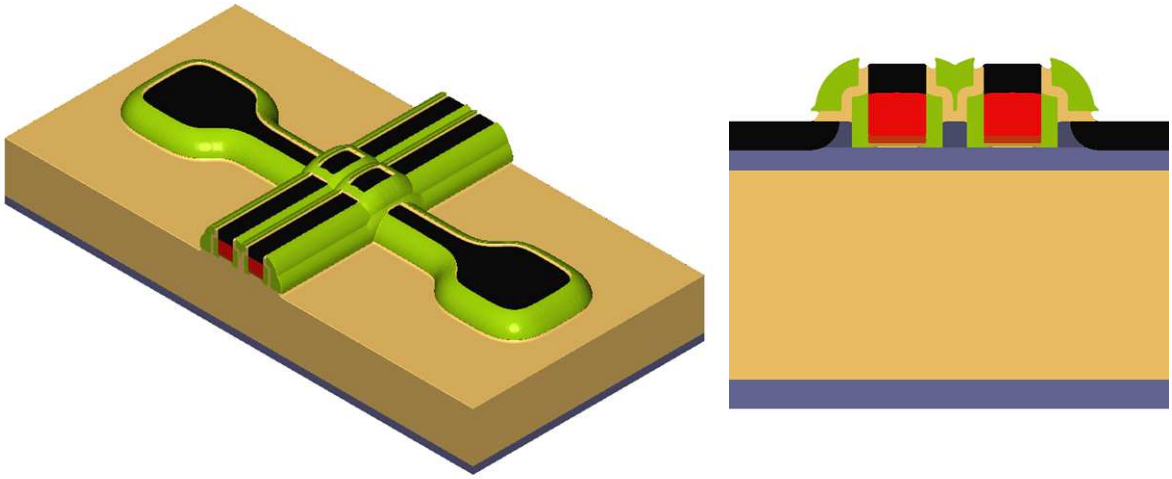


Figure 3.15 *Pump geometry. This exact device is studied in the last part of chapter 4. The left panel is a 3D schematic taken after metallization of the gates and the channel and the right panel is a longitudinal cut along the nanowire. Compare to the last figure 3.14, the two gates are now in serie along the nanowire. The reader shall notice that for that device, the spacer 0 was short. This is the reason why in between the gates we do not fully protect this inner area and some dopants will diffuse towards this inner region.*

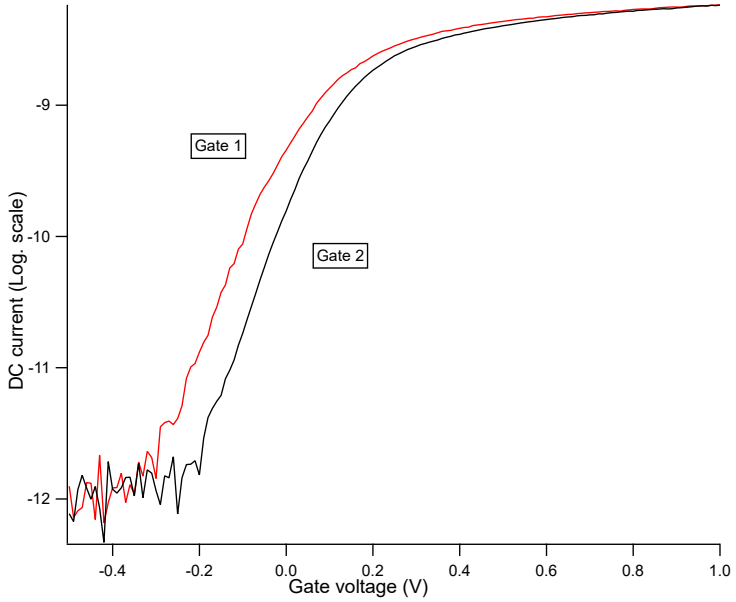


Figure 3.16 *Field effect characterization for both topgates of the P-type pump device presented in chapter 4. T=300K, Vdc=500µV, the other topgate being grounded.*

3.3 Electronic Setup

During this PhD I have worked on three different types of cryostat. First I used *Diluette*, a 1K pot-free wet dilution fridge using a Joule-Thompson impedance to precool the mixture around T=1 K. The experiments and results described in the next chapter about the three dot device were done in this fridge. Unfortunately, the wiring (mostly microcoaxials) in place allowed only for transport measurements. Second, I ran the first cooldowns of the new homemade Helium 3 dry dilution fridge of the laboratory, *Tritonito*. Working with Helium 3 offers the advantage of tuning the base temperature between T=350 mK to T=1.2 K. It has worked well for the last 6 months. Third and last, I finally worked on a classical wet dilution fridge with its 1K pot, *Dilu06*. The results presented in the final chapter 5 on this thesis have been done on that fridge. In this part I will focus on the electronics inside and around *Dilu06*.

3.3.1 Electronics for the radiofrequency reflectometry and the pulse lines

As I will explain in the last chapter, we need for the reflectometry setup to send a tone at several hundreds of MHz and read the reflected signal. To do that, many practical ways can be used. In the next part, I will explain in detail the one I used the most, involving a UHF (standing for *Ultra High Frequency*) lock-in demodulator but first I want to present an alternative which does not require a UHF lock-in demodulator but rather a HF (*High Frequency*) lock-in demodulator. Such HF lock-in demodulator works in the tens of megaHertz range. To do so, we need to proceed to a down-conversion technique[16]

A word about the setups not involving the UHF demodulator

Historically, the first experiments involving reflectometry measurements on LETI's devices in the laboratory were carried by X. Jehl. and A. Orlov from University of Notre-Dame, Indiana [72]. At that time, no UHF lock-in demodulator were available so they used to use a HF lock-in demodulator (working range up to 50 MHz). Moreover, because of the low SNR, they had to double the demodulation.

At the beginning of my reflectometry experiments I did not have the choice but to use a HF demodulator. The resonance frequencies of the tank circuits are still in the hundreds of MHz range though I could only acquire signals below 50 MHz of frequency.

[16]For informations about the HF and UHF lock-in demodulator, the interested reader shall go to the zurich instrument website www.zhisnt.com

The RF incoming signal going down to the device is at the resonance frequency, around 400 MHz. The RF reflected signal going up to the acquisition system is also at the resonance frequency. To be able to analyse it, we have to down convert this reflected signal into a lower frequency signal, below 50 MHz. I will not go into the detail. However the interested reader shall read the section V of the following article [20]. It deals with superconducting qubits apparatus but the same measurement setup is needed.

Setup with the UHF demodulator and wiring inside the fridge

The cryostat has been used since 2006 and is "made in the lab". During these years, the electronic setup as well as the cryogenic setup have evolved to fit practical reasons over different experiments. Originally, this cryostat was set up for simple transport experiments, therefore four DC sources were used, two for the topgates bias, one for the backgate bias and one last for the source drain-bias. On top of the DC lines, this fridge now features 4 hermetic SMA feedthroughs entering from the helium bath into the IVC (Inner Vacuum Chamber), the hermetic chamber where the sample is placed in. Originally two were used for electron pumps experiments (see [77], for example). Then the two others have been used for the dual Radio-Frequency Reflectometry setup initiated by A. Orlov (in particular for this article [72]). They sent both the RF and the DC tone onto the topgates thanks to a bias tee placed in the helium bath.

Back in may 2018 when I started working on that frigde, I got a pair of lines going onto the topgates (each line has it own bias tee to add the DC bias and the RF signals for the reflectometry) and a pair of independant lines (called the *pump lines*) supporting high frequency signal. The power source used for the backgate bias will be used to bias the metal line instead.

Moreover, the original sample holder of this fridge was quite unique in the lab, not allowing easy transfer of devices from one fridge to another. We decided to change the sample holder and replace it by the new standard PCB (standing for *Printed Circuit Board*) used in the lab. The next figure 3.17 presents both the old and the next sample holder. On the latter, 24 DC lines and 4 RF lines can now be plugged.

In the last chapter, I will explain the last experiment that I have realized on that fridge but for the sake of clarity I am here going to only present the experimental needs for such experiment.

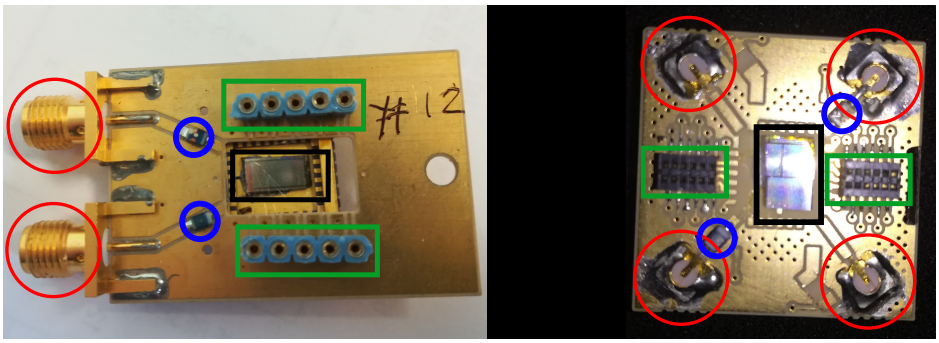


Figure 3.17 *Left panel: old sample holder. 10 DC lines, 2 RF lines . Right panel: new sample holder, 24 DC lines, 4 RF lines. The silicon piece of wafer is highlighted in black, the RF PCB connectors are in red, the DC connectors are in green and the inductors used for the tank circuit are in blue. Practically, one has to microbound between the elements using the metallic lines of the circuit (these bounds are barely visible on the left panel). Note that, on the new sample holder, the PCB connectors front side is hidden (this picture shows the back side of these mini-SMP connectors) and we were usingonly two out of the four channels at that time.*

We want a setup that allow us to DC bias, to send a RF tone and to pulse quickly onto both topgates, so three different signal bandwidths on the same wire at the end. We already have the DC and the RF signals added together through a bias tee. This bias tee, a mini-circuits *ZFBT-4R2GW+*[17] has a wide bandwidth on the RF port, from 100 kHz to 4.2 GHz. However we need a third tone to pulse fast. We finally decided to cascade this bias tee and a diplexer marki *DPXNM50*[18]. The next figure 3.18 is a picture of the setup wired in the cryostat can for only one channel. The reader shall know that we replaced the former electronical setup by this new one while the device being still in the IVC on its sample holder and the grounds placed at the very end of the line being disconnected !

Both the incoming and the reflected RF tone are represented by white arrows, the DC bias by a grey arrow and the pulsed signal by a brown arrow. From top to bottom, we first see the RF directional coupler (mini-circuits *ZFDC-20-50*, from 20 MHz to 2GHz), pointed in red, which separates the incoming and the reflected RF signal. The incoming signal goes down to the high frequency port (top port, 70 MHz to 10 GHz) of the diplexer , pointed in blue, through the blue wire while the reflected signal goes up to the outside of the cryostat through the *out* line (right output) of the directional coupler. On the right side of the diplexer is the bias tee. The DC bias voltage is sent to its DC port (top port) while the fast pulsed signal is sent to its RF port (right port). The outcome of the bias tee is sent to the low frequency

[17] commonly used in that fridge at 4K.
[18] details on www.markimicrowave.com

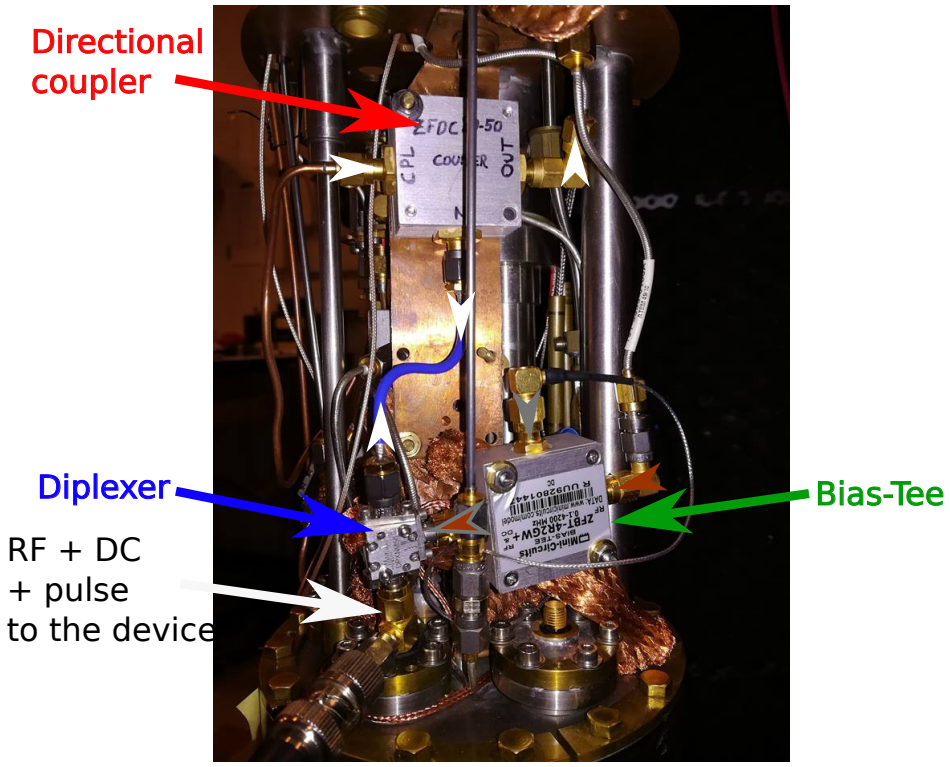


Figure 3.18 *Close picture of one full channel consisting of a bias tee cascading a diplexer. On top of the picture is the directinonal coupler (red) for the RF tone (white arrow) connected to the high frequency port diplexer (blue) with the blue wire. Close to the diplexer is the bias tee (green), summing the DC bias (grey arrow) and the pulsed signal (brown arrow). The output is sent to the low frequency port of the diplexer. The final signal coming from the diplexer is sent to one of the two gates of the device. The other gate has is own full channel.*

port of the diplexer (left port, DC to 35 MHz). Finally, the output signal of the diplexer is connected to one of the two gates of the device. The other channel has its own coupler, bias tee and diplexer. The next picture 3.19 illustrates the different bandwidths of these electronical components.

The really new part of this line is the pulse part, going through the high frequency port of the bias tee and the low frequency port of the diplexer. This line must support a single square pulse with very short rising time over a wide range of duration time, going from a few microseconds to a few milliseconds. I characterized the two new pulse lines before closing the cryostat and cooling it down. The picture 3.18 was in fact taken during this characterization as the reader can see the standard black coaxial connection connected to an oscilloscope at the very bottom left of the picture. Though this characterization will be pretty

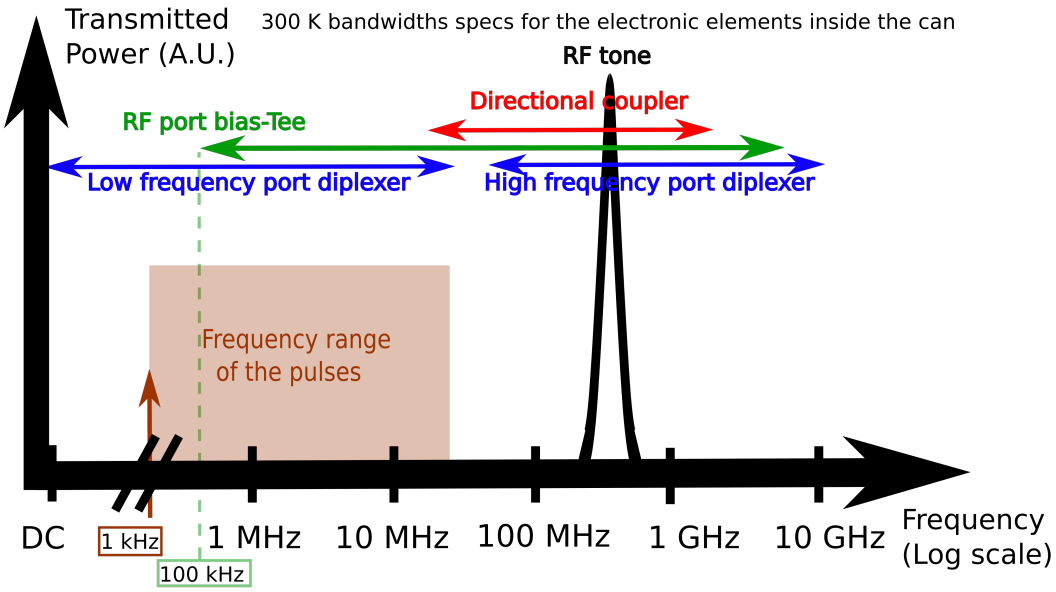
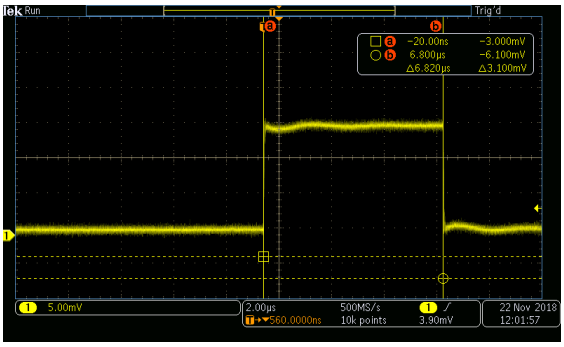


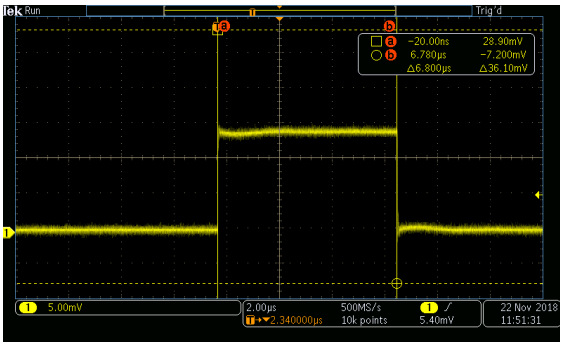
Figure 3.19 *Illustration of the bandwidths at 300 K of the electronic components inside the cryostat can. The RF tone, in black, is peaked at the resonance frequency of the tank circuit around 400 MHz. The two blue arrows correspond to both the low (DC to 35 MHz) and the high (70 MHz to 10 GHz) frequency ports of the diplexer. The green arrow represents the bandwidth of both the low and the high frequency ports of the bias-Tee (DC to 5 GHz). The red arrow delimits the bandwidth of the directionnal coupler (20 MHz to 2 GHz). Finally, the area in faint brown represents the full interval of the pulses involved in the experiment going from 1 kHz to tens of MHz.*

uncomplete, I can only test the lines at room temperature, it will give us a rather good idea of our accessible bandwidth.

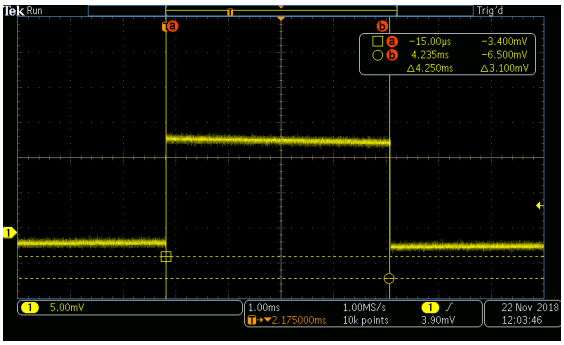
The characterizations of the line is pretty straightforward since the bandwidths are quite limited, one has to send a square pulse through the line and to record the transmitted signal with an oscilloscope. The figure 3.20 shows such transmitted signals for both channels 1 and 2 on the left panels (3.20a, 3.20c) and the right panels respectively (3.20b, 3.20d). The top panels show a short pulse of 7 µs while the bottom panels show a long pulse of 1 ms. The rising time of all of the transmitted square pulses is 24 ns. We can easily see that the overall shape of the square pulse is preserved except for a little wiggling at the start of the short pulse for both channels and a non-perfect square shape (the signal decreasing a bit with time) for the long pulse with the channel 2.



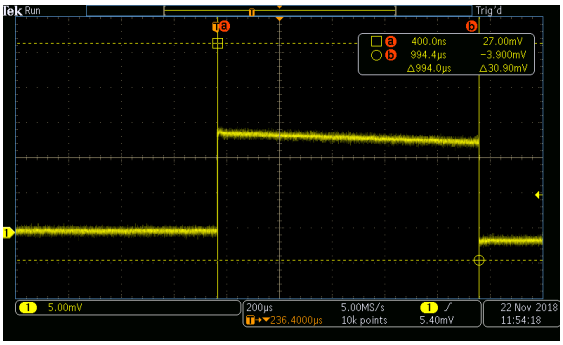
(a) 7 µs square pulse through the channel 1.



(b) 7 µs square pulse through the channel 2.



(c) 1 ms square pulse through the channel 1.



(d) 1 ms square pulse through the channel 2.

Figure 3.20 *Pulse characterizations for the two channels. Left panels: Channel 1 caracterization with a short, 7 µs pulse on the top panel and a long, 1 ms pulse on the bottom panel. There is a 900 kΩ resistor on top of the DC 1 line. Right panels: Channel 2 characterization with agin a short, 7 µs and a long, 1 ms pulse on the top and the bottom panels respectively. There is also a resistor on top of the DC 2 line but its value of 10 MΩ is bigger.*

However, the reader shall know that at the beginning of the characterization, the DC ports of the bias tees were *open*, the DC coaxial cables of the gate voltages were not connected, thus the bias tees were not 50 ohm-matched. This is why I was able to send a sharp square pulse between 1 µs and 1ms through the RF port of this mini circuits bias tee which, in principle, is not designed for very low and very high frequency signals. In fact, as soon as I did connect these DC coaxial cables, the transmitted signals were completely different with a huge RC effect exhibiting exponential rises and falls over hundreds of microseconds. To solve this issue I decided to put a resistor in serie on top of each DC line, outside the cryostat. This will bring the bias tees in an favorable regime again as it was at the beginning with the DC ports open.

Finally, I did the characterization while testing some values of resistors for both gates and ended up with a 900 kΩ resistor for the channel 1 and a 10 MΩ resistor for the channel 2 in

order to be able to transmit a square pulse between a few microseconds and a millisecond. The signals of the figure 3.20 were recorded with these values of resistors for both channels.

The reader shall notice that there is an order of magnitude between the two values of the resistors while the two channels were supposed to be identical. To this day, we think that the multiple thermal cycles involved during the cool down and the warm up of the cryostat could be responsible for possible alterations of the solders between inner components of the bias-Tees. On top of that, the cool downs are particularly brutal and quick, over a few minutes only, for this wet cryostat. These alterations are unpredictible and, most probably, they have not impacted the two bias-Tees in the exact same way.

We eventually succeeded in having a cryostat that allows us to DC bias, to send a RF tone and read its reflected signal and to pulse over a fair range of time, from a few microseconds to a couple of milliseconds on the two gates at the same time. These were the prerequisites for the experiment that I will present in chapter 5. On top of the mandatory components presented earlier we also put some attenuators along the lines inside the cryostat can. They achieve two main roles: first they will attenuate standings waves occuring all along the lines because of imperfect cables and connectors, thus leadind to parasitic reflections. Second, they are used to prevent the black-body radiation of the incoming, hot signal towards the cold region of the fridge by ensuring the thermal enchoring at each stage. The following figure 3.21 shows a schematic of the wiring inside the fridge.

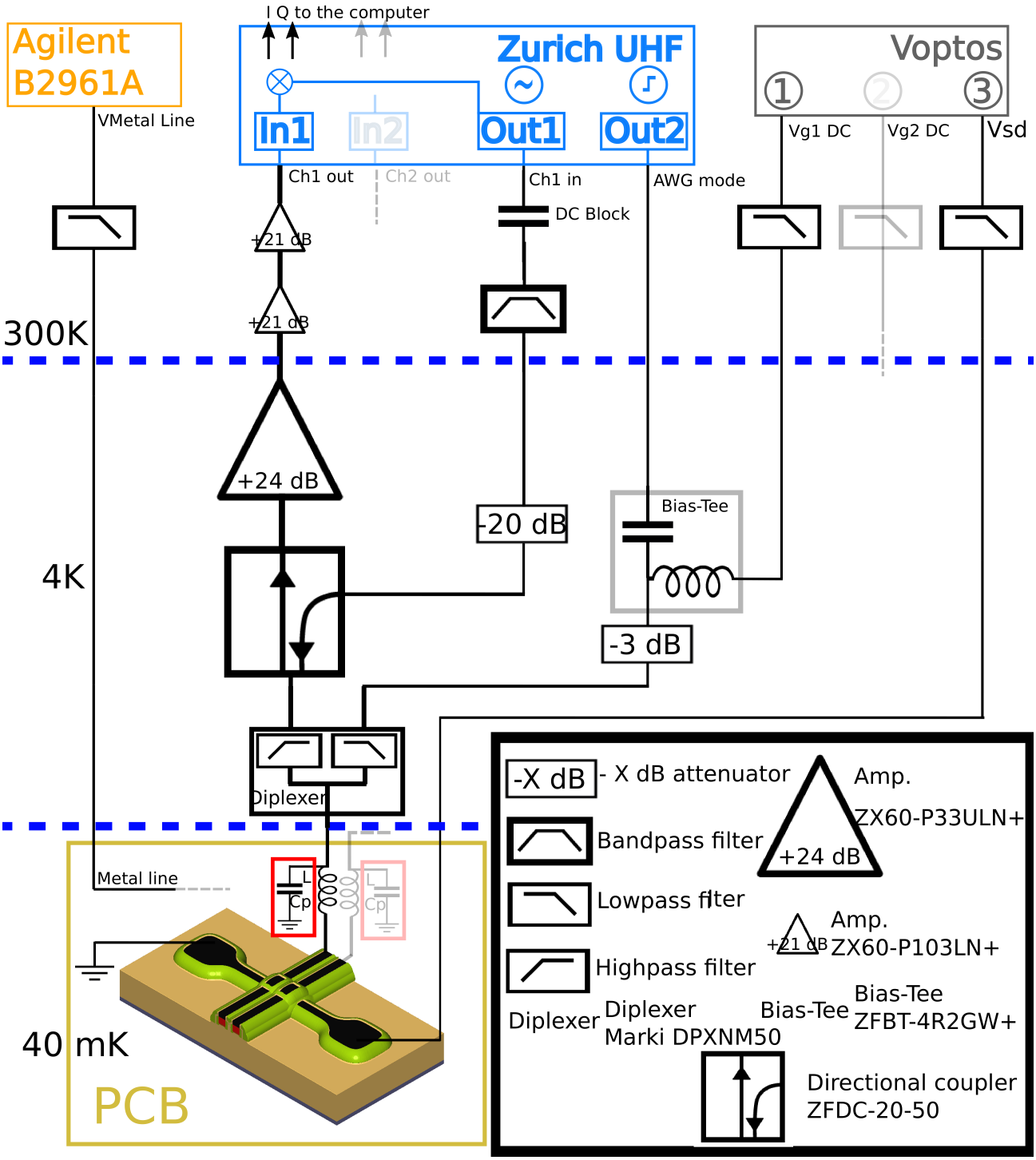


Figure 3.21 *Legend on the next page.*

Figure 3.21 *Schematic of the wiring setup inside and outside the cryostat can. For the sake of simplicity I only represented one channel of reflectometry, though both channels for both gates have been set up in the cryostat. Every line in grey is related to the second channel of reflectometry. Moreover, I did not represent the channel used to amplify and meausre the current going through the nanowire. 300 K stage: we can see the voltage source for the backgate/metal line in yellow, the Zurich Instrument (ZI) UHF lock-in demodulator in blue and the DC voltage sources (called Voptos),in grey, biasing the topgates and the nanowire. I will now focus on the most important part of the setup. The output 1 of the ZI UHF provides the 400MHz RF tone. The second output is controlled by the AWG module within the ZI UHF and generates the pulse sequence. Both inputs of the ZI UHF are dedicated for the reading of the reflected reflectometry signal for both channel. The part of the setup introduced earlier and placed in the cryostat can corresponds to the 4 K stage. The RF tone is sent from the output 1 to the coupler line of the directionnal coupler. The pulse sequence, generated by the AWG module, is sent from the output 2 to the high frequency part of the bias-Tee while the DC bias coming from the Voptos voltage source 1 is sent through the DC port of the bias-Tee. The output of the latter, combining the DC bias and the pulsed signal, is then sent to the low frequency part of the diplexer. The high frequency part of the diplexer is connected to the output of the directional coupler, to the RF tone. Finally, in the base temperature stage, the output of the diplexer is sent to one gate passing through a tank circuit (highlighted in red) made of an inductance L and a parasitic capacitance C_p . The Yellow square represents the new PCB sample holder and corresponds to the right panel of figure 3.17. The reflected signal goes back through the diplexer and the normal line of the directional coupler, is amplified at 4 K, then at 300 K and is eventually demodulated by the ZI UHF lock-in demodulator.*

Chapter 4

Tunability of the couplings

"Protons give an atom its identity, electrons its personality."
-Bill Bryson, 2003

Résumé

Ce premier chapitre expérimental est dédié au couplage entre deux boîtes quantiques et, plus particulièrement, aux différentes façons d'ajuster ce couplage inter-boîte.

La première section présente la façon 'historique' d'ajuster le couplage inter-boîte dans un dispositif du LETI grâce à l'utilisation de la grille arrière dans le cas d'un dispositif double boîtes à électrons en géométrie parallèle. J'expliquerai pourquoi c'est la voie naturelle et quelles en sont les limites.

La deuxième section discutera d'une nouvelle façon d'ajuster le couplage inter-boîte inspirée de la méthode de la grille arrière, l'utilisation de la ligne métallique. Il s'agit en fait d'un nouveau degré de liberté disponible sur les lots les plus récents. Une démonstration de son impact sera présentée dans le cas d'un dispositif double boîtes à trous en géométrie parallèle.

Enfin, la dernière section sera dédiée au cas d'un couplage de deux boîtes quantiques *via* un médiateur quantique. Je montrerai d'abord comment on peut ajuster le couplage inter-boîte dans un tel système. Ensuite, je présenterai une situation particulière où le système se comporte comme un système parfait de deux boîtes quantiques couplées. Enfin, une tentative de remplissage du diagramme de stabilité dans un cas plus simple ainsi qu'une discussion sur les états excités clôture la section et le chapitre.

A central challenge in quantum bit systems is about to control the different couplings between the leads and the dots. In many semiconductor devices such as GaAs 2DEG heterostructures, these couplings are directly set by specified gates (for example, see ref. [46]). However, a crucial requirement for scalability is to reduce this number of gates, which together with MOS process constraints is why LETI's devices have a drastically lower number of them than such 2DEG platforms.

We will focus on the two main types of coupling impacting the physics of coupled quantum dots systems :

- Dot-lead coupling: reducing the dot-lead coupling will tend to isolate the quantum dots which is very important in Qbits systems. The more the system is isolated, the longer the characteristic times like the relaxation time will be.
- Dot-dot coupling: changing the regime between strong and weak coupling is important in some experiments. For instance, a possible protocol to propagate informations is to propagate the carriers themselves. This is called the shuttling of electrons/holes [78], [79]. The shuttling time between consecutive quantum dots $\tau_C = \frac{\hbar}{t_C}$, t_C being the tunneling energy of the carriers, must be shorter than the decoherence time of the quantum state T_2^*, meaning $\tau_C << T_2^*$.

I will present 3 ways of controlling the different couplings : the backgate, the metal line and the quantum mediator approaches, though I will mainly focus on the latter since the backgate approach had been studied by former students of the group and the metal line is nothing but another degree of freedom just depending on the device production processes.
I shall notice that in that chapter I will never talk about any reflectometry and spins experiments. The electronic system in place in the fridge at that time did not allow us to probe the system through RF-reflectometry but only with current measurements.

4.1 The backgate approach

4.1.1 A natural degree of freedom in SOI devices

In chapter 3, I presented the standard process flow provided by LETI's facilities. More particularly in the figure 3.4, the silicon nanowire is designed and lies on the buried oxide. The undoped silicon-buried oxide-nanowire system acts as a capacitor. By polarizing the silicon back layer we can polarize the nanowire. Thus, in addition to the top wrapped gate(s), the MOSFET technology provides another way of varying the electrostatic landscape in the

silicon channel, which we call the backgate. This is shown in the figure 4.1, panel a). It is worth knowing that, in most of the cases, the backgate is doped and is called a well, see panel b). The last panel c) shows a simulation of the impact of the backgate voltage on the electronic wavefunction in a face-to-face double quantum dot system.

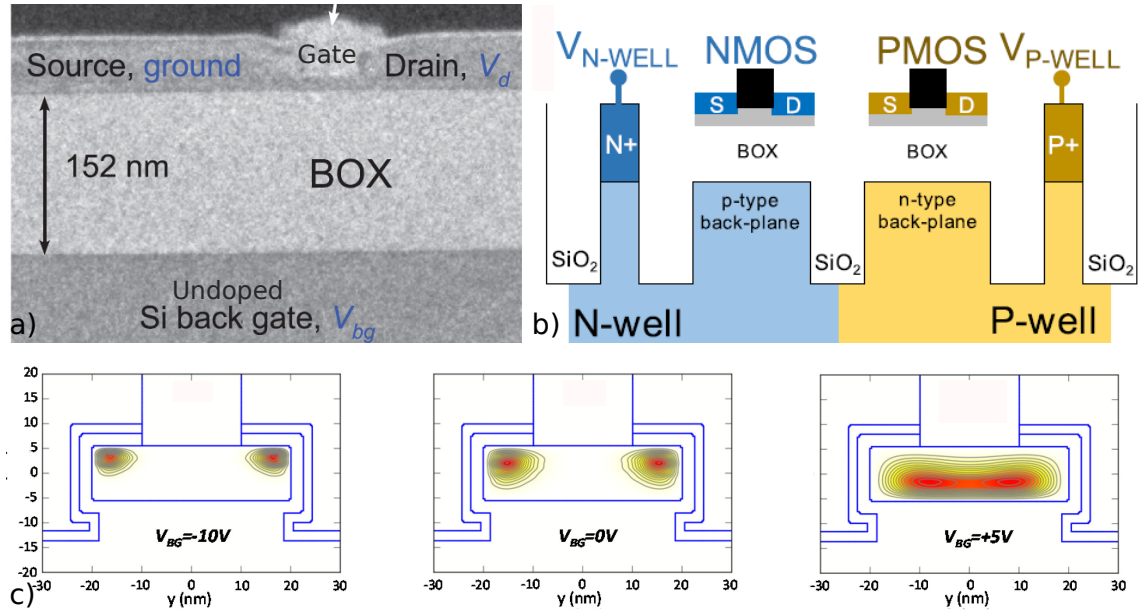


Figure 4.1 *Panel a) TEM Picture of a typical LETI MOSFET device. From bottom to top, the backgate, the 152 nm buried oxide called the BOX and the silicon nanowire. The bakcgate is polarized by biasing the sample holder uppermost layer itself made of gold. Panel b) schematic of a pair of a NMOS and a PMOS devices. The BOXs are in white, in between the back plane, also called the wells, and the channels. Each well is doped as a function of the doping of the device, N or P and can be directly adressed by a voltage. Taken from [80] The last panel c) shows a simulation of the squared wavefunction in a N-type parallel double quantum dot LETI's device. From left to right, the backgate voltage is increased. In the first case, the negative voltage tends to push the electronic cloud up to the gates. The inderdot coupling is weak. For intermediate backgate voltages, the electronic cloud lies more in the middle of the nanowire. the interdot coupling increases. In the last case, the positive backgate voltage pulls down the electronic cloud which lies in the bottom of the nanowire. In that case, the two dots have merged leading to a single, big, quantum dot. Taken from [81]*

Unfortunately, this silicon substrate is not naturally suitable for changing the voltage at low temperature[1]. In fact, below a certain critical temperature, the carriers in the silicon freeze

[1] I shall mention that this is true for the typical LETI process flow where the silicon backgate is undoped, see panel a) of figure 4.1. In different processes like the ST FDSOI one presented in the panel b) of the figure 4.1, the backgate is doped and one does not need to shine any light to activate the carriers.

out[2]. As a consequence, varying the backgate voltage leads to very slow relaxations in the substrate making experiments impossible[3]. One solution has been found: shining light with a LED through an optical fiber directly over the sample just before and after changing the voltage value in order to activate the carriers [82]. Thanks to this trick, it becomes possible to experimentally study the impact of the backgate.

4.1.2 Some examples of backgate polarization

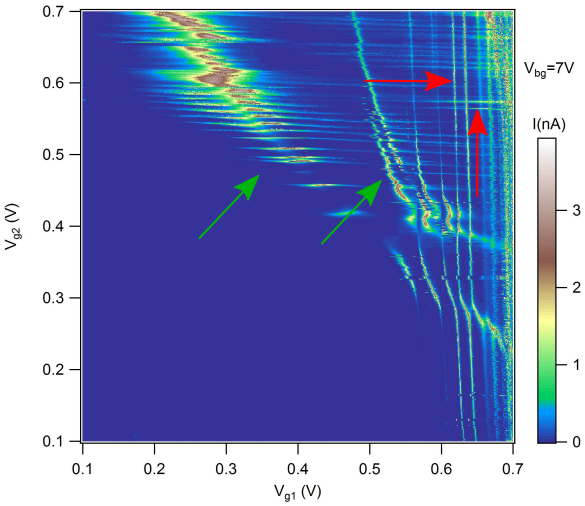
As written before, this degree of freedom had been studied a lot by former students. For example, it is possible to tune a transistor from field effect mode to single electron mode at 4.2K [82] or to vary the threshold voltage of a transistor both at room and cryogenic temperature. In fact, this backgate degree of freedom is a major advantage of FDSOI (standing for *Fully Depleted Silicon On Insulator*) technology as it allows to tune the performance of the device, mostly in terms of leakage versus ON current [83, 84].

The following figure 4.2 shows experimental results of the impact of the backgate on an N-type parallel double dot device (geometry presented in figure 3.14). I recorded three stability diagrams in transport for three different backgate voltages: V_{bg}=7 V for figure 4.2a, V_{bg}=11 V for figure 4.2b and V_{bg}=13 V for figure 4.2c, taken at T=60 mK and V_{bias}=100 µV.

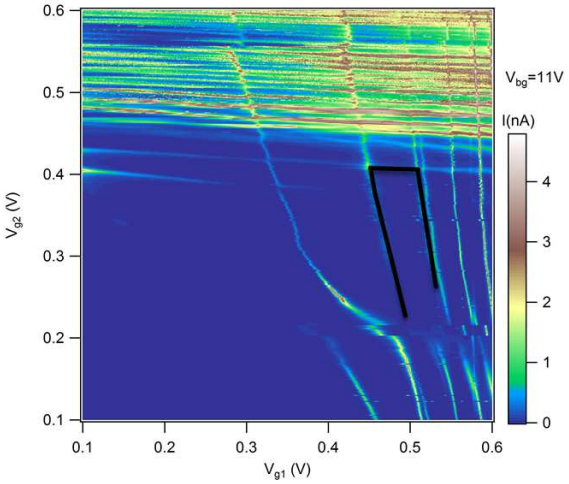
This is an N-type system, the carriers are electrons. A positive backgate voltage will then push up the the carriers density towards the top of the silicon channel, so towards the two topgates, increasing the lever-arm parameter and the proximity between the two electrostatically defined quantum dots. Indeed, the typical signature of a parallel (quasi) uncoupled double dot system is a (quasi) square lattice in the stability diagram [30] (for example, see figures 4.2a, red arrows and 4.2b, top right quadrant). When the backgate voltage is positive enough, the two dots get closer and start interacting, so the square lattice is stretched and the crossing points of the former square lattice tend to open [30] (see figure 4.2b, 4.2c, again top right quadrant. The evolution of the black shape illustrates this point).

The reader can also see a couple of lines passing accross the diagrams, indicated by green arrows in 4.2a. Both are attributed to dopants for two reasons: first, the slopes of these lines are different from the slopes of the lattice, indicating different capacitive couplings (with the topgates) between the objects responsible for the lattice (the dots) and the objects responsible for the two lines. This point is presented in the paper [85]. Second, the lines and the lattice

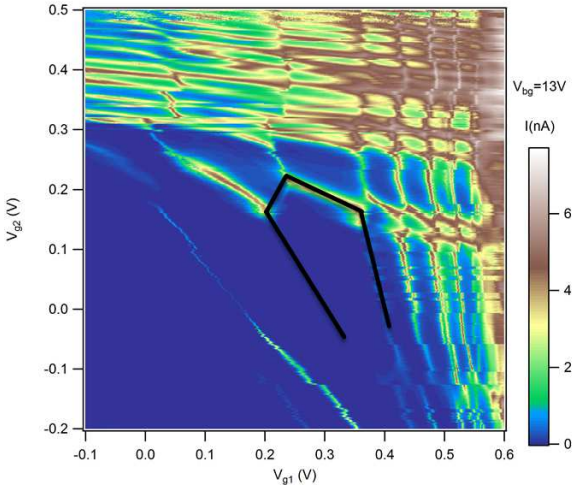
[2]The critical temperature depends on the device. In practice, this temperature is device dependant.
[3]These relaxations may occur over days ! for example, see Max Hofheinz's thesis [29]



(a) *Stability diagram taken at V_{bg}=7 V.*



(b) *Stability diagram taken at V_{bg}=11 V.*



(c) *Stability diagram taken at V_{bg}=13 V.*

Figure 4.2 *A parallel N-type double dot system probed in DC transport. Three stability diagrams (current in linear scale) taken at 3 different backgate values. One can see the lattice corresponding to the parallel double dots (indicated by red arrows in (a)) and two more lines corresponding most likely to dopants (green arrows). The black shape in (b) and (c) is just a guide for the eyes, showing the deformation of the lattice with respect to the backgate voltage.*

do not have the same dependency when we vary the backgate. These two arguments ensure that the dots are not responsible for the two lines, but rather that arsenic dopants are. Indeed, the regions between the leads and the spacers is lightly doped with arsenic, which diffuse below the spacers very near the region where the dots are defined [86].

4.1.3 Advantages and disadvantages

The fact that it is quite simple to implement makes the backgate a powerful and natural tool to tune the device. One just needs to glue the sample onto the sample holder with silver paste and bias the sample holder without forgetting the LED trick. This works very well for transport measurements (as seen in figure 4.2). Furthermore, the 150 nm thickness of the buried oxide allows us to span a large interval in backgate voltage, typically between -40 V to +40V, meaning that we have access to a large choice of backgate regime, from the large depletion to the large conduction regimes.

However, a reflectometry measurement relies on measuring a tiny change of a capacitance, namely the quantum capacitance, see the last section of chapter 2. Let's suppose one takes a device similar to one of the devices studied and embeds it in a tank circuit to perform radiofrequency reflectometry for different backgate voltages. At first, as long as this voltage is unchanged [4], everything will be alright. Yet, if you want to modify the voltage at base temperature, you need to shine LED light onto your device. This implies a reconfiguration of the frozen charges in the silicon substrate. In fact, this is like adding a new capacitor (made of the collection of frozen dopants) and, thus shifts significantly the resonance. It has even been shown that one can cross the under-to-over matched transition just by varying the backgate. Finally the backgate approach is not approriate for very small devices. The acting surface of the backgate onto the channel is so small that the electric field is highly screened by the topgates, the source and the drain potential leading to almost no effect of the backgate [87].

4.2 The metal line approach

4.2.1 A new tool from the recent batches

The LETI has added another degree of freedom on their last batches which we call the metal line. It consists in a copper line defined at *Metal 1* layer in the back-end-of-line process, hence it is lying 300 nm above the active (channel) layer. As shown in figure 3.11, right panel, this metal line is *always orthogonal to the silicon channel*. Being metallic, we can bias it without any needs of the LED light and then without any relaxation processes. This makes the metal line a more suitable degree of freedom for reflectometry measurements than the backgate.

[4] for example $V_{backgate}$=0 V both at room and base temperature.

4.2.2 Comparison with the backgate

While the backgate has an impact on the overall electrostatic landscape of the silicon channel, we expected the metal line to impact only on the leads tunnel barriers as well as the coupling between dots. Indeed, the electric field generated by the metal line is screened by the topgates and, thus, does not affect the areas underneath these topgates. Moreover, if the device has been designed with this metal line, it is even simplier to bias it than the backgate. One just needs to apply a DC voltage, even at dilution temperature. Additionally to this, the theoretical possible spanned range in voltage is even bigger than the backgate approach thanks to the 300 nm thick oxide. However, from a practical point of view, at some point the metal line starts leaking to the channel, around V=$\pm$50 V. Eventually we will work in the same voltage regime than in the backgate approach. I should also mention that the backgate is closer to the channel than the metal line. The lever arm parameter of the metal line to the channel should be smaller than in the backgate case.

4.2.3 Results

During this thesis, I have not fully characterized the metal line. I just wanted to see whether we get what we expected, meaning a dependence of the opacity of the tunnel barriers, as well as the coupling between dots, with the metal line, and try to use it later to tune the interdot coupling to a desirable range.

I decided to quantify these metal line effects on a P-type face-to-face device as this kind of devices has been almost unexplored previously in the laboratory. The carriers are holes so the essential difference with the device studied in figure 4.2 (which was also a face-to-face) is the sign of the electric charge. Then, the stability diagram is fully reversed [5]. If we want similar effects than in figure 4.2 we have to decrease the metal line voltage towards negative values.

The following figure 4.3 shows the evolution of a portion of a stability diagram as a function of the metal line voltage for six values of metal line voltage[6], starting from V_M=-200 mV in figure 4.3a to V_M=-1.2 V in figure 4.3f at T=45 mK and without bias voltage. We recorded in that study the phase of the refected signal (relative to the incoming signal) of

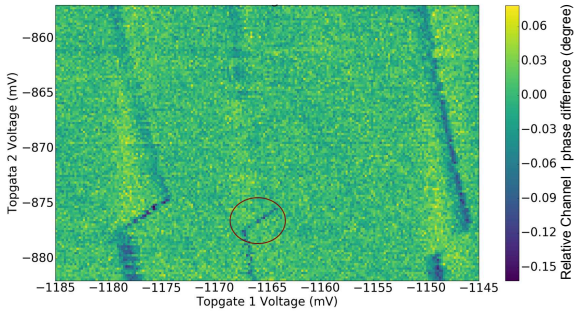
[5] for example, the many carriers regime illustrated by a typical honeycomb shape in the top right quadrant for electrons in figure 4.2c would be observed in the bottom left quadrant for holes in figure 4.3.

[6] All six measurements were realized in a row just by changing the metal line voltage between each map at base temperature.

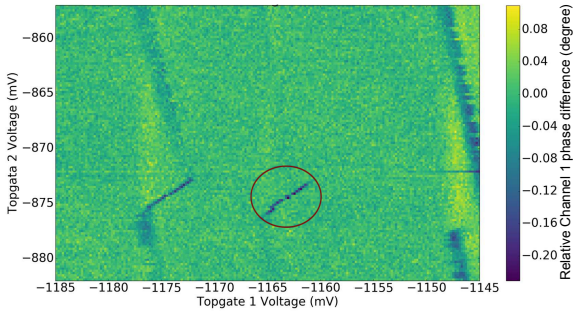
the channel 1, corresponding to the topgate 1. This is the reason why we only see (quasi) vertical dot-lead transitions corresponding to the dot below the topgate 1.

From these measurements one can extract a lot of information about the impact of the metal line. For example the following figure 4.4 shows the evolution of:(a) the position of the central interdot [7] and (b) the length of the interdot, both as a function of the metal line voltage and projected on V_{g1} axis. We then extract lever-arm parameters quantifying the voltage shifts occuring in the stability diagram with respect to the metal line voltage. We get for the position of the dot-lead-transition and interdot position: $\alpha_{Vg1/M}$=-0.014 and (by projecting on V_{g2}) $\alpha_{Vg2/M}$=-0.01 as a function of V_{g1} and V_{g2} respectively. The reader has to be aware that it is quite hard to do the same study with the dot-lead transitions. In practice these transistions strongly evolve non linearly with respect to the metal line voltage. Some of them are visible at a certain metal line volage value while they are not at others voltages.

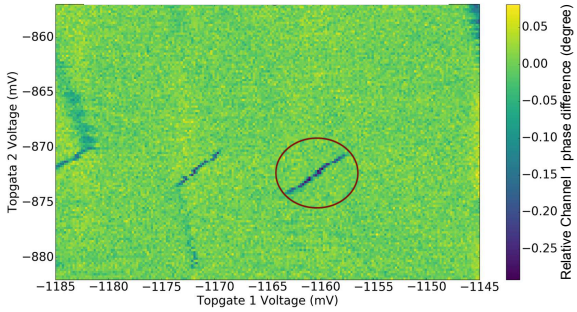
[7] I took the first-from-left triple point, the common point of the interdot and the bottom dot-lead transition.



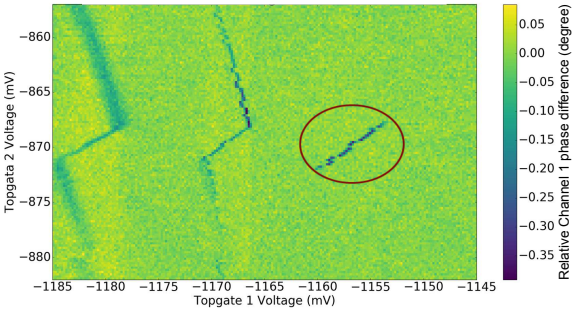
(a) *Stability diagram taken at V_M=-200 mV.*



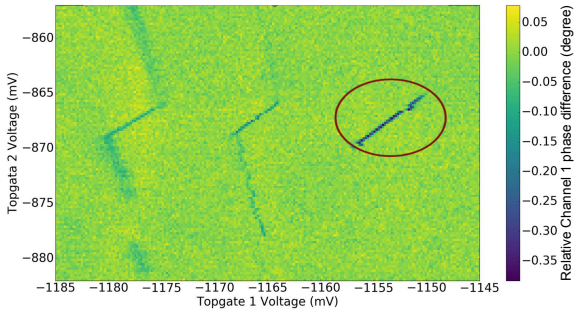
(b) *Stability diagram taken at V_M=-400 mV.*



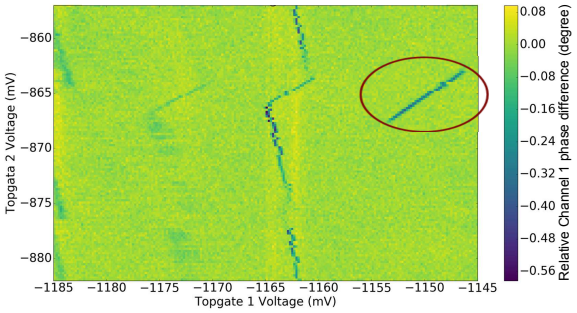
(c) *Stability diagram taken at V_M=-600 mV.*



(d) *Stability diagram taken at V_M=-800 mV.*

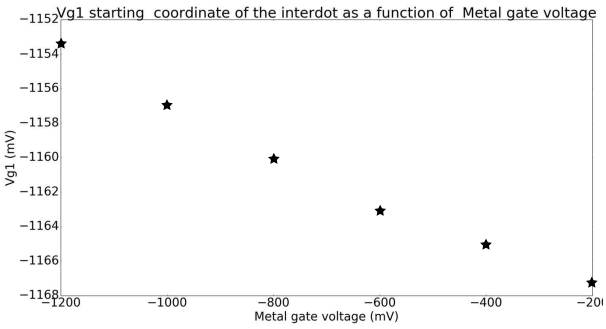


(e) *Stability diagram taken at V_M=-1 V.*

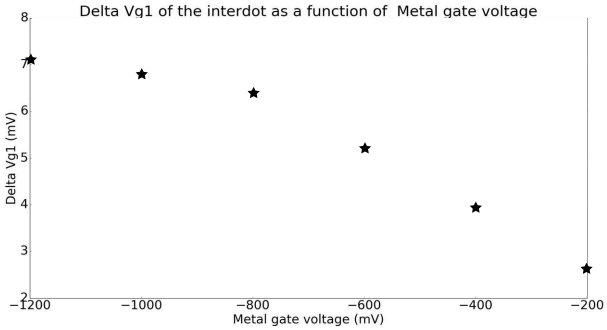


(f) *Stability diagram taken at V_M=-1.2 V.*

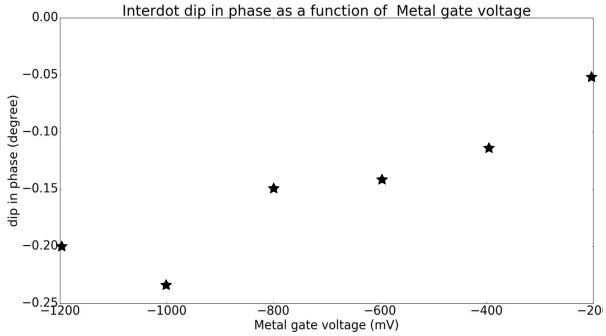
Figure 4.3 *Evolution of the stability diagram as a function of the metal line voltage recorded in reflectometry through the channel 1 (the phase is plotted). We focus on a couple of interdots and dot-lead transitions. We clearly see two mains effects: first, the intensity and the positions of the dot-lead transitions are modified. The displacement of the dot-lead transitions is monotonic with the metal line voltage but it is not the case for the intensities. Second, the interdot transitions seem to be stretched out, meaning an increase of the capacitive/tunnel coupling between the dots. The are getting closer to each other and/or the tunnel barrier between both dots is reduced. The red circle emphasizes one specific interdot, making easier for the reader to follow its evolution.*



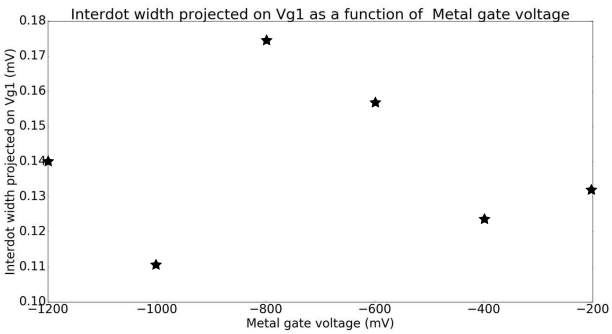
(a) *Interdot position as a function of metal line voltage, projected on Vg1.*



(b) *Interdot length as a function of metal line voltage, projected on Vg1.*



(c) *Interdot dip in phase as a function of metal line voltage.*



(d) *Interdot width as a function of metal line voltage, projected on Vg1.*

Figure 4.4 *Evolution of the interdot (the one emphasized in figure 4.3) characteristics as a function of the metal line voltage. First, we see in figure 4.4a that the interdot position (and so the dot-lead transition position) is shifted towards higher values in Vg1 while decreasing the metal line, meaning thinner tunnels barriers between the dots and the leads. Second, in figure 4.4b, we clearly see an increase of the interdot length while decreasing the metal line voltage, which is fully consistent with dots getting closer and a thinner tunnel barrier between them. Then, the figure 4.4c shows an increase in absolute value of the phase signal on the interdot line while decreasing the metal line voltage. Finally, the figure 4.4d shows the interdot width, projected on V_{g1}, as a function of metal line voltage. No clear evidence of any dependence can be deduced.*

Finally, the measurements confirmed our preliminary expectations. The metal line has a non-negligible impact both on dot-lead tunnel barriers and the interdot tunnel barrier. Thanks to these lever-arm parameters, it is possible to predict the position of an interdot for any values of the metal line knowing the position of this interdot for one specific value of the metal line. Morevover, we now know that the metal line impacts the coupling between the dots. Although it is quite hard to quantitatively predict the exact value of the dot-dot tunnel rate for a specific value of metal line voltage, this degree of freedom is likely to be a powerful experimental knob to tune the interdot coupling.

4.3 The use of a quantum mediator

4.3.1 Interest in such systems

I just presented two ways, two degrees of freedom allowing us to tune the the overall electrostatic landscape of the channel, including the interdot coupling. However, as introduced in chapter 2, there is a whole part of the research focusing on the notion of quantum mediator. Instead of having specified topgates (like in GaAs heterostructures) or other external ways to modify the electrostatic potential of the channel (like in this work with the backgate and the metal line) in order to tune the interdot coupling, there is a third way where one places a quantum object between two quantum dots. The coupling between these latter two quantum dots will strongly depend on the state of the central quantum object [44, 88, 79]. Many goals might be achevied by this way: for instance one can push one electron from a quantum dot A to another, different, quantum dot B through others quantum dots. This is called the coherent shuttling [47].

However, one can also use a wave to transfer carriers from one point to another. I will not go into the details but the reader should know about the *flying qubit* experiment which uses an electric wave [89] or about the Surface Acoustic Waves (*SAW*) experiments where a SAW resonator generates a sound wave [90] to generate the the propagation of the carriers. A last possibility to transfer quantum states consists in coupling quantum dots and photons through cavities [91].

4.3.2 Experimental realization and results

We therefore need a more sophisticated device than what we used before. We choose an N-type double gate device in series but with one specificity compared to the others studied before: the short spacers. As explained in chapter 3, the spacers define areas in the channel which are protected against the doping process. They are responsible for the tunnel barriers between the leads and the dots. However in a multigate device, there is some space between the topgates themselves. Although this area is well protected during the implantation when one uses long spacers there are also devices designed with short spacers. This allows the implantation of dopants in between the topgates, and so in between the dots, as shown in the right panel of the figure 4.5.

Usually, the dot formed by central dopants contains a lot of carriers and, thus, is a metallic dot. Indeed, the dose implanted during the *LDD* is high so if the place available between the

gates is big enough (tens of nanometers) one will get a huge number of dopants [8]. Moreover the source-drain epitaxy and the silicidation steps allowing the leads to become metallic also affects the central region. The thickness of this doped region increases by more than a factor 2. In most of the cases, one ends up with two topgates and one big metallic dot and can bring the device into an *electron pump* configuration [92].

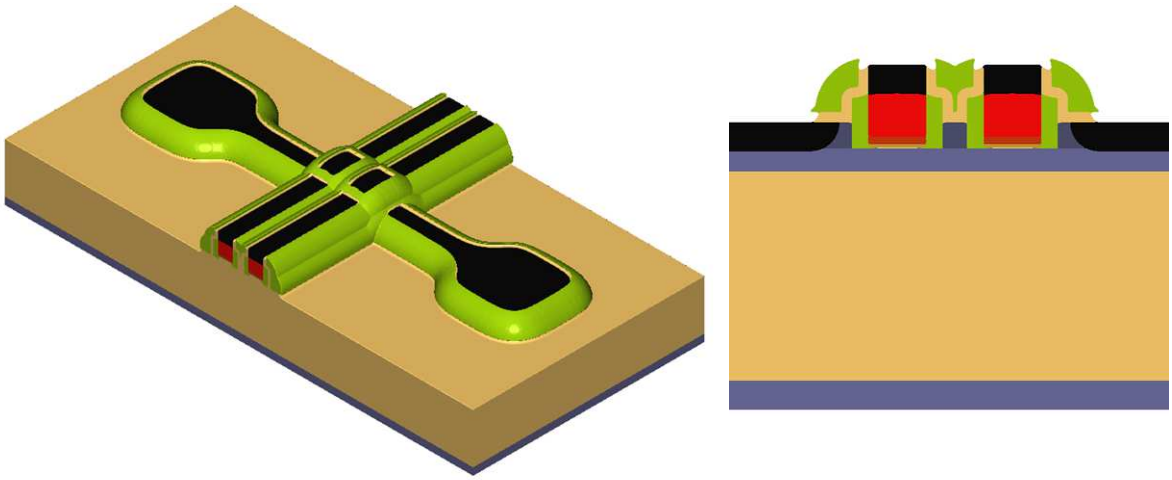


Figure 4.5 *Left panel: 3D schematic of a device nominally identical to the one used during the experiment. It consists of two topgates in serie, represented by the red and black multilayer, which define quantum dots just below those gates in the hidden channel. Leads are also in black at both ends of the channel. Right panel: longitudinal cut along the channel. From bottom to top: the end of the natural silicon layer, the BOX, the natural silicon channel in light blue, the doped zone in darker blue, the insulating spacers in green, the metallic gates in red and black, the silicidation of the leads in black on both sides. The reader can see that the region in between the two topgates is lightly doped. because of that dose, some dopants have got in the channel. The gate length (along the channel) is 35 nm, the space between the two gates is 30 nm and the width of the channel is 18 nm.*

Back to chapter 2 we have shown an electrostatic model for our triple dot device and some simulations in figure 2.16. The full experimental stability diagram of this device is shown in the following figure 4.6 recorded in DC transport (Log scale) at T=60 mK, V_{bias}=750 µV and a backgate voltage V_{Bg}=+35 V. At large scale, this stability diagram exhibits almost no features. This was the first surprise of that device which does not exhibit clean antidiagonals, signature of a singular dot between two gates, the *pump* compfiguration. Instead, we do see fainted antidiagonals and some *pointillism* along and in between them. It seems to appear that the dot is very small, so small that it does not behave as expected.

[8] about 10 000.

In fact the original point of that device is the intrinsic nature of the quantum dot formed by the cluster of few dopants in the middle of the channel. Indeed, while the two dots defined by the topgates can be modeled by orthodox metallic dots well described by the standard theory in the studied regime, the cluster of dopants cannot be modeled like that. The charging energy of this dot is big compared to the one of the two others due to the dopant nature of the dot. On top of that, in the figure 4.6 we clearly see that the antidiagonals are not fully straight. This is probably due to a voltage dependent shape of the electronic wavefunction. Depending of the topgate voltages, the electronic cloud is more or less coupled to one or the other gate.

A tunable coupling

Another interesting feature appears when one zooms onto the large stability diagram, around an antidiagonal. The left figure of 4.7 shows such a close picture on what is going on at small scale (red square in figure 4.6). While out of the antidiagonal we see an almost perfect square lattice, referring to the two outer dots weakly interacting together, the patterns appearing along the antidiagonal are more complex, being composed of hexagons *and* pentagons, referring to a three dots system.

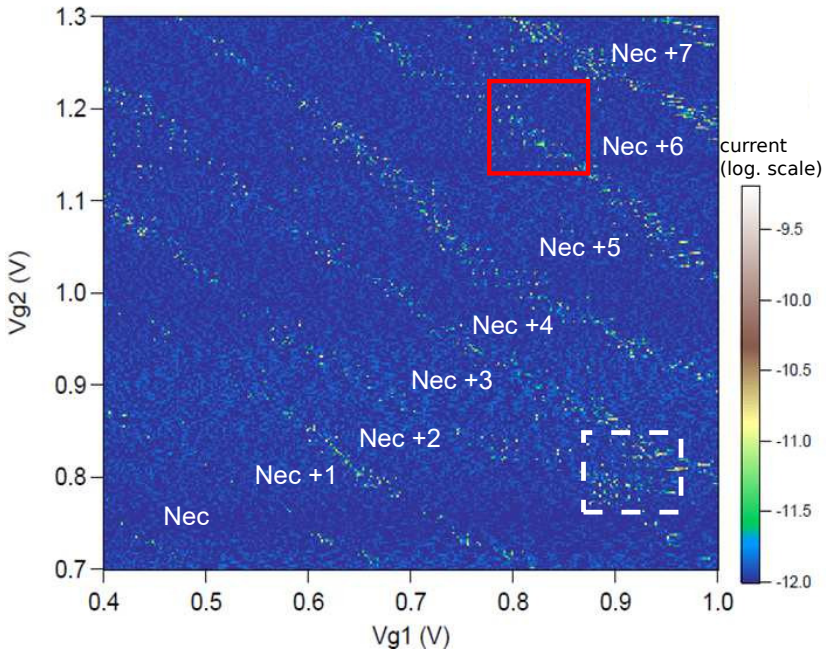


Figure 4.6 *Large stability diagram of the three quantum dot device recorded in DC current (log scale) at 50 mK, for a bias of 750 µV and a backgate voltage of +35 V. The reader shall notice that we almost see no current. Indeed this is what we expect for three quantum dots in series. Non-zero current means an alignment of the three electrochemical potentials. However one can see a set of (almost) parallel 45 degrees slope lines delimiting areas with a constant number of electron, N_{ec} in the central dot. The red area is shown in the figure 4.7 while the white dashed area in the figure 4.8.*

Remarkably, we can find areas where we go from an uncoupled to a strongly coupled double dot system. This is enlightened in the right figure of 4.7. First the zoom shows how the coupling between the outer dots evolves in the stability diagram when one varies the topgate 1 voltage. Second, I plot here the voltage splitting between the two bias triangles as a function of the topgate 1 voltage. The splitting takes one order of magnitude in voltage close to the antidiagonal compare to out of the line. When the electrochemical potential of the central dot start being aligned with the two other ones, both start strongly interacting together. This is only controlled by the topgate 1 voltage, or equivalently the number of electrons in the dot 1.

The possibility to electrically control the coupling between two dots through another in between quantum object may be a powerful tool in the context of a quantum bit read by another dot. Indeed, one can imagine one dot, the dot 2, in the few electrons regime while the dot 1 is in the many electrons regime. On one hand, the dot 2 would be the quantum bit read

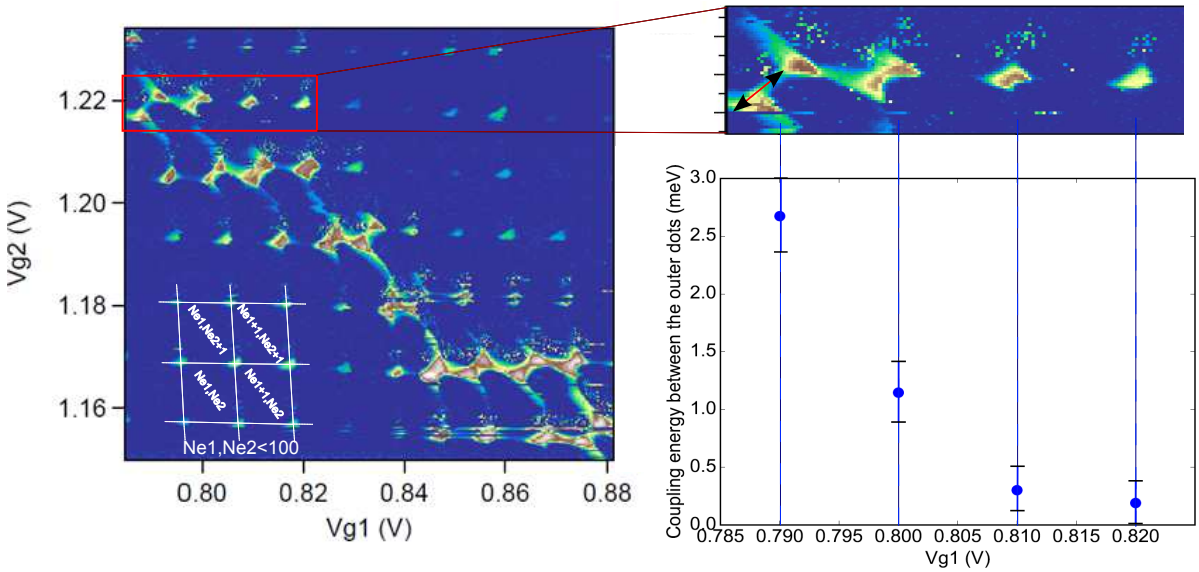


Figure 4.7 *Left: zoom in the red square of figure 4.6 around an antidiagonal. We see basically two different features: first there is a complex structure along the antidiagonal with pentagons and hexagons, signature of a triple dot system. Second, in the vicinity of the antidiagonal we see an almost square lattice, signature of an almost uncoupled double quantum dot (highlighted in white). To sum up, we see out of the antidiagonal the stability diagram of the two outer dots whereas the three dots strongly interact along the antidiagonal. Right: zoom on one triple points row highlighted in red in the left figure plus a plot showing the bias triangle split as a function of topgate 1 voltage (or, equivalently, as a function of the number of electrons in the quantum dot 1). Eventually, we are able to control the coupling between two electrostatically defined quantum dots thanks to the tuning of the electrochemical potential of a last central dot.*

by the dot 1 when both interact. On the other hand, the quantum bit would be manipulated when they do not interact, potentially limiting the decoherence caused by the dot 1. The initialization of the quantum bit would be achieved when both interact, by pulsing through the interdot line.

A textbook double dots system in a three dots device

During the study of this device, we first noticed the interesting property of a tunable coupling which I described previously. On top of that, other regions in the stability diagram are worth seeing. I will present two of them.

The first area which surprised me is highlighted by the white dashed square in the figure 4.6 and showed in the following figure 4.8. The reader shall recognize the honeycomb pattern introduced in chapter 2, figure 2.8, panel b). These features, typical signature of a clean double dots system, were unexpectable in this three dots device. Moreover the periodicity of the honeycomb is very close to the one of the square lattice in the figure 4.6 out of the antidiagonal. This indicates that the two outer dots are responsible for this pattern. Indeed, in this area, these two dots interact together thanks to the central dot *but* without the central dot disturbing the double dot system. Moreover, as wee can see in the inset of the figure 4.8 which is a close up of a pair of triple points, the dots interact in the strong coupling regime, the bias triangles being not straight anymore but rather having a crescent shape.

One specificity of this area is the close distance between the two antidiagonals. We think that this fact is responsible for what we see here. Having the two antidiagonals close to each other means that the two electrochemical potentials related to the state N_c and N_c+1 are also close to each other in energy. Then it becomes possible to imagine a kind of hybridation of these two states. The extra electron would be delocalized over both electronic wavefunctions of the outer dots acting as a covalent bound electron. Another way to understand what is going on would be to consider both electronic wavefunctions overlapping on the central dot, allowing a strong coupling between the two outer dots.

Last but not least, in that situation, the cotunneling is very strong compared to the one when we look at out of the antidiagonal in the figure 4.6. Having the central dot in this *hybridized state* allows the electrons to cotunnel the dots with a higher probability than the uncoupled situation. This whole analysis suggests that the two electronic wavefunctions are spread out of the dots, overlapping on the central dot.

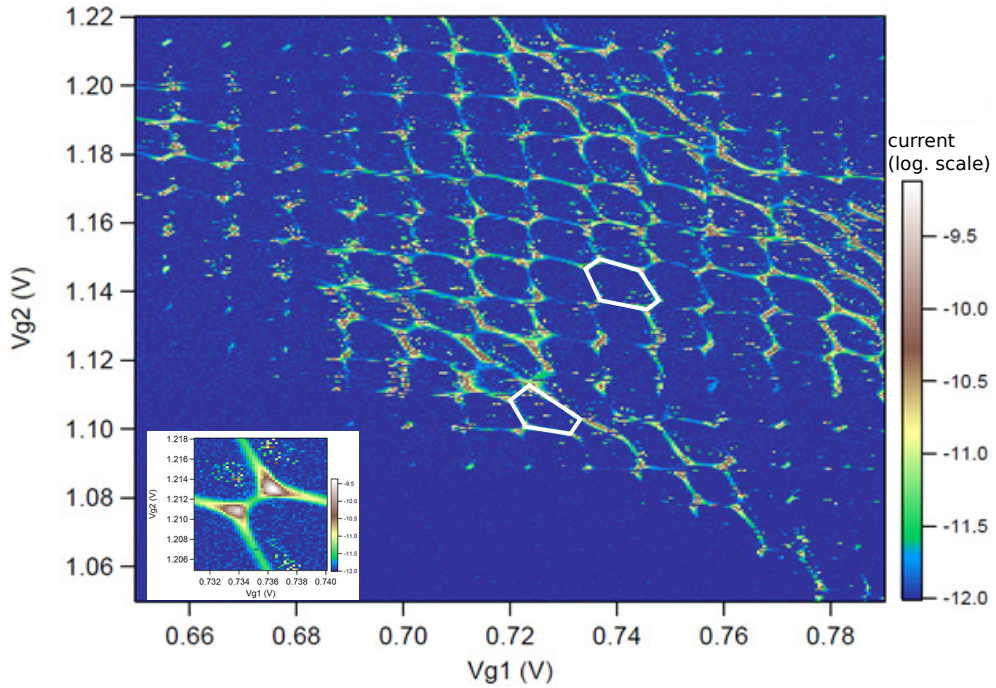


Figure 4.8 *Zoom in the white dashed square of the figure 4.6. We recognize the honeycomb pattern, typical stability diagram of a double dots system. It appears where the two antidiagonals tend to get closer to each other. Along the dot leads transitions, the honeycomb has the same periodicity than the square lattice in the figure 4.6. We get here the two outer dots, interacting through the central dot, behaving like a single double dot system ! Highlighted in white are the typical hexagons of a double dots system and pentagons of triple dots sysyem. The inset is a close up of two triple points. The two bias triangles are not straight anymore but rather tend to a crescent shape. This is a signature of two dots interacting in the strong coupling regime. Taken at 60 mK for a bias of 500 µV and a backgate voltage of +30 V.*

This situation may or may not be relevant for future prospects in quantum computing. However it allows us to understand a bit more the role of the central dot and how its state impacts the overall electric transport of the system. Finally, the peculiar nature of this central dot and its voltage dependant coupling can be another powerful experimental tool. I shall note that having two topgates for three dots is not an ideal case. We lack of degrees of freedom. Since this was the first device I ever probed, the set of masks was not thought to design a specific metal line lying on top of the device at that time. In the future, It could be interesting to study such a short spacers two serial topgates small device with the metal line and hope to independently control the state of the central dot and thus explore a bigger stability diagram.

The last region: a canonic stability diagram and excited states

The previously explored regions were complicated stability diagrams with many electrons involved in the three dots. To further study this device we lastly decided to go to a region where only one outer dot (the dot 2, controlled by the gate 2, vertical axis of the figure 4.6) is in the many electrons regime while the two other dots (dot 1, controlled by the gate 1, horizontal axis of the figure 4.6) and the central dot carry 0 or 1 electron. This is illustrated in the left panel of the following figure 4.9. As one can see, the voltage of the topgate 1 is nearly close to zero ensuring a very low number of carriers in the dot 1. We also focus on the N_c= 0 to N_c=1 transition of the central dot population. This transition is seen in the diagram as a break in the almost vertical line of triangles (along V_{g2}). The right panel of the figure 4.9 shows the same area but with a different color scale, allowing us to better see the different features. However, even by choosing an easier region than before, it is still quite difficult to index this stability diagram so here is an attempt inspired by Schröer's article [46]. Recently, another team has indexed a portion of a triple quantum dot stability diagram in the few electrons regime, see [93].

This region was recorded at base temperature, with a backgate voltage of +30 V and a bias voltage of +1.35 mV. This relatively high bias voltage applied here induces big bias triangles as one can see on the figure 4.9. If the reader looks closer to these triangles he will then see lines parallel to the base of the triangles indicating excited states. The top left panel of the figure 4.10 gives a close-up onto such one pair of bias triangles for a higher bias voltage of +2.25 mV. The top right panel gives another similar pair of triangles but for a very positive topgate 1 voltage, meaning many electrons carried by the dot 1. In this latter pair we do not see the excited states anymore. This strongly suggests that these excited states eventually come out of the dot 1. The bottom panel of the figure 4.10 gives a possible explanation of this spectroscopy.

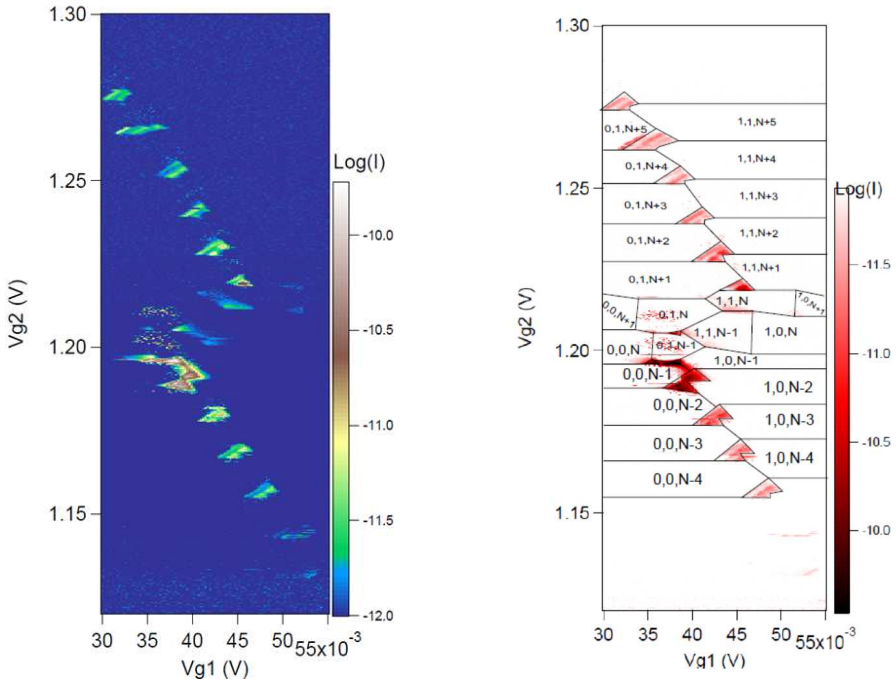


Figure 4.9 *Left panel: A stability diagram recorded in log scale at base temperature in the configuration where only the outer dot 2 carries many electrons. The backgate voltge is +30 V and the bias voltage is +1.35 mV. In this region the topgate 1 voltage is close to 0 V ensuring the dot 1 to carry a low numbers of electrons. Moreover the break in the line of triangles indicates a change of the number of electrons of the central dot. Finally the big bias voltage eventually opens big bias triangles. Right panel: Same area but with a different color scale. We make here an attempt to index the stability diagram. Inside the bias triangles wee also see lines parallel to the base of the triangles indicatind excited states.*

4.4 Conclusion and outlook

Through this section I presented different ways to manipulate the coupling betweeen two electrostatically defined quantum dots. The two first ones were related to accessible degrees of freedom of the system such as the backgate or the metal line. While the backgate is naturally present, the metal line requires a specific mask to design this line from the copper plan (which is always designed) laying on top of the device and the metallic connections from the metal line towards the uppermost layer containing the contact pads. However the latter is more suitable for reflectometry measurements because of charge reconfigurations in the undoped silicon backgate which change the overall capacitance of the system.
Finally, I presented a specific device made of two electrostatically defined quantum dots and one central dot in between. The intrinsic nature of this central dot, made of a small number of dopants, was quite unexpected and allows for a tunable coupling between the two outer dots.

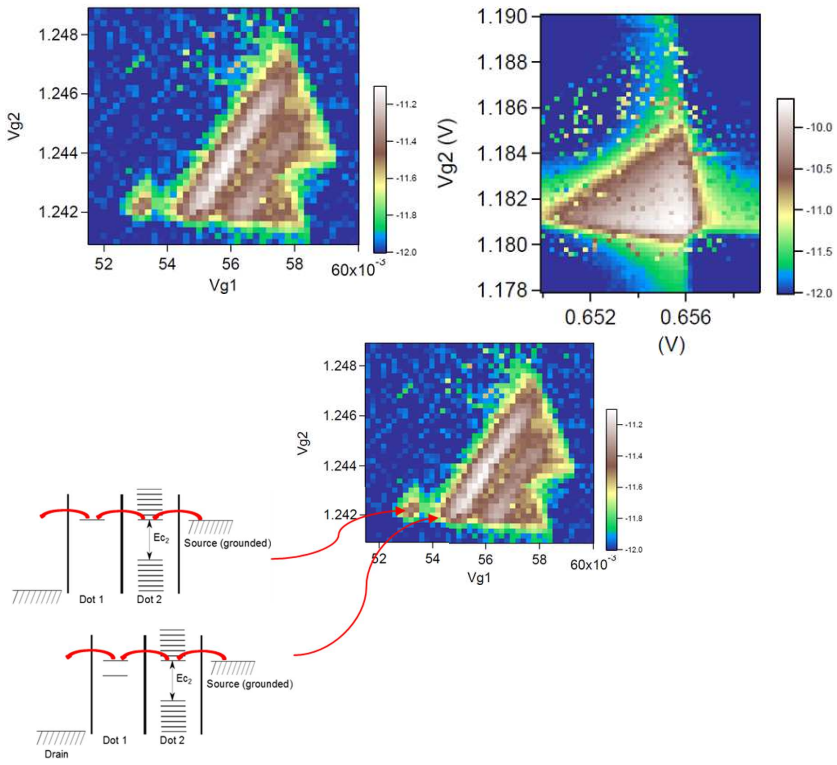


Figure 4.10 *Top panel: two pairs of bias triangles taken for a bias voltage of 2.25 mV for two different values of V_{g1}. The left one was measured in the same region as in the last figure 4.9 while the right one for a way higher value of V_{g1} and thus for a large number of electrons in the dot 1. In the latter, we do not see the excited states anymore indicating that these states seen previously belong to the dot 1. Bottom panel: schematic of the electronic transport through the states of the system. The ground state of the dot 1 is responsible for the baseline of the bias triangles while the first excited state gives rise to the first line inside the bias trangles. The other lines appaear thanks to other excited states in the same manner.*

Moreover, we discovered interesting regions in the stability diagram of that device. First, a beautiful honeycomb pattern attributed to the two outer dots in a strong coupling regime. It perfectly shows how the state of the central dot can change completely the dynamic of the overall system. Second, we tried to index the stability diagram in a simpler area and eventually find excited states in the bias triangles. These states appear to belong to the dot 1. Whatever the impact this system could have on the community of solid state quantum computing, it has interesting properties and versatile behavior.
As always, a serie of measurements brings new questions to mind: what are the first charges transitions in the stability diagram ? Is the transport of spins through the central dot coherent ? I shall remenber that in that chapter, I have never talked about reflectometry and spins because of the limited electronic setup of the fridge which, at that time, did not allow us to probe the system through RF-reflectometry. However I guess it would be very nice to use the reflectometry technic on that kind of device in order to probe transition lines which do not lead to any current through the device, for instance. Finally, we never turned on the magnetic field, again limited at 2 Teslas at that time. We considered the system already to complex just by dealing with the charges. It is clear that a magnetic field dependent experiment probed with a reflectometry setup would give us more informations about that specific questions.

Chapter 5

Dynamical experiments towards energy selective spin readout

"At the heart of quantum mechanics is a rule that sometimes governs politicians or CEOs - as long as no one is watching, anything goes."

-Lawrence M. Krauss, 2012

Résumé

Ce deuxième et dernier chapitre expérimental concerne la mise en place de la lecture de spin par sélectivité en énergie sur un dispositif double boîtes dopé P, en géométrie parallèle.

La première section discute des motivations derrière une telle expérience. Je présente les principales réalisations expérimentales fondatrices qui ont eu lieu lors de ces 20 dernières années. En particulier, grâce à la possibilité de 'mesure unique' offerte par cette lecture de spin et à la potentielle intégrabilité à grande échelle de la réflectométrie radio-fréquence sur grille, cette expérience est cruciale pour la suite de la recherche sur les boîtes quantiques à base de nanofils silicium MOSFET.

La deuxième section concerne les nécessités pratiques de l'expérience. *In fine*, nous avons besoin d'une ligne DC, d'une ligne radio-fréquence et d'une ligne dédiée aux impulsions électriques (dont la caractérisation est présentée dans le chapitre 3) *pour chaque grille*.

La prochaine section présente les mesures statiques, préliminaires, comme les diagrammes de stabilité enregistrés en courant et par réflectométrie, autorisant une comparaison directe

entre les deux méthodes. De plus, des diamants de Coulomb seront extraits.
La fin de cette section présente les premières mesures où l'on utilise les lignes d'impulsions électriques. Ces mesures consistent en des enregistrements de diagrammes de stabilité lors desquels nous envoyons des impulsions sur l'une des deux grilles et nous lisons la réflectométrie associée à l'autre grille. Ces mesures préliminaires ont été réalisé avec et sans champ magnétique. Bien qu'il fut compliqué de conclure avec certitude sur ces mesures, il semble clair que, même lors de ces mesures préliminaires, il se passe quelque chose sous champ magnétique.

La dernière section introduit à proprement parlé la lecture de spin par sélectivité en énergie et, plus précisément, la séquence d'impulsions électriques nécessaire utilisée, la séquence *Charger-Lire-Vider-Attendre*, constituée de quatre signaux carrés mis à la suite.
J'expose également le problème de la calibration. En effet, l'expérimentateur doit être certain d'envoyer la tension souhaitée pendant la durée souhaitée sur la grille du dispositif.
Enfin, je présente les résultats expérimentaux. L'expérience marche parfaitement bien sans champ magnétique. On obtient absolument ce à quoi l'on s'attendait. En revanche, les conclusions deviennent beaucoup plus difficiles à extraire dans le cas d'un champ magnétique non nul. Pour la plupart des points triples étudiés, il ne se passe rien. Pour certains, d'entre eux, il se passe bel et bien quelque chose dans cette situation mais, pour le moment, il est impossible de conclure sur un véritable signal de spin. Cependant, nous avons le sentiment qu'il est possible de repérer quels sont les points triples intéressants en regardant l'aspect des points triples dans un diagramme de stabilité enregistré à champ magnétique fini.

5.1 Motivation

In 2004 J.M. Elzerman and coworkers in the Kouwenhoven team experimentally demonstrated for the first time a novel single-shot spin readout technique in the well-known paper [41]. They used a specific pulse sequence to implement a spin-to-charge conversion mechanism based on energy selectivity. This proof of concept was implemented in a GaAs heterostructure and probed by a QPC[1], the detector. They eventually extracted the relaxation time T_1 of an electron and estimated the fidelity of their readout scheme.

In 2010 A. S. Dzurak, A. Morello and coworkers reproduced this experiment in a silicon 2DEG and extracted the relaxation time of an electron and its dependancy with the magnetic field, the visibility and the fidelidy of their readout setup. These results were recorded with a SET and are presented in the paper [39].

[1] Quantum Point Contact.

In 2017 G. Katsaros and his team used this pulse scheme to extract the tunneling times of holes in germanium hut wires. This was probed by Lead-coupled radiofrequency reflectometry and presented in the paper [40]. They eventually realized the single shot readout of holes in the same kind of system, extracted the relaxation time and its magnetic field dependancy. This is presented in [94].

Being a proof of concept, the first experiment is not easy to scale up. The second experiment consists of an island of phosphorus donors probed by a SET. This is hardly to scale up as well. While using Lead-coupled radiofrequency reflectometry, the germanium hut wires used in the two last experiments are not seen to be scalable neither.

During this PhD, I proposed to implement this time-triggered pulse scheme on a LETI device and perform Gate-coupled radiofrequency reflectometry to record the signal. This would be the most scalable *hardware+readout* scheme in the semiconductors quantum dots litterature.
In order to realize that experiment, we need a clean device with an experimental possibility of tuning the overall tunnel rates. We decided to focus on a P-type double gate face-to-face device. This geometry has been presented in the chapter 3, figure 3.14. We have also performed some characterizations of the metal line of this device in the last chapter 4 (see figures 4.3 and 4.4). Taken from the last batch I received, T18S0063 (MOSQUITO II), this metal line allows us to tune the coupling between the two dots and the tunnel barriers between the dots and the leads.

5.2 Practical requirements for such experiment

We want to experimentaly realize the readout of a hole spin belonging to one dot thanks to the other dot with an energy selective spin readout. First, the two dots have to be capacitively coupled, one dot has to "see" the charge transitions of the other.

Second, one dot must be in a many holes regime, thus a metallic dot with regularly spaced transitions while the other one must carry a very few number of holes in order to populate quantum levels and more specifically spin levels. The metallic dot will be called *the detector* while the few holes dot will be called *the quantum dot* of interest. This second prerequisite will set the working point areas, meaning the regions in the stability diagram we are going to exploit.
Third, the lead barriers have to be asymetric: one dot, the detector, in the many carriers regime should be able to exchange quickly with the leads while the other one, the quantum dot of interest in the few carriers regime must be well isolated from the other leads (the

tunnel rate of these barriers should be lower than the inverse of the relaxation time of the spin excited state). The unique experimental solution we have to achieve these prerequisites is the metal line. We will put V_M= +20 V to limit the tunnel coupling between the two dots and to reduce the tunnel rates of both lead barriers.

To sum up a bit what we practically need: we want a metallic dot, the detector, to be capacitively coupled with a few holes quantum dot. This detector has to be well coupled to its lead while the other quantum dot has to be more isolated from the leads. In a stability diagram, we will only focus on transition lines which are broken due to sensing of the charging/discharging of another quantum object, without any visible interdot.
The following picture 5.1 taken from [39] illustrates the measurement scheme which I will explain now.

Since we are dealing with spin states, we need a permanent magnetic field to split appart the two spin states. The basic principle of the experiment is the following and is presented in the figure 5.1: we will quickly pulse onto the quantum object's gate in order to shift its electrochemical potentials. The pulse sequence is a succession of three square pulses, the Load, the Read and the Empty pulse. The Load stage allows one to load a carrier with an unknown spin state in the few carriers quantum dot. The Read stage is the core of this readout scheme: depending on the spin state of the loaded carrier, tunnel transfer between the quantum dot and the prober is allowed if the spin is in the up state or forbidden if the spin is in the down state. As a consequence, current will flow (during a typical time of the order of the inverse of the tunnel rates of the prober) in the first scenario while there will be no current in the second scenario. This allows one to discriminate two spin states thanks to a charge state configuration of the double quantum dots. The last stage is the Empty stage where one empties the few carriers quantum dot in order to process another three stage sequence.

Instead of using current based measurements, we will probe the system with gate-based radiofrequency reflectometry on both gates. The setup used for the experiment is described in the last section of chapter 3. The UHF demodulator will send both RF tones and read the incoming signal by homodyne detection thanks to its pair of RF channels. Moreover we need to pulse on top of one of the two gates while recording phase signal through the other channel. The most recent UHF in the laboratory has an AWG function (stanting for *Arbitrary Waveform Generator*), a digital instrument which generates waveforms for pulse experiments. Eventually, the UHF will be responsible both for the readout with reflectometry and the pulse sequence. However, having only two RF channels means that during the experiment, one

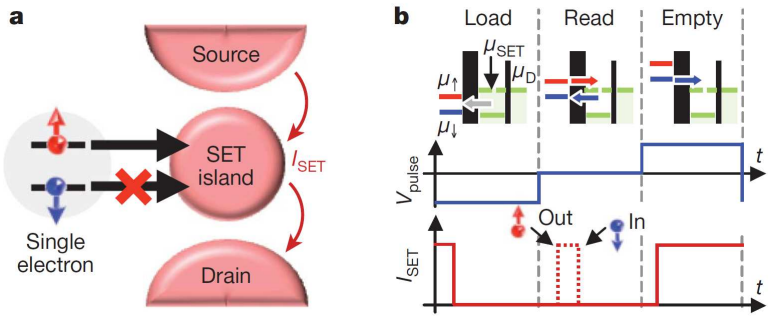


Figure 5.1 *Energy selective spin readout scheme. a: schematic of the quantum system. Two parallel dots coupled together. The left one, very weakly coupled to the leads, is in the few carriers regime and is the quantum object of interest while the right one, strongly coupled to the leads, is in the many carriers regime and is the prober. b: principle of the experiment. We will pulse on the left dot. The pulse sequence is a succession of three stages, the Load, the Read and the Empty stage. During the read stage, depending on the spin state of the carrier, the tunneling between the two dots is allowed if the spin is up or forbidden if the spin is down. In the first case current is probed (for a time of the order of the inverse of the tunnel rates between the dots) through the right quantum dot whereas no current flow in the second case. Extracted from [39].*

channel is used for the readout on one gate while the other channel is used for pulsing onto the other gate.

5.3 Preliminary results

This section will be a presentation of basic measurements such that stability diagrams and Coulomb Diamonds in order to extract characteristics of the quantum dots. Then I will give interesting results we obtained by recording a phase stability diagram while continuously pulsing on top of one gate. This experiment will give us first insights on quantum dots dynamical behaviors before the time-trigerred acquisition measurement, namely the Morello's experiment.

I shall remind the reader that this device comes from the last batch I received, namely *MOSQUITO II*. It is a P-type double gate in face-to-face configuration and has been presented in chapter 3 (figure 3.14). I also characterized the impact of the Metal line on that device in chapter 4 (figures 4.3, for example).

5.3.1 Stability diagrams

The characterizations of both gates at 300 K are presented in chapter 3 in the figure 3.13. The next step is to extract the stability diagram of that P-type face-to-face device at dilution temperature. The experimental setup allows for both a DC current and RF reflectometry measurements, simultaneously. The former is presented in the figure 5.2 and the latter in the figures 5.4 and 5.5, for both reflectometry channels, one for each gate. The figures 5.3a and 5.3b shows 1D Id-Vg curves for Vg_1 and Vg_2, respectively, extracted from 5.2. These measurements were performed at 60 mK with a source-drain DC bias sets to half a millivolt and a metal line biased with + 14V.

From the current measurement, which is plotted in logarithm scale as a function of both DC gate voltages, we can say that the two dots are strongly capacitively coupled to their own gate and weakly coupled to the other gate. The bench of transition lines are almost straight vertical for the dot 1 (with a slope of about -11) and a quite horizontal for the dot 2 (with a slope of about -0.050). On top of that, we can say that the two dots are similar. Indeed, the periodicity of the lines is around 12 mV for the dot 2 and around 9 mV for the dot 2. These periods are directly related to the charging energy of the dots through the proportionnal coefficient α, the lever-arm parameter. The difference between the two periodicity may be explain by a slight difference in charging energy and/or a slight difference in the lever-arm parameter. Practically, this is due to a slight difference of size and/or a slight difference in electrostatic control of the dot by its control gate.

This DC current stability diagram can be split into four quadrants, delimited here with green lines. The first, top right quadrant shows no charge transitions. In this region, both dots are empty or populated with very few holes[2]. In the top left (second) and its symmetric bottom right (third) quadrants, one dot is populated with many holes while the other one carries a few number of holes. These two regions will be the frame of work for the next experiences, including continuous pulsings and time-triggered sequences. Let's talk finally about the last region, the bottom left (fourth) quadrant, which is the many holes regime where both dots carried a lot of holes (hundreds of them) and, thus, are considered as metallic dots. The dashed blue square portion is highlighted with the inset in the figure 5.2. It exhibits a very regular pattern [3], signature of a regular parallel double dot system . On top of that, the reader can also distinguish a pattern of antiparallels lines overlying the regular double dot

[2]The number of circulating holes is too small to be measured with the current setup.

[3]Except maybe the central region where another quantum object seems to interact with the double dot system.

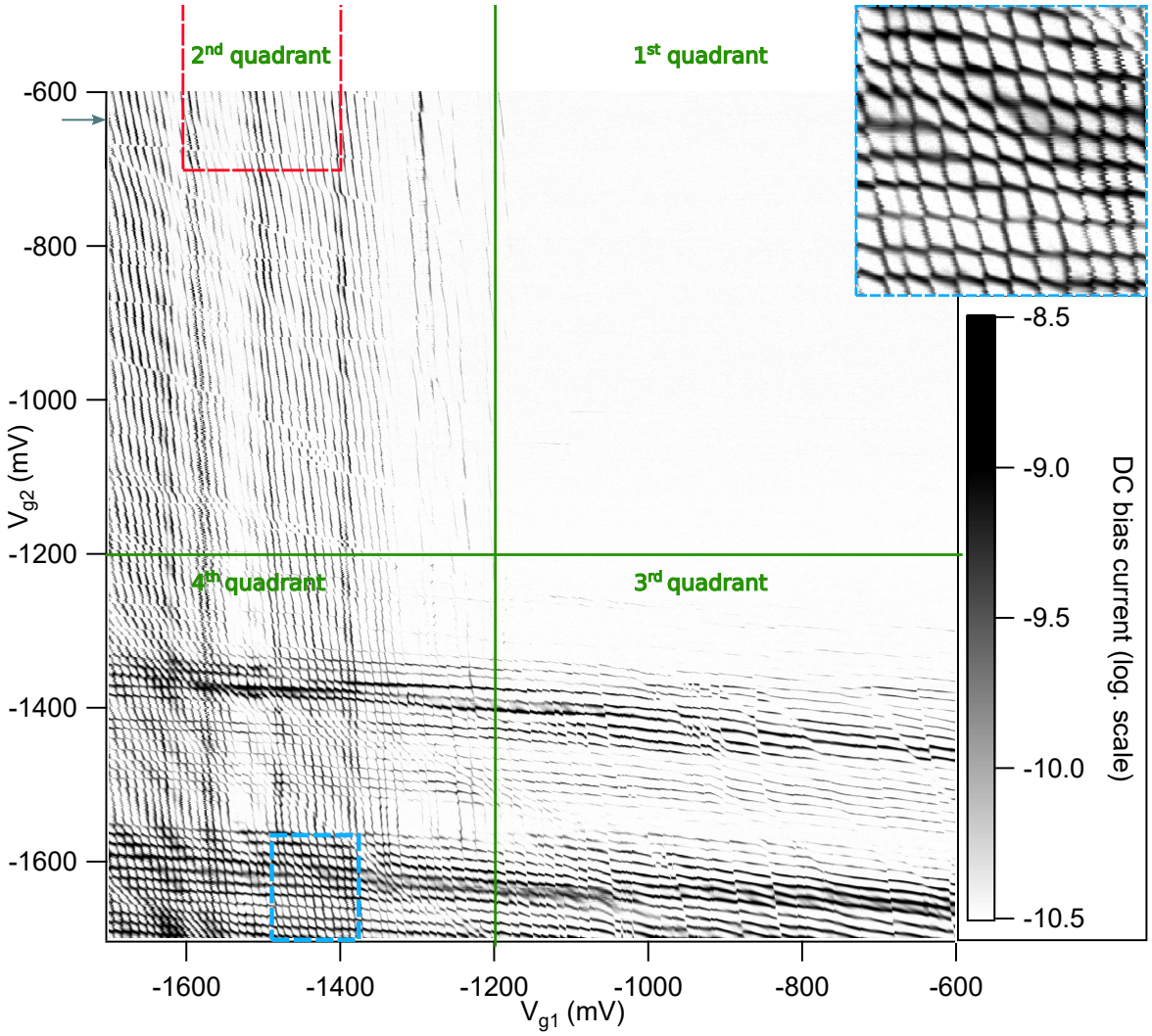
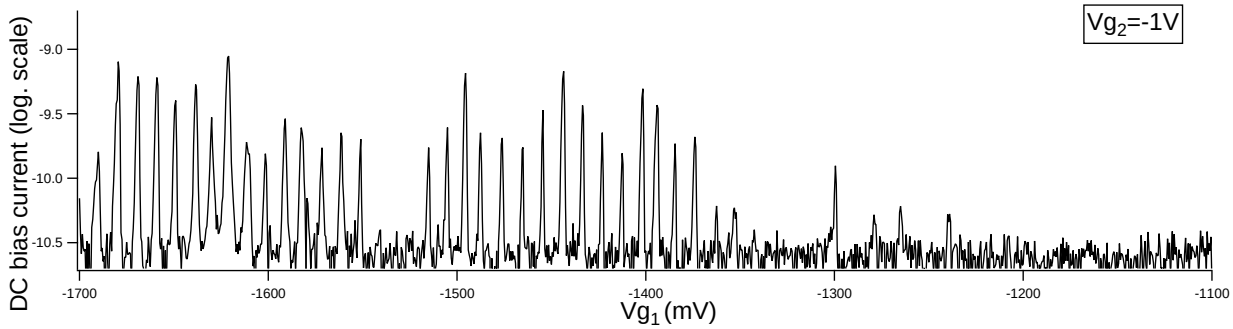
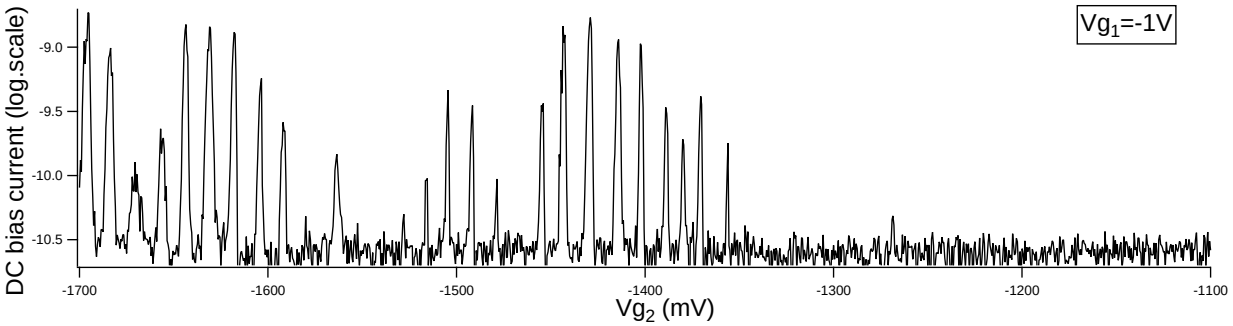


Figure 5.2 *Stability diagram taken at T=60 mK with a 0.5 mV source-drain bias voltage and the metal line is biased at +14 V. Log. scale DC bias current as a function of both topgate voltages. White regions are related to lower current while dark regions to higher current. First, we see two kinds of lines: the quite horizontal lines, with the same negative slope of -0.05 indicating charge transitions occuring in the dot 2 and the quite vertical lines, with a slope of -11 showing charge transitions occuring in the dot 1. The green lines split the diagram into four quatrants. The first quadrant corresponds to the few holes regime for both dots. The second and third quadrants delimit the two regions where one dot carries a few number of holes while the other one is in the metallic limit, carrying many holes (dozens). Lastly, the fourth quadrant corresponds to the case where both dots are in the metallic regime, thus both carrying many holes. In that region, the dashed blue square is highlighted in the inset and shows a regular pattern, characteristic of a many holes, parallel double dot system. At the top of the second quadrant I highlight a red area. This region will be our frame of work in the continuous pulsing results section, namely the figure 5.8. Note that this situation corresponds to a metallic quantum dot 1 and a dot 2 carrying a very few number of holes. Finally, the blue arrow points at the Vg_2=-630 mV line. We will record Coulomb diamonds related to the dot 1 on the line later one this section. There are presented in the figures 5.6a and 5.6b.*



(a) *Horizontal cut along Vg_2=-1V taken from the last figure 5.2. The first Coulomb peaks appear around Vg_1=-1250 mV. At somme point the Coulomb peaks exibit a quite regular period of about 10 mV.*



(b) *Vertical cut along Vg_1=-1V taken from the last figure 5.2. The first Coulomb peak appears around Vg_2=-1280 mV. At somme point the Coulomb peaks exibit a quite regular period of about 13 mV.*

Figure 5.3 *Field effect characterizations of both gate 1 (top panel) and gate 2 (bottom panel) at T=60 mK. The bias voltage is V_{dc} =0.5 mV and the metal line is biased at +14V. Extracted from 5.2.*

pattern. With its almost -1 slope, we can attribute these lines to a central object equivalently coupled to both gates. However, this is not true anymore when one goes to the few holes regime for the dot 2 when these lines tend to be more and more horizontal. This trend says that this third object is mostly coupled to the gate 1 when dot 2 is empty and becomes more and more equivalently coupled to both gates while being filled with holes. We can attribute this behavior to a small, parasitic dot whose shape becomes bigger and bigger *and* tends to be more and more central in the nanowire as its number of carried holes increases.

The highlighted red square in the second quadrant will be our area of interest in the continous pulsing result section and is presented in the figure 5.8. It is located far in the depletion regime of dot 2.
The blue arrow points along the Vg_2=-630 mV line. It indicates the line where Coulomb diamonds of the dot 1 were recorded. They are presented in both figures 5.6b and 5.6a.

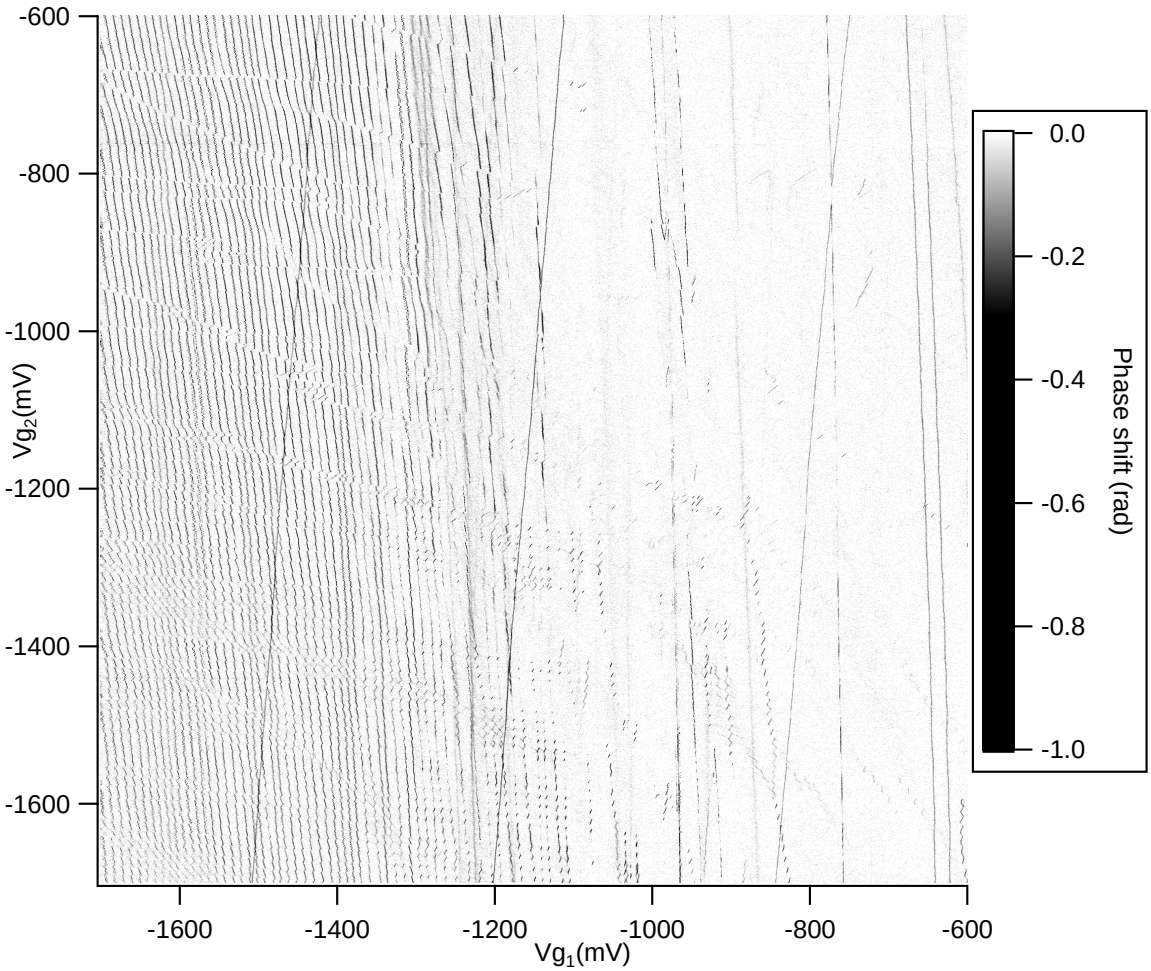


Figure 5.4 *Reflected phase signal stability diagram of the channel 1 recorded at T=60 mK, VMLine=+14 V. We first notice that the reflectometry is strongly selective, the channel 1 being only sensitive to charges transitions occuring in the dot 1, namely the vertical lines. we recognize these lines that we already saw in the previous DC current stability diagram, regularly spaced on the left side. We also discover new lines that we can organize in two families. The first lines appear on the right side and get the same slope than the ones already discussed. These are in fact the first charge transition lines occuring in dot 1, in the few carrier regime. The other ones are lines with a positive slope. We can see 3 of them, regularly spaced. The positive slope indicates that the quantum object responsible for these charge transitions is not in the channel. It is probably a dopant in the residual polysilicon laying ouside the device or a charge trap in the gate stack.*

Now let's talk about the two other stability diagrams which were recorded through reflectometry setups. The figure 5.4 shows the result for the gate 1 setup and the other figure 5.5 for the gate 2 setup. Before going further in the analysis, I have to mention that the gate-based radiofrequency reflectometry is very selective. Even though the two topgates and the two

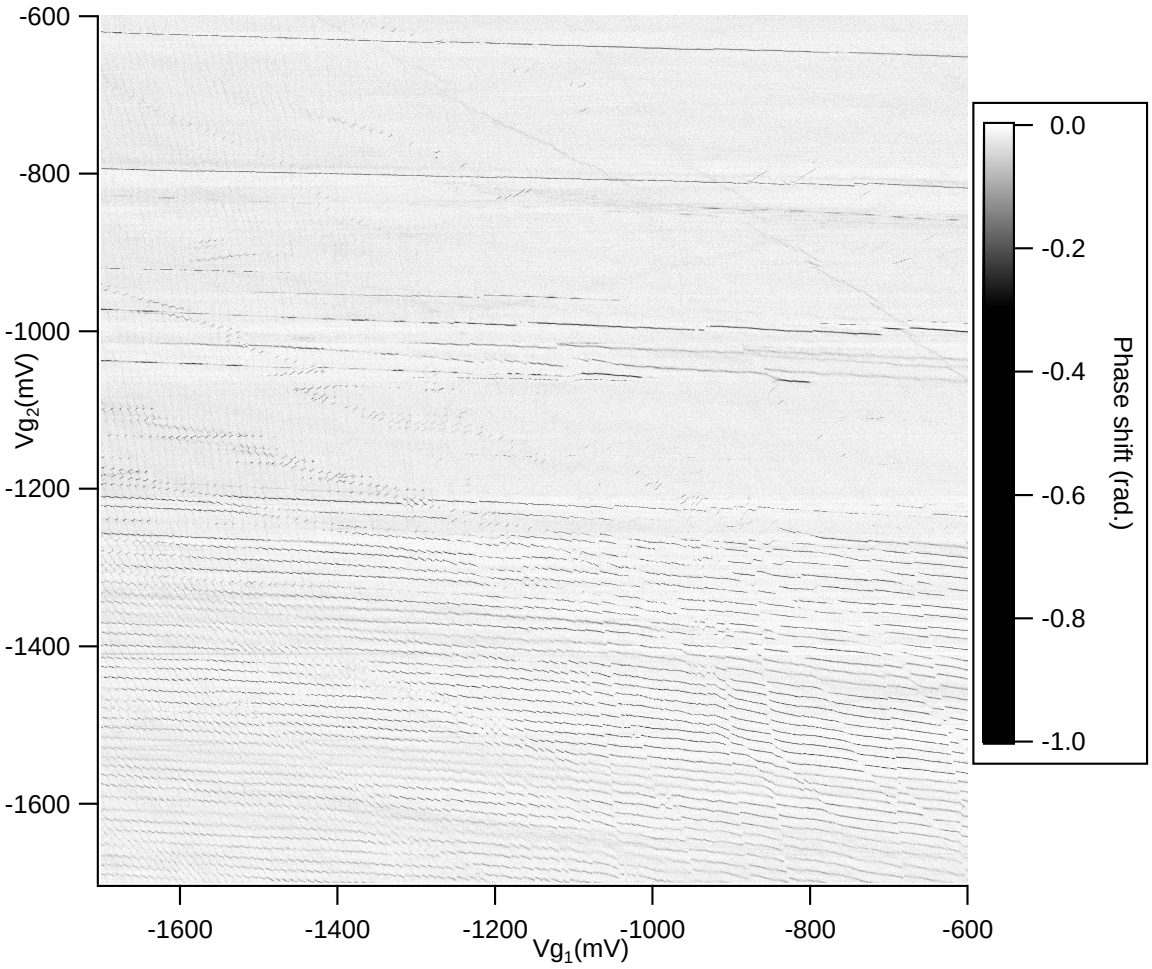


Figure 5.5 *Reflected phase signal stability diagram of the channel 2 recorded at T=60 mK, VMLine=+14 V. Again, We notice that the reflectometry is strongly selective, the channel 2 being only sensitive to charges transitions occuring in the dot 2, the horizontal lines. we recognize these lines that we already saw in the previous DC current stability diagram, regularly spaced on the bottom side. We also discover new lines that we can organize in two families. The first lines appear on the top side and get the same slope than the ones already discussed. These are in fact the first charge transition lines occuring in dot 2, in the few carrier regime. The other ones are lines with a different negative slope.Only one of them is quite visible. The negative slope (-0.43) is very different from what we have got for the standard charge transition lines of the 2 quantum dots. The responsible quantum object is coupled to both gates. This extra quantum object is attributed to a dopant lying around the two quantum dots of interest and can interact with them.*

dots are spatially very close, the channel 1 plugged into the gate 1 is only sensitive to the vertical transitions, that is the transition occuring in the dot 1. The same logic applies for channel 2 and the dot 2.

At first sight, we can already say that we see the same bench of transition lines in these stability diagrams than in the DC current stalibity diagram. As said earlier about the DC current stability diagram, these transition lines exhibit a regular periodicity, signature of so-called metallic dots. Due to the many carrier carried by each dot, the different quantum levels tend to be stacked together and form bands separated by an energy gap equal to the charging energy of the dot.[4]. Interestingly and for both gates, the regularly spaced charge transitions appear at the same voltage than the first visible transition lines in the DC current stability diagram, that is about -1200 mV.

We can also see more lines with the reflectometry setup. In particular we can access transition lines earlier in the stability (at lower gate voltage, for both gates). These transitions lines exhibit the same slope than the ones seen in the DC current stability diagram, meaning that they are related to the same objects, namely the two electrostatically defined quantum dots. However, the previously highlighted periodicities do not stand anymore. These "new lines" show up in the first, top right, quadrant. This regime is the so-called few carrier regime where the probed quantum dot levels are directly single (or spin degenerated) discrete quantum states. The energy separating two successive transition lines is the sum of the dot charging energy ang the energy difference between two successive quantum states.

I should mention that we also see tilted lines in figure 5.5, especially visible in the top half of the diagram. They have a slope of about -0.43 mV/mV. They could be attributed to dopants lying around the two quantum dots showing that the device is not a perfect, clean device.

On top of the negative slopes transition lines, we also distinguish three equally spaced, positive slope transition lines in the figure 5.4. These charge transitions are related to charging and decharging quantum objects which do not lie in the nanowire. Typically, this object may be a charged trap or a dopant in the gate stack or in the polysilicon layer being out of the nanowire. Because the lines are quite vertical and do not appear in the channel 2 stability diagram, we can conclude that this extra quantum object is very close to the gate 1.

To sum up this data analysis, we see more lines in the reflectometry stability diagrams, including usual negative slopes charge transition lines related to the quantum dots which were not visible in the current stability diagram and positive slope transition lines related to

[4]The same phenomenum occurs in solids where the immense number of carriers involved leads to energy bands separated with gaps.

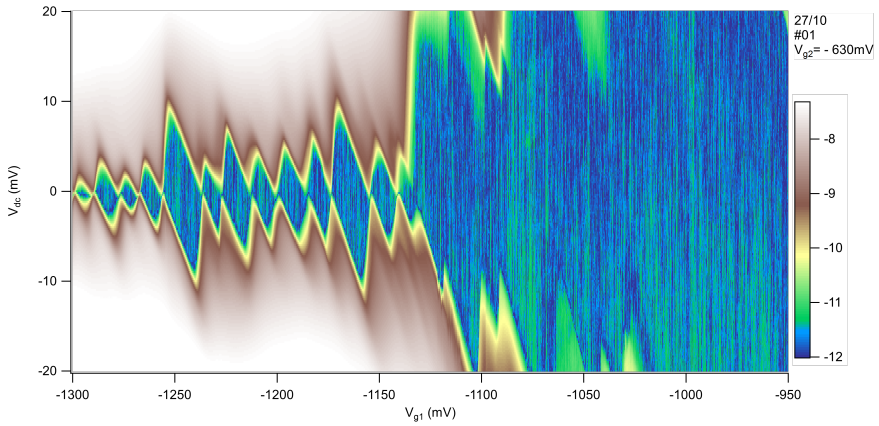
other quantum objects which are located outside the nanowire. The most important point which is being able to catch charge transition lines in the few holes regime will be of prime importance in the next series of experiments. The only drawback though is the fact that the complete stability diagram is the combination of two partial stability diagrams, one for each gate through two reflectometry channels, the reflectometry being very spacially selective.
Lastly, I shall add a comment to this analysis. The gate-based radiofrequency reflectometry is strongly dependant to the tunnel rates between the leads and the dots. For instance, in a case where the spacers are too short or the channel width is too big, equivalently when the current is too high, we would not be able to see the charge transision lines in the many carriers regime anymore. This is not true for lead-based radiofrequency reflectometry. Remarkably in that experiment, the DC current and the reflected phase signal never saturate. This stands for the low carriers regime as well as the many carriers regime and over a very wide range of gate voltage.

5.3.2 Coulomb diamonds

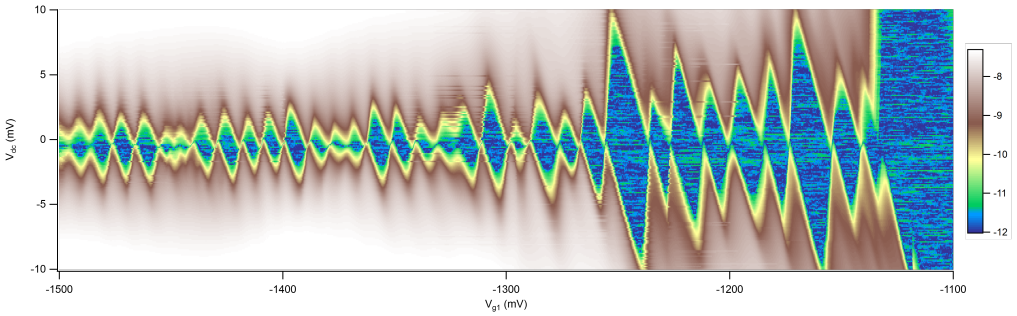
Another fundamental measurement is the extraction of Coulomb diamonds, telling a lot about the charging energy and the lever-arm parameter of a quantum dot. The two next figures 5.6a and 5.6b shows such diamonds for dot 1 charge transition lines since we are cutting along an horizontal where Vg_2 is set at -630 mV. The log. scale DC current is plotted as a function of Vg_1 and V_{dc}. The more we go to the right side, the less holes the dot carries until it is almost empty, the very right area of the figure 5.6a, and the half right of figure 5.6b. The the diamonds get bigger, hence, showing a higher charging energy.

When we go leftward, from Vg_1=-1250 mV we can say that we got a quite regular serie of diamonds, related to a metallic dot, except for three areas: around Vg_1=-1450 mV, Vg_1=-1380 mV and Vg_1=-1320 mV. These areas coincides with areas of channel 2 stability diagrams where tilted negative slope transition lines crosse the horizontal line sets at Vg_2=-630 mV. This means that these disturbances are due to the extra quantum object responsible for these tiltes lines (see chapter 5 of [29] for more informations).

The analysis of the diamonds leads to a very good knowledge of the figures of merit of quantum dot 1. As presented in the theoretical part, the half height of the diamonds gives the addition energy while the difference between two successive diamond peaks is related to the gate capacitance C_g of the dot. I will focus now on the many holes regime, meaning the area below Vg_1=-1300 mV, where the diamonds are more similar, apart from the three aforementionned areas disturbed by another quantum object. In average, I found an addition



(a) *Coulomb diamonds related to the dot 1 in the few holes regime taken along the Vg_2=-630 mV line. Going rightward, the height of the diamonds, hence the addition energy, gets bigger and bigger. This is a strong indication that effectively we are reaching the few hole regime. Unfortunately, the actual setup did not allow us to go beyond Vdc=20 mV. The many hole regime is presented in the other figure 5.6b.*



(b) *Coulomb diamonds related to the dot 1 in the many holes regime. This is the following of the last figure 5.6a when one goes leftward. Below Vg_1=-1300 mV, all the diamonds have pretty much the same shape, except for three areas: around Vg_1=-1450 mV, Vg_1=-1380 mV and Vg_1=-1320 mV. In these regions, the diamonds are altered. This is due to dopant transition lines crossing the horizontal line. These lines are barely visible on the large stability diagrams presented before but the first line crossing the Vg_2=-630 mV line can be seen on the next figure 5.7.*

Figure 5.6 *Coulomb diamonds related to the dot 1. From these measurements, one can extract the addition energy (in the many carriers regime, this is equivalent to the charging energy) which is extracted from the half height of the diamonds and the lever-arm parameter, being equal to the ratio width over half height, among others figures of merit. It is clear that these characteristics depend on the number of carriers carried by the dot. In the many holes regimes for instance, very left area in figure 5.6b, the charging energy is equal to about 2.4 meV and the lever-arm parameter is about 0.24 for all diamonds (except of course for three areas where the diamonds are perturbated) while in the other case, the few hole regime, these parameters vary from one diamond to another. As another example, the big diamond located at about Vg_1=-1250 mV has an addition energy of about 10 meV and its related lever-arm parameter is around 0.70.*

energy of 2.4 meV. This addition energy is equal to the charging energy in the metallic regime, therefore E_C=2.4 meV. We can now extract the total capacitance C_Σ=C_S+C_D+C_g=66 aF. From the difference between two consecutives Coulomb peaks which, in average, is equal to 10 mV, we can deduce C_g=16 aF. Therefore α, the lever-arm parameter, defined as the ratio $\frac{C_g}{C_\Sigma}$ is equal to 0.24.

Thanks to these static measurements, we got all we need to know about the quantum dots. In the next section, I am going to present what we call continuous pulsing experiments. Being practically less demanding than time-triggered acquisitions, it is easier to proceed and I will show that we can already highlight interesting (yet puzzling) behaviors.

5.3.3 Continuous pulsing

In this section, I am going to present all the experimental results that involve continuous pulsing, meaning without any time-triggered acquisition.

Initially, we should only realize time-triggered acquisition in the spirit of Morello's experiment. We then realized that a simpler study was also possible and might lead to interesting results too. Instead of a time-triggered acquisitions we decided to continuously pulse through one gate while recording the stability diagram with the other gate reflectometry channel. In order to satisfy Morello's experimental conditions, we must have one dot in the metallic regime probing the other dot carrying a very few carriers. On top of that, the tunnel rates between the two dots should not be to high. If so, we would not be able to follow high speed charge transitions. To do so we decided to focus on the second quadrant of the stability diagram where dot 1 is metallic and dot 2 carries a few number of holes. This region, highlighted by the dashed red square in the figure 5.2 is presented in the next figure 5.7. I shall mention that this figure shows the phase signal of reflectometry channel 1.

This region exhibits a regular pattern for the dot 1, confirming its metallic behavior and we clearly see 3 shifts, indicated by arrows: At Vg_1=-1600 mV, these shifts occur for Vg_2=-300 mV, Vg_2=-470 mV and Vg_2=-600 mV. From top to bottom, the slopes are -0.6, -0.32, -0.27. These values are one order of magnitude bigger than the extracted slope of the transition lines of dot 2 in the metallic regime. This means that in this region, the dot 1 is sensitive to charge transitions which do not occur in dot 2 but rather in dopants. Indeed, we know from both stability diagrams recorded by reflectometry, figures 5.4 and 5.5, that the double dots system is not perfect in a sense that others quantum objects lie in the canal below the gates along with the two electrostatically defined quantum dots. Most of the cases, these

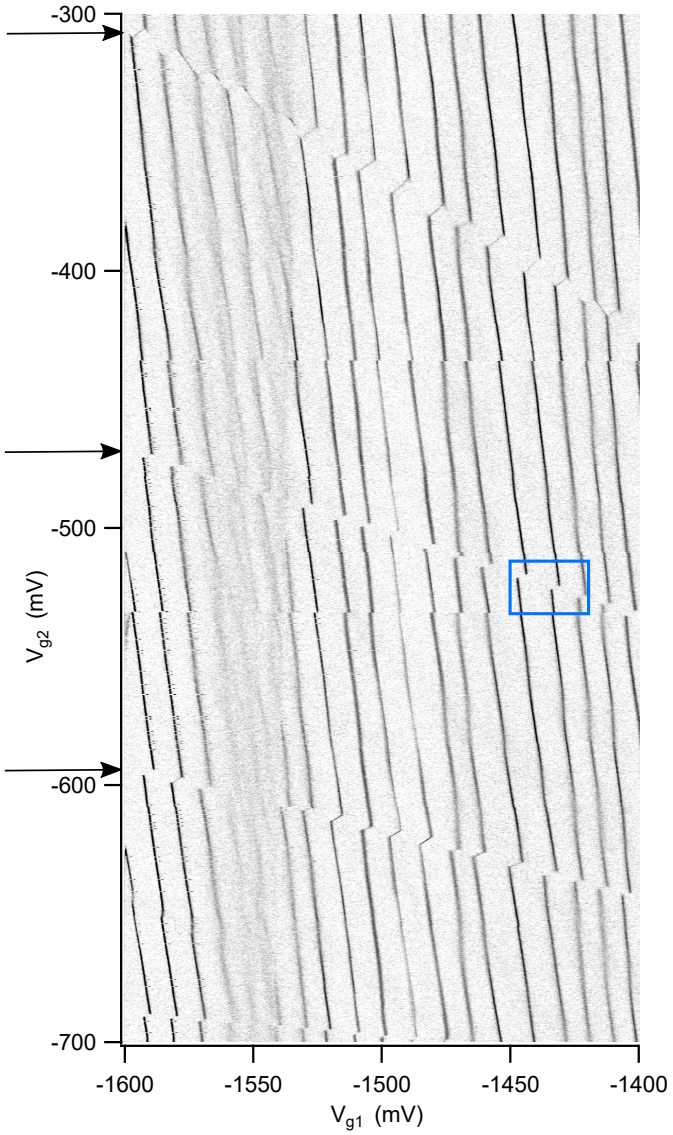


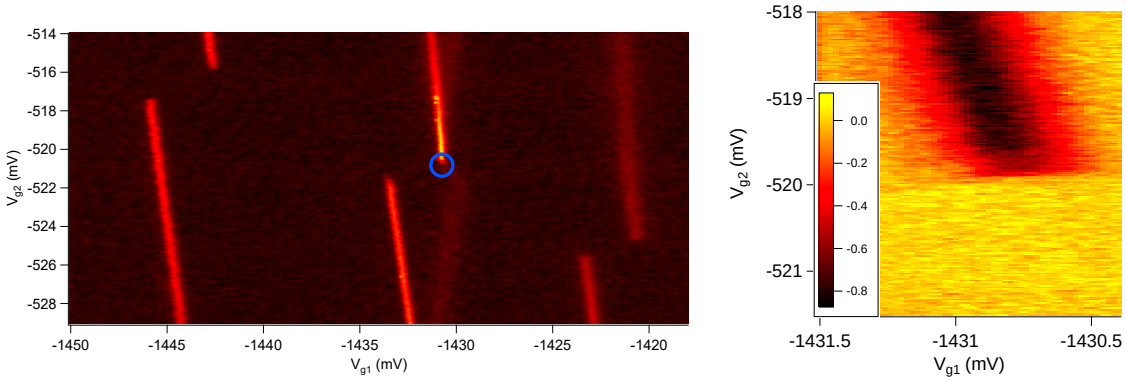
Figure 5.7 *Zoom in the dashed red area of figure 5.2. The phase of reflectometry channel 1 is plotted as a function of both topgate voltages with no source-drain bias and a Metal line sets at +20V. The vertical charge transition lines of dot 1 are regularly spaced showing that dot 1 is in the metallic regime. On top of that, we clearly see three shifts in that regular pattern pointed by arrows. From top to bottom, the slopes are -0.6, -0.32 and -0.27, far from the original -0.05 extracted for the dot 2 charge transition lines. Instead these 3 lines probably emerged from dopant charge transitions. Finally, the blue square highlights the next zoom, presented in the figure 5.8*

parasitic quantum dots are dopants. In the channel 1 stability diagram, figure 5.4, we clearly distinghuish faint lines, especially in the second quadrant [5]. If one would zoom onto these

[5] defined in figure 5.2

lines, one would see similar transitions than the three I showed in the figure 5.7. Along with this remark, the reader shall notice that these transitions are barely visible in channel 2 stability diagram, figure 5.5. but they are still recorded in that channel 2. Indeed, even though we cannot see the dot-lead-transitions like in channel 1, we still are able to detect the interdot transitions in channel 2, whenever there is one in channel 1.

We now have to focus on one dot-lead transition only[6]. We need to zoom again. The left panel on the figure 5.8 presents a zoom of the blue square. On the right panel is a zoom, again, on the edge of central, single top dot lead.



(a) *Zoom of the blue area of figure 5.7 showing three consecutives charge transition line occuring in the dot 1 crossed by a dopant transition line. We do not see the interdot lines nor the dot-lead transition lines of the dopant. We are only capacitively coupled to that dopant.*

(b) *Zoom on the blue circle of the left panel showing a single dot-lead transition. This transition will be the frame of work for all the continuous pulsing experiments presented in this manuscript.*

Figure 5.8 *Left panel: zoom on three consecutive charge transition lines of the dot 1. Right panel: zoom on the blue circle of left panel, highlighting one dot-lead transition. From now on, we will focus on this top, central dot-lead transition. All the following presented work about continuous pulsing had been done on that single dot-lead transition.*

The simple case: without any magnetic field

The protocol is the following: we continuously apply a square voltage with a duty cycle equal to 1 on top of the topgate 2, vertically in that case, while recording the reflected phase signal through the channel 1. We play with both the voltage amplitude and the period of the square pulses. I will come back later about the duty cycle.

[6] remember from our practical requirements that we must only see one broken dot-lead transition without the interdot line transition nor the other crossing dot-lead transition.

peut être une petite figure illustrative pour les pulses ? peut être pas nécessaire aussi....

I start with no magnetic field. In that case the spin states are degenerated so we do not expect to see any spin features. However, we still do expect an effect of the pulse sequence on the stability diagram. Indeed, the recorded stability diagram will be an average of two stability diagrams. The first one corresponds to the 0 voltage stage and the other one is the same but shifted (here, vertically, along Vg_2) by the voltage amplitude of the square pulse and weighted by the duty cycle, here 50 %. This duty cycle ensures that the square pulses sequence spends half of the time in the 0 voltage stage and the other half in the finite voltage stage.
For a first step, I am going to focus on long period square pulses, typically in the millisecond range, close to our bandwidth limit. In that limit, we can easily suppose that every characteristic times of the system are shorter than the period of the square signal, including tunneling times or even relaxation times. We thus expect to record a stability diagram which is the average of the one presented in the right panel of figure 5.8 and the same one but shifted by the voltage amplitude of the square pulse.

The following figure 5.9 gives an illustration of such average. The left panel of 5.9 is a handmade construction of the expected final stability diagram in the long period limit. It consists of the average of the left panel of figure 5.8, corresponding to the zero voltage stage and the same data but shifted by -1 mV along Vg_2, corresponding to the -1 mV voltage stage. Qualitatively, we see an extension of the dot-lead transition of -1 mV. Quantitatively, the intensity of this extended dot-lead transition is the half of the original dot-lead transition intensity. This is due to the fact that we spend half of the time in the finite voltage stage. The right panel of figure 5.9 is the experimental result for a period of -1 mV voltage amplitude during 1 ms and another millisecond spent in the 0 voltage stage.

The next figure 5.10 presents cuts along the dot-lead transition to see quantitatively the correspondance between the two maps.

The two cuts are very similar, with a 1 mV plateau of half the signal of the original dot-lead transition phase signal, as expected. Even though the two traces are not exactly overlapping each other, we got the expected feature for the long pulse duration limit.

In the case of very long pulse time and no magnetic field, we quite easily understood what should happen. In fact, we were expecting similar behaviors for shorter pulse times because

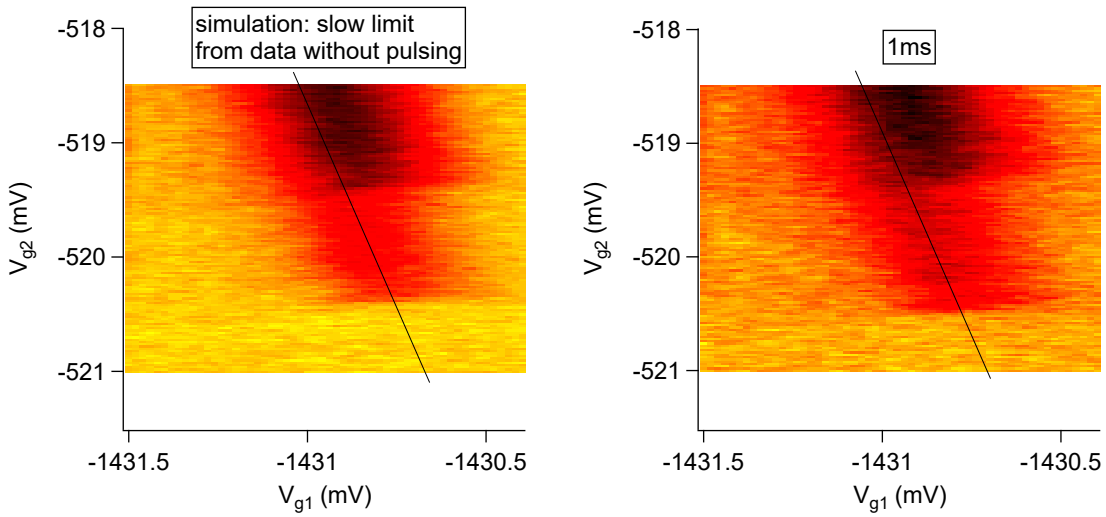


Figure 5.9 *Expectation and measurement of a stability diagram while continuously pulsing along one axis, here the vertical axis. In this case, the square pulse sequence is decomposed in one stage at 0 voltage and another one at -1 mV of same duration, 1 ms. The duty cycle is equal to 50 % so we spend half of the time in the first stage and the other half in the second stage. The left panel is a handmade construction of the expected stability diagrams under such conditions. We simply average the original stability diagram (right panel of figure 5.8) with the same stability but shifted by -1 mV along vertical axis. The black line shows the direction of the cuts which are presented in the next figure 5.10.*

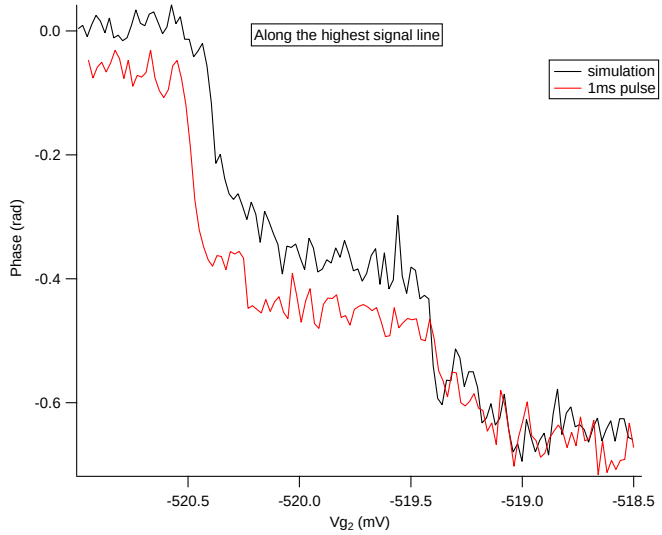


Figure 5.10 *Cut along the highest signal line, the black line of the previous figure. The two traces are similar, yet not completely overlapping each other. The big difference is the signal amplitude, about 0.07 radian, in the no signal area (right part of the curve) and in the plateau area (middle part of the curve).*

the spin states are degenerated without any magnetic field.
The figure 5.11 presents the results for shorter periods. From left to right, top to bottom, we can see the result for a pulse duration of 0 s (right panel of 5.8), 1 μs, 10 μs, 100 μs and 1 ms (right panel of figure 5.9). Indeed, we got similar results for any pulse duration.

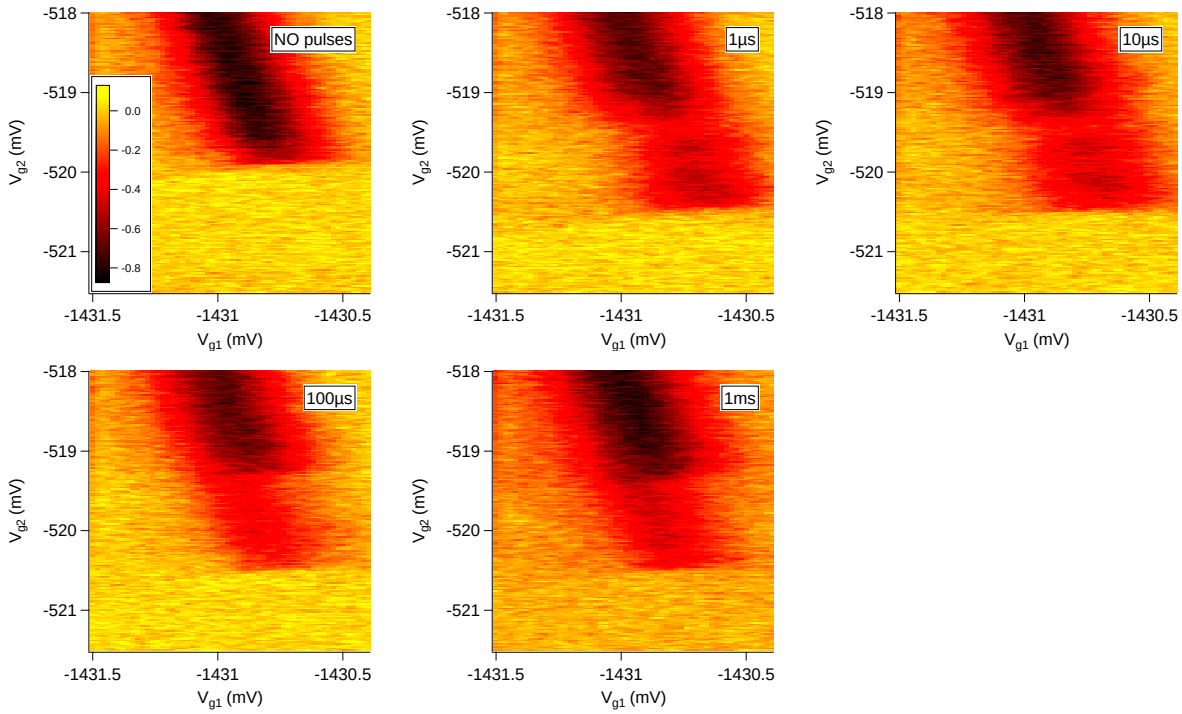


Figure 5.11 *Continuous pulsing measurements for no magnetic field. The top left plot shows the single dot-lead transition without any pulse. The four other plots present the results for a given duration of the square voltage, from 1 µs to 1ms. At first sight, all the plots are very similar. We see the expected 1mV extension of the dot-lead transition.*

The figure 5.12 presents cuts along the dot-lead transition for each pulse duration presented in figure 5.11. At first order, we do recover a 1 mV plateau (equal to the absolute voltage value of the finite voltage stage) with an amplitude of about half the amplitude of the original dot-lead transition. However, some discrepancies with the expected results can be noticed: first, the amplitude level of the middle plateau is not exactly at half the original amplitude. Second and most intriguing point is the presence of peaks at the entrance and at rougthly the third of the dot-lead extension, around Vg_2=-519.5 mV and Vg_2=-520 mV for both cases of 1 μs and 10 μs pulses.

To finish the presentation of the results for the canonical 0 magnetic field case, I shall mention a last thing about the duty cycle. Indeed, during the whole study, we have kept the

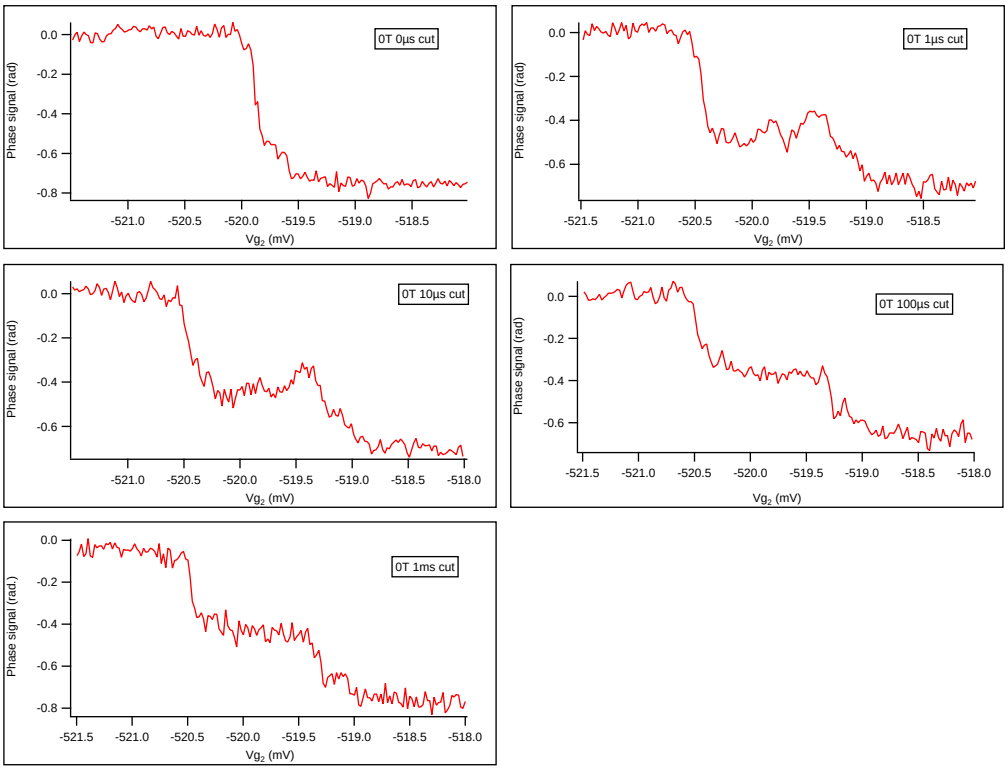


Figure 5.12 *Serie of 1D traces corresponding to the cut along each dot-lead transition line presented in figure 5.11. When the duration time of the pulse is not too slow nor too fast, we see a structure made of peaks and dips emerging. Though it is hard to relate these features to any physical properties, it is still interesting to see that, even at zero magnetic field, something has a dynamic in the range of hundreds of microseconds.*

pulse sequence duty cycle to 50 %: half of the time down in the 0 voltage stage and the other half of the time in the finite voltage stage. However, this is also a degree of freedom one can easily change. Unfortunately, I decided not to experiment with such non-unitary duty cycle sequence. In fact, this continuous pulsing experiment was not the originial goal so I decided not to explore all the parameter space. However, we can still figure out what would happen in such case.

We fixed the duty cycle to 50 %. We then spend the same amount of time in both stages. As we saw, this locked parameter implies that the extension of the dot-lead has an amplitude equals to half the amplitude of the original extension: $\phi_{ext} = \frac{1}{2}\phi_{orig} + \frac{1}{2}\phi_{nosign}$ with ϕ_{ext} the phase signal at an extension point, ϕ_{orig} the phase signal at the corresponding point in the original dot-lead transition point[7] and ϕ_{nosign} is the recorded phase when there is no transition signal, in the yellow portion of the graph. If you suppose this ϕ_{nosign} to be equal to 0, which is pretty much the case, you end up with a phase value in the extension being half the phase value of the original dot-lead transition. To sum up, when the duty cycle is 50 %, the weight factors for both phase terms is $\frac{1}{2}$. However when the duty cycle is not 50 %, the weight factors will change. Let suppose that your pulse period is composed first with a zero voltage stage for $\frac{3}{4}$ of the time and followed by a -1 mV square pulse for $\frac{1}{4}$ of the time, phase value in the extension would be equal to: $\phi_{ext} = \frac{3}{4}\phi_{orig} + \frac{1}{4}\phi_{nosign}$. Again, if one assumes ϕ_{nosign} to be equal to 0, one ends up with a 1 mV long extension plateau of $\frac{3}{4}$ the phase value of the original dot-lead transition.

The other case: non-zero magnetic field

The zero magnetic field case has already shown interesting features. We then decided to apply a magetic field of 4 T and look at similar measurements. The results are presented in figures 5.13 and 5.14.

[7] for instance, in the studied case of a square voltage of -1 mV applied on topgate 2, if the original dot-lead transition point is the point $\{Vg_1, Vg_2\} = \{-1431mV, -519mV\}$, its corresponding point will be $\{Vg_1, Vg_2\} = \{-1431mV, -520mV\}$

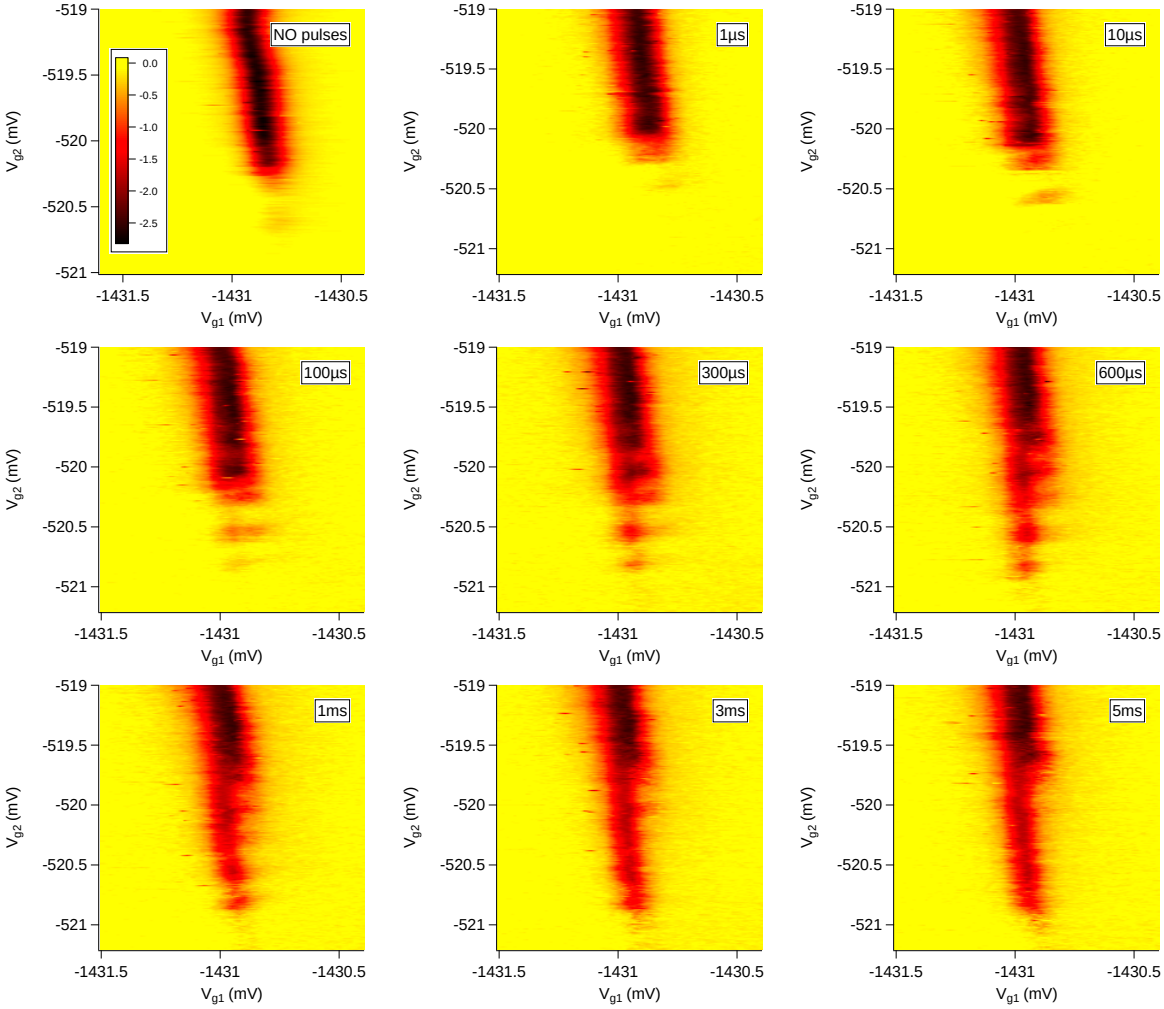


Figure 5.13 *Continuous pulsing measurements for a magnetic field of 4 T. The top left plot shows the single dot-lead transition without any pulse. The eight other plots present the results for a given duration of the square voltage, from 1 µs to 5ms. When we increase the duration time of the pulse, we see peaks and dips emerging. When the duration time is too long, a few milliseconds, we recover what we expect, a continuation of the dot-lead over the voltage value of the pulse.*

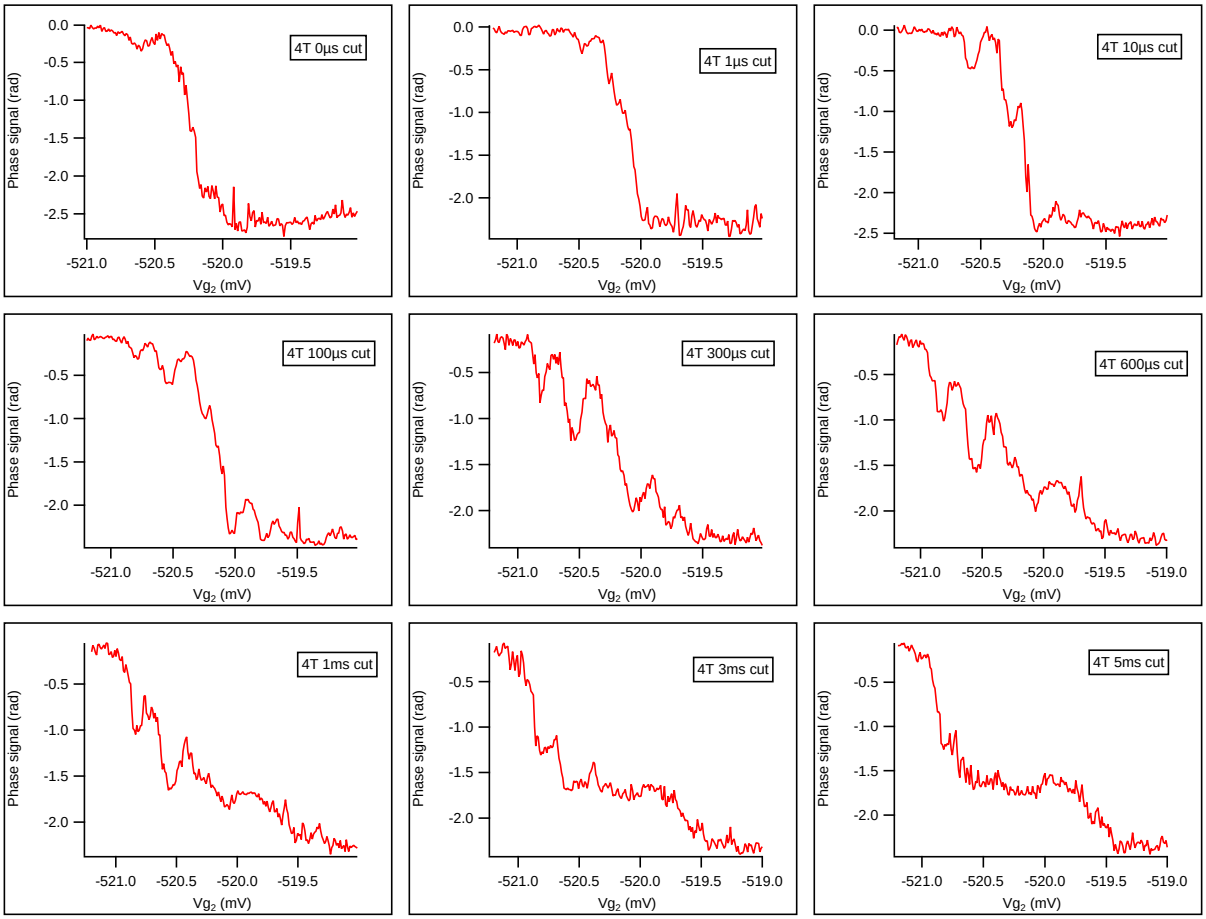


Figure 5.14 *Serie of 1D traces corresponding to the cut along each dot-lead transition line presented in figure 5.13. When the duration time of the pulse is not too slow nor too fast, we see a structure made of peaks and dips emerging. Though it is hard to relate these features to any physical properties, it is still interesting that at finite magnetic field and simply by continuous pulsing, we are sensitive to the dynamic of a physical system in a range of hundreds of microseconds.*

Although this experiment ends up mostly with qualitative results, we believe that a more complex sequence can give us interesting informations about the dynamic of the system.
In the next section, I will present the LREW sequence and its application on three triple points. The first studied one is the one we used to make that continuous pulsing experiments.

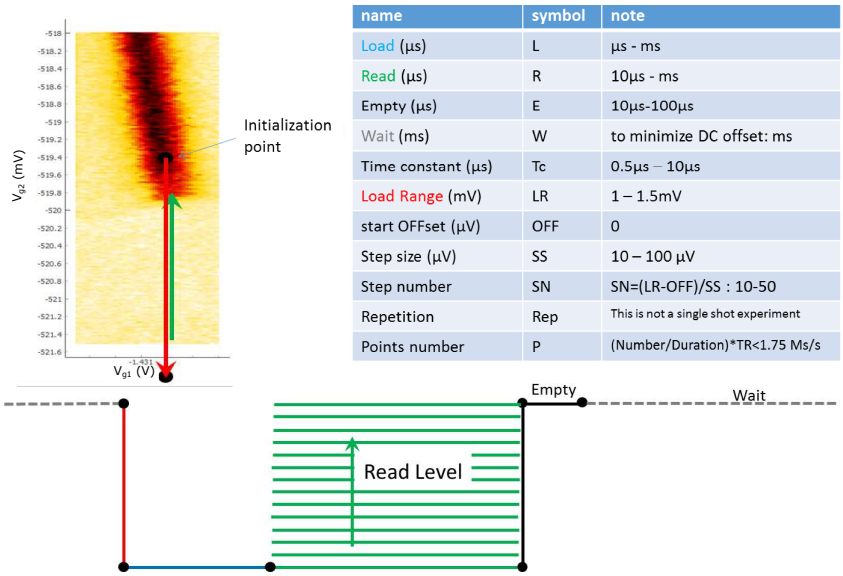
5.4 The Load-Read-Empty-Wait (LREW) sequence

I have already mentionned that we have changed the sample holder and we have also modified the electronical setup inside the fridge (see chapter 3, figure 3.18) to allow dynamic experiments. On top of that, we decided to move from Labview to Python in order to unify the different softwares around the laboratory and we now use the open source *qcodes* code. I will present the results in the following section but first I want to describe the routine, how to prepare the electronical setup and the software, how to set the AWG module and how to record the signal. However before each dynamical manipulations, we have to be sure about what we are really sending to the device, in other words what is the real voltage level of the pulse that the device does see.

5.4.1 Principle

The LREW sequence is the heart of the last experiment. This sequence should give us the right position (in voltage) for the read stage in order to be able to discriminate the two spins states and realize the spin-to-charge conversion mechanism. The following figure 5.15 gives an insight of this dynamic experiment. The top left panel shows the top dot-lead transition that we want to study. The colored arrows are related to stages of the sequence shown in the bottom panel. The top right panel exhibits the different parameters of the waveform we can play with.

By varying the *Read level*, highlighted in green in the figure 5.15, from the initialization point to the Load point (end of the red arrow in the coulomb blocked region), we will cover a large range in V_{g2}. Inside this voltage range, one should find a small window where the two spins can be distinguished.



name	symbol	note
Load (µs)	L	µs - ms
Read (µs)	R	10µs - ms
Empty (µs)	E	10µs-100µs
Wait (ms)	W	to minimize DC offset: ms
Time constant (µs)	Tc	0.5µs – 10µs
Load Range (mV)	LR	1 – 1.5mV
start OFFset (µV)	OFF	0
Step size (µV)	SS	10 – 100 µV
Step number	SN	SN=(LR-OFF)/SS : 10-50
Repetition	Rep	This is not a single shot experiment
Points number	P	(Number/Duration)*TR<1.75 Ms/s

Figure 5.15 *Principle of LREW experiment. The top left panel shows the dot-lead transition of interest in phase recorded with gate RF reflectometry through the channel 1 (correponding to the gate1). On top of the RF signal, the red and green arrows are related to the load stage and the read stage of the sequence, respectively. This sequence is schematically represented in the bottom panel while the complete set of parameters of the waveform and of the demodulator are shown in the top right panel. The different colors are related to the arrows of the top left panel and to the different steps of the sequence in the bottom panel. The variation of the read level is the key of the experiment. This will give us the voltage window where the two spins states are on each side of the electrochemical potental of the prober, allowing their differentiation.*

The reader shall notice the important number of parameters we need to tune. These parameters will depend on the dot-lead transition one is studying but also on the experiment one wants to make (preliminary calibrations or LREW), the time one wants to spend on a given experiment and the SNR one wants to achieve. Now I am going to present the preliminary calibrations of the pulses in order to be exactly sure about what is really sent to the device. Then, I will present the codes needed for such dynamical, pulsed experiment.

5.4.2 Preliminary calibrations of the pulses

One practical way to calibrate the real voltage level seen by the device is to send a succession of simple square pulses of constant voltage but with a different voltage for each pulse (typically a few tens of microvolts difference between two consecutive square pulses depending on the presision one wants). The initialization point, a couple of values (V_{g1},V_{g2})

in the stability diagram, has to be well defined [8] because this will be the fixed marker of the manipulation. We choose this point on the interesting dot-lead transition, the one we want to dynamically study later, close to one of its two triple points (a few hundreds of microvolts).

The full idea of this technic is to progressively pulse from this initialization point to the coulomb-blocked region and is illustrated in the following figure 5.16 which shows the final result of the calibration. The reflected RF signal will drastically change at the triple point, frontier between the dot-lead transition and the blocked region, see left panel of the figure 5.16. The frontier has to be sharp. By recording each phase response as a function of time for each successive pulse, one will be able to precisely know the correspondance between the real voltage seen by the device and the effective voltage sent by the UHF, see right panel of the figure 5.16. A simple proportionnal factor will then be extracted between the real signal seen by the device and the effective signal sent by the UHF. In this example, the calibration is complete since we get a nice correspondance between the stability diagram and the 2D plot showing the phase signal versus time for different voltage levels of the square pulses. Indeed, we see on the latter that the signal drastically change vor a value of V_{g2} equals to -640 µV away from the initialization point which is exactly the difference between the initialization point and the sharp transition on the stability diagram of the left panel.

To realize such pulse experiments, we need to record the reflected phase signal as a function of time. The typical time scale goes from hundreds of microseconds to a few milliseconds. The problem is that one cannot record such phase signal over so short time with classical loop codes provided by *qcodes*. Indeed, these loops intrisically average over milliseconds time scale. We will overcome that issue by using the Data aquisition module (DAQ) of the UHF, a module that allows for real time, trigguered acquisition.

The appendix A of this manuscript gives all the practical aspects one needs to realize the LREW experiment. Especially, I present the different codes that I wrote and used to perform that experiment.

In the next section, I am going to present the results, both in the case of no magnetic field and with a finite magnetic field.

[8] and it will be as well for the rest of the chapter.

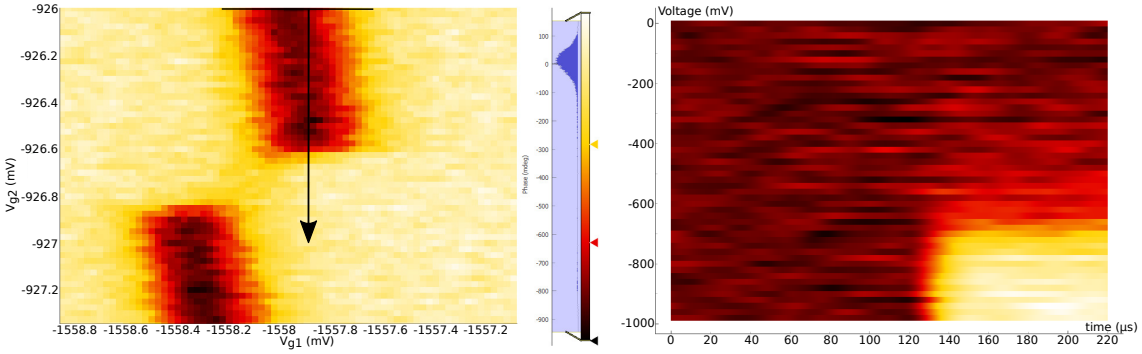


Figure 5.16 *Preliminary calibration. Left panel: Dot-lead transition of interest. The black horizontal line at V_{g2}= -926 mV indicates the initialization value for V_{g2} while we will pulse at constant V_{g1}= -1557.9 mV along the black arrow. We will successively pulse from the initialization point to a finite voltage value in V_{g2}. In this example, we realized 50 successive pulses with a -20 µV increment between two pulses. The pulses are constituted of a 100 µs zero voltage where we stay on the initialization point and a 100 µs finite voltage where we reach a finite value of V_{g2}. Right panel: 2D plot showing the phase signal versus time for the different voltage levels. Each row is a single reflected phase signal filtered by a 50 µs time constant RC-filter and averaged over 2000 repetitions with an effective voltage level relative to the initialization point (from 0 to -1 mV). We see a sharp transition of the phase signal around a relative voltage value of - 640 µV. This corresponds exaclty to the difference between the initialization point and the sharp transition, along V_{g2} seen in the left panel. If these two values of V_{g2} would not have been the same, one would have to modify the effective voltage value sent by the UHF by simply multiplying this effective value by the ratio of the two values where we do see a sharp transition.*

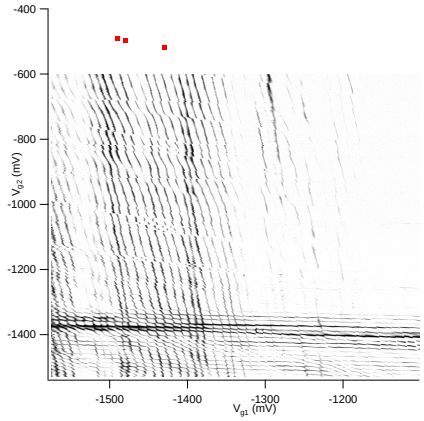
5.4.3 Results

I will present a LREW measurement for three triple points in the two cases: without magnetic field and with a non-zero magnetic field.

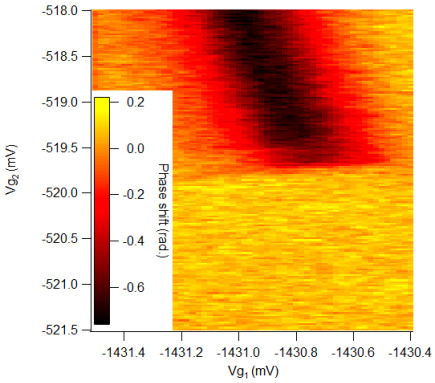
The figure 5.17a is the same stability diagram than the one presented in the figure 5.2 except that I added the position of the three studied triple points. I shall remember that we need to have one dot in the many carrier regime, in a *SET charge sensor* configuration being the detector and the other one being in the few carrier regime where the two-level system lies in. Because of that, it is important to know where we are working in the stability diagram.

The first studied triple point is presented in the figure 5.17b showing the phase shift of the channel 1[9] as a function of both topgate voltages. Only one dot-lead charge transition line, the top vertical line related to the dot 1/lead transition, is clearly visible while its counterpart

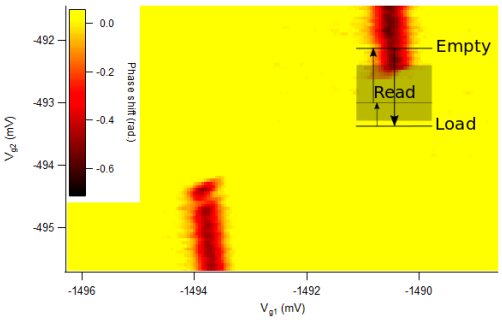
[9]It is recorded through the channel 1 of the reflectometry setup connected to the gate 1.



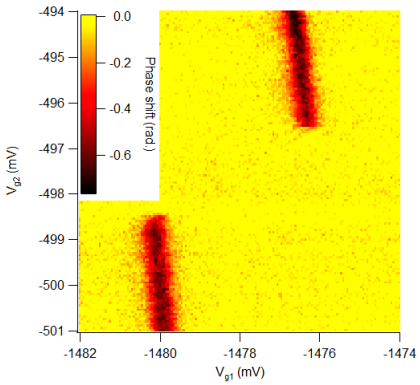
(a) *Large scale stability diagram showing the postion of the studied triple dot.*



(b) *First triple point of interest.*



(c) *Second triple point of interest.*



(d) *Third triple point of interest.*

Figure 5.17 *Presentation of the studied triple points. For the first triple point, I could not find any good figure containing both dot-lead transitions. For informations, the inderdot shift is about to 2.5 mV.*

is out of the figure. On top of that, the other pair of dot-lead transition lines, which would be horizontal, is not visible at all. This point suggests that the tunnel barriers are asymetric: The dot 1/lead tunnel barrier is more transparent than the other dot 2/lead tunnel barrier[10]. The interdot charge transition line is not visible, indicating a zero tunnel barrier between both dots.

In a similar fashion, the two figures 5.17c and 5.17d show the second and third studied triple points recorded with the channel 1. In both cases, the interdot is still not visible

[10]The reader may wonder that we are in fact recording the stability diagram with the channel 1 only. Then it should be obvious that we cannot probe the other pair of dot/lead charge transition lines with this channel. However we have checked that the other pair is also not visible with the other reflectometry channel.

suggesting no interdot charge transitions. Moreover, the two visible dot/lead transition lines are separated by a few millivolts, indicating a large capacitive coupling between the dots.

The next section presents the results without any magnetic field. In this case, the Zeeman splitting energy is 0. Thus, we expect to see only the impact of the pulse sequence without any signal from spin states.

Without magnetic field

The principle of the LREW experiment has already been presented in figure 5.15. We will send the pulse sequence on gate 2, i.e, we will pulse vertically, for one value of Vg_1 in the stability diagram. The sequence is schematicaly represented in the figure 5.17c. The arrows are horizontally shifted for the sake of clarity. The starting point of the sequence is on the upper dot/lead charge transition, labeled 'Empty'. We pulse down to the Coulomb Blockade area, bottom right quadrant to a point labeled 'Load'. This is the *load stage*. Then we pull up this voltage level. This is the *read stage*. Finally we go back to the starting point, the *empty stage*. Each sequence is repeated a certain amount of times[11]. Eventually, We apply this sequence for different read levels, represented by the grey area, labeled 'Read'. If spin states do contribute to the final result, we should see a non trivial signal at the beginning of the read stage above a certain value of read level voltage. On the contrary we expect a completely flat signal all along the Read stage if no spin-related mechanisms are at play.

The results are presented in figure 5.18 for the first studied triple point, figure 5.17b. This 2D colorplot shows the phase shift of channel 1 as a function of the Read level voltage in y axis and time in x axis. This 2D colorplot is very similar to the one presented in the right panel of the figure 2.13.

The 2D colorplot is splitted in four different section by the black dashed lines, the Load, Read and Empty sections. The phase value of the Load area is constant and equal to the Coulomb blockade phase value. The white dashed line shows the transition of the phase value in the Read area between the Coulomb blockade value and the dot/lead transition value, around Read-level=1000 μV. This point corresponds to the bottom edge of the dot/lead transition. The phase value of the Empty area is non-zero, constant and equals to to phase value of the dot/lead transition line.

[11] This point makes the readout not a single-shot one.

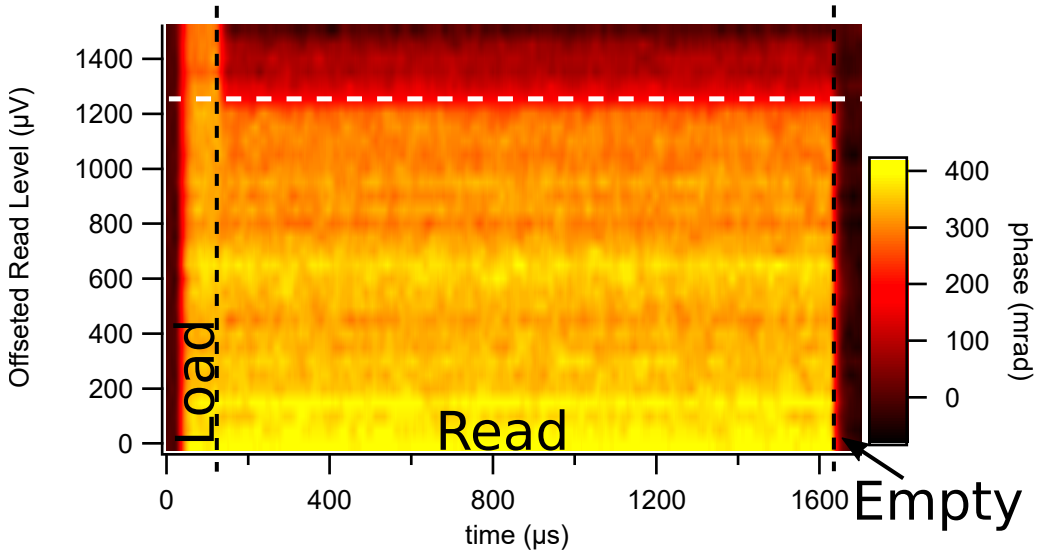


Figure 5.18 *LREW sequences realized for different read level voltages for the first triple point, figure 5.17b. Each line in this plot is the average of 20000 single LREW pulses. We pulse vertically. 2D colorplot of the phase shift as a function of time (x axis) and the read level voltages (y axis). The black dashed lines separate the different parts of the sequence, Load, Read Empty and Wait. The starting point (Empty point) of the sequence is (Vg_1;Vg_2)=(-1430.8 mV;-519.18 mV). The Load point of the sequence is (Vg_1;Vg_2)=(-1430.8 mV;-520.68 mV). In that case, the Load stage lasts for 100 µs, The Read stage lasts for 1500 µs and the Empty stage lasts for 100 µs. The time constant of the lock-in amplifier is set at 5µs. The white dashed line shows the transition between the Coulomb bockade regime and the dot/lead charge transtion corresponding to the bottom edge of the dot/lead transition in the figure 5.17b.*

Between the different areas, the phase signal always vary sharply[12]. There is no signal coming from any spin or quantum states. The experiment works very well without any magnectic field and gives the expected "clean" behaviour.

We did the experiment for the two other triple points, figures 5.17c and 5.17d. Respectively, the results are presented in figures 5.19 and 5.20.

I only presented three of the many different LREW sequences realized over many different triple points. The experiment has always showed the expected results at zero magnetic field. This serie of experiments tells us that indeed we are able to precisely pulse on a topgate while we record the phase.

[12]The time constant is small enough to avoid any artificial damping effect, see figure A.3

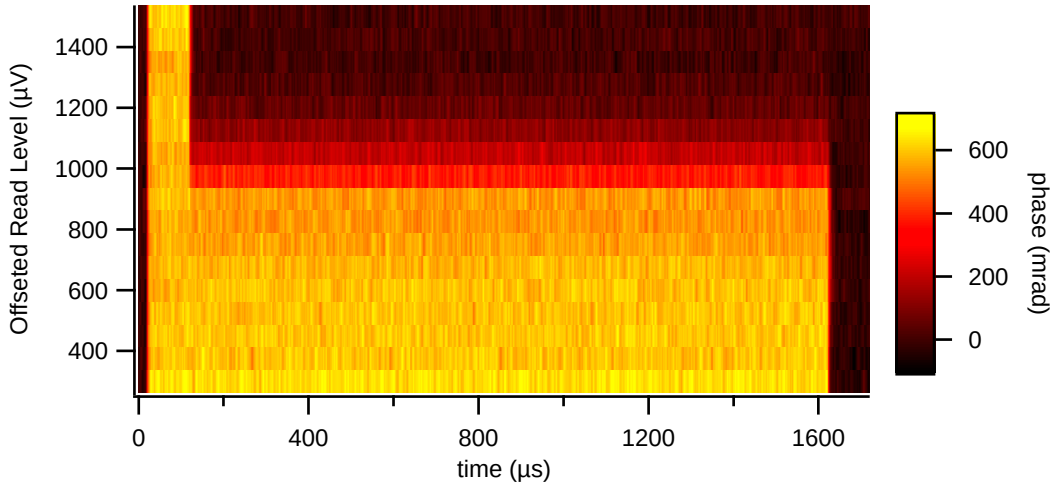


Figure 5.19 *LREW sequences realized for different read level voltages for the first triple point, figure 5.17c. Each line in this plot is the average of 20000 single LREW pulses. We pulse vertically. 2D colorplot of the phase shift as a function of time (x axis) and the read level voltages (y axis). The starting point (Empty point) of the sequence is (Vg_1;Vg_2)=(-1490.3 mV;-491.7 mV). The Load point of the sequence is (Vg_1;Vg_2)=(-1490.3 mV;-493.2 mV). The first measured Read level is 300 µV above the Load point. In that case, the Load stage lasts for 100 µs, The Read stage lasts for 1500 µs and the Empty stage lasts for 100 µs. The time constant of the lock-in amplifier is set at 1µs.*

Now let's work at non zero magnetic field. The reader will see that the results are quite unexpected.

With magnetic field

In order to probe spin states, we must turn on the magnetic field. I will present similar results than the one presented in the last section.

Figure 5.21 shows a 2D colorplot of a LREW experiment for the first studied triple point, figure 5.17b. The magnetic field is set at 4 T. Figure 5.22 shows a 2D colorplot of a LREW experiment for the second triple point. The magnetic field is set at 5 T. Figure 5.23 shows a 2D colorplot of a LREW experiment for the third triple point. The magnetic field is set at 5 T.

In that three cases, we see that we do not end up with the same colorplot. Indeed, for the three cases, the transitions between the Load stage and the Read stage and between the Read stage and Empty stage are not sharp anymore. We carefully checked that this was not an artificial damping effect. Indeed, the first transition between the first Empty stage and the

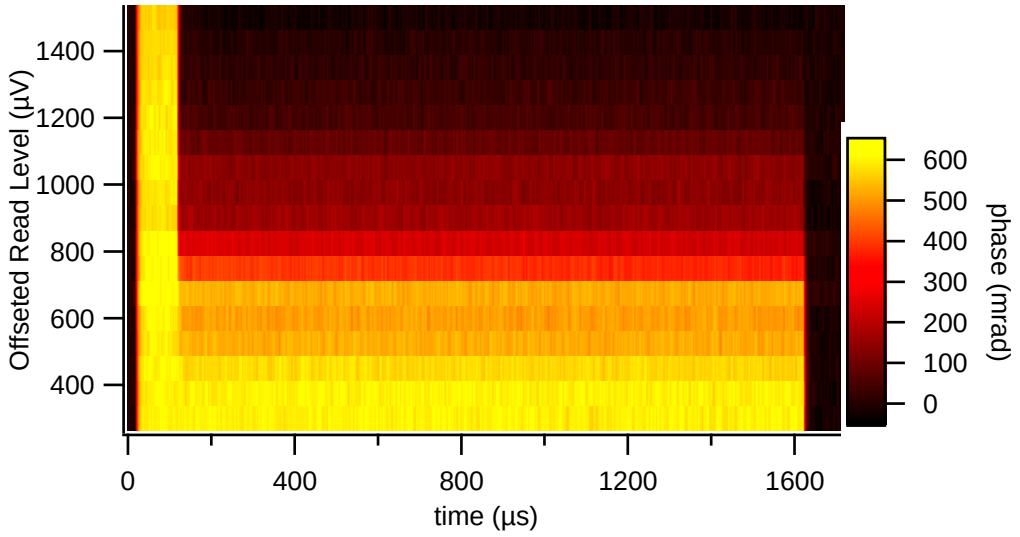


Figure 5.20 *LREW sequences realized for different read level voltages for the third triple point, figure 5.17d. Each line in this plot is the average of 100000 single LREW pulses We pulse vertically. 2D colorplot of the phase shift as a function of time (x axis) and the read level voltages (y axis). The first measured Read level is 300 µV above the Load point. The starting point (Empty point) of the sequence is (Vg_1;Vg_2)=(-1476.26 mV;-496 mV). The Load point of the sequence is (Vg_1;Vg_2)=(-1476.26 mV;-497.5 mV). In that case, the Load stage lasts for 100 µs, The Read stage lasts for 1500 µs and the Empty stage lasts for 100 µs. The time constant of the lock-in amplifier is set at 1µs.*

Load stage remains sharp for the three 2D plots and for all the Read level voltage values. This strongly suggests that something is going on under magnetic field.

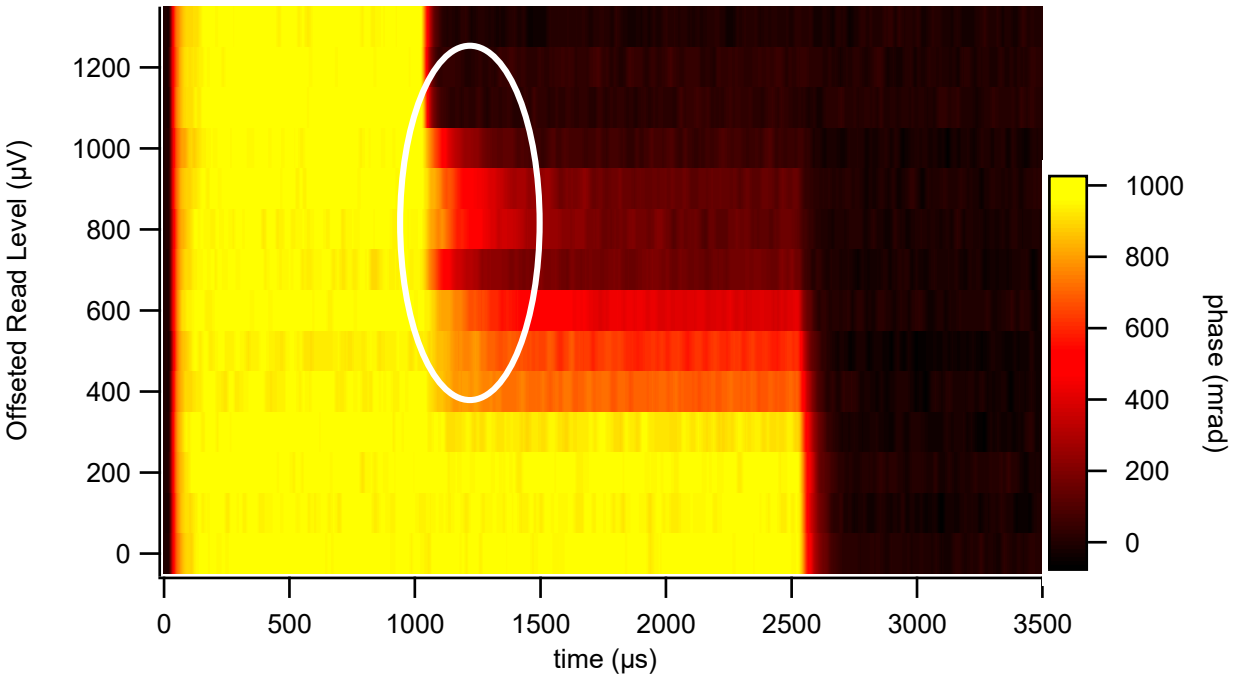


Figure 5.21 *LREW sequences realized for different read level voltages for the first triple point, figure 5.17b. Each line in this plot is the average of 10000 single LREW pulses. The magnetic field is set at 4 T. We pulse vertically. 2D colorplot of the phase shift as a function of time (x axis) and the read level voltages (y axis). The starting point (Empty point) of the sequence is (Vg_1;Vg_2)=(-1430.92 mV;-518.8 mV). The Load point of the sequence is (Vg_1;Vg_2)=(-1430.92 mV;-520.1 mV). In that case, the Load stage lasts for 1000 µs, The Read stage lasts for 1550 µs and the Empty stage lasts for 1000 µs. The time constant of the lock-in is set at 5µs. The reader can see that the transition between the Load area and the Read area, circled in white, is not sharp anymore. This is a strong indication that something is going on under magnetic field.*

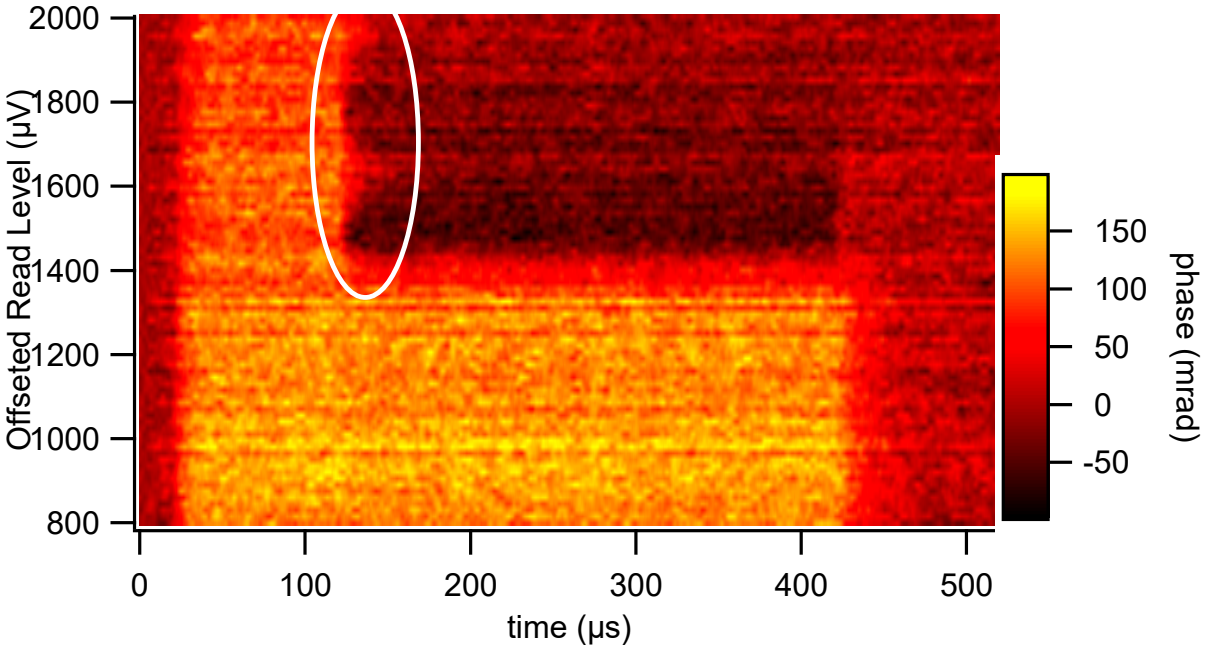


Figure 5.22 *LREW sequences realized for different read level voltages for the second triple point, figure 5.17c. Each line in this plot is the average of 50000 single LREW pulses. The magnetic field is set at 5 T. We pulse vertically. 2D colorplot of the phase shift as a function of time (x axis) and the read level voltages (y axis). The starting point (Empty point) of the sequence is (Vg_1;Vg_2)=(-1460.65 mV;-491.45 mV). The Load point of the sequence is (Vg_1;Vg_2)=(-1460.65 mV;-492.85 mV). The first measured Read level is 800 µV above the Load point. In that case, the Load stage lasts for 100 µs, The Read stage lasts for 300 µs and the Empty stage lasts for 100 µs. The time constant of the lock-in amplifier is set at 1µs. We clearly see that the transition between the stages are not regular nor sharp anymore.*

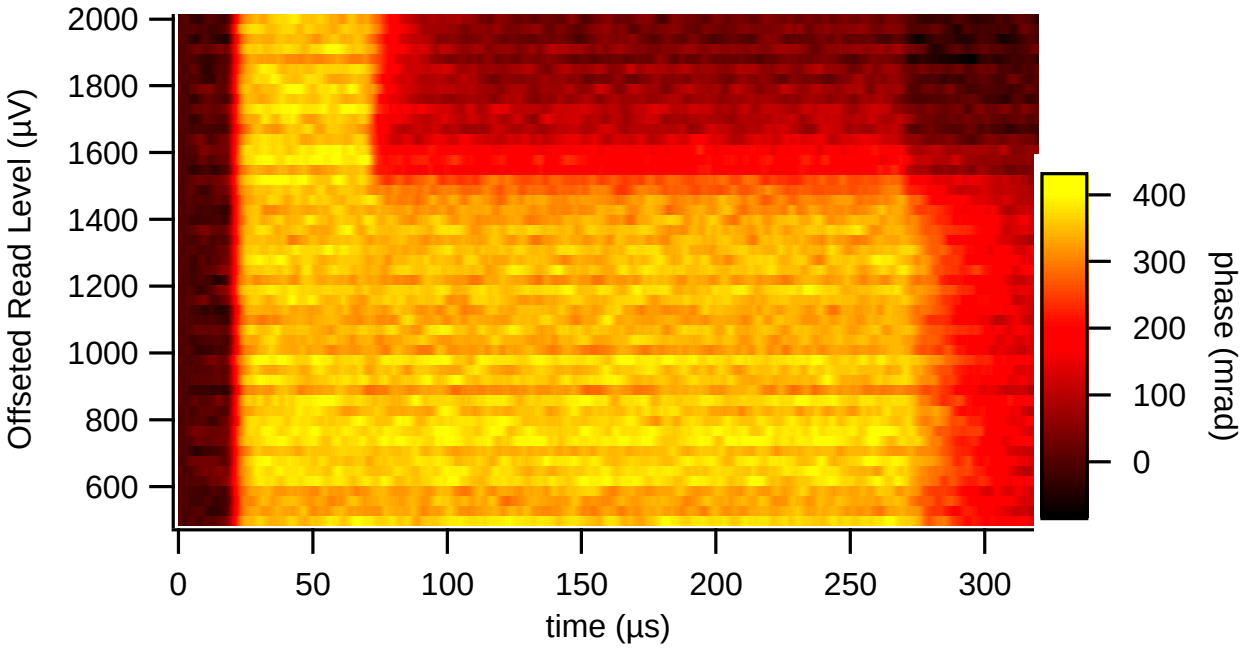


Figure 5.23 *LREW sequences realized for different read level voltages for the third triple point, figure 5.17d. Each line in this plot is the average of 50000 single LREW pulses. The magnetic field is set at 5 T. We pulse vertically. 2D colorplot of the phase shift as a function of time (x axis) and the read level voltages (y axis). The starting point (Empty point) of the sequence is (Vg_1;Vg_2)=(-1475.8 mV;-496.2 mV). The Load point of the sequence is (Vg_1;Vg_2)=(-1475.8 mV;-498.2 mV). The first measured Read level is 500 µV above the Load point. In that case, the Load stage lasts for 50 µs, The Read stage lasts for 500 µs and the Empty stage lasts for 50 µs. The time constant of the lock-in amplifier is set at 1µs. We clearly see that the transition between the stages are neither regular nor sharp anymore.*

Among all the triple points we have studied, only these three points have shown peculiar results at non zero magnetic fied. We found out that these three triple points share common characteristics when recorded with reflectometry without any pulse sequence involved and at finite magnetic field. They are presented in the figure 5.24.

When the triple points are recorded at finite magnetic field without any pulse sequence involved, interesting features show up, the dot-lead transition line is not homogeneous anymore, especially close to the interdot region. Lines parallel to the interdot line emerge.

For the first triple point, presented in the left panel of figure 5.24, I measured $\Delta V \approx 420$ $\mu V \pm 40$ μV, corresponding to the splitting between the undermost line and the dot-lead transition.
The measured LREW at 4 T for this triple point, presented in figure 5.21, exhibits an anusual

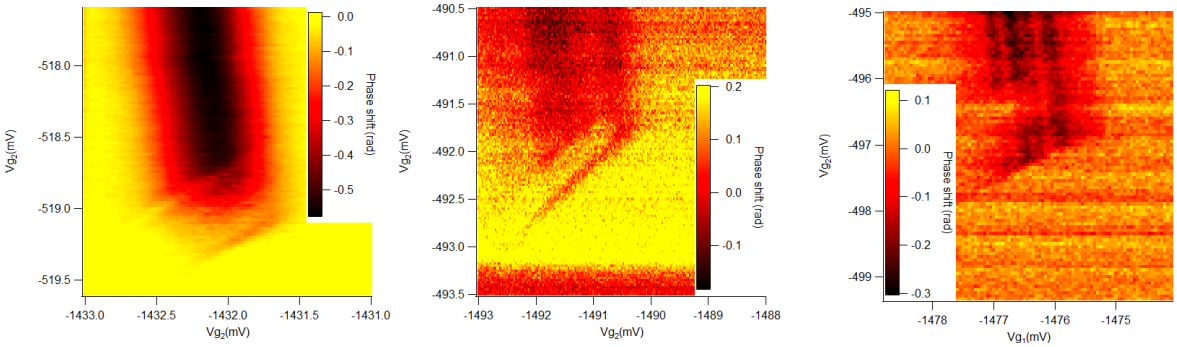


Figure 5.24 *The three studied triple points recorded at finite magnetic field without any pulse sequence. From left to right are the first, the second and the third triple point, respectively. We clearly see lines emerging at the bottom of the dot-lead transition.*

feature circled in white. This peculiar region extends over a range of about 350 μV $\pm$ 100 μV.

In the case of the second triple point, middle panel of figure 5.24, I measured ΔV $\approx$ 450 μV $\pm$ 100 μV, corresponding to the splitting between the undermost line and the dot-lead transition.
The measured LREW at 5 T for this triple point, presented in figure 5.22, exhibits two anusual features circled in white. The undermost signal covers a range of about 300μV $\pm$ 150 μV and the uppermost is not complete, its top part is outside the plot. The uncertainties are quite high because of the weak signal-to-noise ratio of the data.

Finally, in the case of the last triple point, right panel of the figure 5.24, I measured ΔV $\approx$ 400 μV $\pm$ 200 μV, the measure is too noisy, I cannot be more precise.
The measured LREW at 5 T for this triple point, presented in figure 5.23, shows smooth transition for all the Load-Read and Read-Empty edge. From this, it is hard to extract a range over which the peculiar signal spans.

Conclusion

A major goal of my PhD was to set up an experimental apparatus allowing one to perform energy selective spin readout in our devices. First we manage to set up the new lines dedicated to the pulse sequences. These lines can support signals from below the kHz to few MHz. After recording the stability diagrams and Coulomb diamonds, we decided to continuously pulse on one gate while recording the stability diagram in reflectometry thanks to the other channel. We end up with qualitative, yet to be fully understood, results. In particular, we

saw that at finite magnetic field and for some triple points, the dynamics was in the range of ten-to-hundred of kHz.

Then I implement the so-called LREW sequence, a 3-stage pulse sequence. We used the UHF lockin to send the pulse sequence thanks to its Arbitrary Waveform (AWG) Generator module and read the time-dependent data thanks to its Data Acquisition Module (DAC). We wrote the codes for both the DAC and the AWG, as well as the python code to collect the data. We also see that it was mandatory to calibrate the pulses sent to the device.

Eventually, we were able to perform LREW experiments. First we tried the setup without any magnetic field. We tried over lots of triple points. Without any doubt, the experiment works perfectly without magnetic field. Hence we looked for spin signals.

Again, we tried to get a spin signal over a lot of triple points. Most of the time, nothing happened. However for a few cases, the one presented in this manuscript, something did happen. We found out that something happened in the LREW 2D colorplot if and only if the triple point stability diagram showed peculiar features at the edge of the dot-lead lines, even without any pulse sequence, at finite magnetic field.

Chapter 6

Conclusion

"Quantum mechanics was, and continues to be, revolutionary, primarily because it demands the introduction of radically new concepts to better describe the world. In addition we have argued that conceptual quantum revolutions in turn enable technological quantum revolutions."

-Alain Aspect, 2004

In the past 20 years, a very impressive effort has been pursued by lots of scientists all around the world to unlock, step by step, the ultimate goal of a functional quantum computer. 40 years after the invention of that revolutionary concept and after a lot of different studied hosts for the qubits, we just reached the number of 53 superconducting qubits on a chip. Even if this is the record in 2020, we are still far from the hundreds of thousands of connected physical qubits and, thus, scalability is one of the biggest technical challenges in that field. On long term prospects, superconducting qubits do not seem to be the perfect candidate to realize a (universal gate-based fault tolerant) quantum computer.

In such wide and competitive framework, the commited position of this thesis is to support Silicon, foundry compatible, based qubits, made of electrostatically defined quantum dots in a silicon nanowire, mainly for the two following reasons: the physical properties of silicon materials and the maturity of the industrial CMOS technology are together undeniable advantages, at least in terms of scalability, in the long term race. More precisely, two crucial aspects of the qubit implementation are investigated: the control of the coupling between two quantum dots and a rather new way of measuring the spin states of a quantum dot, namely the energy selective spin readout.

In order for the Silicon based qubits to be competitive in terms of scalability, one does not just need to have industrial CMOS technology, one also has to perfom the measurement in a scalable way and it is clear that current based measurements or nearby charge sensor based measurements (probed in conductance of in radiofrequency reflectometry) are not the ultimate solutions. Since 10 years, the group has worked on a more *in situ*, dispersive, ingenious technique to probe changes in the quantum dot capacitance and eventually to probe quantum states, namely the *gate*-coupled radiofrequency reflectometry.

During the first year of this thesis, I studied a peculiar linear triple quantum dots system made of two outer electrostatically defined quantum dots and an inner, dopants-based quantum dot. The probing was realized by DC source-drain current measurement. It is in that context that we showed that the interdot coupling between the outer dots is strongly correlated to the state of the inner quantum dot. More precisely, we can go from (quasi) independent outer dots when the inner dot is Coulomb blocked to a strong interdot coupling between the outer dots when the inner dot state is aligned with the two other outer dot states. This effect could be used to quickly modulate the inderdot coupling between two MOSFET-based quantum dots through a quantum mediator, which is an important process in some quantum computing protocols.

Following this work about interdot coupling modulation, I learnt how to probe devices with radiofrequency reflectometry. Thanks to this new probing technique, I started the second year by quantifying the impact of another degree of freedom coming from a new design in the process flow which was not developped in the former batches, namely the metal line. In particular, we showed that the metal line has a direct influence on the electrostatics of the device, acting both on the interdot and on the dot-lead couplings. Here is another way to modulate couplings in a MOSFET-based quantum dot system.

Lastly, from the end of the second year, we deciced to focus on a powerful way of probing spin states in quantum dot devices, the energy selective spin readout, coming from the semiconductor community. It offers the advantage to be implemented as single shot measurement. To this day, single shot readout has been realized on MOSFET-based quantum dots only with the help of latched Pauli spin blockade mechanism. . The last year was devoted to the implementation of gate base radiofrequency reflectometry energy selective spin readout involving pulse sequences. First, we changed the setup in the homemade dilution cryostat in order to incorporate dedicated lines for the pulse sequences. After a couple of preliminary experiments, we showed that the experiment works perfectly without any magnetic field, i.e.

without any spin states. Eventually, we spent the whole year searching for a signature of spin. We eventually found three triple points showing non trivial behaviours at finite magnetic field. Although these results have not been completely understood yet, it is relatively clear that something is going on under magnetic field. At the end, we saw that these "magical" triple points exhibiting non trivial signals in LREW experiments under magnetic field also exhibit strange features in the static stability diagram under magnetic field. In the future, it will be easier to search for working triple points by knowing that these triple points directly exhibit features at finite magnetic field.

Of course, this work is only a small contribution to the ultimately complex goal of quantum computation. 4 years ago in 2016, the first Silicon-MOS based qubit was presented by our group. It was realized in a serial double quantum dot system, one dot carries the two level system, the other one acts as a detector. The spin-to-charge conversion was realized thanks to Pauli spin blockade mechanism and the detection was DC-current based. From that starting point, we decided to go to the face-to-face configuration with the detector and the two-level system in parallel. On top of that, the DC-current based measurement was replaced by gate based radiofrequency reflectometry. Finally, I tried to implement another spin-to-charge conversion mechanism, namely energy-selective spin readout.

I shall tell a few words about the doping. During my PhD I have mostly worked on P-type devices with holes being the charge carriers. It follows the previous work about the few-hole quantum dot in our device, which had lead to the realization of the first CMOS hole spin qubit. In fact there is a good reason to the use of P-type devices. In such devices where holes are the charge carriers, the intrisic spin-orbit couling allows for direct *electrical* manipulation of the spin. On the other side, electrons driven by ESR (standig for *Electron Spin Resonance*) lines providing a local magnetic field is another option, mostly pursued for now by our collegues of Institut Néel.
Overall during this PhD, I worked on few different tools and points of a toolbox among the vast set of all the improvable and needed points.

To conclude, many more points have to be improved in the quest of a Silicon-MOS based quantum computer. First, both the state manipulation and the state readout have to be mastered in order to have the required fiability. Eventually, we would have 1 relevant qubit. Then, an important work has to be done on the structure of the qubit network, whether it is from the material or the design point of view. Coherence of the qubits and connectivity also has to be mastered. Once we will have enough coherent interconnected qubits, fault

tolerant quantum computation could be possible. In parallel of all of that, a full research field is dedicated to cryo-CMOS electronics. That cryo-electronics will surround and support the qubit network in the cryostat. In the end, would it be possible to find trade-offs between qubit density, power dissipation, noise signal and decoherence ? Will the future quantum electronical engineers be able to master device variability at such incredible scales ? The race is far from over.

Conclusion

Au cours des 20 dernières années, un effort très impressionnant a été mené par de nombreux scientifiques dans le monde entier pour débloquer, étape par étape, l'objectif ultime d'un ordinateur quantique fonctionnel. 40 ans après l'invention de ce concept révolutionnaire et après de nombreuses études sur les différents hôtes possibles pour les qubits, nous venons d'atteindre le nombre de 53 qubits supraconducteurs sur une puce. Bien qu'étant le record en 2020, nous sommes encore loin des centaines de milliers de qubits physiques connectés et, par conséquent, l'intégrabilité à grande échelle est l'un des plus grands défis techniques dans ce domaine. Dans une perspective à long terme, les qubits supraconducteurs ne semblent pas être de candidats idéaux pour réaliser un ordinateur quantique (efficace, basé sur un ensemble de portes logiques quantiques, autorisant les codes de correction d'erreurs).

Dans un cadre aussi large et compétitif, la position de cette thèse est de soutenir les qubits réalisés à partir de boîtes quantiques définies électrostatiquement dans un nanofil de silicium, compatible avec l'industrie de la microélectronique, principalement pour les deux raisons suivantes : les propriétés physiques des matériaux en silicium et la maturité de la technologie CMOS industrielle, tous deux sont d'indéniables avantages, au moins en terme d'intégrabilité, dans une perspective à long terme. Plus précisément, deux éléments cruciaux dans la mise en œuvre de qubits sont étudiés : le contrôle du couplage entre deux boîtes quantiques et une façon assez nouvelle de mesurer les états de spin d'un porteur de charge localisé dans une boîte quantique, à savoir la lecture du spin par sélectivité en énergie.

Pour que les qubits à base de silicium soient compétitifs en termes d'intégrabilité, il ne suffit pas de se reposer sur la technologie CMOS industrielle, il faut également optimiser la mesure du qubit de manière intégrable et il est clair que les mesures basées sur le courant source-drain ou des capteurs de charge de proximité (sondés en conductance ou en réflectométrie radio-fréquence) ne sont pas les solutions ultimes. Depuis 10 ans, le groupe travaille sur une approche plus in situ, plus dispersive. Cette technique ingénieuse pour sonder les changements de capacité des boîtes quantiques et, finalement, pour sonder les états quantiques est la réflectométrie radio-fréquence sur grille.

Pendant la première année de cette thèse, j'ai étudié un système original de trois boîtes quantiques en série composé de deux boîtes quantiques externes définies électrostatiquement et d'une boîte quantique centrale réalisée à base de dopants. La mesure est réalisée par l'enregistrement du courant continu source-drain. C'est dans ce contexte que nous avons

montré que le couplage entre les boîtes externes est fortement corrélé à l'état de la boîte quantique interne. Plus précisément, on peut passer de deux boîtes externes (quasi-)indépendantes lorsque la boîte interne bloque le courant par blocage de Coulomb à deux boîtes externes fortement couplées lorsque l'état de la boîte intérieure est aligné avec les deux autres états des boîtes extérieures. Ce résultat pourrait être utilisé pour moduler rapidement le couplage inter-boîte entre deux boîtes quantiques basées sur des MOSFET par l'intermédiaire d'un médiateur quantique, qui est un processus important dans certains protocoles.

Suite à ce travail sur la modulation du couplage inter-boîte, j'ai appris à maîtriser le nouvel outil permettant de sonder les dispositifs, la réflectométrie radio-fréquence sur grille. Grâce à cette nouvelle technique de sondage, j'ai commencé la deuxième année en quantifiant l'impact d'un nouveau degré de liberté, la ligne métallique. Ce degré de liberté n'était pas dessiné dans les précédents lots. En particulier, nous avons montré que la ligne métallique a une influence directe sur l'électrostatique dans le nanofil, agissant à la fois sur le couplage inter-boîte et sur le couplage boîte-réservoir. Voilà un autre moyen de moduler les couplages dans un système de boîtes quantiques basé sur des MOSFET.

Enfin, dès la fin de la deuxième année, nous avons décidé de nous concentrer sur un moyen puissant de sonder des états de spin dans les dispositifs de boîtes quantiques, la lecture de spin par sélectivité en énergie, provenant de la communauté des semi-conducteurs. Cette méthode offre l'avantage de mesurer l'état de spin en une seule mesure, sans avoir à répéter la mesure plusieurs fois pour obtenir un signal mesurable. À ce jour, la lecture d'états de spin en une seule mesure sur des boîtes quantiques à base de MOSFET n'a été réalisé qu'à l'aide du mécanisme de blocage de spin de Pauli verrouillé. La dernière année a été consacrée à la mise en œuvre de la réflectométrie radio-fréquence sur grille pour la lecture du spin par sélectivité en énergie impliquant des d'impulsions électriques. Tout d'abord, nous avons modifié la configuration du cryostat à dilution fait maison afin d'incorporer des lignes dédiées pour ces impulsions électriques. Après quelques expériences préliminaires, nous avons montré que l'expérience fonctionne parfaitement sans aucun champ magnétique, c'est-à-dire sans aucun état de spin. Finalement, nous avons passé toute l'année à chercher un signal de spin. Nous avons finalement trouvé trois points triples montrant des comportements non triviaux à champ magnétique fini. Bien que ces résultats n'aient pas encore été complètement compris, il est relativement clair que quelque chose se passe sous champ magnétique. A la fin, nous avons vu que ces points triples "originaux" présentant des signaux non triviaux dans les expériences sous champ magnétique présentent également des caractéristiques étranges dans le diagramme de stabilité sous champ magnétique. À l'avenir, il sera plus facile de rechercher

des points triples intéressants en sachant que ces points triples exposent directement des caractéristiques non triviales dans le diagramme de stabilité à un champ magnétique fini.

Bien entendu, ce travail n'est qu'une petite contribution à l'objectif final et complexe d'un ordinateur quantique. Il y a 4 ans, en 2016, le premier qubit basé sur du Silicium-MOS a été présenté par notre groupe. Il a été réalisé dans un système de double boîtes quantiques en série, une boîte porte les deux niveaux du qubit, l'autre sert de détecteur. La conversion spin-charge a été réalisée grâce au mécanisme du blocage de spin de Pauli et la détection était basée sur la mesure du courant continu source-drain. Aujourd'hui, nous avons décidé de passer à la configuration en face à face avec le détecteur et le système à deux niveaux en parallèle. En outre, la mesure basée sur le courant continu a été remplacée par une mesure de réflectométrie radio-fréquence sur grille. Enfin, j'ai essayé de mettre en œuvre une autre méthode de conversion spin-charge, à savoir la lecture du spin par sélectivité en énergie.

Je vais dire quelques mots sur le dopage. Au cours de mon doctorat, j'ai surtout travaillé sur les systèmes de type P, des trous étant les porteurs de charge. Cela fait suite aux travaux précédents sur les boîtes quantiques à quelques trous qui avait conduit à la réalisation du premier qubit CMOS avec des spins de trous. En fait, il y a une bonne raison d'utiliser des dispositifs de type P. Dans ces dispositifs où les trous sont les porteurs de charge, le couplage spin-orbite intrinsèque autorise la manipulation *électrique* directe du spin. D'un autre côté, les électrons manipulés par une ligne ESR (Résonance électronique de spin) générant un champ magnétique local est une autre option, principalement poursuivie pour l'instant par nos collègues de l'Institut Néel.
Dans l'ensemble, au cours de ce doctorat, j'ai travaillé sur quelques outils et points spécifiques parmi les vaste ensemble de tous les points améliorables et nécessaires.

Pour conclure, de nombreux autres points doivent être améliorés dans la quête d'un ordinateur quantique basé sur du silicium MOS. Premièrement, la manipulation et la lecture de l'état doivent être maîtrisée afin d'avoir la fiabilité requise. Au final, nous aurions 1 qubit pertinent. Ensuite, un travail important doit être fait sur la structure du réseau de qubits, qu'il s'agisse du point de vue des matériaux ou de l'architecture. La cohérence des qubits et leur connectivité doivent également être maîtrisées. Lorsque nous aurons suffisamment de qubits cohérents et interconnectés, les codes de corrections d'erreurs pourront être implémenté. Parallèlement à tout cela, une recherche complète est consacré à l'électronique cryo-CMOS. Cette cryo-électronique entourera et soutiendra le réseau de qubits dans le cryostat. Au final, serait-il possible de trouver des compromis entre densité de qubits, dissipation de puissance,

signal de bruit et décohérence ? Est-ce que les futurs ingénieurs en électronique quantique seront capables de maîtriser la variabilité des dispositifs à des échelles aussi incroyables ? La course est loin d'être terminée.

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Appendix A

Presentation of the Arbitrary Waveform Generator (AWG) and the acquisition codes

A.0.1 The Data Acquisition module of the UHF

The reader shall know that the entire two next sections have been done in order for other experimentalists to have a complete, didactic procedure to follow.

As mentionned just earlier, the classical *qcodes* loops are not suitable for real time measurements of the phase, for example. I am going to present the Data acquisition module (DAQ) of the UHF allowing real time, trigguered acquisitions. The DAQ can obviously be piloted directly with the LabOne interface, the common interface of all modules of the UHF. However, we want to be able to set the important parameters of the DAQ in the python code like the numbers of points, the total duration of the record and the number of repetitions we want for each record. The two first ones a directly related to each other through the transfer rate of the UHF[1] while the last one depends on the Signal-to-Noise Ratio (SNR) one wants for its measurement. Eventually, all the parameters of the DAQ can be set inside the python code.

The following code presented in the Listing A.1 shows a portion of the python code *Qcodes_for_dilu06*. This close-up can be split in two parts separated by the code line 510.

[1] for instance, we want to record for x microseconds, the maximum achievable transfer rate, which depends on the length of the total waveform, is y MHz meaning y points per microseconds. Finally, the maximum number of points without loosing any data will be equal to x times y.

Above are parameters related to the pulse sequence itself: the demodulator channel used to read the reflected signal, the total duration of the pulse sequence (in seconds) and a recall of a function that I called *Read_level*. I will go back to this function later when I introduce the AWG module. Then the next line allows one to set the output power of the wanted RF channel (in dBm). After that, one can choose an initialization point in the stability stability diagram by changing the V_{g1} and the V_{g2} values and the bias voltage V_{dc}.

Following the initialization point setup is the value of the time constant. The next line define the total acquisition duration, the duration of the sequence plus two times ten microseconds before and after the sequence. This will be the total time recorded by the DAQ. The two next lines are important parameters related to the DAQ. First, one can set the number of repetitions he wants per sequence (line 498). The higher this number, the higher the SNR but the longer the experiment will take. Then comes the number of points. This parameter has to be ajusted both with the total acquisition duration and the transfer rate of the UHF. This relation is explained in the previous page. Then on line 500 we define the right demodulator trigger relative to data transfer. Here it is set on *AWGtrigger1 High*. This trigger has to be the same than the selected trigger of the useful demodulator in the LabOne interface (data transfer panel) and than in the AWG module but I will go back to this later on when I talk about this AWG module. The next line allows us to set the data transfer rate of the chosen demodulator in Hz. The next interesting line 504 set the time constant of the demodulator at the value we chose in line 495. In this example the demodulator 1 is used to read the RF tone. This is why one can read *TC1*.... If one wants to use the demodulator 2, do not forget to change the number from 1 to 2 in that line. The two next lines allow to enable or disable the AWG module and the output power through which the sequence will be send, respectively. Both must be enable if one wants to have the sequence sent to the device.

From the line 512 are the intrisic settings of the DAQ, first the trigger settings (from line 512) and second the grid settings (from line 519). Basically the only parameters one needs to change here are defined earlier. These are the number of points (line 499), the aquisition duration (line 497) and the number of repetitions (line 498). Finally the reader has to be careful with the trigger name of the line 512. As I said earlier for the data transfer trigger, this second trigger also has to be the same used in the AWG module that I am going to present later. The two last lines 533 and 534 define the parameter *phase_pulsed*. Both have to be refreshed each time you change any parameter related to the AWG or the DAQ. Finally the command *phase_pulse.get()* will give us a row of the averaged value of the phase (depending on the number of repetitions) for each point of the grid and, thus, as a function of time. In the

right panel of the last figure 5.16, each row of this 2D plot has been given by this command *phase_pulse.get()*.

Listing A.1 *Close-up of the python code showing the parts related to the DAQ and the pulse sequence. Everytime one wants to launch a new dynamic experiment, one must be sure about the parameters one sets here.*

```
484 demod=1
    imp.reload(SpecialParameters_dilu06)
486 Total_duration=200e-6 #need to be ajusted to the duration of your
       X steps sequence, in second (without taking into account the 2
       x10 us before and after the sequence)
    Read_level=SpecialParameters_dilu06.ReadLevel(ziUhf,
       User_register_window_sec=Total_duration) # This is set for a
       sampling rate of 225 MHz. Care in the special parameters, this
       frequency is called sequencer clock frequency and must be the
       same here in python and in the AWG module
488
    # Configure the parameters for the sequence
490
    ziUhf.signal_output1_amplitude.set(-45) #amplitude of the output 1
       in dBm
492 Vg2(-926)
    Vg1(-1557.9) #couple of values of the initialization point (in mV)
494 Vdc(0)
    TC=100e-6 # value of the time constant of desired demodulator in
       second
496
    acquisition_duration =Total_duration + 20e-6    # length of time
       to record (s)
498 repetitions = 1000 # number of repetitions for the averaging
    points = 1000 # number of points in the acquisition window : to be
       ajusted with the transfer rate, the duration of the sequence
       and the total duration of the recorded signal
500 ziUhf.daq.setInt('/dev2226/demods/%d/trigger'%(demod-1), 16777216)
       # demodulator trigger (relative to the data transfer) set on
       AWGtrigger1 High
    ziUhf.daq.setDouble('/dev2226/demods/%d/rate' %(demod-1),2000000)
       # transfer rate of demod 1 (in Hz)
502 ziUhf.daq.flush()
    time.sleep(1)
504 TC1_val.set(TC)  #Set the time constant of the UHF, in seconds
506 ziUhf.daq.setInt('/dev2226/awgs/0/enable', 1) # 1 = enable;   0 =
       disabled of the AWG module
    ziUhf.daq.setInt('/dev2226/sigouts/1/on', 1)  # 1 = enable;   0 =
       disabled of the output 2 (the channel trough which the sequence
       is sent, the other channel being used for reflectometry)
508 ziUhf.daq.sync()
510 #below are the parameters of the Data acquisition module, first
       the trigger and then the grid. Nothing has to be changed except
       what is set above (points etc)
512 trigger_setting = [['dataAcquisitionModule/triggernode', '/dev2226
       /demods/%d/sample.TrigAWGTrig2' %(demod-1)],  # trigger node is
       AWG trigger number 2
```

```
                    ['dataAcquisitionModule/type', 6],  # this
                        setting is related to the AWG trigger
514                 ['dataAcquisitionModule/edge', 1],  # trigger
                        on the positive edge. 3 = both, 1=positive
                    ['dataAcquisitionModule/count', 1], # number of
                        trigger events to count
516                 ['dataAcquisitionModule/holdoff/time', 0], #
                        hold off time
                    ['dataAcquisitionModule/holdoff/count', 0],  #
                        hold off count
518                 ['dataAcquisitionModule/delay', 0], # trigger
                        delay (s)
                    ['dataAcquisitionModule/endless', 0]] # endless
                        disabled = 0
520
grid_setting =    [['dataAcquisitionModule/grid/mode', 2], # mode.
    2 = Linear interpolation
522                 ['dataAcquisitionModule/grid/cols', points], #
                        number of points in the acquisition window
                    ['dataAcquisitionModule/duration',
                        acquisition_duration], # length of time to
                        record (s)
524                 ['dataAcquisitionModule/grid/rows', 1], # rows
                    ['dataAcquisitionModule/grid/direction', 0], #
                        scan direction. 0 = forward
526                 ['dataAcquisitionModule/grid/repetitions',
                        repetitions], # number of repetitions for
                        the averaging
                    ['dataAcquisitionModule/awgcontrol', 0], # set
                        the AWG control
528                 ['dataAcquisitionModule/save/fileformat', 1]]
                        # 1 = CSV format
530 #The two next and last lines define functions which are used to
       record the triggered phase in real time.
    #Need to refresh the following phase_pulsed parameters each time
       you change something above in the Data acquisition parameters
532
    phase_pulsed = SpecialParameters_dilu06.Pulsed_readout(ziUhf,
       demod, repetitions, returnOnePoint=False, treat_backgnd=False)
534 phase_pulsed.setSettings(trigger_setting, grid_setting)
```

This part of the python code sets all the important parameters relative to the DAQ, the triggers and the initialization point. Unfortunately, the AWG parameters cannot be set in python, we have to move to the AWG module of the UHF.

A.0.2 Setup the AWG module

During the last part I refered many times to the AWG module. Indeed, the python code and the AWG module has to be coherent to each other, same called triggers, same time between the set time of the sequence and the recorded time of the DAQ set in the code etc. Now I am

going to present the AWG code with the sequence used to realize the preliminary calibrations. This code is presented in the next Listing A.2.

Listing A.2 *Close-up of the AWG code for the sequence used for the preliminary calibrations, figure 5.16.*

```
const conversion_factor = 85.12; //this is the conversion factor
    you have to ajust thanks to the preliminary calibration
const ReadBurst_on_device_real = -20e-6;  //steps between 2
    consecutive pulses (in V)
const step_numbers=50; //numbers of steps you want to have (here
    50*-20e-6=-1 mV scanned)
const ReadBurst_AWG_real = ReadBurst_on_device_real*
    conversion_factor;                    //(V) REAL pulse amplitude
     seen by the device
const ReadBurst = ReadBurst_AWG_real/0.15; // convert the wanted
    voltage into a voltage number intrisic to the UHF

const burstwidth_sec =100e-6; //duration of the burst (in s)

const f_s =225e6; //AWG sampling rate
const f_seq = 225e6; //sequencer clock frequency

const burstwidth = burstwidth_sec*f_s;  // length in points or
    samples, for the burst.

wave zero_burst = rect(burstwidth, 0); // zero voltage for the
    same duration time as the burst (in s)
wave ReadWave;
cvar i;
for(i=0; i<step_numbers+1; i=i+1){
  ReadWave = join(ReadWave, rect(burstwidth, ReadBurst*(i)),
      zero_burst);
} //here we define a succession of elementary sequences. Each
    elementary sequence is defined by a zero voltage part followed
    by a fixed voltage part (define by the step number times the
    voltage step defined at line 2) both during the same time (here
    , 100 microseconds each). This ReadWave contains all the
    elementary sequences. We will just have to select which one has
     to be sent at the right time and this is done later in the
    code.

//definitions of the triggers:
void gate_start() {
  setTrigger(0b0001); // activate gate signal (AWG Trigger 1) to
      allow data transfer
  wait(f_s*10e-6); // wait a certain time (at least the inverse of
       the demodulator sample rate) to make the rising edge of AWG
      Trigger 2 visible in the demodulator data stream
  setTrigger(0b0011); // activate trigger signal for the Data
      Acquisition module (AWG Trigger2)
}
void gate_stop() {
  setTrigger(0b00); // reset gate and trigger signal
}

while (true) {
  gate_start();
  wait(f_seq*10e-6);
```

```
34    waitWave();
      playWaveIndexed(2, ReadWave, getUserReg(0), 2*burstwidth,
          AWG_RATE_225MHZ);
36    waitWave();
      wait(f_seq*10e-6);
38    gate_stop();
      wait(f_s*3e-3);
40
}//This is the core of the code, the activation/desactivation of
    the triggers and the while loop sending the waveform. Note that
     we wait 10 microsends just after the opening of the triggers
    and just before closing the triggers to be sure that we take
    all datas. We also wait for a long time after the wave (here it
     is 3 milliseconds). By doing that, the overall DC offset
    brought by the waveform is close to 0. A waiting time of 10
    times the duration of the non zero signals is enough.
42  //The most difficult part of the code is to understand what is the
     function playWaveIndexed. I am going to explain it in the main
     text.
```

The overall code for such preliminary calibrations is quite straightforward. The major difficulty comes from the line 35 and the function *playWaveIndexed* which is an extension of the function *playWave*, the basic function to send waveforms. This more sophisticated function allows one to send only a precise part of the overall waveform. This is exaclty what we need: we have created ReadWave, a complex waveform formed with a succession of elementary sequences. We now want to send each elementary sequence one by one. *playWaveIndexed* depends on 5 parameters: the first one is the channel number through which you want to send your sequence, here it is channel 2. The second is the name of the waveform you want to play, here it is ReadWave. The third one can be seen as an offset time (defined in samples, or equivalently in time thanks to the sampling rate) and is related to the variable called *getUserReg(0)*. The fourth one is a time window (again defined in sample) and in that example it is equal to the duration of the zero voltage part plus the burst part, namely 200 microseconds.

This time window and offset (through *getUserReg(0)*) have to be set such that the time window covers one full elementary sequence and the offset shifts from the beginning of an elementary sequence to the beginning of the newt one. Practically, the *playWaveIndexed* function, thanks to these two parameters, simply plays a portion of the full waveform from the offset point and during the set time window. Finally, the fifth one is the actual value of the AWG transfer rate. This rate converts time in samples, the elementary unit of time in the frame of the AWG.

When one has defined a waveform, succession of elementary sequences defined by their elementary time window in the AWG module, one needs to get back to the python code and ensure coherence between both codes. This means one most important thing: the *Total_duration* parameter at line 486 in python code should be exactly the same than the time window parameter defined in the *playWaveIndexed* function in the AWG module. Indeed, even the *Read_level* parameter defined line 487 also depends on this *Total_duration* through what I called the *User_register_window_sec* which intrisically define the right offset value in seconds.

Let's suppose that one wants to send the full waveform we used for the picture 5.16, namely a succession of 50 elementarty pulses of two times 100 microseconds with -20 microvolts in between each elementary pulses. Let's also suppose that everything has been well done in the python code and the AWG module. If one wants to send the tenth elementary sequence, corresponding to 10 times -20 microvolts, so the elementary sequence of -200 microvolts, one just has to call *Read_level(10)*.

I am going to end that subsection by showing the final loop alllowing to plot such 2D maps presented in the right panel of the figure 5.16. This loop is shown in the next Listing A.3.

Listing A.3 *Close-up of the final loop code allowing one to extract similar 2D maps that I presended in the left panel of the figure 5.16.*

```
steps_in_uV=20 #absolut value of the diffence in voltage between
    two consecutive elementary sequences
steps=50 #number of elementary sequences you are going to send
Phase_array=np.zeros((steps+1, points)) #define an initial zero
    array with the right dimensions (here 50 rows, the number of
    elementary sequences and the points number, so the time, in
    column)
for N in np.arange(steps+1): #the for loop over the number of
    different elementary sequences
    ziUhf.daq.flush()
    Read_level.set(N) # set the read_level function, practically
        it just selects the right elementary sequence.
    start=time.time()
    phase = phase_pulsed.get() #the function that extract the
        phase versus time.
    Phase_array[N,:] = phase #The array is filled during the loop
        with the different phase vs time values
    plt = mpl.pyplot.plot(phase*180000/3.14159)
    mpl.pyplot.ylabel('phase (millidegree)')
    mpl.pyplot.xlabel('grid points equivalent to time') # define a
        1D plot with all the different phase traces on the same
        plot
    end=time.time()
    print (N+1, 'step over ', steps+1, 'steps in ', (end-start),
        'secondes ( about ' , round((end-start)/60, 2), 'minutes
        )' )
```

```
564 # To save the data in a .txt file
566 np.savetxt('O:\\110-PHELIQS\\110.05-LATEQS\\110.05.01-
        QuantumSilicon\\Dilu06␣experiments\\data\\data\\2019-04-23\\002
        _m1557p9_B_1T_variable_square_pulse_100us_ConvFac85p12_
        Startm926mV_R_4MHz_dur_%.2fms_%.fuVSteps%.dSteps_TC1_%.2
        fus_repet_%.d_times.txt'%(acquisition_duration*1000,steps_in_uV
        , steps, TC*1000000, repetitions), Phase_array, fmt='%.8f',
        delimiter='␣␣␣')
568 #This is to 2D-plot the data : x=points (time), y=steps (voltage)
        and z is the phase data
    plt2D=qc.QtPlot()
570 plt2D.add(x=np.arange(points), y=-np.arange(steps+1)*steps_in_uV,
        z=Phase_array*180000./3.14159) #This define the final 2D plot
        like in the right panel of figure \ref{preliminary}
572 plt2D.save('O:\\110-PHELIQS\\110.05-LATEQS\\110.05.01-
        QuantumSilicon\\Dilu06␣experiments\\data\\data\\2019-07-06\\002
        _2D_m1557p9_B_1T_variable_square_pulse_100us_
        ConvFac85p12_Startm926mV_R_4MHz_dur_%.2fms_%.fuVSteps%.
        dSteps_TC1_%.2fus_repet_%.d_times.png'%(acquisition_duration
        *1000,steps_in_uV, steps, TC*1000000, repetitions)) # save the
        2D plot
```

This final code is pretty straightforward. One just has to care about the right correspondance of the steps number and the steps value set at lines 549 and 550 with the AWG code. Fundamentaly the work is fully done by executing the full code from the line 552 to line 562. I just presented the core of both python and AWG codes for a preliminary calibration experiment. Now I will present the sequence of interest, the Load-Read-Empty-Wait (LREW) sequence. I am going to first present the principles of the sequence, what it looks like and what are the parameters of interest then I will give the AWG code to generate such sequence.

A.0.3 AWG code for the Load-Read-Empty-Wait (LREW) sequence

The following code is the full AWG code for such a LREW sequence:

Listing A.4 *Close-up of the AWG code for the LREW sequence represented in the figure 5.15.*

```
// Variable read level, LREW sequence
2
const conversion_factor = 100; //take into account -20dB att + 0.9
    factor between AWG and real amplitude
4
// The following constants are the REAL amplitudes seen by the
    device. These are the parameter you have to change if you want
    to change any voltage level
6 const ReadBurst_on_device_real = 70e-6; // steps between
    successive read levels in Volts
const LoadBurst_on_device_real = -2000e-6; // voltage to access
    the coulomb blocked region, that is the Load level voltage in
    Volts
```

```
const offset_L_R_on_device_real= 600e-6;    // first point of the read level from the Load level voltage. Offset between the Load level and the first Read level in Volts
const step_number=20; \\number of read levels you want to scan

//real amplitude sent by the AWG
const ReadBurst_AWG_real = ReadBurst_on_device_real*conversion_factor;
const LoadBurst_AWG_real=LoadBurst_on_device_real*conversion_factor;
const offset_L_R_AWG_real = offset_L_R_on_device_real *conversion_factor;

// amplitude 'inside' the AWG, taking into account the range of amplitude
const ReadBurst = ReadBurst_AWG_real/0.15; //1.5 for 750mV range, 0.15 for 75mV range
const LoadBurst = LoadBurst_AWG_real/0.15;
const offset_L_R= offset_L_R_AWG_real/0.15;

// real time duration of each stage of the sequence Load-Read-Empty. These are the parameters you have to change if you want to change any duration of the different stages
const LoadWidth_sec=1e-6;
const Readwidth_sec =100e-6;
const EmptyWidth_sec = 100e-6; //every time here are in seconds

const f_s = 225e6;                    // AWG sampling rate, usually set to 225Ms/s
const f_seq = 225e6;                  // sequencer clock frequency (same)

// time 'inside' the AWG converted in samples
const EmptyWidth = EmptyWidth_sec*f_s;
const LoadWidth = LoadWidth_sec*f_s;
const Readwidth = Readwidth_sec*f_s;


const Total_duration= EmptyWidth + LoadWidth + Readwidth;

wave zero_burst = rect(EmptyWidth , 0);
wave LoadWave = rect(LoadWidth, LoadBurst);
wave Sequence;


cvar i;
for(i=0; i<step_number+1; i=i+1){
  Sequence = join (Sequence,LoadWave,rect(Readwidth, LoadBurst + offset_L_R +  ReadBurst*(i)), zero_burst); //This the for loop to define the different read levels. The i index gives the nomber of steps
} // Here we define the full waveform containing the successibe elementary LREW sequences for each read level.


//Triggers
void gate_start() {
  setTrigger(0b0001); // activate gate signal (AWG Trigger 1)
  wait(f_s*1e-6); // wait a certain time (at least the inverse of the demodulator sample rate) to make the rising edge of AWG Trigger 2 visible in the demodulator data stream
```

```
52    setTrigger(0b0011); // activate trigger signal for Data
          Acquisition tool (AWG Trigger2)
  }
54
  void gate_stop() {
56    setTrigger(0b00); // reset gate and trigger signal
  }
58
  // The loop played by the AWG
60 while (true) {
    gate_start();
62    wait(f_seq*10e-6); // just a wait between the the start of the
          trigger  and the start of the sequence

64    playWaveIndexed(2, Sequence, getUserReg(0), Total_duration,
          AWG_RATE_225MHZ);
   // The sequence. To loop on the read level, you need to vary the
      so called User Register. This is done semi-automatically in
      the python program as a function of the total duration of the
      sequence
66
    waitWave();
68    wait(f_seq*10e-6);
    gate_stop();
70    wait(f_seq*2e-3);// The waiting between each LREW sequence
          corresponding to the 'W' in LREW. We wait for a long enough
          time to avoid an anoying DC offset generated by the sequence.
  }
```

This code is very similar to the one I presented before for the preliminary calibration pulses (Listing A.2). We vary one stage of the sequence while keeping constant the others. One has just more parameters to tune like the duration of the three stages, the voltage value of the Load stage. As I mentionned before while dealing with the calibration stage, the coherence between this AWG code and the python code has to be perfect. It means that the *Total_duration* defined line 35 (Listing A.4) should have the exact same value than the *Total_duration* defined in the python code line 486 (Listing A.1). On top of that, the steps number and the step values (line 6 and 9 in the Listing A.4) must match the same parameters in the final loop of the python code (line 549 and 550 in the Listing A.3). Finally, all the triggers called in the AWG module (line 50 and 52) must be the same than the ones called in the python code (line 500 and 512).

We now have generated a succession of LREW sequences, each has its one Read level value. Let me sum up the full procedure:

1. One needs to find a serie of triple points of interest, meaning, in our situation, a low tunnel barrier between the quantum dots themselves and a strong asymetry between the two pairs of dot-lead transtions (one pair is visible on its own RF channel while the other one is not visible on its own RF channel).

2. One zooms on a pair of triple points.

3. One choose an initialization point on a dot-lead transition, not so far from the triple point (as we did on the left panel of the figure 5.16). Be sure that the maximum phase signal has been reached. This will set our future empty level.

4. At the stage, one needs to calibrate the pulse voltage exaclty like I did in figure 5.16. When one is absolutely sure about the voltage seen by the device, he is now ready to dynamically manipulate the device.

5. Now we will set the LREW sequence in the AWG code, Listing A.4:

   One chooses the *Load level* voltage to reach the coulomb blocked region (line 7 in the last AWG code)

6. One chooses now the *Read Level*, the steps between two successive Read level voltages (line 6)

7. One defines the *Offset*, the voltage shift between the Load level and the first Read level (line 8). This is mostly useful when you have a good idea where the interesting window is.

8. One chooses the *step numbers*, the number of different read levels one wants to set (line 9). This has to be set coinjointly with the value between two successive read levels (line 6).

9. One has to set the durations of each stage (line 22 to 24). This will define the *Total duration* of an elementary LREW sequence (line 35).

10. To finish with the AWG module, one just needs to save the code. Now the waveform is loaded.

11. From now on we go back to the python code (Listing A.1):

    The first thing one must do is to set the *Total duration* in the python code (line 486) according to the total duration value of the AWG code (line 35). Do not take into account the two times ten microseconds before and after an LREW elementary sequence.

12. One has to recall the *Read level* parameter (line 487) which depends on the total duration set earlier.

13. The next thing is to choose the right demodulator of the UHF, the one we want to use to read the phase signal.

14. This is time to set the parameters of the acquisitions: first one chooses number of repetitions (line 498) for each elementary LREW sequence.

15. Second, one has to set the number of points of the DAQ grid and conjointly the transfer rate. This is a non trivial part. The transfer rate defines a number of points sent to the computer per second and has to be ajusted as a function of the ratio of the total duration of an elementary LREW sequence (line 35) over the overall duration, including the long waiting time between two successives LREW sequence (line 70 in the last example and is equal here to two milliseconds).

    Practically one has to increase the transfer rate untill its highest value while not loosing datas[2]. When the transfer rate is fixed, one has to set the number of points in the grid. By knowing the transfer rate (a number of transfered data points per second) and the total duration of an elementary sequence (a time in second), one can define the right number of points for the grid.

16. One has to choose the time constant of the filter of the demodulator (the value is set at line 495 and the channel is set at line 504). The shorter the time constant, the faster the events one can detect but the smaller the SNR will be for a given number of points.

17. The parameters have now been well chosen, both for the sequence and the acquisition. It is time to excute this whole python code (ListingA.1), from the line 484 to the line 534. Eventually the AWG should be enable as well as the given channel (line 506 and 507 set on '1').

18. One now can record the phase as a function of time thanks to the final for-loop in the python code (Listing A.3).

    The first thing to do is to set the right step voltage in microvolts and the right number of steps (line 549 and 550) according to the values set in the AWG code (line 6 and 9, respectively in the Listing A.4).

19. One should care about the filenames (line 566 for the .txt file and line 572 for the .png 2D plot file) and the date of the data folder. The filename must contain as much informations as possible about the waveform and the acquisition parameters.

[2]this will be indicated by a red spot in the LabOne interface

20. Now one is ready to execute the whole code from the line 549 to the line 572, Listing A.3. Eventually one will end up with a 1D plot with the different phase vs points (time) for the different read level voltages, a text file with the whole data and a 2D plot with the points in abscissa, the different read level voltage values in ordinate and the phase signal as a colormap.

21. Thanks to the text file one can easily post-processes the datas to get the time in abscissa and to suppress the potential background in the phase signal.

The following figures A.1 and A.2 give an example of typical raw datas.

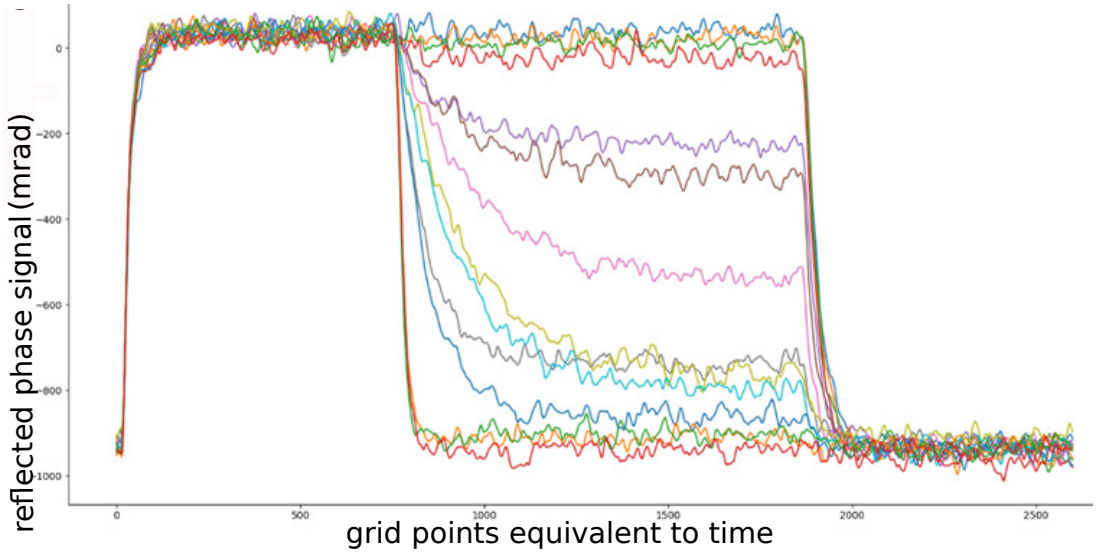

Figure A.1 *Ensemble of 1D traces showing the phase response of the channel 1 as a function of the grid points. Each trace correspond to one unique read level voltage. We pulsed onto the gate two for this measurement so the quantum dot two is the quantum object of interest. The load stage voltage is equal to -1.3mV for 1 ms, the read stage lasts for 1.5 ms and the empty stage lasts for 1 ms. The number of steps is 13 and there is a 100 µV shift between each successive read level voltage corresponding to a total spanning voltage of 1.3 mv. There is no offset here. The time constant of the channel 1 is equal to 5 µs and we repeat each trace 10000 times.*

I shall mention a last practical detail. During the setup of the Data Acquisition Module, one has to choose the Time Constant of the lockin filter, called *TC* (line 494 of Listing A.1 for instance). This parameter is of prime importance as it could completely modify the final result. The figure A.3 shows two batches of traces of two different LREWs sequences. Each trace is related to one Read level voltage. If we omit the durations of the Load and Read

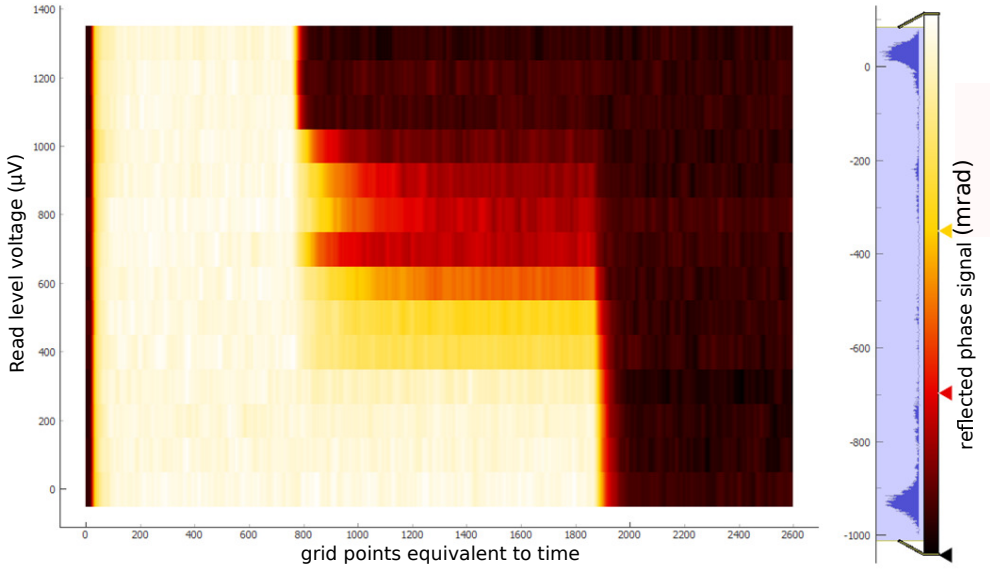

Figure A.2 *2D plot showing the phase signal in color as a function of the points grid in absissa and the read level voltage relative to the initialization point in ordinate. Each row of that plot corresponds to a single trace of the last 1D plot A.1. Thus the parameters of the sequence and of the acquisition are the same.*

stages, the major difference between the two batches is the value of the time constant. The top panel has been recorded with TC= 1μs whereas the bottom panel has been recorded with TC= 5μs.

Eventually, after all these preliminary calibrations and the presentation of a typical measurement of the LREW experiment, we can proceed to the experiment.

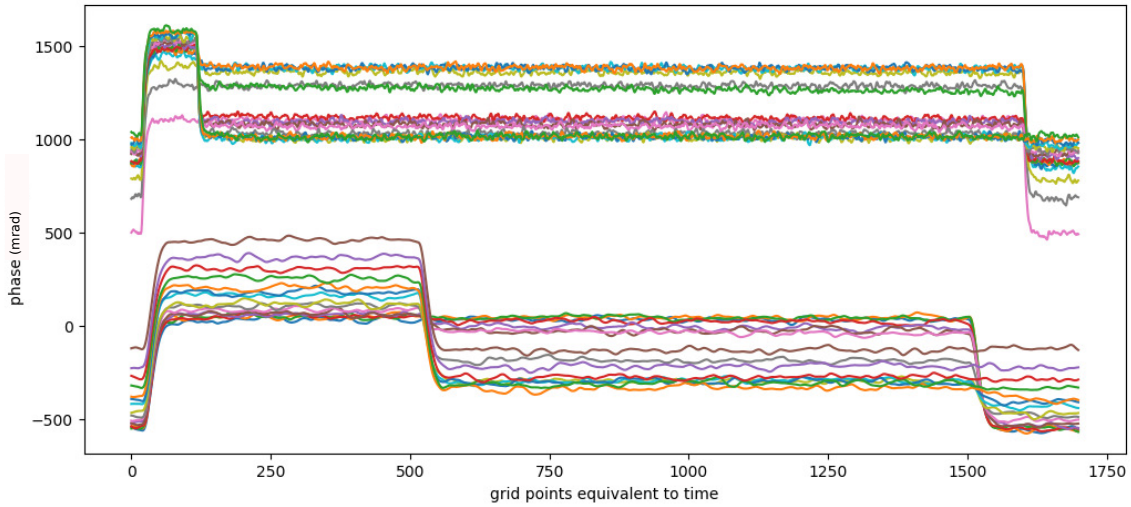

Figure A.3 *Impact of the Time constant (TC) on the acquisition of the data. Top panel: batch of traces (each trace corresponds to a single value of the Read level voltage) of a LREW sequence recorded with TC = 1µs. Bottom panel: batch of traces recorded with TC = 5µs. Even though the difference between both values of TC is not gigantic, we do see an effect of a too high value of TC. While, in the top panel, the transitions between the different stages of the sequence is sharp, we do see that the transitions are smoother in the bottom panel. The higher the TC value, the smoother the real sharp transition will be. It is simply a damping effect of the lock-in low pass filter.*