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How to upgrade a pixel detector: lessons from Phase-1 being applied to Phase-2 CMS Pixel Upgrade

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The High-Luminosity Large Hadron Collider at CERN is expected to produce proton-proton collisions at a center-of-mass energy of 14 TeV, aiming to achieve an unprecedented peak instantaneous luminosity of 7.5 x 10^{34} $cm^{-2}s^{-1}$, resulting in an average pileup of 200. To cope with these running conditions, the CMS detector will undergo an extensive upgrade: Phase-2. This upgrade includes the complete replacement of the CMS silicon pixel detector, introducing improvements such as increased radiation resilience, finer granularity, and capability to manage increased data rates among other changes. This is, however, the second time CMS has replaced their pixel detector. The differences and similarities between the Phase-1 and Phase-2 upgrades of the Inner Tracker of CMS will be outlined. Specific lessons learned from the operation of the Phase-1 detector will be highlighted, along with how this experience has informed the approach of the design and assembly of the Phase-2 Inner Tracker as preproduction of modules is approaching.

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1. Introduction

Pixel detectors in LHC experiments are complex devices consisting of millions of channels installed in a magnetic field able to withstand radiation environments. As running conditions of the LHC change, we need to adapt our detectors. This also gives us the opportunity to take advantage of advancing technology as we upgrade our pixel detectors. Looking back at problems from previous CMS pixel upgrades can be instructive as we upgrade our pixel detector today.

The CMS pixel detector will be upgraded in two phases [1]. First, it was upgraded to a digital readout in Phase-1. This upgrade took the number of channels from 66 million to 124 million. The second upgrade is almost in pre-production for module assembly and will bring the detector to 2 billion channels [2].

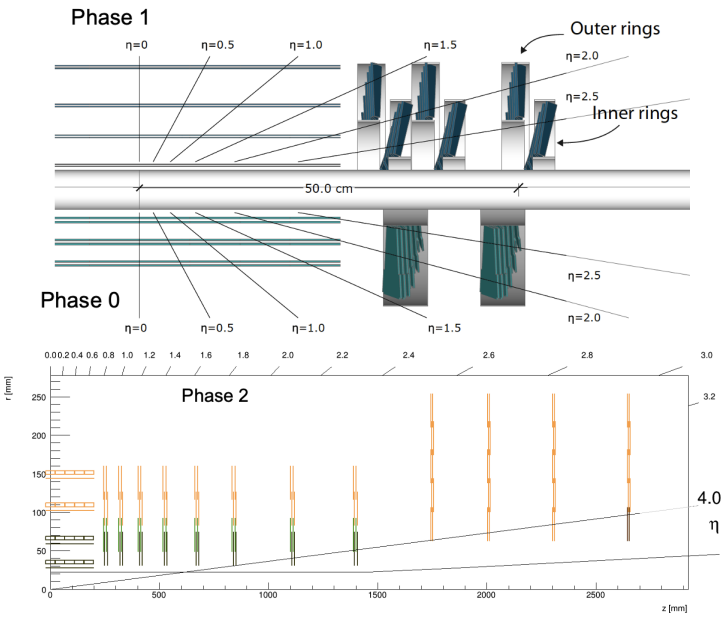

Figure 1: The layout of the original CMS pixel detector, labeled "Phase 0", can be seen along with Phase-1 (upper) [3] and Phase-2 (lower) [4]. While all 3 versions of the CMS pixel detector share a cylindrical geometry, It is easy to see they are different just from their layout. In the barrel region, there are 3 layers for the original CMS pixel and four for Phase-1 and Phase-2. The changes are even more stark in the forward region. The original CMS pixel had placards in the forward regions in two disks. Phase-1 has three toroidal disks with tilted blades. Phase-2 returns to a simpler geometry as modules are mounted on flat disks, but there are many more disks in Phase-2 extending high resolution hit sensitivity to a pseudorapidity of 4.

While Phase-1 kept the same pixel size of 100 x 150 μm^2 and the same number of readout chips (ROCs) per module, as the original CMS pixel detector, one can see in Fig. 1 there were substantial changes including an additional layer in the barrel region and an additional disk in the forward region. A fully digital readout and a CO_2 based evaporative cooling system were also some of the advances in technology that were used in the Phase-1 upgrade.The Phase-1 pixel modules share the overall structure of the pixel modules from the original detector. They consist of active silicon sensors that are bump bonded to 2 x 8 ROCs. These ROCs then communicate with the Token Bit

Manager (TBM) [5] via the High Density Interconnect (HDI). The HDI is connected to the ROC via a series of wire bonds. The silicon sensors are n+ in n sensors with a pitch of $100\,x\,150\,\mu m^2$ like in the previous CMS pixel detector, however the TBM and ROC were changed to cope with the higher particle rates.

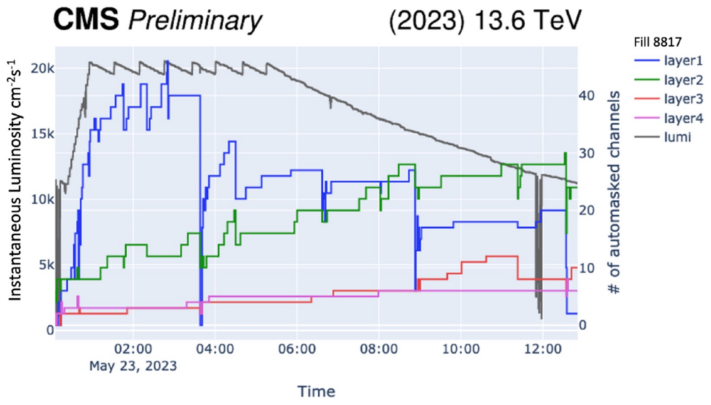

Figure 2: Plot showing a soft error recovery storm during May 23, 2024 for each of the 4 pixel barrel layers. The number of automasked channels in layer 1 (blue) can be seen climbing with luminosity (black). The dip in automasked channels just before 4 hours into the run is due to a pause and resume sent by global DAQ. The number of automasked channels from layer 2 (green) can be seen climbing the entire fill. These are due to stuck TBMs which accumulate during the run and are only cleared via a power cycle [6].

2. Stability is hard to come by

To recover stuck parts of the detector, a soft error recovery (SER) mechanism was created. This is a way to recovery from SEU (single event upset) or SEU-like events by only briefly interrupting data taking. SER recovers port cards and front end chips by refreshing the configurations of stuck parts. A full configuration would interrupt data taking for a much longer time. If the SER is not successful after several attempts, the channel is then automatically masked or "automasked". In Run 2 CMS started to experience SER "storms" when pileup exceeded 60. These were events during a run where the pixel would continuously go into SER and data taking would be interrupted very frequently for a few minutes. As seen in Fig. 2, the number of automasked channels in layer 1 is high until the pause and resume sequence is issued just before 4 hours into the fill, clearing the list of masked channels and allowing for reprogramming of devices at a lower PU near the end of the luminosity leveling phase of the fill. It was found that by adjusting the working point of the layer 1 channels these storms could be minimized but not entirely solved. Stuck channels in layer 2 continue to climb the entire fill and is not reduced by a pause and resume due to a vulnerability in the TBM. These stuck TBMs are how the DC-DC problem was discovered in 2017.

3. DC-DC converter saga

The author of this conference report notes that most people attending this session were aware of the DC-DC problem with the CMS Phase-1 pixel but not the details. To the graduate student

who is reading this conference report 10 years later: #1 good for you, #2 details of this saga are here [7] and here [8]. A short summary is given below.

The TBM is an ASIC that merges data from the ROCs with 320 Mbps readout rate. There are three versions of the TBM used in the Phase-1 CMS pixel detector: the TBMs output a single data stream for barrel pixel layers 3, 4, and all disks of forward pixel, two data streams for barrel pixel layer 2, and four data streams for barrel pixel layer 1. There are two TBMs on layer 1 modules to cope with the high particles rates expected. Early in running, it was discovered that a logic mistake allows for a possible locking of the Phase-1 TBM circuit. No reset was put on this circuit, so the only way to reset the TBM was to power cycle it. While power cycles clear the TBM lock, they are a heavy procedure and can result in voltage trips or a control crate needing to be reset. *Luckily* there exists a mechanism to power off and on the detector with finer granularity: by enabling or disabling the DC-DC converters.

In order to provide power to many more modules in Phase-1 than the original CMS pixel detector consisted of, the CMS pixel detector uses DC-DC converters to step from 10 V to 3 V. As this was an upgrade scheduled to be installed during an extended year end technical stop, the number of cables was fixed. 1184 converters based on the radiation-hard FEAST2 ASIC developed at CERN were needed for the Phase-1 upgrade. The pixel operations team used the enable/disable function in the FEAST2 chip to power cycle stuck TBMs in 2017. However after about 30 fb^{-1}, DC-DC converters started to break. By the end of 2017 data taking, 5% of the converters were broken. While problems in the CMS Phase-1 pixel system are unfortunate, its design allows it to be extracted and reinstalled quickly. There was however large concern for the LHC community because many less accessible detector systems were planning on using the FEAST2 DC-DC converters for the HL-LHC. Hence, there was much interest from the community. These converters have now been substituted with the bPOL converters because the FEAST production fab closed.

All DC-DC converters were replaced during year end technical stop 2017/2018. This allowed for detailed testing where it was found that 65 were broken and 333 exhibited high current. It was thought that the high current mode might be an initial sign of deterioration, but it is now understood that there were actually two failure modes, both related to trapped charge in the chip. In the disabled state, the current on the 220 nF capacitor increases as seen in Fig. 3. This causes voltage spikes well beyond the 3.3 V this part of the chip can handle. This part of the chip provides current to the drivers of the power transistors, so after a voltage spike the chip is dead and will not turn on. Similarly increase leakage current after irradiation damages the current mirror, causing high current DC-DC converters. During 2018, a workaround was developed to power cycle the stuck TBM modules from the power supply and also to reduce to 9 V so there were smaller currents during the power cycle sequence. The problem was permanently resolved with new DC-DC converters equipped with a new version of the FEAST2 ASIC that were installed during long shutdown 2 (LS2).

There is an unfortunate addendum to the DC-DC converter saga. Some modules were permanently damaged during running with their low voltage off due to broken DC-DC converters, but their high voltage on. A running configuration, coming about due to a mismatch in the LV and HV powering granularity, was not considered nor studied before. The turned-off readout chips could not drain the leakage current off the sensor efficiently, this damaged the preamplifier. Most damage can be seen in the modules where there were high particle rates, so in the affected forward pixel modules, the readout chips nearest the beam line are almost dead, but the readout chips furthest

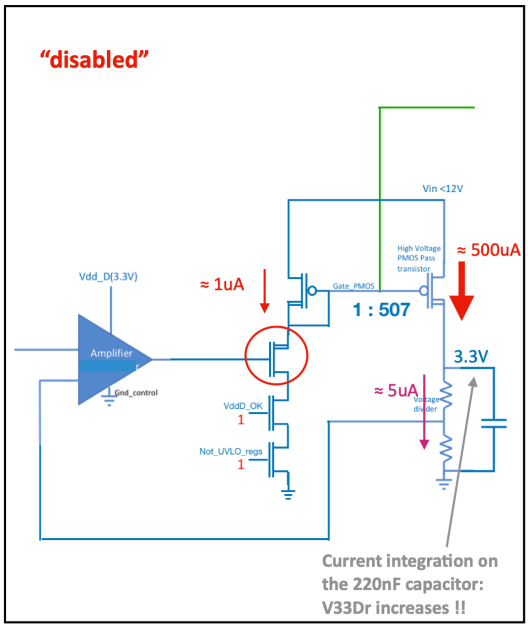

Figure 3: Diagram showing a section of the FEAST chip in disabled state. In this state, leakage currents are amplified and lead to a charge-up of a capacitor up to the input voltage (11.4 V in 2017) instead of the specified 3.3 V. The discharge when the converter gets enabled can damage the connected electronics irreversibly. Alternatively, a new ohmic path to ground can form. The latter case explains the occurrence of converters with higher power consumption in the disabled state. [8].

away from the beam line on the same module still provide good data for physics. Fortunately with the planned replacement of layer 1 during LS2, few enough modules were damaged so that the physics performance of the pixel was preserved.

4. Don't let sparks fly

Some lessons we have to learn twice. In 2018, two layer 1 modules were damaged during a 600 V biasing test. To avoid more damage, layer 1 was operated at 450 V for the rest of Run 2. During LS2 these modules, along with the entire layer 1, were replaced. Damage was caused due to sparking between a pad on the HDI and the guard ring. Layer 1 takes data at the highest bias voltage in the pixel detector because it receives the most radiation and is closest to the beam line. To avoid this failure mode, the replacement layer 1 was made with HDIs that had 3 times more space between the bonding pads and the edge. The forward pixel did not have this same vulnerability as their modules were encapsulated with Sylguard. Unfortunately, Sylguard turns to glass at the doses expected from the HL-LHC. Spark protection is essential for Phase-2 to avoid sparks between the sensor's guard ring and the test pads on the readout chip. For Phase-2 we are coating with Parylene.

While this insulator can withstand the high doses expect from the HL-LHC, it is deposited via gas deposition and gets everywhere, even the backside of the pixel modules. Heat transfers away from the modules via thermal contact with the mechanics. Adding a layer of Parylene between the modules reduces thermal conductivity. Masking and masking the delicate back of the pixel module before and after Parylene coating also introduces a risk for damage. Studies are ongoing for the best way forward.

5. Conclusion

Giving a talk, or in this case conference report, like this is risky. The author does not want the reader to think that the physicists and engineers designing and building our detectors do not know what they are doing. Solving the problems in CMS was a huge team effort by many experts. Instead, this author hopes to detail some unexpected problems encountered despite lots of testing prior to construction. We urge future detector builders to engage experts even after the detector is delivered, allocate more resources at the beginning of operation, and run more system tests with realistic running conditions to elicit problems that have yet to be discovered. Even after all the irradiation campaigns, thermal cycles, and test beams for Phase-2, physicists should expect the unexpected and look forward to solving mysteries with their new detectors. Despite the problems described in this report, the CMS Phase-1 pixel detector is running at high efficiency and taking good physics data.

References

[1] The CMS Collaboration, “The CMS experiment at the CERN LHC", **JINST** 3 (2008) S08004. doi:10.1088/1748-0221/3/08/S08004

[2] The CMS Collaboration, “The Phase-2 Upgrade of the CMS Tracker”, **CERN-LHCC-2017-009, CMS-TDR-014**, (2017). doi:10.17181/CERN.QZ28.FLHW

[3] CMS Tracker Group of the CMS Collaboration, “The CMS Phase-1 Pixel Detector Upgrade”, **JINST** 16 (2021) P02027. doi:10.1088/1748-0221/16/02/P02027

[4] CMS Tracker Layout Modelling Group, “CMS tkLayout: OT801-IT701”, https://cms-tklayout.web.cern.ch/cms-tklayout/layouts/recent-layouts/OT801_IT701/index.html.

[5] Bartz, E., “The token bit manager chip for the CMS pixel readout", 185-189, (2003), **9th Workshop on Electronics for LHC Experiments**. doi:10.5170/CERN-2003-006.185

[6] The CMS Collaboration, “Pixel Auto-masked Channels", **CMS-DP-2023-080**. https://cds.cern.ch/record/2876547

[7] The CMS Collaboration, “Phase-I Pixel ROC Thresholds and DC-DC Converter Characterization in 2018", **CMS-DP-2020-005**. https://cds.cern.ch/record/2714878

[8] F. Faccio, S. Michelis, G. Ripamonti, “Summary of measurements on FEAST2 modules to understand the failures observed in the CMS pixel system”, **CERN EP-ESE-ME**, October 15, 2018, CERN. https://power-distribution.web.cern.ch/assets/datasheets/SummaryMeasurements18.pdf