Characterization of FPGA based TDC with RPC detector

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Introduction

In the India-based Neutrino Observatory (INO) [1] experiment, the glass resistive plate chamber (RPC) detectors are being used as the active detector element. The in-house developed ANUSPARSH ASICs [2] are being used as front-end electronics (FEE) of the detector. The 2m X 2m RPC detector has 64-readout channels on X-side and 64-readout channels on Y-side. It is required to characterize the FEE with RPC detector before integrating the FEE in the INO detector stack. The parameters that are required to be measured for the FEE characterization include strip rate, detector efficiency, and time resolution. To measure these parameters a Spartan-6 Field Programmable Gate Array (FPGA) based 128-channel data acquisition system (DAQ) has been developed. Along with the firmware for measuring strip rate and detector efficiency, a precision time-to-digital converter (TDC) is also implemented in the same FPGA to measure the time resolution.

This paper presents the developmental aspects of the FPGA based TDC and experimental results with RPC detector. The FPGA based TDC is characterized with the ANUSPARSH FEE ASIC interfaced to the RPC detector of size 1m x 1m.

RPC FEE signal interface and DAQ

The signals (Hits) from the RPC detector are amplified and discriminated by the FEE module. The LVDS output of the FEE module is interfaced to a DAQ. The DAQ system is developed using Spartan-6 FPGA and ARM-cortex-M4 micro controller. The LVDS pulses are received by the on-chip differential receivers of the FPGA. The RPC event data was recorded and analyzed using a three-fold coincidence trigger, obtained from the scintillation paddles aligned with the RPC channel (readout strip). The channel aligned with the paddles can be selected in the FPGA firmware. To measure the time resolution, the time-of-arrival of the 'Hits' in the readout strip aligned with the paddle on the X-side and the Y-side is measured with respect to the trigger. It is also required to measure the pulse widths of the 'Hits'. To meet these requirements an 8-channel TDC is implemented in the FPGA in the following configuration: two TDC-channels per readout side for time-of-arrival measurement and two TDC-channels per side for width measurement. The timing data is interfaced to a readout buffer and is sent to the user interface through Ethernet implemented in ARM cortex-M4 micro controller. The detailed data analysis software is developed using LabView to display the time spectrums on the user interface.

Developmental aspects of FPGA TDC

The TDC is implemented in Spartan-6 FPGA using the Flash architecture. In this architecture the time of arrival of a hit and trigger is measured using a course counter and a fine interpolator as shown in Fig. 1. The coarse counter gives the coarse time in steps of integer number of reference clock periods with a resolution of one clock period (T_b). The fine time within the one clock period is obtained using the fine interpolator (T_a, T_c). The fine interpolator consists of a delay line having a number of delay cells. The cumulative delay of all the delay cells in the delay line is equal to one clock period. The coarse counter and delay line constitute one TDC channel. The detailed design aspects of course counter, delay line and final time calculation are reported in [3]. The time-of-arrival of the Hit (T_{Hit}) and trigger ($T_{trigger}$) are measured based on

the values of coarse counter and delay line of the particular channel. A dynamic range window is opened on the rising edge of the Hit. If the trigger is falling in the dynamic range window then the final time between Hit and trigger is given by ($T_{Hit} - T_{trigger} = T_a + T_b - T_c$). In the present design, the reference clock period is 5 ns and it is covered by 69 delay cells resulting in the least significant bit (LSB) of 72.4 ps. The dynamic range for the RPC characterization is set at 500 ns.

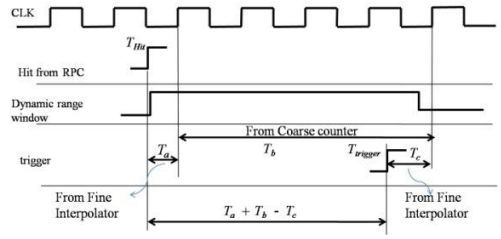

Fig. 1 Method of time-of-arrival measurement

Experimental Setup and Test results

The TDC is characterized with the experimental setup shown in Fig.2. The 1m x 1m RPC detector is used for this characterization. The RPC detector is interfaced with four FEE boards on X-side and four FEE boards on Y-side. Each FEE board has 8-channels. The detector high voltage is 10 kV. The threshold voltage of the ANUSPARSH FEE is set at +35 mV. In this RPC detector, the X-side pickup strips and Y-side pick strips are arranged along the same direction. The time-of-arrival between the Hit and trigger is measured as explained in the previous section.

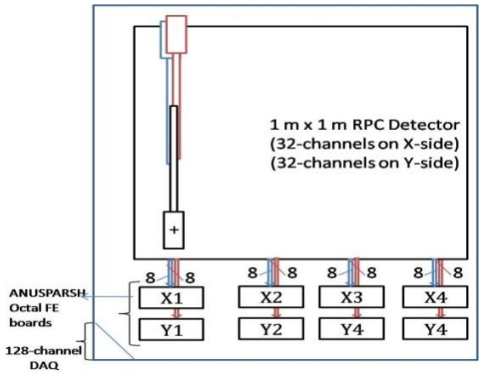

Fig. 2 The experimental setup

The mean (μ) and standard deviation (σ) of the time-of-arrival of the Hits with respect to the trigger of a selected channel of the FEE boards are tabulated in Table 1. The time spectrum of channel-3 of the X1 board is shown in Fig. 3. The standard deviation mentioned in the Table 1 and Fig. 3 includes the contribution of the jitter due to scintillator paddles. The strip rates were stable throughout the experiments.

Table 1: μ and σ of the time measurements with ANUSPARSH FEE boards

parameter / Board(channel)	μ in ns	σ in ns
X1 (3)	106.2	2.45
Y1 (3)	108.1	2.66
X2 (3)	106.0	2.14
Y2 (3)	107.6	2.21

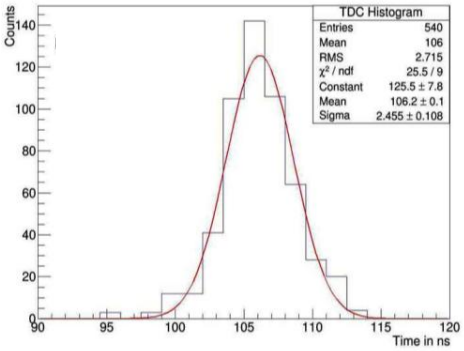

Fig. 3 Time spectrum of channel-3 of X1 board

Conclusion

The TDC is developed in the FPGA of the DAQ system and it is characterized with the RPC detector. The measured values of the standard deviation (σ) are in the range 2.1 ns to 2.7 ns across FEE boards with the RPC.

References

[1] https://arxiv.org/abs/1505.07380
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[3] K. Hari Prasad, V.B. Chandratre, Calibration techniques in ASIC and FPGA based time-to-digital converters, in the proceedings of ICCTA-2021, accepted for publication.