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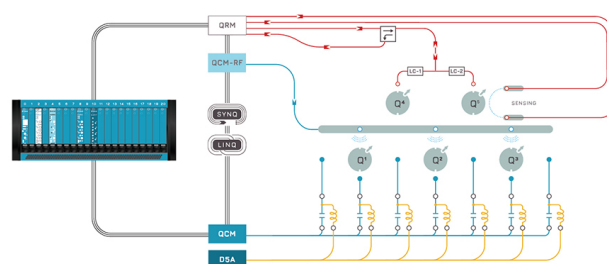


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Analysis and mitigation of interface losses in trenched superconducting coplanar waveguide resonators

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Improving the performance of superconducting qubits and resonators generally results from a combination of materials and fabrication process improvements and design modifications that reduce device sensitivity to residual losses. One instance of this approach is to use trenching into the device substrate in combination with superconductors and dielectrics with low intrinsic losses to improve quality factors and coherence times. Here, we demonstrate titanium nitride coplanar waveguide resonators with mean quality factors exceeding two million and controlled trenching reaching $2.2\ \mu\text{m}$ in the silicon substrate. Additionally, we measure sets of resonators with a range of sizes and trench depths and compare these results with finite-element simulations to demonstrate quantitative agreement with a model of interface dielectric loss. We then apply this analysis to determine the extent to which trenching can improve resonator performance. © 2018 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>). <https://doi.org/10.1063/1.5006888>

Dielectric loss associated with two-level systems (TLSs) at material interfaces is a major contributor limiting coherence times and quality factors in superconducting qubit and resonator devices.^{1–5} In order to mitigate these losses, previous work has employed a combination of improving materials, optimizing fabrication, and modifying designs.^{6–10} Materials and fabrication efforts have focused primarily on lowering the density of TLS defects in bulk materials¹¹ and reducing the presence of TLS-containing dielectrics¹² and chemical residues.¹³ Device geometry and design parameter modifications have in turn been used to reduce device sensitivity to material losses by tailoring the structure's electromagnetic field profile.^{14–16} Together, these advances have yielded qubit T_1 times exceeding $50\ \mu\text{s}$ (Refs. 16–18) and resonator internal quality factors (Q_i) reaching 70 million at single photon-excitation powers.¹⁹

Despite these remarkable accomplishments, developing a complete understanding of interfacial TLS loss mechanisms has remained a challenge. For example, although materials with reduced TLS losses such as titanium nitride (TiN) have been used to realize high Q_i resonators and long T_1 qubits,²⁰ the results often exhibit poor reproducibility in part due to the metal's sensitivity to ambient oxygen.²¹ Additionally, while improvements in T_1 and Q_i have been demonstrated through the use of substrate trenching to reduce interface participation,^{10,22,23} the depth dependence and the degree to which deeper trenching improves device performance remain unclear. Finite-element electromagnetic modeling of dielectric losses can be used to study these effects, but it must be paired with highly controllable and

reproducible fabrication processes to make quantitative comparisons between experiment and simulations.

In this work, we present TiN coplanar waveguide (CPW) resonators with quality factors exceeding two million fabricated using a process capable of controlled trenching in the silicon substrate. To analyze losses in these devices, we perform finite-element electromagnetic simulations of a range of resonator geometries in order to analyze interfacial and substrate dielectric losses. We then demonstrate quantitative agreement between measured CPW resonator Q_i values and a model of interface losses. Furthermore, we use this tool to predict the marginal benefits of deep trenching for reducing losses in superconducting CPW resonators. The agreement supports the accuracy of interface participation ratio-based modeling of device losses and indicates future pathways for reducing loss in superconducting devices.

We study superconducting CPW quarter-wave resonators with a center trace width w ranging from $3\ \mu\text{m}$ to $22\ \mu\text{m}$ and gap g to ground ranging from $1.5\ \mu\text{m}$ to $11\ \mu\text{m}$ [see Fig. 1(a)]. The devices were fabricated using a subtractive etch process on high resistivity 200 mm (001) silicon substrates ($\geq 3500\ \Omega\text{-cm}$). Prior to metal deposition, the substrates were prepared using an RCA clean without any oxide removal step in conjunction with megasonication. Without additional oxide removal steps or buffer layers, we reactively sputtered 150 nm of TiN using a titanium target in the presence of argon and nitrogen gas. We patterned the resonators using optical lithography and then etched the metal and underlying substrate using a combination of BCl_3 and Cl_2 gases. The total etch time was adjusted to control the trench depth (d). We then used an *in situ* oxygen plasma ash followed by an *ex situ* hydroxylamine-based wet strip to remove the remaining photoresist. Figure 1(b) shows a

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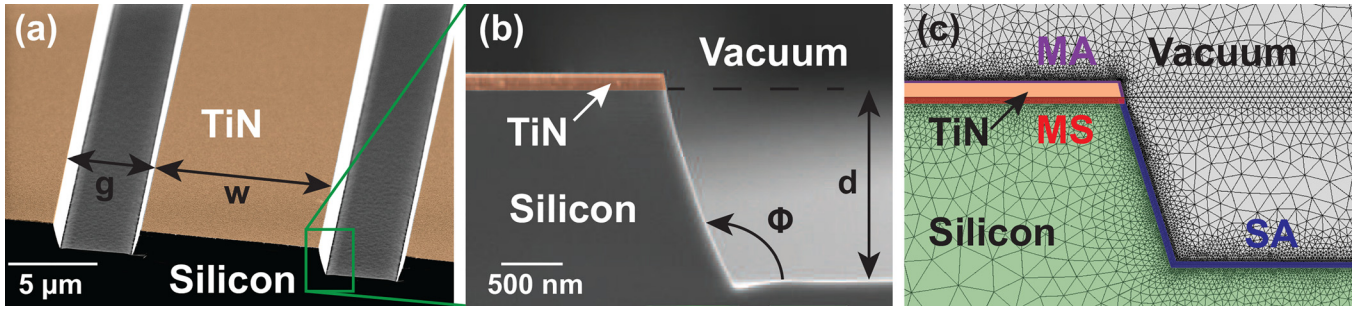


FIG. 1. (a) Scanning electron microscopy (SEM) image of a representative TiN (false-colored orange) resonator with width (w) and gap (g) to ground plane. (b) Cross-sectional SEM image of the same TiN resonator with trench depth (d) and sidewall angle (Φ). (c) 2D finite-element mesh used to calculate participation ratios with the dielectric regions false-colored as follows: the metal-to-substrate interface (MS, red), the substrate-to-air/vacuum interface (SA, blue), the metal-to-air/vacuum interface (MA, purple), and the bulk silicon substrate (Si, green).

representative CPW resonator cross-section. With the sole exception of the variable etch time, we use a nominally identical fabrication process for all samples and therefore attribute differences in Q_i to the trench depth and not to changes in the interfacial loss tangents. Further details of the chip design and fabrication process are provided in the [supplementary material](#).

TLS losses in superconducting CPW resonators can be understood by applying an interface participation ratio model similar to those used in Refs. 7, 9, 10, and 14. In this model, the resonator dielectric losses are a linear combination of the loss tangents ($\tan \delta_i$) associated with energy absorbing TLSs in each region i , weighted by the fraction of the total electric field energy stored in that region, the participation ratio p_i :

$$\frac{1}{Q_{\text{TLS}}} = \sum_i p_i \tan \delta_i. \quad (1)$$

Because each lossy region contains an unknown combination of interface dielectrics and fabrication residues, in our analysis, we assign a unique $\tan \delta_i$ to each interface that is exposed to a distinct fabrication process. The participation ratios of the dielectric regions in our devices were calculated using two-dimensional (2D) COMSOL electrostatic simulations.²⁴ We partition the device into the following lossy dielectric regions: the metal-to-silicon (MS, red), substrate-to-air/vacuum (SA, blue), and metal-to-air/vacuum (MA, purple) interfaces and the bulk silicon substrate (Si, green), as depicted by the false coloring in Fig. 1(c). To reduce the computational complexity, the interface participation ratio calculations were performed using 10 nm thick defect layers of a fixed dielectric constant $\epsilon = 10$, despite general uncertainty in the actual interface properties. This results in ambiguity in the resulting values for $\tan \delta_i$. However, due to the manner in which participation ratios scale with the thickness and dielectric constant in the limit of a thin layer,¹⁴ we can parameterize $1/Q_{\text{TLS}}$ in Eq. (1) using scaled participation ratios P_i and “loss factors” x_i that are independent of these quantities and are defined by $\sum_i p_i \tan \delta_i = \sum_i P_i x_i$. For details, see [supplementary material](#). For all resonator geometries, the trench sidewall angle Φ and depth d were determined using cross-sectional scanning electron microscopy in order to accurately model the device electric field distribution. All devices exhibit angled sidewalls with Φ ranging from 93° to 109° depending on the etch time and feature size.

To compare our interface loss simulations with our fabricated device performance, we characterized a series of resonators with a range of geometries by measuring the resonator chip transmission spectrum at 25 mK in a dilution refrigerator. Background ambient magnetic fields were reduced by mounting the package in a superconducting aluminum enclosure surrounded by a high magnetic permeability shield (Cryoperm). In each cooldown, twelve packages each containing a single chip comprising five resonators were measured using two separate measurement chains that incorporated a pair of 1×6 microwave switches operating at the base temperature stage of the dilution refrigerator. Each measurement chain included a series of microwave attenuators, filters, and isolators to reduce the samples’ exposure to thermal radiation from hotter temperature stages. A broadband traveling wave parametric amplifier,²⁵ a low-noise high-electron-mobility-transistor amplifier, and a room temperature microwave amplifier were used to amplify the transmitted signal before the measurement using a vector network analyzer. Each resonator was measured over a range of internal circulating powers from the single-photon limit up to approximately 10^6 photons using a non-linear frequency spacing to minimize data acquisition times. Resonator parameters were extracted using the fitting methods presented in Ref. 26. Each device was measured repeatedly in the single-photon limit for approximately five hours, and the results were averaged in order to account for time-dependent Q_i fluctuations. Similarly, multiple copies of the same device were measured to account for device-to-device variations and to establish error bars for each sample set.

Figure 2(a) shows an example of the dependence of Q_i on the number of photons circulating in the resonator. The trend shows the typical saturation behavior of internal losses associated with TLSs. At low internal photon numbers (circulating power), Q_i , which we label Q_{LP} , is dominated by absorption due to unsaturated TLSs.³ At higher photon numbers, this loss mechanism saturates and Q_i increases until it reaches another limiting value Q_{HP} . At this power, the losses cease to be dominated by TLSs and are instead dominated by an unknown combination of other mechanisms such as vortices,^{27,28} radiation/packaging loss,⁵ and/or non-equilibrium quasiparticles.²⁹ Q_{LP} and Q_{HP} shown in Fig. 2(a) are typical of our highest mean Q_i fabrication process with mean Q_i of 2.2×10^6 for a sample set of 15 resonators with $(w, g, d) = (16 \mu\text{m}, 8 \mu\text{m}, 0.68 \mu\text{m})$. Further trenching of these devices was not possible

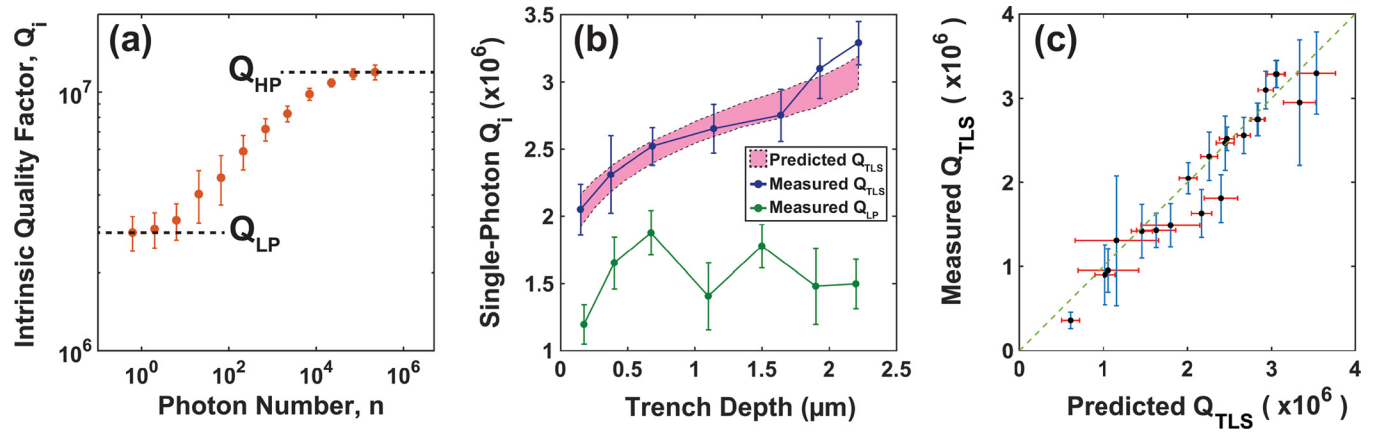


FIG. 2. (a) Representative intrinsic quality factor (Q_i) as a function of photon number for a resonator with $(w, g, d) = (16 \mu\text{m}, 8 \mu\text{m}, 0.68 \mu\text{m})$. The low-power and high-power limits are indicated with dashed lines. (b) Q_i as a function of trench depth with the same CPW geometry as in (a). Each data point represents the mean Q_i obtained from 10 to 15 nominally identical resonators. The green data points represent the low-power quality factor (Q_{LP}), and the blue data points represent the TLS-limited quality factors (Q_{TLS}). The pink shaded region represents the 95% confidence interval of the predicted Q_{TLS} . (c) Predicted Q_i (red error bars) compared to measured Q_{TLS} (blue error bars). The dashed line corresponds to the ideal case where the two values are equal. All error bars represent 95% confidence intervals.

without degrading the etch mask and thinning of the metalization layer. To study the effects of trenching down to a depth of $2.2 \mu\text{m}$, we instead fabricate devices using a process similar to the one used for the device set presented in Fig. 2(a) but with a thicker photoresist mask ($4 \mu\text{m}$ vs. $1.1 \mu\text{m}$) and a higher temperature post-etch ash. This leads to an approximate and reproducible 15% reduction in mean Q_{TLS} for a comparable set of devices with this resonator geometry and trench depth. To assess the reproducibility of this fabrication process, for the shallowest trenching shown here (150 nm), we have measured approximately 100 nominally identical resonators and observed that greater than 87% show Q_i values higher than 1×10^6 (mean of 1.6×10^6).

Although TLSs are generally the dominant source of loss in superconducting CPW resonators at low temperature and circulating power, the losses that persist when TLSs are saturated can still reduce total Q_i and contribute to device-to-device variation. All the resonators we characterized exhibited TLS-saturation behavior similar to the data shown in Fig. 2(a); yet, we observed significant variation in Q_{HP} . As a result, the differences we observed in mean Q_{LP} were sometimes dominated by systematic Q_{HP} variations rather than altered interface participation. This resulted in behavior such as shown in Fig. 2(b) (green points and lines) where no discernible trend in Q_{LP} vs. trench depth is observed. However, we can independently determine Q_{HP} by measuring each resonator at a power that produces an internal electric field large enough to saturate all TLSs, effectively “turning off” the Q_{TLS} contribution to total Q_i . We can then subtract the aggregate loss contribution from these power-independent mechanisms to determine Q_{TLS} from Q_{LP}

$$\frac{1}{Q_{TLS}} = \frac{1}{Q_{LP}} - \frac{1}{Q_{HP}}. \quad (2)$$

The blue points and lines in Fig. 2(b) show the Q_{TLS} values determined from the Q_{LP} values (green points and lines) vs. trench depth when this correction is performed independently for each device in the set that generates each mean Q_i value. This set of values exhibits the expected monotonic

improvement in Q_i as interface participation ratios decrease with increasing trench depths. The need for this correction results from the fact that although the devices were limited by TLS losses at low excitation power, these losses were low enough to be comparable to losses associated with background, power-dependent mechanisms. Separating out the contribution from these high-power mechanisms allows us to probe TLS losses in high Q_i devices despite this variability. See [supplementary material](#) for further data and analysis of this process. The error bars represent 95% confidence intervals resulting from measuring 10–15 nominally identical devices for each depth.

In order to develop a quantitative model of interface losses in our devices, we additionally characterized a series of resonator geometries ranging from $(w, g) = (3 \mu\text{m}, 1.5 \mu\text{m})$ to $(w, g) = (22 \mu\text{m}, 11 \mu\text{m})$ for trench depths between $0.15 \mu\text{m}$ and $2.2 \mu\text{m}$. Each geometry in this dataset provides a linear equation of the form of Eq. (1) relating device Q_{TLS} to loss factors associated with each dielectric region. While a single relationship is insufficient to determine each region’s losses, multiple geometries with varying combinations of participation ratios form a set of linear equations that can in principle be used to determine each individual loss factor. However, in general, this matrix of participation ratios is very nearly singular for a wide range of planar geometries. This collinearity is readily apparent in the approximate proportionality of the MS and SA interface participation ratios at all depths shown in Fig. 3. As a result, errors associated with the input Q_{TLS} values and modeling inaccuracy prevent the determination of a unique solution to the system of equations.³⁰ Nevertheless, we can perform a Monte Carlo analysis of the constrained least square optimization solution using our measured Q_{TLS} values and error bars in order to determine a corresponding distribution of loss factors for the dielectric regions. For comparisons to previously reported loss tangents, see [supplementary material](#). A comparison between the measured Q_{TLS} and Q_{TLS} values predicted by this model is shown in Fig. 2(c) with the corresponding error bars for the 19 device geometries that we measured. The dashed green line represents the values where

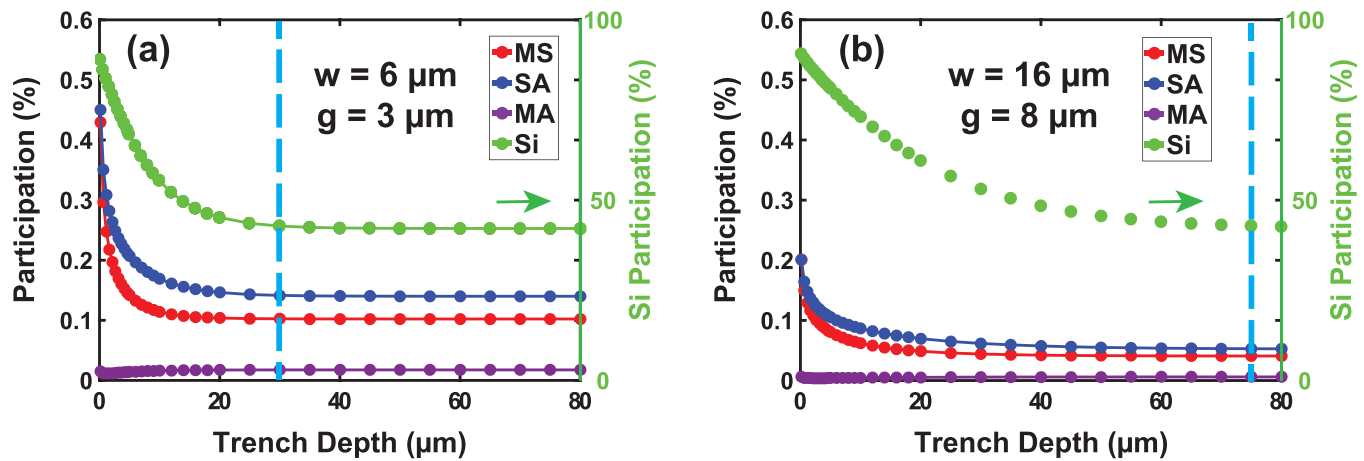


FIG. 3. Participation ratios as a function of trench depth for two representative resonator geometries (a) $(w, g) = (6 \mu\text{m}, 3 \mu\text{m})$ and (b) $(w, g) = (16 \mu\text{m}, 8 \mu\text{m})$. MS (red), SA (blue), and MA (purple) participation ratios are plotted on the left axis, and the Si participation ratio (green) is plotted on the right axis.

the measured and predicted Q_{TLS} correspond exactly. The qualitative agreement between the measured and predicted Q_{TLS} indicates that the range of dielectric losses encompassing this model accurately describes our devices. Furthermore, this indicates that this model can also be used to determine predictive bounds for resonator Q_{TLS} for devices with similar sets of participation ratios (i.e., planar devices with anisotropic trenching). The region of 95% confidence in this prediction is shown in Fig. 2(b) for $(w, g) = (16 \mu\text{m}, 8 \mu\text{m})$ devices (pink shaded region) over the range of trench depths we studied. The predicted Q_{TLS} values agree well with the measured trend, indicating that the interface losses are likely uniform between resonators with different trench depths.

To determine the extent to which Q_{TLS} can be improved with the increasing trench depth, we simulate the interface participation ratios for depths comparable to those achievable through deep silicon etching²³ for multiple geometries and assuming perpendicular sidewall angles ($\Phi = 90^\circ$). Figures 3(a) and 3(b) show MS (red), SA (blue), MA (purple), and Si (green) participation ratios for two representative coplanar resonator geometries $(w, g) = (6 \mu\text{m}, 3 \mu\text{m})$ and $(16 \mu\text{m}, 8 \mu\text{m})$ as a function of trench depth from $d = 0.15 \mu\text{m}$ to $d = 80 \mu\text{m}$. The interface participation decreases with the trench depth, and it asymptotes beyond a depth that is dependent on the CPW gap. The blue dashed line indicates the depth at which the total bulk and interface participation reaches within 1% of the asymptotic value. In general, we observe that trenching beyond a depth of approximately $d = 10g$ ceases to further reduce the participation ratios in the device interfaces or the silicon substrate. This asymptotic behavior can be contrasted with the logarithmic dependence at $1\text{--}10 \mu\text{m}$ depths simulated in Ref. 10.

In summary, we have demonstrated trenched TiN resonators with a mean Q_i of 2.2 million. Characterization of sets of devices with a range of CPW dimensions and trench depths has enabled us to produce a model of dielectric losses that quantitatively agrees with our measured Q_i values and can be used to predict device performance within the bounds set by the model uncertainty. Furthermore, we have used this form of participation ratio-based device modeling to predict the extent to which deep trenching can improve dielectric losses in superconducting CPW resonators. Altogether, these

results indicate that trenching significantly reduces aggregate interface dielectric losses in superconducting CPW resonators and that significant further improvements in total Q_i are possible by mitigating loss contributions from non-TLS related sources. Additionally, it may be possible to combine the analysis method we use to model dielectric losses in our system with more drastic geometry changes in order to more accurately determine interface losses as a tool for process qualification and device improvement. Both approaches would provide essential information for reducing dielectric losses in superconducting quantum devices.

See [supplementary material](#) for the details of fabrication methods, experimental hardware, power-independent loss subtraction, and participation ratio-based loss calculations and analysis.

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