



# Noise properties in the Coulomb blockade region of FinFETs

Tetsufumi Tanamoto<sup>1\*</sup>, Keiji Ono<sup>2</sup>, Jun Deguchi<sup>3</sup>, Junji Wadatsumi<sup>3</sup>, and Ryuichi Fujimoto<sup>3</sup>

<sup>1</sup>Department of Information and Electronic Engineering, Teikyo University, 1-1, Toyosatodai, UtSunomiya, Tochigi 320-8551, Japan

<sup>2</sup>Advanced Device Laboratory, RIKEN, Wako-shi, Saitama 351-0198, Japan

<sup>3</sup>Kioxia Corporation, 2-5-1 Kasama, Sakae-ku, Yokohama-shi, Kanagawa 247-8585, Japan

\*E-mail: [tanamoto@ics.teikyo-u.co.jp](mailto:tanamoto@ics.teikyo-u.co.jp)

Received October 6, 2023; revised January 23, 2024; accepted February 8, 2024; published online March 5, 2024

Fin FETs (FinFETs) are a promising candidate for the platform of Si quantum computers. The noise properties of commercial FinFETs were experimentally investigated at temperatures below 10 K. The drain current showed Coulomb oscillation, indicating that the FinFET channel became a single quantum dot. Moreover, the noise in the drain current was analyzed, and the basic properties of commercial FinFETs in the low-temperature region were discussed. © 2024 The Author(s). Published on behalf of The Japan Society of Applied Physics by IOP Publishing Ltd

## 1. Introduction

Silicon quantum computers are among the most important fields in physics and engineering.<sup>1,2)</sup> Silicon qubits are desirable for integration using accumulated technologies for silicon transistors and large integrated circuits. In general, qubits use electron (or hole) spins confined in a quantum dot (QD) structure. Silicon quantum computers using cutting-edge CMOS technology are attracting attention. At present, experiments of qubits are controlled by a lot of high-performance equipment outside a chip. The equipment will be integrated into a single chip including qubits in the future. Fin FETs (FinFETs) are the most widely used transistors in several consumer electronics, such as smartphones. Thus, by employing FinFETs as a component of spin qubits, in addition to control circuits, the development cost of silicon quantum computers can be reduced, making them a promising platform for spin qubits.<sup>3,4)</sup>

Several spin qubits are proposed based on the fin structure. The Intel group fabricated spin qubits using the fin structure to form and control QDs in the substrate.<sup>4)</sup> Lansbergen et al. proved that holes at the corners of fin channel between the source and drain can be used as electrically induced qubits.<sup>5)</sup> We also proposed a qubit based on FinFETs in which QDs are inserted between the fin structures of the conventional FinFET.<sup>6,7)</sup> Because spin qubits operate at low temperatures, the electronic properties of the conventional FinFETs in the low-temperature region should be further investigated.

In general, the width of the fin structure is small below 30 nm. Then, some quantum effects are expected to emerge in the transport properties of the conventional FinFET itself in low temperature region. Sellier et al. demonstrated that Coulomb oscillations can be observed in fin-like devices in the low-temperature region.<sup>8)</sup> However, whether Coulomb oscillations can be observed in even conventional FinFETs remains unknown. Moreover, investigating the noise characteristics of the FinFET itself is necessary because spin qubits are vulnerable to charge fluctuations in devices.<sup>9)</sup> Currently, various noises are observed in conventional transistors.<sup>10–18)</sup> To correctly control spin qubits, the magnitude of the noise in FinFETs should be estimated.

In this study, we experimentally investigated the transport properties of a commercial p-type FinFET, focusing on the

noise characteristics in the low-temperature region.<sup>19)</sup> The time-dependent noise characteristics were analyzed and compared using a simple simulation. It was demonstrated that the conventional FinFET exhibited a clear Coulomb blockade (CB) and could be treated as a QD in the low-temperature region. More importantly, the amplitude of the noise was small compared to the Coulomb oscillations. In Ref. 19, we have shown basic results of our experiments. In this study, we have extended the experiments and newly added Figs. 6 and 7.

The remainder of this paper is organized as follows. The experimental methods and results are presented in Sects. 2 and 3, respectively. Section 4 involves a statistical analysis of the experimental results, and Sect. 5 presents the simulations conducted to explain these results. In Sect. 6, we discuss the results, and finally, Sect. 7 summarizes and concludes the study.

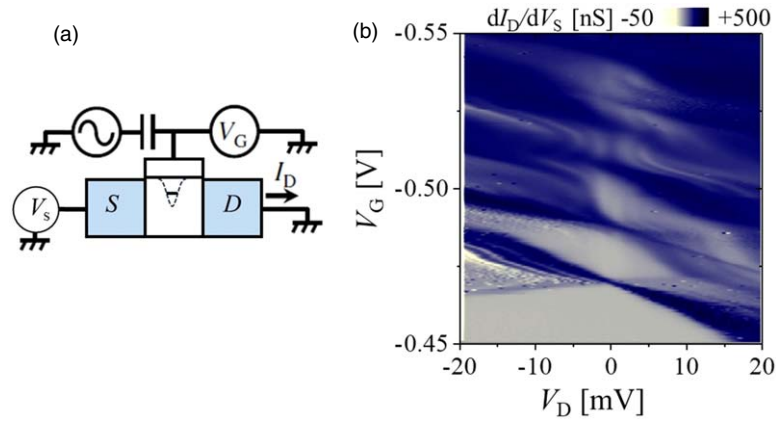
## 2. Experimental methods

We used a commercial, factory-manufactured p-type FinFET with a gate length and width of less than 100 nm. Note that there is no additional designated qubit structure. The detailed size and fabrication process are confidential owing to a contractual agreement. The device was diced into approximately 3 mm squares, mounted on a ceramic package, and subsequently wired through wire bonding. The package was cooled to a minimum temperature of 1.5 K in a helium-4 refrigerator. A DC magnetic field was applied using a superconducting electromagnet. Figure 1(a) shows a schematic diagram of the measurement. A source voltage  $V_S$  and a gate voltage  $V_G$  were applied to the device, and the drain current  $I_D$  was measured. An analog current amplifier was used for current measurement, and its time constant was 0.3 s. This time constant determines the time resolution of the noise measurement, which is described later. The Coulomb oscillation is observed in this system and we consider that the Coulomb oscillation comes from some QD in the channel region abstractly drawn in Fig. 1(a).

## 3. Single-electron tunneling in FinFETs

Figure 1(b) shows the color intensity plot of the differential conductance  $dI_D/dV_S$  as a function of  $V_S$  and  $V_G$ . This plot



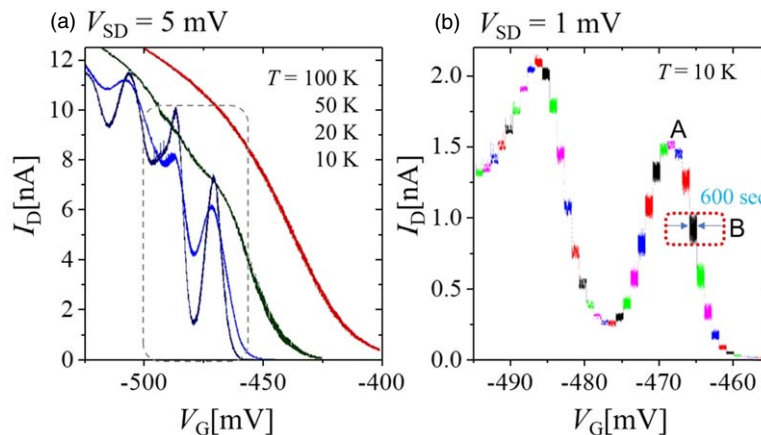


**Fig. 1.** (a) Schematic diagram of the FinFET and measurement setup. It is considered that a QD structure is formed in the channel. (b) Color intensity plot of differential conductance  $dI_D/dV_S$ , measured at  $T = 1.5$  K, showing Coulomb diamonds.

shows the so-called Coulomb diamond structure, a characteristic diamond-shaped region where  $I_D$  is suppressed owing to the CB. The largest lateral size ( $\sim 20$  mV) of the diamond-shaped region indicates the additional energy (single electron charging energy + discrete energy due to quantum confinement) of approximately 20 meV for the first hole in the “QD.” The total self-capacitance of the QD can be estimated from  $C = e/\Delta V_G = 8.02$  aF, with  $e = 1.602 \times 10^{-19}$  and  $\Delta V_G = 20$  mV. This total capacitance includes the capacitances of the channel with the source ( $C_{s0}$ ), drain ( $C_{d0}$ ), gate ( $C_{g0}$ ) and other part of the device. In general, the ratio of  $C_{s0}$ ,  $C_{d0}$  and  $C_{g0}$  can be roughly estimated from the Coulomb diamond structure. However, the shape of the observed diamond [Fig. 1(b)] is blurred, and it is difficult to estimate the ratios between capacitances from this diamond. Thus, we simply take  $C_{s0}$ ,  $C_{d0}$ , and  $C_{g0}$  as 8 aF divided by three. In Sect. 5, we apply each capacitance 2 aF for simplicity.

Figure 2(a) shows the  $I_D$ - $V_G$  characteristics of the FinFET measured at various temperatures.  $I_D$  oscillates as a function of  $V_G$ , which is a clear characteristic of the so-called Coulomb oscillation, in which the CB is periodically lifted owing to a one-by-one increase in the number of holes in QD. The Coulomb oscillation can be observed at lower temperatures ( $< 20$  K). A slight oscillation is still visible even at 50 K. This is consistent with the observed additional energy of approximately 20 meV from the Coulomb diamond measurement.

In our FinFET device, there was no intentionally fabricated QD structure. The formation of a QD structure was discussed by Sellier et al. in their fin-like devices,<sup>8)</sup> in which a nanowire-like n-type mesa channel of the FET was partially covered by a narrow overlapping gate electrode, and both sides of the gate were supported by spacers. By increasing  $V_G$ , the barrier height in the source-channel-drain potential diagram was decreased and eventually became sufficiently low, at which the FET is in the ON state. For a  $V_G$  slightly below the threshold, the potential underneath the gate was sufficiently low; however, the potential underneath the spacer region remains high, thereby forming a double barrier structure (i.e. a QD structure between the double barriers) in the channel. Thus, the device can be treated as a single QD in low-temperature and low- $V_D$  regions. In general, there is no double barrier structure in the channel region of the conventional transistors. However, the low temperature behaviors are different from those at RT region. We have observed similar Coulomb oscillations in other sample. Therefore, it is reasonable to assume that the hole QD is formed in the channel of our FinFET device for  $V_G$ 's slightly below the threshold at low temperature region. The formation of a QD or a single dopant has been discussed for MOSFETs in the presence of potential fluctuations in the channel.<sup>20–24)</sup> Thus, it is natural to consider that the QD structure of our FinFET also originates from dopants or unexpected trap sites around the oxide interface.<sup>25)</sup> For a basic transistor in the



**Fig. 2.** (a) Temperature dependence of  $I_D$ - $V_G$ . (b) Time dependence of  $I_D$  where the gate voltage is swept (from  $-495$  to  $-455$  mV) at 1 mV steps for 600 s in each step, showing noise amplitudes for each  $V_G$ s. The color is used to observe the different voltage region clearly.

ballistic region, a barrier was formed between the source and the channel, as discussed in Ref. 26. This might be also the origin of the QD structure at low temperature regions. The extensive investigations are near-future issues.

#### 4. Current noise in single-electron regime

The noise properties were investigated by measuring  $I_D$ . Figure 2(b) shows the amplitude of  $I_D$  noise for fixed  $V_G$ s; the measurement details are provided in the caption. The two peaks correspond to the Coulomb oscillations, as indicated by the gray dashed box in Fig. 2(a). The typical amplitude of noise is on the order of 0.1 nA depending on  $V_G$ s. When CB is used to manipulate spin qubits, the magnitude of the Coulomb oscillation can serve as a guideline signal for qubit manipulation. Thus, the considerably smaller amplitude of noise compared to the Coulomb oscillation, as presented here, makes the FinFET a preferable device platform for spin qubits.

Figures 3 and 4 show the time dependence of  $I_D$ s at points A and B in Fig. 2(b) ( $V_G = -468$  and  $-466$  mV) and the corresponding histograms of  $I_D$ . The noise at the middle point (B) in Fig. 4 is larger than that at the peak point (A) in Fig. 3. This means that the electron sensitivity increases at the middle points of the Coulomb oscillation, resulting in larger noise. At each point, at a lower temperature ( $T = 8$  K), a clearer multilevel telegraph noise structure can be observed. Compared with conventional “two-level” telegraph noise,<sup>6)</sup> many levels can be observed.

Figure 5 shows the distribution of the color intensity plot of the  $I_D$  histograms, such as those in Figs. 3(b) and 3(d) and Figs. 4(b) and 4(d), as a function of  $V_G$ , which corresponds to the lateral axis in Fig. 2(b). When we compare Fig. 5(b) with Fig. 5(a), we can see that dots (measured currents) are separately distributed. These separations indicate multiple peaks. As previously mentioned, a single peak in the histograms at  $T = 10$  K [Fig. 5(a)] exhibit multiple peaks at  $T = 8$  K [Fig. 5(b)]. A comparison with Fig. 2(b) shows that  $\Delta I_D$  becomes wider when the electron sensitivity increases, such as at point B.

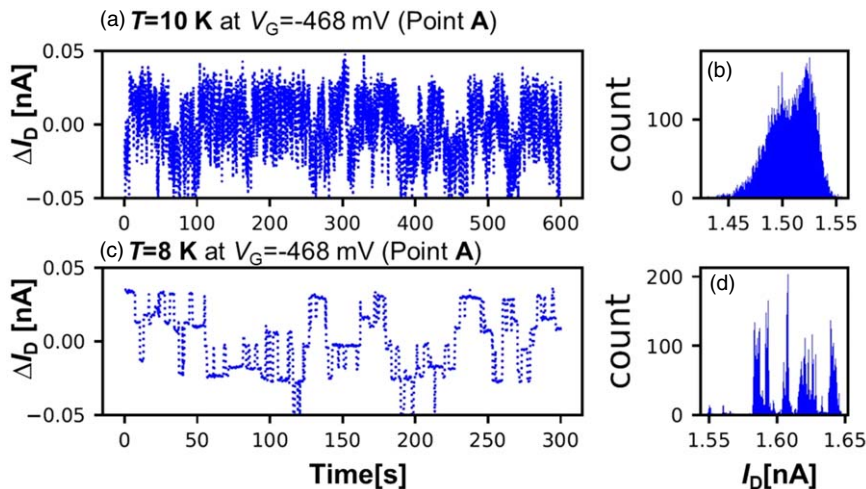
Current noise in the single-electron region is known to result from background charge fluctuations.<sup>27)</sup> The background charge is due to the charge transfer between the QD and the

unintentionally introduced trap sites near the QD or that between multiple trap sites. The series of measurements and analyzes (Figs. 3–5) contain information on the number of trap sites and the frequency of charge transfer that cannot be obtained from the noise amplitude measurement [Fig. 2(b)] alone. For example, in Fig. 4(d), the histogram has approximately eight peaks. This can be interpreted as the existence of approximately eight configurations of background charges and the transitions between these configurations. As this transition becomes more frequent at higher temperatures, the noise changes from multilevel telegraph noise close to Gaussian type noise.

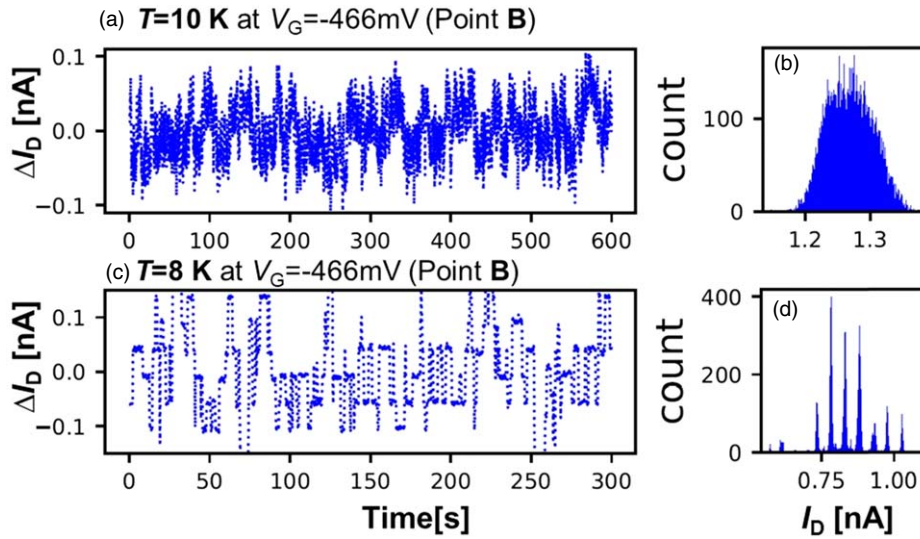
The transitions of the histogram peaks for different  $V_G$  values are shown in Figs. 6 and 7. Figure 6 shows the changes in the trap peaks around point B. The figure shows that the noise distribution changes according to the change in  $V_G$  on the order of mV. Figure 7 shows the noise characteristics at approximately  $V_G = -478$  mV (red arrow in Fig. 5), which represents the lowest swing when compared with points A and B. The red arrow corresponds to the central bottom of the Coulomb oscillation of Fig. 2(b). In contrast to the peak of the Coulomb oscillation where the number of electron change and the noise becomes larger, at the bottom of the Coulomb oscillation the number of the electrons does not change. Therefore, at the bottom of the Coulomb oscillation (red arrow), smallest noise is expected. The number of peaks, which correspond to the number of background charges, varies between 11 and 16. Even in this low-noise region, the noise characteristics change with variations in  $V_G$  on the order of mV. Thus, the noise properties are sensitive to changes in  $V_G$ . Although the noise distribution is sensitive to  $V_G$ , similar distributions were observed during the repeated measurements. Thus, the noise distribution can be used as a physically unclonable function, as discussed in Ref. 28.

#### 5. Simulation

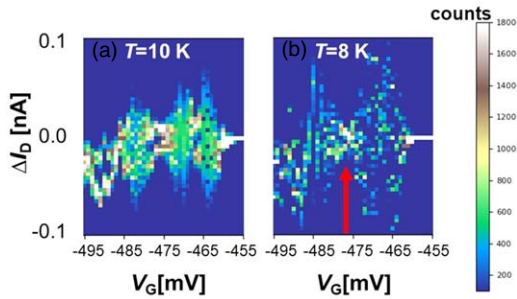
As mentioned previously, the magnitude of the current fluctuation  $\Delta I_D$  changes depending on the position of the Coulomb oscillations, as shown in Fig. 2. In this section, the origin of the current fluctuation in the CB phenomena is analyzed by introducing randomness to a previously reported analytical formula.<sup>29)</sup> Two types of fluctuations (capacitance



**Fig. 3.** (a) and (c) Current noise and (b) and (d) histogram of current for point A in Fig. 2(b). (a) and (b)  $T = 10$  K. (c) and (d)  $T = 8$  K. In (a) and (b), the center of the current is adjusted to 0.



**Fig. 4.** (a) and (c) Current noise and (b) and (d) histogram of current for the point B in Fig. 2(b). (a) and (b)  $T = 10$  K. (c) and (d)  $T = 8$  K. In (a) and (b), the center of the current is adjusted to 0.



**Fig. 5.** Noise current variation as a function of the entire  $V_G$  region, with  $V_G$  changing by 1 mV over 600 s. The center is set at the middle of  $\Delta I_D$ . (a)  $T = 10$  K and (b)  $T = 8$  K. The red arrow indicates the smallest amplitude of noise, which is further discussed in Fig. 7.

random number is added to  $V_D$ , which is given by

$$V_D = V_{D0}(1 + \text{rnd1}), \quad (1)$$

where  $V_{D0} = 1$  mV, and  $\text{rnd1}$  is the random number of  $-0.01 < \text{rnd1} < 0.01$ . The variation in the current induced by the noise appears around the peaks of the Coulomb oscillations. Figure 8(b) shows the  $I_D$ - $V_G$  characteristics, in which a random number is added to the capacitances of the source ( $C_s$ ), drain ( $C_d$ ), and gate ( $C_g$ ) as follows:

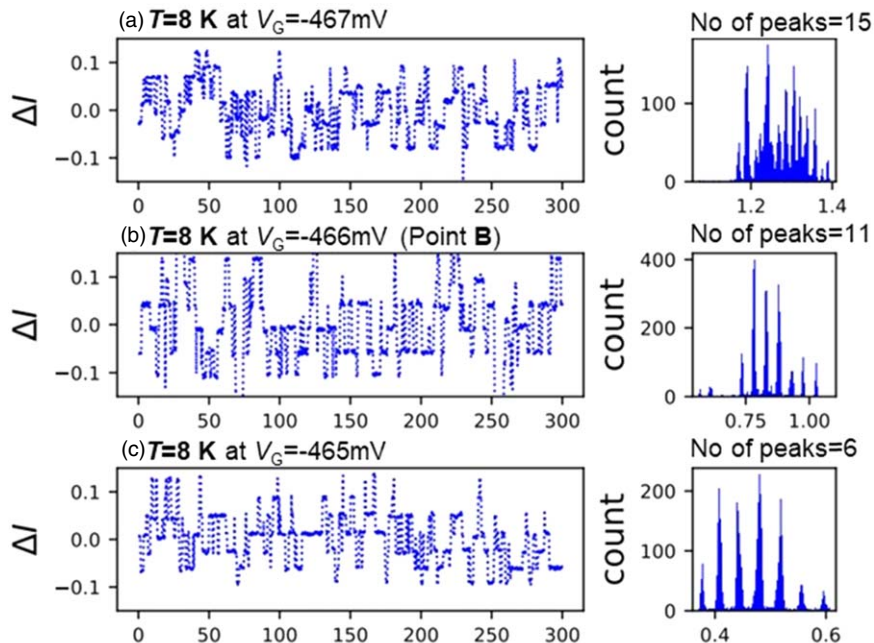
$$C_s = C_{s0}(1 + \text{rnd2}), \quad (2)$$

$$C_d = C_{d0}(1 + \text{rnd3}), \quad (3)$$

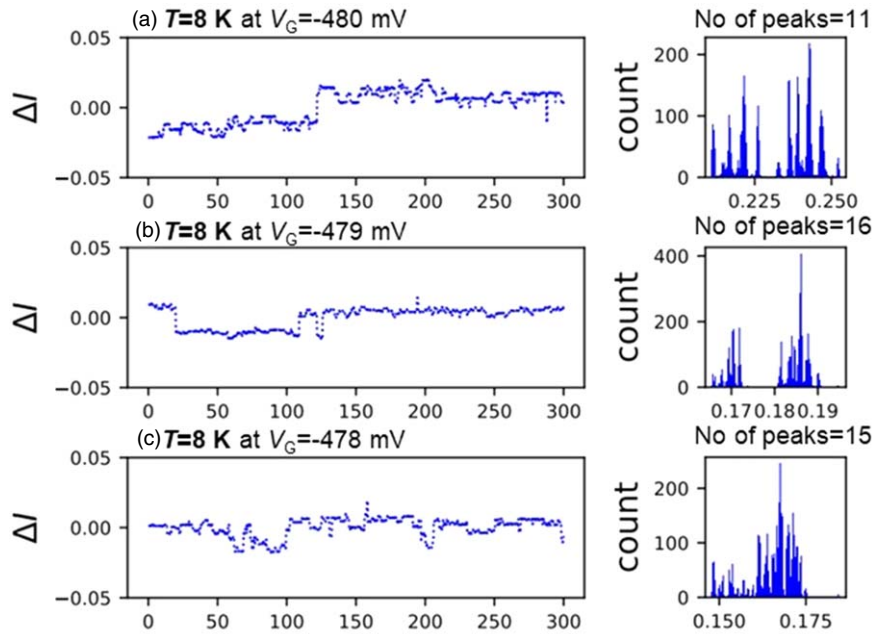
$$C_g = C_{g0}(1 + \text{rnd4}), \quad (4)$$

and drain voltage fluctuations) are investigated using random numbers. Figure 8(a) shows the  $I_D$ - $V_G$  characteristics when a

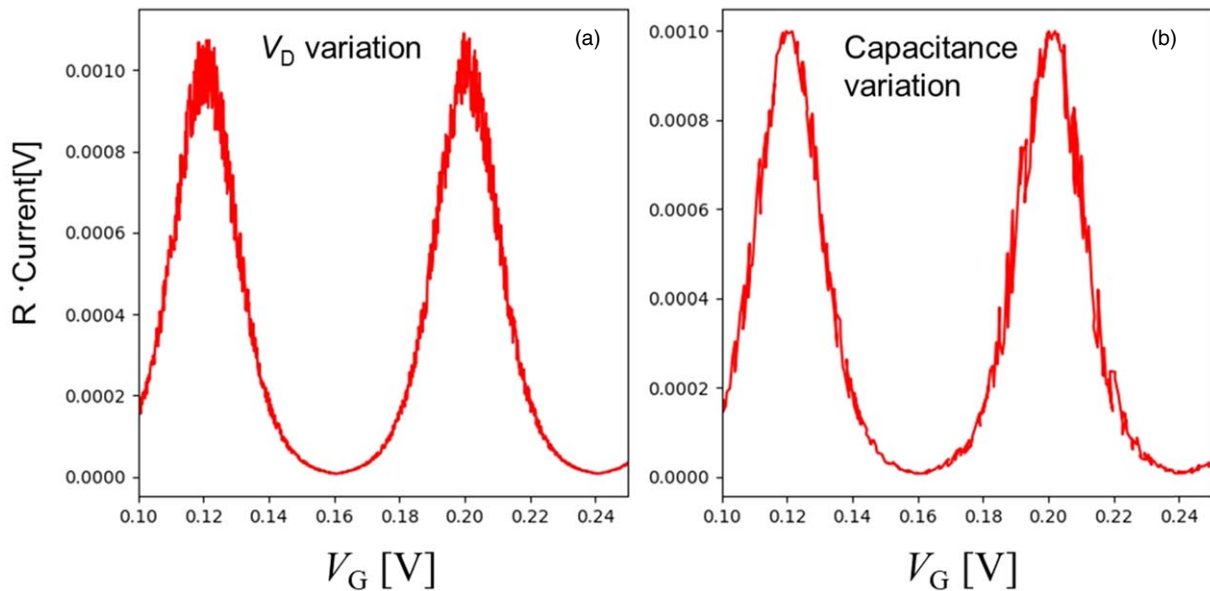
where  $C_{s0} = C_{d0} = C_{g0} = 2a$  F, and  $\text{rnd2}$ ,  $\text{rnd3}$ , and  $\text{rnd4}$  represent the random numbers such that  $-0.01 < \text{rnd2}, \text{rnd3},$



**Fig. 6.** Transition of the noise current around point B at  $T = 8$  K. (a)  $V_G = -467$  mV, (b)  $V_G = -466$  mV, and (c)  $V_G = -465$  mV.



**Fig. 7.** Transition of the noise current around  $V_G = -479$  mV at  $T = 8$  K. (a)  $V_G = -480$  mV, (b)  $V_G = -479$  mV, and (c)  $V_G = -478$  mV.



**Fig. 8.** Analysis of current based on previous work.<sup>7)</sup> (a) Random fluctuation is added to  $V_{ds}(1 + \text{rnd})$ . (b) Random fluctuations are added to  $C_i(1 + \text{rnd})$  ( $i = s, d, g$ ), where  $\text{rnd}$  changes around 1% ( $-0.01 < \text{rnd} < 0.01$ ).

$\text{rnd} < 0.01$ . The largest variation in the current occurs in the middle of the Coulomb oscillations. Thus, depending on the variations in the parameters, the current is affected at different points in the Coulomb oscillation. Figure 2 shows a more pronounced noise oscillation in the middle of the Coulomb oscillation, which originates from charge fluctuations due to the capacitance couplings. As discussed in the previous section, the noise distributions are sensitive to  $V_G$ , and the present simulations prove that noise is particularly sensitive to the electric field associated with the capacitances between the QD and the electrodes.

## 6. Discussions

In the current experiments, the noise changes as the gate voltage changes. Thus, the lifetimes of the trap and detrap are

considered to be relatively short in the present measurement timescale (300–600 s per  $V_G$ ). If the measurement time is shorter than the lifetime, such that the telegraph peaks do not change, a new computing method such as reservoir computing might be possible;<sup>30)</sup> this topic is a subject for future research.

In spin qubits, the spin direction is controlled by a large static magnetic field and an oscillating magnetic field perpendicular to the static magnetic field. The effect of the magnetic field on noise was also investigated. Although the figures are not presented here, the noise properties were measured under varying magnetic field conditions from  $-10$  to  $10$  mT, and no significant effect of the magnetic field on the current noise was observed such as shown in Ref. 24. Magnetic fields do not have a prominent effect on the spin states of the trap sites.

A side-QD structure is realized when QDs are inserted between the fins of FinFETs,<sup>6)</sup> and the channel of the FinFET can be treated as a QD, as shown above. In this case, the energy levels of the side QDs can potentially be measured using a FinFET.<sup>31,32)</sup> Further investigations will be necessary in the future.

In general, the threshold voltage of FinFETs shifts when the operation temperature changes.<sup>25)</sup> However, the position of the Coulomb peaks does not change as shown in Fig. 2. We would like to investigate the detailed relationship between the FinFET and the noise of the CB in the near-future.

## 7. Conclusions

An experimental investigation of the noise properties of a FinFET as a platform for spin qubits has been reported. The low-temperature region of a commercial FinFET exhibits Coulomb oscillation, which indicates that the channel part becomes a QD. Compared to the amplitude of the Coulomb oscillations, the amplitude of the noise fluctuations was extremely small. This indicates that the longitudinal relaxation rate  $T_1$  of commercial FinFETs is expected to be small. The measurement of the transverse relaxation rate  $T_2$  is a future issue when the qubit structure is constructed. At present, it can be said that commercial FinFETs are suitable for spin qubits, in which minimizing noise is crucial owing to their sensitivity. The noise signals show multiple trap levels with weak magnetic field dependence. Although it is possible that the addition of spin-qubit structure to the conventional FinFET changes the noise characteristics, it can be said that FinFETs are suitable platforms for spin qubits.

## Acknowledgments

TT acknowledges S. Takagi for fruitful discussions.

## ORCID iDs

Tetsufumi Tanamoto  <https://orcid.org/0000-0002-1373-2812>

- 1) A. Noiri, K. Takeda, T. Nakajima, T. Kobayashi, A. Sammak, G. Scappucci, and S. Tarucha, *Nature* **601**, 338 (2022).
- 2) S. G. J. Philips et al., *Nature* **609**, 919 (2022).

- 3) A. Fuhrer et al., 2022 Int. Electron Devices Meeting (IEDM) (San Francisco, CA, USA), 2022, p. 14.1.1.
- 4) R. Kotlyar et al., 2022 Int. Electron Devices Meeting (IEDM) (San Francisco, CA, USA), 2022, p. 8.4.1.
- 5) G. P. Lansbergen, R. Rahman, C. J. Wellard, I. Woo, J. Caro, N. Collaert, S. Biesemans, G. Klimeck, L. C. L. Hollenberg, and S. Rogge, *Nat. Phys.* **4**, 656 (2008).
- 6) T. Tanamoto and K. Ono, *AIP Adv.* **11**, 045004 (2021).
- 7) E. A. Pérez-Rodríguez, M. T. Orvañanos-Guerrero, and T. Tanamoto, *Jpn. J. Appl. Phys.* **62**, SC1065 (2023).
- 8) H. Sellier, G. P. Lansbergen, J. Caro, S. Rogge, N. Collaert, I. Ferain, M. Jurczak, and S. Biesemans, *Phys. Rev. Lett.* **97**, 206805 (2006).
- 9) T. Nakajima et al., *Phys. Rev. X* **10**, 011060 (2020).
- 10) D. Bauza, *IEEE Electron Device Lett.* **23**, 658 (2002).
- 11) M. G. Peters, J. I. Dijkhuis, and L. W. Molenkamp, *J. Appl. Phys.* **86**, 1523 (1999).
- 12) H. Oka, T. Matsukawa, K. Kato, S. Iizuka, W. Mizubayashi, K. Endo, T. Yasuda, and T. Mori, 2020 IEEE Symp. on VLSI Technology (Honolulu, HI, USA), 2020, p. 1.
- 13) M.-S. Kang, K. Sumita, H. Oka, T. Mori, K. Toprasertpong, M. Takenaka, and S. Takagi, *Jpn. J. Appl. Phys.* **62**, SC1062 (2023).
- 14) B. Paz, M. Casse, C. Theodorou, G. Ghibardo, T. Kammler, L. Pirro, M. Vinet, S. Franceschi, T. Meunier, and F. Gaillard, *IEEE Trans. Electron Devices* **67**, 4563 (2020).
- 15) A. Beckers, F. Jazaeri, A. Grill, S. Narasimhamoorthy, B. Parvais, and C. Enz, *IEEE J. Electron Devices Soc.* **8**, 780 (2020).
- 16) S. Sekiguchi, M.-J. Ahn, T. Saraya, M. Kobayashi, and T. Hiramoto, 2021 5th IEEE Electron Devices Technology & Manufacturing Conf. (EDTM) (Chengdu, China), 2021, p. 1.
- 17) J. Chen, T. Tanamoto, H. Noguchi, and Y. Mitani, 2015 Symp. on VLSI Technology (VLSI Technology) (Kyoto, Japan), 2015, p. T40.
- 18) Y. F. Lim et al., *IEEE Electron Device Lett.* **27**, 765 (2006).
- 19) T. Tanamoto, K. Ono, J. Deguchi, J. Wadatsumi, and R. Fujimoto, 2023 Int. Conf. Solid-state Devices and Materials (SSDM23), 2023, PS-9-08.
- 20) K. Y. Tan et al., *Nano Lett.* **10**, 11 (2010).
- 21) M. Pierre, R. Wacquez, X. Jehl, M. Sanquer, M. Vinet, and O. Cueto, *Nat. Nanotechnol.* **5**, 133 (2010).
- 22) K. Ono, T. Tanamoto, and T. Ohguro, *Appl. Phys. Lett.* **103**, 183107 (2013).
- 23) M. F. Gonzalez-Zalba, A. Saraiva, M. J. Calderón, D. Heiss, B. Koiller, and A. J. Ferguson, *Nano Lett.* **14**, 5672 (2014).
- 24) K. Ono, G. Giavaras, T. Tanamoto, T. Ohguro, X. Hu, and F. Nori, *Phys. Rev. Lett.* **119**, 156802 (2017).
- 25) X.-R. Yu et al., 2023 Int. Electron Devices Meeting (IEDM) (San Francisco, CA, USA), 2023, p. 2.
- 26) K. Natori, *J. Appl. Phys.* **76**, 4879 (1994).
- 27) A. B. Zorin, F.-J. Ahlers, J. Niemeyer, T. Weimann, H. Wolf, V. A. Krupenin, and S. V. Lotkhov, *Phys. Rev. B* **53**, 13682 (1996).
- 28) T. Tanamoto, Y. Nishi, and K. Ono, *Appl. Phys. Lett.* **115**, 033504 (2019).
- 29) K. Uchida, K. Matsuzawa, J. Koga, R. Ohba, S. Takagi, and A. Toriumi, *Jpn. J. Appl. Phys.* **39**, 2321 (2000).
- 30) H. Jaeger, B. Noheda, and W. G. van der Wiel, *Nat. Commun.* **14**, 4911 (2023).
- 31) T. Tanamoto and T. Aono, *Phys. Rev. B* **106**, 125401 (2022).
- 32) T. Tanamoto and K. Ono, *J. Appl. Phys.* **134**, 214402 (2023).