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A 4-channel waveform sampling ASIC in 0.13 μm CMOS for front-end readout of large-area micro-channel plate detectors

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Abstract

We describe here the development of PSEC-3, a custom integrated circuit designed in the IBM-8RF 0.13 μm CMOS process and intended for fast, low-power waveform sampling. As part of the Large-Area Picosecond Photo-Detector (LAPPD) collaboration, this chip has been designed as a prototype application-specific integrated circuit (ASIC) for the front-end transmission line readout of large-area micro-channel plate photomultiplier tubes (MCP-PMTs). With 4 channels, PSEC-3 has a buffer depth of 256 samples on each channel, a chip-parallel ramp-compare ADC, and a serial data readout that includes the capability for region-of-interest windowing to reduce dead time. Chip calibrations and performance results, including achieved sampling rates of 2.5-17 GSa/s, are reported. Some design issues are identified, in particular the dependence of analog bandwidth on location in the sampling array. The causes have been found and addressed in a subsequent PSEC-4 submission.

Keywords: waveform sampling, CMOS, detector development, front-end electronics

1. Introduction

The development of large-area micro-channel plate (MCP) photo-detectors is currently underway by the Large-Area Picosecond Photo-Detectors (LAPPD) collaboration. The goal of this project is to construct fast, large active-area, and relatively affordable detectors capable of making time-of-flight measurements in physics experiments and other applications [1]. Unlike conventional photo-multiplier tubes (PMTs), the anode of this detector consists of a multi-channel microstrip line configuration, typically consisting of 30 or 40 strips, in which signals are read out on both ends of a transmision line to gather the time and position of the incident pulse [2]. Accordingly, each detector requires 60 or 80 channels of compact, precise readout electronics in order to preserve the fast timing characteristics inherent in the MCP and to best reconstruct the signal event.

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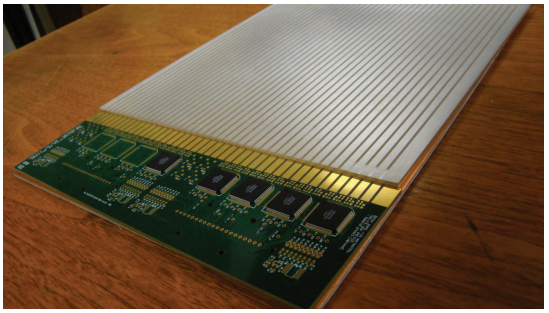

Fig. 1. A photograph of the so-called Analog Card: a 40 channel, 50 Ω matched front-end readout board based on the PSEC-3 ASIC. An array of Z_0 = 50 Ω microstrip anodes (visible to right of PCB) is silk-screened on a glass substrate, which also serves as the base of the hermetically sealed MCP package.

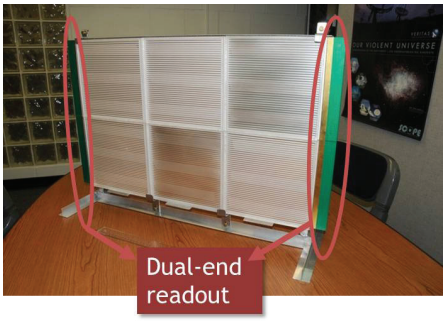

Fig. 2. A mock-up of a 'Super-module' photo-detector made from a 2x3 array of 8x8 in^2 MCP tiles under development by the LAPPD collaboration. D etectors will incorporate a dual-end ≥1 GHz BW transmission line readout using 10 GSa/s PSEC waveform sampling ASICs. Shown in picture are 2 Analog Cards per side (160 channels total).

Among the front-end readout options, waveform sampling not only provides the best timing information [3], but also allows for the detection of pile-up events and the ability to filter out background noise or poorly formed pulses. Commercial waveform sampling devices, such as oscilloscopes, become prohibitively large, power consuming, and costly as the number of channels increases, and therefore detector readout has relied on conventional methods, such as constant-fraction discrimination (CFD) and time-to-digital converters (TDCs). In recent years, modern integrated circuit technology has made the development of such compact, low power 'oscilloscopes on a chip' possible. For example, such custom waveform digitizers have been used in high-energy neutrino detection [4] and particle physics applications [5]. In addition, the timing performance of several waveform sampling ASICs has been shown to rival some of the best commercial (expensive) CFD electronics [6].

For the LAPPD front-end readout we designed PSEC-3, a waveform sampling and digitizing ASIC in 0.13 μm CMOS, intended to address some of the limitations of existing sampling ASICs designed in 0.25 and 0.35 μm processes. Specifically, in an attempt to improve the system timing resolution, PSEC-3 was specified with a sampling rate ≥10 Gigasamples/s [GSa/s] and an analog bandwidth ≥1 GHz. While sampling at a rate higher than that required by the Nyquist theorem does not further enhance the signal information content, oversampling does effectively increase the signal-to-noise ratio (SNR) of the sampled signal, an important factor in picosecond timing resolution[1].

1.1. Detector Integration

The large-area MCP 'tile' currently being constructed consists of an 8x8 in^2 photodetector with 30 or 40 readout transmission lines referenced to a backside ground plane. With a characteristic impedance, Z_0, of 50 Ω, the bandwidth of these transmission lines is ≥1 GHz for all configurations. In order to preserve this bandwidth throughout the system, a careful front-end readout design, in which the impedance is matched at the anode-readout board transition, is necessary. Figure 1 shows such a design: a 40-channel PSEC-3 'Analog Card' integrated with one side of a 40-microstrip line anode.

A benefit of this transmission line anode design is that these MCP tiles may be daisy-chained together if the desired application is of low enough event rate. This affords a reduction in the number of readout channels and an increase in detector active-area *without* sacrificing the overall detector time/position resolution capability. One such configuration, the proposed 'Super Module' detector, is shown in Figure 2, and consists of a 2x3 array of MCP tiles. The PSEC-3 Analog Card design is thus modular - it may be used for a single tile or an arbitrary array of such units.

[1] A simple model of timing resolution with waveform sampling shows it scales linearly with the SNR [7].

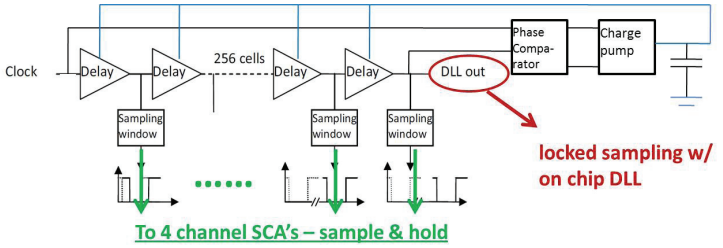

Fig. 3. Block diagram of the PSEC-3 timing generation circuitry. A 256-stage current-starved inverter delay line generates a 100 ps delay per step at 10 GSa/s. An on-chip phase comparator and charge pump complete the delay locked loop (DLL), in which sampling is locked with respect to the external write clock.

2. PSEC-3 Architecture

As the front-end readout ASIC for the LAPPD project, PSEC-3 was designed for fast signals characteristic of MCPs. The primary design specifications included a fast sampling rate (≥10 GSa/s), a high analog bandwidth (≥1 GHz) and robust trigger rate capability of ∼100kHz.

A single-ended switched-capacitor array was implemented, in which each of the 4 channels has 256 sample points per waveform. Each of the 1024 sampling capacitors has a dedicated comparator and a 12 bit register as part of the chip-parallel ramp-compare ADC (1024x 12 bit conversions) that is clocked at 2 GHz. Upon digitization, data readout is performed serially at up to 20 MHz. As this data transfer process is the largest single contribution to chip dead-time, readout may be restricted to regions of interest specified by a channel number and 64-block of registers. Readout of each block takes roughly 3 μs.

An input buffer was not included in the PSEC-3 design in order to maximize the chip bandwidth, as necessary to preserve the signal shape and content from fast MCPs. The LAPPD-made MCPs have already demonstrated single plate gains of 10^5 and signal rise times of a couple hundred picoseconds [8]. With the immediate application of reading out the LAPPD high channel density, large-area MCPs for characterization and testing, a high analog bandwidth ASIC was a design priority.

The fast switching and low capacitance characteristics of 0.13 μm CMOS allows for sampling ≥10 GSa/s with a straightforward current-starved inverter delay line design. A block diagram of the PSEC-3 timing generation is shown in Figure 3. In addition to the delay line, a custom phase comparator and charge pump circuit was implemented to lock sampling on-chip with a relatively low jitter of <40 ps. The fidelity of the sample-lock can be monitored by the control FPGA.

3. Evaluation Board

An evaluation board, shown in Figure 4, was designed to test and characterize PSEC-3. The board employs a USB 2.0 PC interface[2] for a user-friendly 'plug-and-play' testing experience. A single 5V power supply is required, from which 300-500 mA is drawn, depending on operating conditions. In addition, a hardware trigger input is available. The overall board control, PSEC-3 state machine logic and USB firmware drivers are programmed in an Altera Cyclone III FPGA. A block of RAM was implemented in the FPGA to buffer data between the ASIC and the USB-protocol PC readout.

Evaluation software was developed in parallel, and a screen-shot of the oscilloscope-like GUI is shown in Figure 5. The code is written in C++ and the user-interface was created utilizing the open-source wxWidgets library [9]. PSEC-3 configurable parameters such as sampling rate, trigger mode and pedestal-voltage may be set with this GUI interface.

[2]The interface uses a Cypress CY7C6803-56 USB Microcontroller in FIFO mode

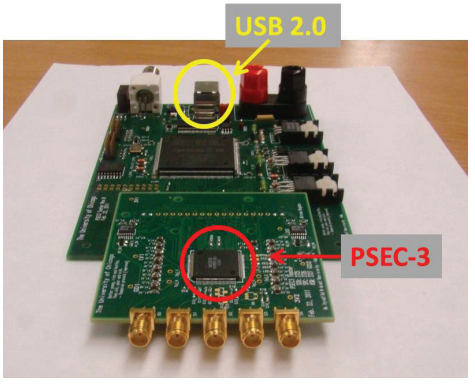

Fig. 4. PSEC-3 evaluation board with USB 2.0 PC interface. Board requires a single 5V power supply and employs an Altera Cyclone III FPGA.

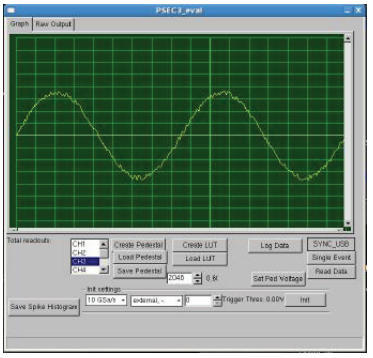

Fig. 5. Screen-shot of accompanying evaluation software. This version incorporates an oscilloscope-like interface.

4. Test Results

4.1. Sampling Rate

Pushing for higher sampling rates in waveform sampling ASICs was one of the primary goals of PSEC-3. This rate is adjusted via two symmetric control voltages on the 256-stage delay line. The measured and simulated PSEC-3 sampling rates are shown in Figure 6.

The sampling rate was measured by fitting a 100 MHz sine wave input to extract the rate. A sampling rate of up to 17 GSa/s has been demonstrated, although typical PSEC-3 operation keeps the rate at 10 GSa/s, providing a 25 ns window (sampled on 256 points) per triggered event.

4.2. Frequency Response

The target analog bandwidth for the PSEC-3 design was ≥1 GHz in order to match the system bandwidth and preserve the expected signal power spectral content. The bandwidth in waveform sampling ASICs is, in most cases, limited by the parasitic input capacitance where

$$f_{3dB} = \frac{1}{2\pi Z_{in} C_{parasitic}} \tag{1}$$

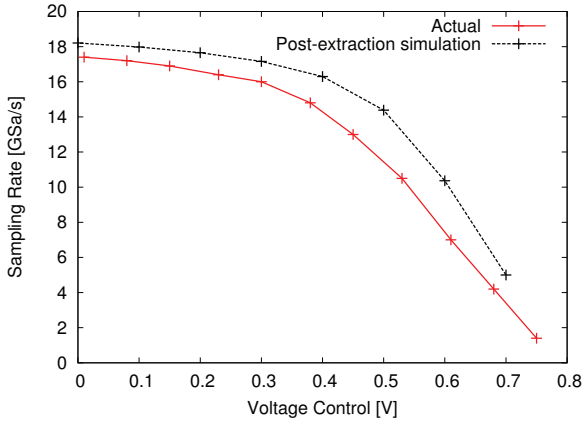

Fig. 6. Sampling rate as a function of the NMOS bias voltage on current-starved inverter stage. Good agreement is shown between post layout simulation and actual values. Rates up to 17 GSa/s have been achieved.

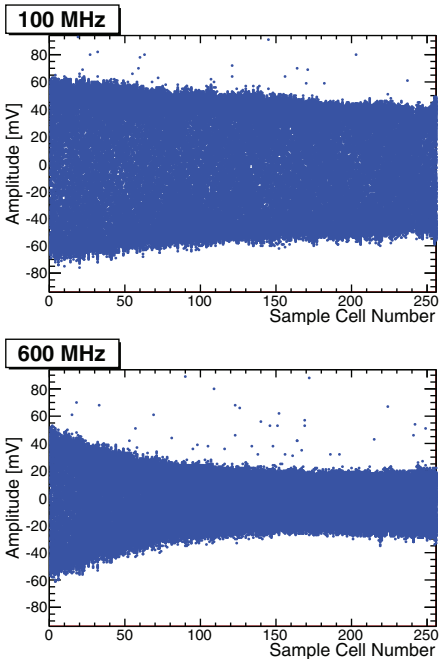

Fig. 7. Three-hundred readouts overlaid for a 100 and 600 MHz sine wave input, plotted as a function of sample cell number. The visible attenuation at higher input frequency along the input line (higher sample cell #) is due to the relatively high series resistance along the input (160Ω over entire length).

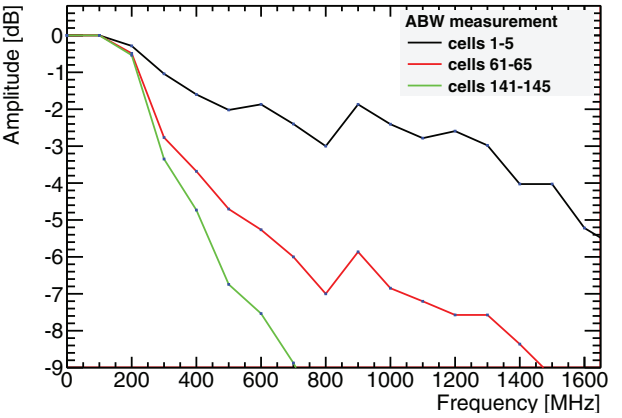

Fig. 8. The frequency response of PSEC-3 is shown for three different input regions: sample cells 1-5, cells 61-66 and cells 141-145. The bandwidth (f_{3dB}) is ~1.3 GHz for the first few sample cells along the input line, but drops off to ~300 MHz for sample cells further down. See Figure 7 for a visualization of this effect.

The PSEC-3 input impedance, Z_{in}= 50Ω, is given by the transmission-line matched termination resistance at the chip input. Hence, the bandwidth is maximized by minimizing $C_{parasitic}$ of the input trace. With this goal in mind, a narrow, 50Ω co-planar input line on an intermediate metal layer was implemented to reduce undesired couplings. However, a critical feature was overlooked with this layout design as a non-negligible series resistance (160 Ω) was introduced along the signal input line, contributing an additional low-pass pole to the transfer function that depends on sample cell location. A comparison of sine wave data at 100 MHz and 600 MHz is given in Figure 7, showing visible attenuation for cells further along (higher sample cell number) this resistive input line.

This trend complicates an analysis of PSEC-3 data since each sample cell has a different effective analog bandwidth, as shown in Figure 8. An f_{3dB} bandwidth of 1.3 GHz is observed for the first few sample cells, but falls off to 300 MHz for higher sample cell values. This problem of bandwidth attenuation may be solved by increasing the width of the trace and moving to a higher, thicker metal layer in the process to reduce the series resistance of the input. By doing so, a factor of 25 reduction in the input line resistance is easily achieved, and with this improvement, simulation shows a bandwidth of ≥1 GHz can be extended to all sample cells.

5. Calibration

Several calibration steps must be undertaken in order to get the best performance results from PSEC-3. For example, a raw ADC readout of an 80 MHz sine wave input is shown in Figure 9.

5.1. Pedestal Correction

There is significant fixed channel pedestal spread due to cell-to-cell device mismatch, as shown in Figure 10. For this measurement, the offset voltage was set to 620 mV and the ADC was run at about 10 bit

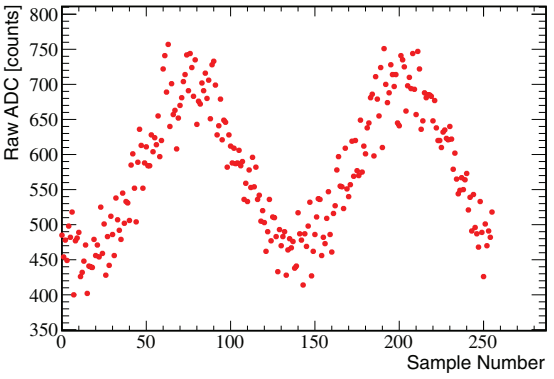

Fig. 9. Raw PSEC-3 data readout for a 220 mV_{pp}, 80 MHz sine input. ADC count values are plotted as a function of sample cell number.

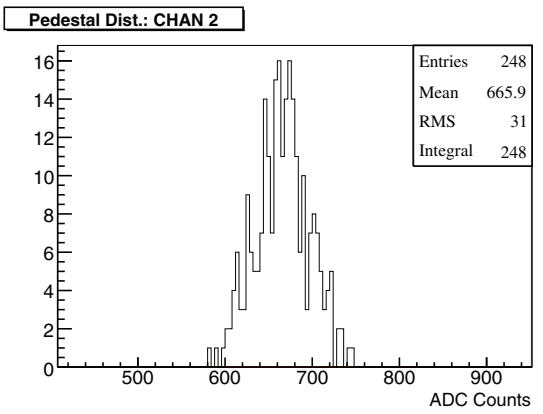

Fig. 10. Histogram of pedestal values from a single channel in PSEC-3. The spread is dominated by comparator threshold variations that are removed via a simple offset correction.

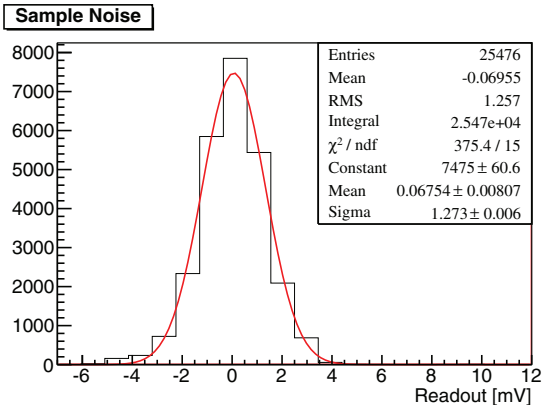

Fig. 11. Noise histogram from a single PSEC-3 channel after offset (pedestal) correction. Noise σ ~1.2-1.5 mV on all channels.

resolution (this varies slightly channel-to-channel). By doing several subsequent pedestal readouts, these offset values are calculated and this effect is easily calibrated out.

Once offset-corrected, the inherent random noise of PSEC-3 remains as shown in Figure 11 and was found to be ~1.2-1.5 mV on all tested channels. Several noise sources have been diagnosed, of which the primary culprit is attributed to integrated noise from the ADC ramp-distributing buffer amplifiers.

5.2. Linearity

A linearity correction to data output must be performed depending on the input signal voltage swing. The response of PSEC-3 to a linear DC-voltage scan and a linear fit are shown for one chip in Figure 12. There is a very good agreement between the fit and response between ~400-850 mV, in which no correction to the ADC output is necessary. The deviation below ~400 mV is due to charge injection in the sample-and-hold switch that feeds each sampling capacitor. To correct for this, and to use the full dynamic range of 50-900mV, the linearization is implemented in a look-up-table (LUT). A readout of an 80 MHz sine input, after both pedestal and linearity corrections are applied, is presented in Figure 13.

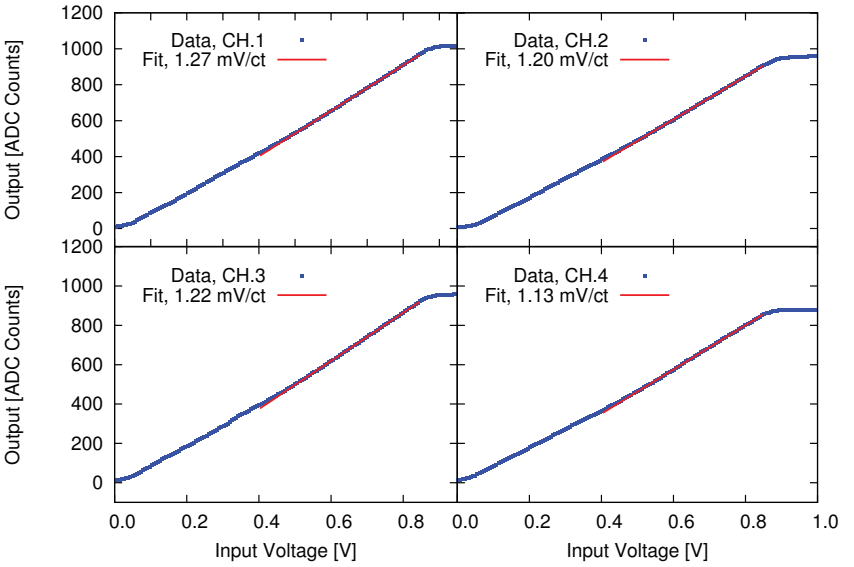

Fig. 12. DC transfer curves of PSEC-3 running in ~10 bit mode on all four channels of a single chip. The dynamic range is limited to ~50-900 mV (out of 1.2V possible). Linear fits (red lines), applied between 400 and 850 mV, show good linearity in this region. To use the full dynamic range, the linearization is implemented in a look-up-detable (LUT).

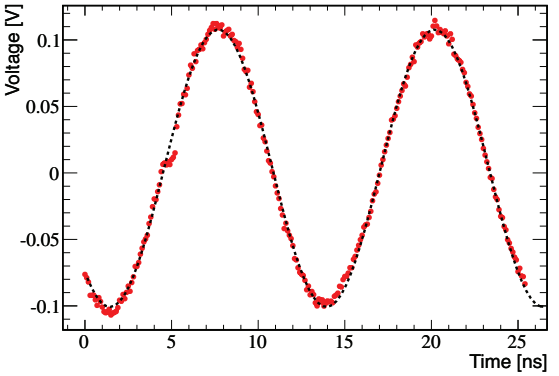

Fig. 13. A readout of a 220 mV_{pp}, 80 MHz sine input (same event as in Fig. 9) is shown after both pedestal and linearity correction (red data points). With a sampling rate of 10 GSa/s, the nominal time-step of 100 ps per cell is plotted on the x-axis. The black line is a sine fit to the data with floated amplitude, phase and DC-offset. The feature just below 5 ns is at the 'wrap-around' location of the DLL, the point at which 4-6 cells are still in sample mode at the time of a common-stop trigger. These cells are not allowed adequate settling-time to accurately track the input waveform.

5.3. Timing Calibration

For precision timing measurements with waveform digitizing ASICs, both the overall time-base of the delay line and the cell-to-cell time step variations must be corrected. With a rate-locking DLL, the overall PSEC-3 time-base is servo-controlled to be stable, leaving the remaining task to be the calibration of the time differential non-linearity (DNL) of the 256 delays. Using a sine wave input of known frequency, we employ a novel timing calibration technique using correlations between pairs of samples that converges for a relatively small data set (~10^3 events), a significant improvement compared to other methods [10].

6. PSEC-4

Based upon lessons learned from the PSEC-3 prototype, we have improved the design and submitted PSEC-4, a 6-channel waveform sampling and digitizing ASIC. The main deficiency addressed was the input analog bandwidth, which is now expected to be ≥1 GHz for all sampling cells. A noise reduction was also achieved by removing ADC ramp fan-out buffers, with an expected RMS noise of ≤ 1 mV. In addition, design improvements in the overall power distribution and digital output-bus capacitance will allow for at least twice the readout speed of PSEC-3.

A comparison between PSEC-3 results and PSEC-4 expectations is shown in Table 1. As only the minimal, necessary changes were made to the already working PSEC-3, we expect a fully functional ASIC when the fabricated parts are received in September, 2011. With the shift from a 40-microstrip anode and the 4-channel PSEC-3 ASIC to a 30-strip anode and the 6-channel PSEC-4 ASIC, we have reduced the chip count per 8”-wide tile array by a factor of 2, from 10 chips per end to 5. As such, PSEC-4 is targeted as the baseline readout ASIC for the upcoming large-area MCP-PMTs with achievable sampling rates of 10-15 GSa/s and an analog bandwidth of 1.5 GHz.

Table 1. Specifications and results from PSEC-3 compared to PSEC-4, a 130 nm production design submitted on 9-May 2011. The two designs share similar architectures, but the primary improvements of PSEC-4 over its predecessor are highlighed in red. The key specifications of PSEC-4 are 6 signal channels, a 10-15 GSa/s sampling rate and ≥1 GHz ABW.

	PSEC-3		PSEC-4
	SPECIFICATION	ACTUAL	SPECIFICATION
Sampling Rate	500 MSa/s-17GSa/s	2.5 - 17GSa/s	2.5 – 17 GSa/s
# Channels	4	4	6 (or 2)
Sampling Depth	256 cells	256 Cells	256 (or 768) points
Sampling Window	256*(Sampling Rate)$^{-1}$	256*(Sampling Rate)$^{-1}$	Depth*(Sampling Rate)$^{-1}$
Input Noise	1 mV RMS	1.2-1.5 mV RMS	<1 mV RMS
Dynamic Range	0-1V	0.05-0.9V	0-1V
Analog Bandwidth	1.5 GHz	Average 600 MHz	1.5 GHz
ADC conversion	Up to 12 bit @ 2GHz	Up to ~10 bit @ 2GHz	Up to 12 bit @ 2GHz
Latency	2 µs (min) – 16 µs (max)	3 µs (min) – 30 µs (max)	2 µs (min) – 16 µs (max)

7. Conclusion

We have described the design, testing, and initial characterization of a prototype waveform digitizing ASIC in the IBM 0.13 μm CMOS process in the context of the large-area MCP-PMT development effort of the LAPPD collaboration. With a sampling rate of up to 17 GSa/s, relatively low noise ≤1.5 mV, and compact channel density, PSEC-3 is well suited for the transmission line readout of these detectors. A few issues were encountered in the PSEC-3 design, most notably the analog bandwidth attenuation along the signal input line, in which the measured BW of 1.3 GHz on the first few cells falls off to ~300 MHz further along the input line.

These issues have been corrected in the PSEC-4 ASIC currently in fabrication. PSEC-4 shares the same overall architecture with its predecessor, but with increased performance in terms of noise, analog bandwidth consistency, dead time, and dynamic range. The new ASIC also incorporates a higher channel density (6 per chip) that will reduce cost per channel when instrumenting a detector. Once thoroughly tested, a DAQ system using the 10 GSa/s, 1.5 GHz BW PSEC-4 ASIC will be constructed for the readout of the large-area MCP-PMTs.

A more comprehensive description and complete characterization of PSEC-3 is underway and a report is in preperation [11]. In addition to the LAPPD front-end readout, as a flexible waveform sampling ASIC,

the PSEC architecture is well-suited for use in many other applications where high sampling rate and fast digitization is desired.

8. Acknowledgements

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References

[1] The Large-Area Picosecond Photo-Detectors Project: see http://psec.uchicago.edu
[2] H. Grabas, E. Oberla, H.J. Frisch, and J.-F. Genat, D. McGinnis, B. Adams, M. Wetstein, "Studies of Transmission Line Anodes in a MCP-based Detector", to be submitted to JINST. Sept., 2011.
[3] J.-F. Genat,G.S. Varner, F. Tang, H.J. Frisch, "Signal Processing for Pico-second Resolution Timing Measurements", Nucl.Instrum.Meth.A607:387-393, Oct., 2009.
[4] G.S. Varner, L.L Ruckman, J.W. Nam, R.J. Nichol, J. Cao, P.W. Gorham, M. Wilcox, "The Large Analog Bandwidth Recorder and Digitizer With Ordered Readout (LABRADOR) ASIC", Nucl.Instrum.Meth.A583:447-460,Dec., 2007.
[5] S. Ritt, "The DRS Chip: Cheap Waveform Digitization in the GHz Range", Nucl.Instrum.Meth.A518:470-471, Feb., 2004
[6] D. Breton, E. Delagnes, J. Maalmi, K. Nishimura, L.L. Ruckman, G. Varner, J. Va'vra, "High Resolution Photon Timing with MCP-PMTs: A Comparison of Commercial Constant Franction Discriminator (CFD) with ASIC-based waveform digitizers TARGET and WaveCatcher", SLAC-PUB-1408, Aug., 2010.
[7] S. Ritt, "The Role of Analog Bandwidth and S/N in Timing", talk at *The Factors that Limit Timing Resolution in Photodetectors*, workshop at the University of Chicago, Apr., 2011.
[8] M. Wetstein, et al., "Systems-Level Characterization of Microchannel Plate Detector Assemblies Using a Pulsed sub-Picosecond Laser", this Proceedings.
[9] wxWidgets Cross-Platform GUI Library: www.wxwidgets.org
[10] K. Nishimura, et al., "A Correlation-Based Timing Calibration & Diagnostic Technique for Fast Digitization ASICs", this Proceedings.
[11] E. Oberla, et al., "A Prototype Waveform Digitizing ASIC in 0.13 μm CMOS for Precision Timing Measurements", NIM-A submission in-progress, 2011.