TM-565
0405.000

A 53 MHz RANDOMLY TRIGGERED SYNCHRONOUS PREDETERMINED SCALER FOR ACCELERATOR DIAGNOSTICS

March 1975

Edward F. Higgins
Fermi National Accelerator Laboratory*
Batavia, Illinois

SUMMARY

A 53 MHz random triggered recycling, predetermined start-stop scaler is described. The scaler has a range from 2-to-9999 counts, sensitivity of 40 mV rms and provides both NIM and TTL standard logic outputs.

The scaler is composed mainly of standard ECL integrated circuits including universal counters, configured in a "synchronous parallel carry" connection, and ordinary logic gates and flip-flops. Special circuitry has been designed to prevent start-up counting errors due to the phase randomness between the applied start triggering and input signal transitions. Following a start trigger, the scaler cycles until disabled, delivering an output pulse each time the predetermined count is reached. The time jitter of the output pulses with respect to the periodic input signal is less than 0.1 ns.

High resolution examination of the behavior of individual charge bunches within the accelerator is made possible when the scaler is set to count the machine's harmonic number. If the scaler is set one digit away from the harmonic number, the output pulses advance one bunch for each turn around the machine, allowing a sequential display of the contents of each bucket in the machine.

GENERAL

Integrated circuits of the universal counter type (MC10136, MC10137, F95010, F9510)[1] employing Medium Scale Integration technology have become versatile building blocks for high speed, wide range, low jitter, variable modulo scalers. The high frequency universal counter circuits in this device category are usually designed with ECL logic format and generally have 4-bit programming capability (BCD or Hexadecimal) per discrete package. Error-free operation ($f_{out} = f_{in}$/program modulo; exactly) in excess of 100 MHz can be achieved for single devices with 4-bit range, while cascades of the universal counters can be configured into multistage programmable scalers with very large counting ranges. Simple interface circuits, ECL-TTL, TTL-ECL translator[2] IC's or discrete circuits provide straightforward data inputting and outputting.

It is common practice[3] to configure several universal counters and gates in a "synchronous parallel carry" scaler configuration to secure the large range in divide modulus while at the same time maximizing counting speed and minimizing the possibility of counting error due to variations in input signal period. In this configuration, the signal to be scaled is applied to the clocking terminals of all stages within the scaler simultaneously. The carry advance data instead of slowly rippling from one stage to the next, are developed by high-speed external decoder gates and propagated via minimum-delay paths to appropriate carry-in terminals. The scalers cyclic terminal count pulses not only constitute the required scaled output but have the required synchronism and the correct logic levels to meet the presetting/loading control requirements for cyclic operation. The terminal counts are therefore fed-back directly to the preset/load control terminals of each counter in the scaler to establish the cycle-by-cycle preset/loading operations. With the described feedback connection, the scaler can synchronously follow variations of the input frequency adaptively while maintaining programmability even for cycle-to-cycle modifications in the divide modulo. By selecting the appropriate control mode connections, upcount, down count, and preset control or hold count operation and by application of the necessary data to set the divide modulus, the counter begins to cycle upon simultaneous application of the input signal and preset control pulse. The output is obtained either by decoding four output data lines or by utilization of the carry advance information.

Although not normally operated in applications requiring error-free start-stop scaling sequences, the "synchronous parallel carry" configuration can be used in this way if appropriately timed synchronous start-stop triggers are available with nanosecond timing precision. For these situations the feedback arrangement can be modified slightly to accommodate start-stop operations by: (1) ORING the externally applied start preset control pulse with the internally generated triggers that are derived by returning the terminal counts to the preset/load control terminals, and (2) allowing the stop trigger to DISABLE the input signal following the last desired terminal count pulse, thus avoiding possible extra counts or glitching which could be developed by mode shifting while outputting.

As versatile as the described scaler connection is in achieving high speed, adaptability to input period fluctuations, and in cyclic start-stop program flexibility, its utility for the control of accelerator circuits and for use in machine diagnostics is severely limited. The reason for this is twofold: (1) trigger pulses meeting the exacting timing requirements and logic format (ECL, TTL, NIM) for implementing the starting and stopping processes are seldom available, and (2) error-free counting is not possible when the start-stop triggers are asynchronous with the input signal transitions. Errors are developed because of the inability of random triggering to always allow the set-up and hold parameters associated with the counters control inputs to be met within the cycle where the trigger starts.

To remove the stated limitations, a start-stop scaler containing specialized triggering circuits to permit normal presetting and loading but which retains all the relevant features of the "synchronous parallel carry" configuration has been constructed. The scalers control logic is described in the following sections. The device has proven to be a useful circuit element in synchrotron design, control, and for "on-line" diagnostics and data gathering in the Fermilab Main Synchrotron.

TIMING SEQUENCES AND SYNCHRONIZING METHOD

Asynchronous Timing

Figure 1 shows several timing sequences associated with a typical start-stop scaler operating near its

*Operated by Universities Research Association, Inc., Under Contract With the U. S. Energy Research and Development Administration.

upper frequency limit. The figure illustrates how counting errors are developed as a result of asynchronism between start triggering and input signal. The applied start triggers are shown at different times within the timespan of an input cycle, sequence (A). The set-up and hold time intervals are identified together with the extent of the control regions (T_{SU} + T_H sec.), throughout which the preset pulse must exist for proper start-up operation. The preset control pulse sequences (B, C, D) of Figure 1, are based on: (1) all preset control pulses start at the leading edge of the applied start triggers, (2) the input signal being delayed for T_{SU} seconds to force at least one preset control pulse to meet the set-up and hold requirements, and (3) the sequences (B, C, D) are shown for preset control widths of 1, 3/4, and 1/2 period of the input respectively to aid in examination of the timing relationships.

By inspection of sequences (B, C, D) relative to the control regions, it is observed that no every illustrated, preset condition in the sequences satisfy the necessary timing for correct start-up, i.e., only some (those marked +) of the preset control pulses bridge a control region. In the majority of the cases shown, either insufficient set-up or hold time is available for normal control gate functioning or the preset control pulse falls entirely outside (Sequence D Center) the region when normal presetting/loading could be initiated. All of these conditions produce single or multi-count errors or a missed cycle. A similar error generating condition exists for other trigger position, signal delays, and preset control pulse width values. Although a wide first preset control pulse, say 2 periods in width, could be made to always bridge at least one control region, a one count error per counting cycle could be developed owing to the possibility of double triggering and loading with this kind of start-up operation.

Obviously another start-stop triggering technique is required if the scalers preset control pulse is to accommodate the variations caused by the asynchronism between input signal and start triggers. The basic reason for the failure of the triggering technique shown in the sequences of Figure 1 is that the timing uncertainty between triggers and input signal is one full period of the input. It can be shown that a reduction of this uncertainty to $\leq$ 1/2 period will make possible error-free scaling under asynchronous conditions if a suitable signal delay and a specific initial preset control width is selected.

A detailed method to reduce the timing uncertainty is summarized below, while a block diagram, Figure 2, is given as an aid in examining the method. Figure 2 also illustrates the implementation of the method using standard ECL counters, flip-flops and gates.

Synchronizing Method

1. The scalers preset control pulse, and clock lines are normally maintained at a logic level corresponding to $\overline{\text{LOAD}}$; waiting for the pulse and transition which will start the loading and counting process.

2. A pseudo clock signal, delayed by an amount of time corresponding to (T_{SU}), is developed by first, multiplying the applied input signal frequency by an integer N, N>1, (2 for the case shown) and secondly, immediately dividing the resulting product signal by N through the use of a suitable high-speed edge triggered, gated, flip-flop (CLOCKING F-F) which is controlled by a second R-S flip-flop (START F-F) interconnected to the start trigger and the ENABLE terminal of the (CLOCKING F-F), as in Figure 2.

3. The applied start trigger, occurring at any time during the applied clock signal, forces a transition in the state of the (START F-F) which in turn permits the (CLOCKING F-F) to commence toggling only after the receipt of a positive clock input edge, i.e., the first positive-going signal edge following the start trigger establishes the start of a pseudo clocking train whose period equals that of the input signal but without a fractionated first cycle as would result from simple gating processes of the applied signal. The start-up phase of the pseudo clock is therefore always in synchronism with the start trigger and the timing uncertainty has been reduced from (Tc sec) to $\frac{Tc}{N}$ sec.

4. The counters first present control trigger, as required in 1. above, is developed directly from the start triggers leading edge through the use of a ONE-SHOT whose duration (T_p) is adjusted for; $T_p = T_{SU} + T_H + \frac{Tc}{N}$ sec.[4] Follow-on presets, utilized to continue the counting process after the first preset are derived from terminal counts, always T_c in width, fed-back to the preset line through fast gates; see Figure 2. The counter will cycle after starting until a stop trigger is applied to initiate the stop processes.

5. Stopping the counting process is achieved by: (1) reestablishing the pre-start state of the (CLOCKING F-F) gate control terminal thereby ending the pseudo cloc clock signal. This process is delayed however until a terminal count has been completed, i.e., stopping is delayed if a terminal count appears coincident with a stop trigger, and (2) an inter-START/STOP inhibit gate, generated by application of the start and stop triggers to their respective (START F-F) and (STOP F-F), is applied to the decoding gate/s to prevent noise or spurious signals from appearing at the output lines within the time interval between the stop trigger + Tc, and the next start trigger transition times.

SYNCHRONOUS TIMING

The timing sequences resulting from the outlined method are shown in Figure 3. As before, the start triggers represent possible start times and sequence (B) indicates the pseudo signal resulting from the multiplication and division processes. Sequence (C) compares the pseudo signal and preset control region for the applied trigger positions. Note that in contrast with corresponding sequences (B, C, D, and delayed signal) in Figure 1, that the sequence (C) of Figure 3 contains a present control pulse at the correct time (bridging the control region) for all positions of the start triggers. It can be shown, further, that for any other possible position of the start triggers this favorable relationship is maintained when the outlined method is utilized. Note also from Figure 2, that the combined action of the delay (Tc), STOP GATE, and the STOP F-F, that the mode of the synchronous counters can not change during the terminal count interval. As a result, both starting and stopping under asynchronous signal/start-stop triggering is made possible without start-up error or mode shift error during stopping.

SCALER PERFORMANCE

Several scalers using 4 BCD 4-bit universal counters to secure an upper counting range of 9999 have been constructed. These units were configured per Figure 2, and contained measures to minimize jitter to 0.1 ns. (.05% power regulation, hard limiting of input signals, component shielding, isolation, and decoupling, etc.). These scalers were optimized for performance in the 40-60 MHz frequence region and were designed to operate with input RF levels from 40-to-1000 MV rms.

Figure 4A, B, C show typical performance in general start-stop scaling situations in the Fermilab main

synchrotron. The conditions shown in Figure 4A, B, C, are as follows:

4A - Simple start-stop scaling, count = 8, frequency 53 MHz, presets top, pseudo signal bottom.

4B - Main synchrotron bunches - rear of batch 2 start of batch 3, frequency 53 MHz, count = harmonic number 1,113 scaler output to scope horizontal synchrotron.

4C - RF gap voltage beam bunch - 3rd to 6 bunch of 2nd batch relative position, frequency 53 MHz count = harmonic number 1,113, scalers output to scope horizontal synchrotron

CONCLUSION

High speed start-stop scalers have been designed with standard ECL universal counters, gates and flip-flops. A method has been developed which allows error-free counting for situations where the start and stopping triggers are asynchronous with the input signal. Many uses for scalers of this type have been developed in the Fermilab synchrotrons for control and diagnostic purposes.

REFERENCES

1. Motorola and Fairchild Types Respectively.
2. MC10124, MC10125, for example.
3. See Pub., AN-584, Motorola Semiconductor Products, Inc., 1972 and Fermilab Drawing ED-62146.
4. T_p can be made adaptive for broadband operation.

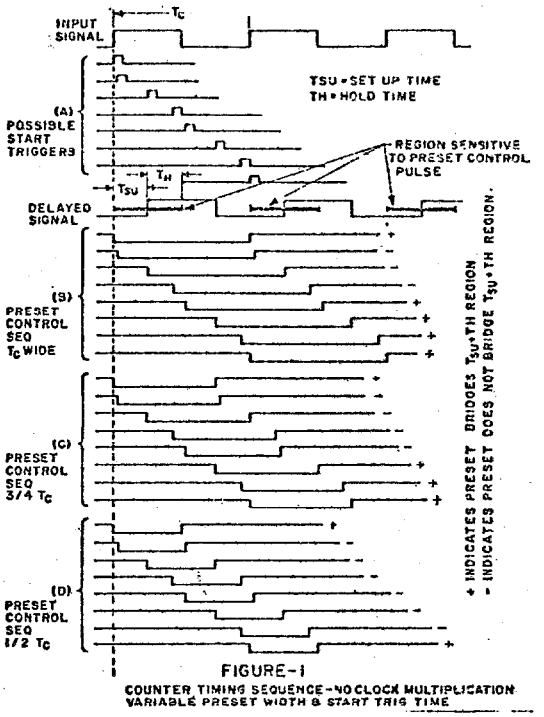

FIGURE-1
COUNTER TIMING SEQUENCE-NO CLOCK MULTIPLICATION VARIABLE PRESET WIDTH & START TRIG TIME

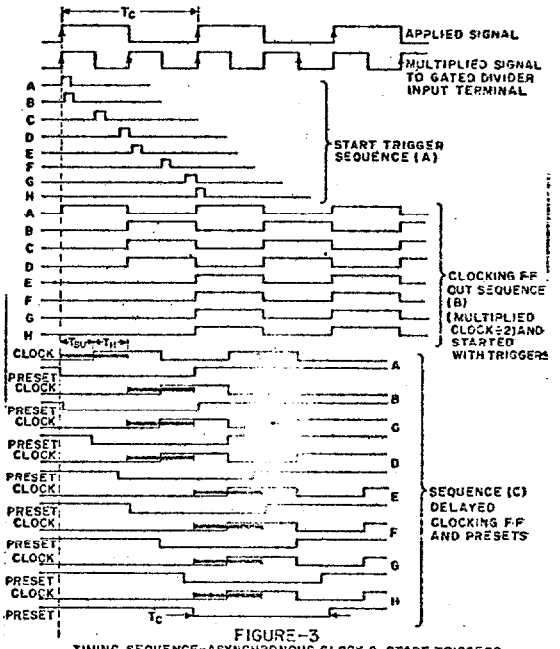

FIGURE-3
TIMING SEQUENCE-ASYNCHRONOUS CLOCK & START TRIGGERS PRESET BRIDGES ($T_{SU}+T_H$) TIME AFTER PROCESSING CLOCK & TRIGGERS. CLOCK MULTIPLICATION, N=2, PRESET CONTROL = T_C SEC

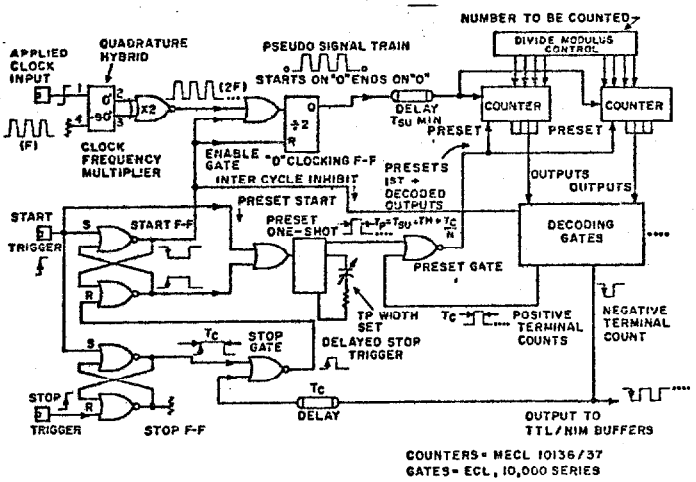

FIGURE-2
BLOCK DIAGRAM, SCALER TRIGGERING METHOD

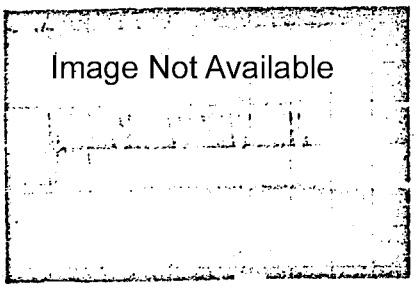

Fig. 4A. Start/Stop Scaling Count = 8, Presets Top, RF Wave Bottom

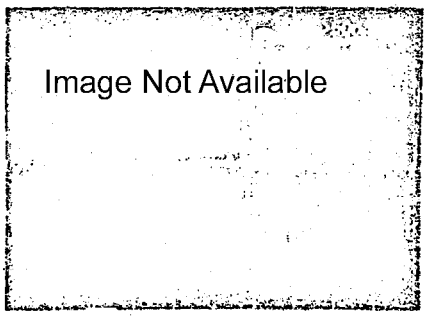

Fig. 4B. Main Synchrotron Bunches Count = 1,113

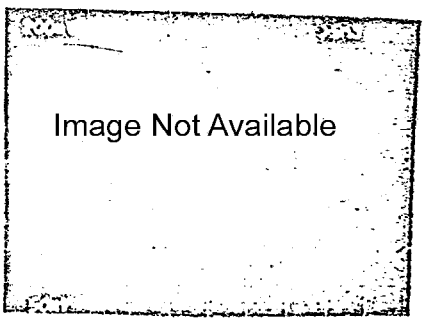

Fig. 4C. Main Synchrotron One RF Station Gap Voltage Top, Bunches Bottom Count = 1,113