FRONT-END ELECTRONICS OF THE CMS ENDCAP MUON SYSTEM

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Abstract

The design and prototype of the front-end readout and trigger electronics for cathode strip chambers in the CMS endcap muon system is described. Preliminary results obtained from beam test of CSC using the prototype electronics at CERN are reported.

1. INTRODUCTION

The CMS Endcap Muon system [1] uses Cathode Strip Chambers (CSC's). Each of the vertical chamber stations are made of 6-layer CSC's which are trapezoidal in shape. In a CSC layer, the anode wires are in the azimuthal direction and the cathode strips are in the radial direction. The bending of charged tracks by the magnetic field in the endcap region is in the azimuthal direction, and the precise measurement of the azimuthal coordinate of a hit is achieved by interpolation of charges induced on neighboring cathode strips. The anode wires provide precise timing measurement of a hit as well as a coarse measurement of its radial position.

The front-end electronics for the CMS Endcap Muon System has two main purposes: 1) to acquire precise muon position and timing information for offline analysis; 2) to generate muon trigger primitives for the Lev-1 trigger system.

2. GENERAL REQUIREMENTS

Since the environment in the CMS endcap muon region is demanding at the LHC with full designed luminosity of 10^{34} $cm^{-2}s^{-1}$ - singles hit rate could be as high as 1 kHz/cm^2 for the inner CSC's - the electronics must be capable of: 1) handling the expected high rates, 2) dead-time free operation, 3) discriminating against random hits due to neutrons and gammas and 4) withstanding the expected radiation level. Furthermore, due to the large channel counts (about 200k channels of cathode electronics and similar numbers of anode channels), custom ASIC's must be used extensively to minimize board sizes, per channel costs and power consumption.

3. PHYSICAL LAYOUT

The CSC front-end electronics consists of four types of boards: cathode front-end boards (FEB's), anode FEB's, DAQ Motherboards (MB-DAQ) and Trigger Motherboards (MB-TRIG). Figure 1 shows how the system is organized.

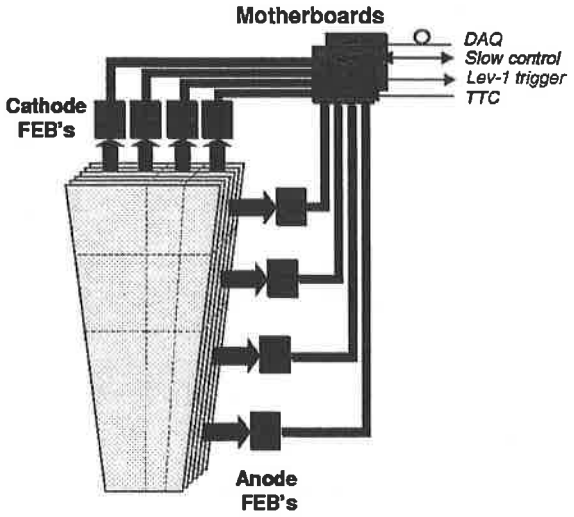

Fig. 1. Schematic layout of the CSC Electronics

Depending on chamber types, there are typically 4 to 5 cathode FEB's, and 3 to 7 anode FEB's per chamber. Each cathode or anode FEB serves 96 input channels. There is one MB-DAQ and one MB-TRIG per chamber. All the FEB's are mounted on the chamber and the motherboards will be housed in crates located aroung the peripheral of each muon station. The data from cathode and anode FEB's will be sent on cables to MB-DAQ and MB-TRIG. The 2 MB's serve as the links between the FEB's and the rest of the experiment. They send the readout and trigger data to the central DAQ system and the Level-1 trigger system. They receive trigger/timing/control (TTC) and slow control signals and distributes them to the FEB's.

4. CATHODE FRONT-END BOARD

The cathode FEB consists of 96 input channels per board. Each front-end board is designed to read out a section of the chamber 16 strips wide by 6 layers deep. The functional diagram of the cathode FEB is shown in Fig 2. The input signals from each of the strips are sent into 16-channel amplifier-shaper ASIC's (There are 6 such ASIC's per FEB). Each input signal is amplified and shaped into voltage pulses. The output pulse shape is semi-Gaussian and the shaper peaking time is 100 ns . To minimize pile-

up effects in high rate environment, circuits to cancel the long tail of the chamber pulse due to ion drift are integrated into the shaper. Channel-by-channel calibration will be done using a set of precisely matched capacitors that couple a test pulse to each channel's input.

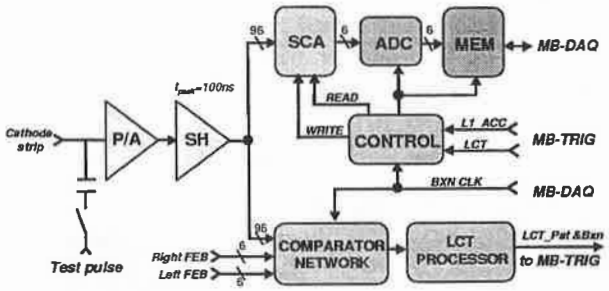

Fig. 2. Functional diagram of the cathode front-end board.

One output of the shaper is connected to the trigger path whose main components are a Comparator Network and a Local Charged Track (LCT) processor. The comparator network locates the centroids of the strip charge clusters in each chamber layer to an accuracy of half the strip width and marks its time. The resulting information is fed into the LCT trigger processor which look for coincidence of cluster centroids from a minimum number of chamber layers which form a "road". The time, location and angle of the LCT are used to determine trigger primitive parameters for the Level-1 muon trigger.

The other output of the shaper is connected to the DAQ readout path. The voltage is sampled every 50 ns (see Fig. 3) and held in a Switch Capacitor Array (SCA) during the Level-1 latency. The readout of the stored samples is data-driven: they are digitized and read out only when an LCT trigger associated with the sampled pulses occurs and that the LCT is time correlated with a Level-1 Accept. This requirement significantly suppresses random background hits induced by neutrons and photons. The digitized data is sent to the MB-DAQ and transmitted to the central DAQ system.

The preamplifier is a charge sensitive amplifier with a gain of 0.9 mv per fC. The input charge corresponding to a minimum ionizing hit is about 110 fC, with nominal high voltage setting for the the CSC. The performance requirements for the cathode front-end electronics are

- preamp noise less than 24 e/pF + 1000 e ,
- 100 ns shaping with tail cancellation,
- 12 bit dynamic range,
- less than 1% deviation from linearity from 0 - 1.5v,
- ½-strip spatial resolution per layer for LCT trigger.

The output voltage of the preamp-shaper is sampled at 20 MHz rate and stored in an SCA channel. There are 6 SCA ASIC's on a cathode FEB. Each SCA ASIC contains 16 channels and each channel has 96 capacitors (cells).

Eight samples for each pulse (see Fig. 3) will be saved. The eight samples include 2 to 3 samples of the baseline voltage for pile-up correction and 5 to 6 samples of the signal pulse for offline reconstruction of the pulse timing and pulse height. The sampling of the preamp-shaper output is a continuous, non-stopping process.

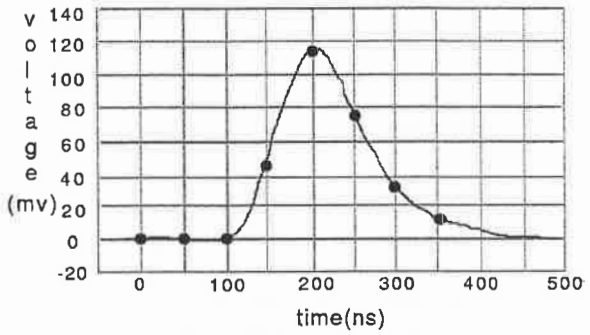

Fig 3. Sampling of the shaper pulse.

The SCA cell addresses for storing the sampled voltage (and addresses for readout of the stored voltages) are generated by the readout control FPGA. The cells to be used in the sampling are kept in a pool of free cells. At any time, 2 blocks (or 16 cells) are taken out of this pool. (since pulses arrive randomly in time, 16 cells are used to ensure the capture of at least 8 samples on a pulse). These cells are put back into the pool a) 800 ns later when no LCT is found (800 ns is LCT decision time); or b) an LCT is found but there is no Level-1 Accept after the Lev-1 latency of 3 μs.

The ½-strip per layer resolution required for the LCT trigger is achieved with the comparator ASIC. Four comparators are used for each input channel of this ASIC. The pulse from the shaper for each strip is compared with a pre-set threshold level. If the pulse exceeds threshold, the peak voltage for a given strip is compared with those from neighboring strips. A strip has the largest charge if its peak voltage is larger than either that of the neighbor strips. The track hit position is then localized to either right or left half of the strip by comparing with pulses between the neighboring strips. The output signals from the comparator ASIC are time-multiplexed into three consecutive bunch crossings. In the first bunch crossing, an output bit represents a hit on either of the strips, while during the following two crossings the output contains encoded information as to the half-strip location of the hit.

The digital signals generated by the comparator ASIC's are brought into the cathode LCT processor which finds track "roads" (see Fig. 4) through the 6 cathode layers within in a time interval of 75 ns.

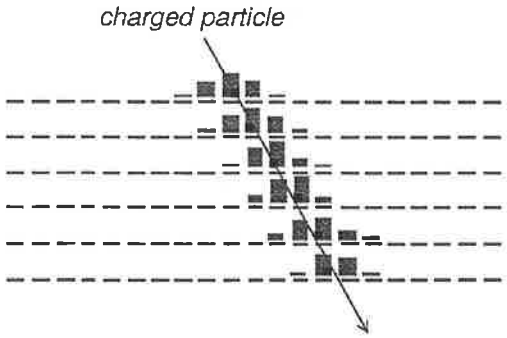

Fig. 4. Peak voltages induced on the strips by a traversing charged particle. The peak charge is localized to ½-strip, shown as black squares.

Since the magnetic field in the Endcap causes bending of charged tracks in the direction transverse to the strips (azimuthal direction), an infinite momentum track would appear to be normal to the strip plan in the view shown. Momentum threshold can therefore be set by requiring maximum number of strips traversed in the direction away from the normal.

Three 96-channel prototype cathode FEB's were built and tested on full-size CSC at CERN in the H2 beam area and at X5 with the GIF facility. Fig. 5 shows the display of the digitized output from a 96-channel board.

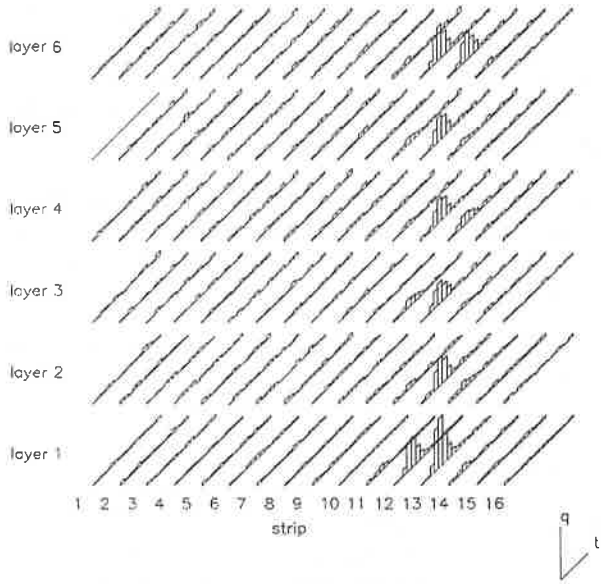

Fig. 5. Digitized data from prototype cathode electronics on a full-size CSC in the CERN H-2 muon test beam.

A muon track is clearly indicated by the space and time correlation of the displayed data. The RMS baseline noise samples is measured to be 1.7 mv, which includes preamplifier noise and SCA cell-to-cell pedestal variation. This noise level satisfies the design requirement.

5. ANODE FRONT-END BOARD

The anode readout is similar to that of the cathode except that the emphasis is on the accuracy of timing instead of pulse height. Each input channel of the anode FEB is a ganged group of wires (10 to 20) within a layer. Each front-end board is designed to read out a section of the chamber 16 wire groups wide by 6 layers deep. The functionality of the anode FEB is shown in Fig 6.

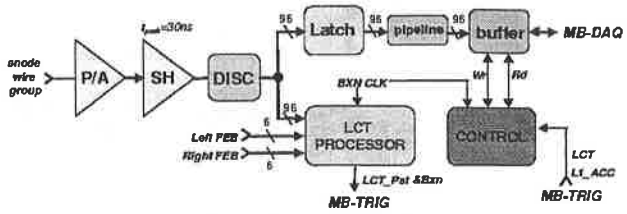

Fig. 6. Functional diagram of the anode front-end board.

The input signals go into 16-channel preamplifier-shaper-discriminator ASIC's (6 per FEB). The amplifiers are similar to the ones on the cathode FEB, but optimized for the summed anode input capacitance. The input charge corresponding to a minimum-ionizing hit is about 140 fC, for the nominal high voltage setting of the CSC. The signals are shaped with shaper peaking time of 30ns and sent into discriminators. The logic pulses from the discriminators are used to form the anode LCT and to determine the bunch crossing time of the track segment. The discriminator output pulses are also latched and pipelined for DAQ readout, providing hit/no-hit information for each of the wire groups.

The performance requirements for the anode front-end electronics are

- preamp noise less than 10,000 e at 200 pF,
- 30 ns shaping with tail cancellation,
- less than 2 ns time slewing of discriminator output,
- bunch crossing tagging efficiency > 92%.

Shorter shaping time results in higher intrinsic electronics noise. For shaping time of 30 ns and for nominal chamber gas gain, the CSC signal arise from the avalanche produced by a single electron is comparable to the equivalent input noise of the amplifier. To stay safely above this noise level, discriminator threshold needs to be set at 7 to 10 initial electrons, which can result in large time jitter. To achieve the 2 ns time slewing requirement the scheme of a two-threshold discriminator has been adopted. In this scheme, a high-threshold discriminator is driven by the initial signal from the amplifier. The threshold level is adjustable from 10% to 70% of a nominal MIP signal. The resulting pulse serves as the enable for the precision-time discriminator. The precision-time discriminator consists of a constant-fraction shaper

and a low-level discriminator. The constant-fraction shaping is done by adding the differentiated amplifier signal and the corresponding delayed and inverted signal. The resulting pulse is further amplified and delivered to the input of a low level zero-crossing discriminator. The zero crossing point corresponds to approximately half the rise time of the input signal.

The anode LCT trigger processor finds track "roads" through the 6 anode layers just as the cathode LCT trigger circuitry does. There are, however, several differences. The anode segmentation is much coarser and the roads are straight lines to the interaction region, independent of P_t. The roads also may differ in different chips and boards due to the changing polar angle. More importantly, the anode LCT timing will be used for bunch crossing identification of the track hit, since the analog preamplifier-shaper is optimized for timing rather than pulse height measurement.

Three 96-channel prototype anode FEB's were built and tested on full-size CSC at CERN in the H2 beam area and at X5 with the GIF facility. The results obtained from this test show that the anode timing requirement have been met. Using the prototype electronics, it has been demonstrated that better than 99% bunch crossing tagging efficiency can be achieved by using information from all six CSC layers.

Fig. 7 shows the measured arrival time distribution of muon hits in a single CSC layer. It has an RMS width of 9.8 ns and full width of about 70 ns - too long for efficient bunch crossing tagging. However, the time distribution for the first (or second, or third etc.) arrival pulses from 6 CSC layers is much narrower. As shown in Fig 8., 99% bunch crossing tagging efficiency can be achieved if either the third or fourth arrival pulse is used.

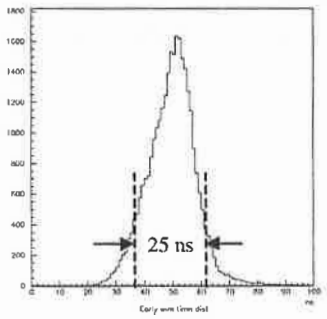

Fig 7. Anode arrival time distribution for muon hits in a single CSC layer.

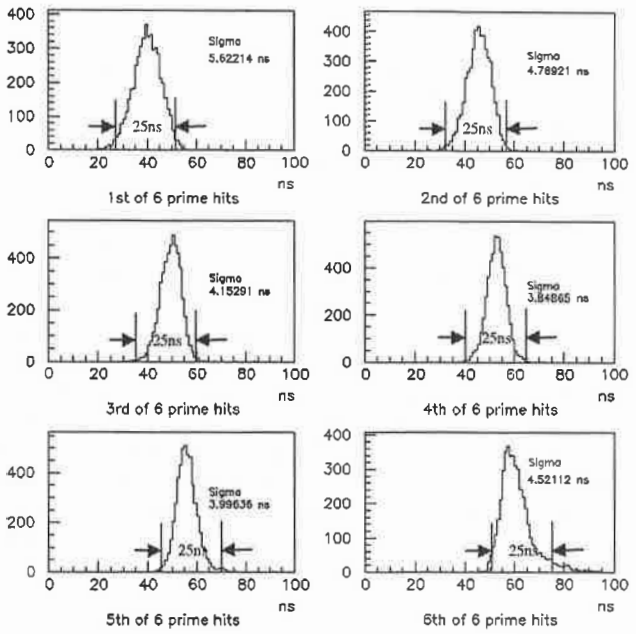

Fig 8. Anode time distribution for first, second, third, fourth, fifth and sixth arrival pulses, plotted respectively, out of all six CSC layers.

6. MOTHERBOARDS

The Motherboards serve as links to the level-1 muon trigger and to the central DAQ of CMS. There is one DAQ and one trigger motherboard for each CSC module. The functionality of the trigger and DAQ Motherboards is shown in Fig.9.

Trigger Motherboard - The information associated with LCT's generated on cathode FEB's and anode FEB's are sent to the Trigger Motherboard. This information includes the bunch crossing time and the location and angle of each LCT. When the timing between a cathode LCT and an anode LCT's is found to agree within ±1 bunch crossing, the LCT is a valid one. When more than one valid LCT is found for the chamber, only the best two, as determined by quality factors, are retained and passed on to the port cards along with the (anode) LCT bunch crossing number. (Each port card spans a 30 degree sector of an endcap station.) The tasks performed by the trigger motherboard are fully pipe-lined and synchronous with the beam-crossing clock. Another function vital to the operation of the front-end electronics, receiving and fanout of TTC signals to the FEB's, is also located on the trigger motherboard.

DAQ Motherboard - The readout of the data from each FEB is coordinated by the DAQ Motherboard. The digitization of the stored voltage samples on the cathode FEB's and latching of the hits on the anode FEB's are initiated by the arrival on the MB of a Level-1 accept which has a bunch crossing number matching that of an LCT. When this occurs, the readout controllers on the FEB's are notified. Digitization will begin on the cathode FEB's. Those pulse samples stored in the corresponding time window for all 96 channels on the FEB are digitized. The digitized data is sent to the output buffer on the motherboard and transferred by optical link to the central DAQ. The DAQ motherboard also acts as an interface to the Run Control and to Slow Control. The Slow Control functions include down-loading of the FPGA and DSP programs, resetting of the readout controller on the FEB, down-loading calibration information, down-loading commands for turning off bad channels, monitoring of low voltage levels and temperature. JTAG will be used for the slow control.

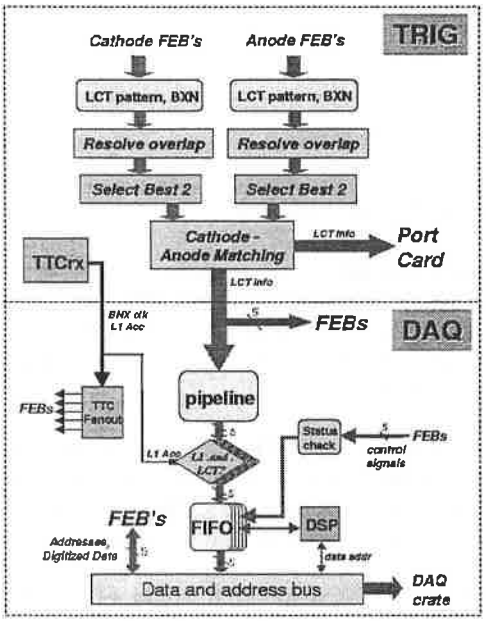

Fig. 9. Functional diagram of the trigger and DAQ motherboards.

Prototype trigger and DAQ motherboards were produced and tested together with the cathode and anode front-end boards in the test beam.

7. DAQ ELECTRONICS IN THE COUNTING ROOM

The DAQ electronics that receives the front-end data will be situated in the underground counting room adjacent to the CMS detector cavern. Each readout crate (6U or 9U VME) will contain standardized front-end driver (FED) boards. The optical data links from the motherboard will be received on PCI-interfaced Mezzanine Cards (PMC) mounted on the FED. These PMC's are detector dependent and they handle data readout/buffering, front-end control and front-end monitoring. Readout from the Mezzanine Cards to the event builder will be performed by a commercial single board PC computer mounted on the FED.

8. SUMMARY

The development of cathode and anode front-end ASIC's for the CMS endcap muon electronics are well advanced. Prototype readout and trigger front-end boards have been produced and tested on full-size CSC in test beams. The preliminary test results demonstrated that key performance requirements of the electronics have been achieved. Next set of prototype electronics will aim to improve rate capability and data throughput rate. The schedule calls for testing of a full-fledged pilot electronics system in the year 2000 before production starts.

Acknowledgements

The work reported here is the joint effort of physicists, engineers and graduate students who are members of the CMS collaboration from the following institutes: Carngie Mellon University, PNPI, Ohio State University, University of California at Davis, University of California at Los Angels, CERN and Rice University. The success of the project owes to the ingenuity and hard work of everyone involved. This work is supported in part by grants from the U.S. Department of Energy.

Refererences

1. The CMS Muon Project, Technical Design Report, CERN/LHCC 97-32, December, 1997.