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A Survey of Microwave-Implemented Superconducting Qubit Control and Readout Circuits

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ABSTRACT Superconducting qubits are pivotal in advancing quantum computing, poised for scale but limited by the complexity and fidelity of their control and readout systems, relying on RF and signal processing infrastructure. This survey serves as a comprehensive and technically grounded review of control and readout architectures tailored for superconducting qubits. Synthesizing insights from device physics, circuit design, microwave engineering, signal processing, and cryogenic integration, this work details the practicalities of RF pulse generation, signal synthesis, and readout signal analysis for quantum systems. It covers key requirements, parameters, and pulse engineering techniques, including commonly used envelopes like Gaussian and DRAG designs. Moving to the system level, this survey systematically classifies and critically analyzes current architectural strategies (covering key areas like frequency conversion, waveform management, and system infrastructure) and technology platforms (including adaptive classical control stacks, cryogenic CMOS circuits, and novel interconnects and interfaces), evaluating their tradeoffs in performance. Extensive literature analysis identifies prevailing limitations such as wiring complexity, thermal budget constraints, latency, and power consumption, while highlighting underexplored opportunities for on-chip signal processing and novel interconnects, drawing analogies to advanced communication system design. By consolidating diverse control paradigms and critically evaluating their tradeoffs, this survey provides a unified foundation for designing next-generation quantum control stacks. Finally, a forward-looking roadmap outlines key trends in monolithic integration, cryo-compatible digital architectures, and physics-informed hardware co-design, offering both a retrospective synthesis and a prospective vision for quantum hardware engineering beyond the noisy intermediate-scale quantum era.

INDEX TERMS Anharmonicity, power efficiency, pulse shaping, quantum control, quantum error correction (QEC), quantum readout, superconducting qubits.

NOMENCLATURE

SNR	Signal-to-noise ratio.
QML	Quantum machine learning.
QuTiP	Quantum Toolbox in Python.
Cryo-CMOS	Cryogenic complementary metal–oxide–semiconductor.
COTS	Commercial off-the-shelf.
AWG	Arbitrary waveform generator.
QEC	Quantum error correction.
IF	Intermediate frequency.
LO	Local oscillator.
DAC	Digital-to-analog converter.
ADC	Analog-to-digital converter.
CORDIC	Co-ordinate Rotation DIgital Computer.
FDM	Frequency-division multiplexing.
API	Application programming interfaces.
NISQ	Noisy intermediate-scale quantum.
MTS	Multitile synchronization.
PLL	Phase-locked loop.
SSB	Single-sideband.

SFDR	Spurious-free dynamic range.
DDS	Direct digital synthesis.
PSD	Power spectral density.
SDR	Software-defined radio.
TDC	Time-to-digital converters.
DRAG	Derivative removal by adiabatic gate.
BER	Bit error rate.
EOM	Electrooptic modulation.
α, β	Complex probability amplitudes of a qubit state.
$\|\psi\rangle$	General quantum state (ket) of a qubit.
$\|\psi\rangle_L$	State of a logical qubit.
α_{DRAG}	Tunable parameter for DRAG pulse shaping.
Γ_1, Γ_ϕ	Energy relaxation and dephasing rates.
ΔR	Change in resistance.
Δt_{jitter}	Timing jitter.
$\Delta\phi$	Error in the microwave drive phase.
σ	Standard deviation of a Gaussian pulse envelope.
χ	Dispersive shift of the resonator frequency.
ω_q, ω_{01}, ω_k	Qubit transition frequency.
ω_R, $\Omega(t)$	Rabi rate/frequency (constant or time-dependent).
ω_r	Readout resonator frequency.
H	Hamiltonian operator.
E_C, E_L, E_J	Charging, inductive, and Josephson energy.
L, C	Inductance and capacitance.
$A(t)$	Time-dependent amplitude envelope of a pulse.
U	Unitary operator.
C_c	Channel capacity (in b/s).
ENBW	Effective noise bandwidth.
f_s	Sampling frequency of a DAC/ADC.
F_G	Gate fidelity.
I, Q	In-phase and quadrature components of a signal.
K_k	Kraus operators for a quantum channel.
Q	Quality factor of a circuit.
$\|s\rangle$	Ancilla or blank quantum state.
$S(\omega)$, $S(f)$	PSD (of noise).
T_1	Amplitude damping/energy relaxation time.
T_2	Phase damping/dephasing time.
$x[n]$	Discrete-time representation of a signal.

I. INTRODUCTION

A. BACKGROUND AND MOTIVATION

Quantum mechanics initially emerged as a theoretical field of study. However, the increasing accumulation of experimental findings progressively revealed the necessity of quantum mechanics for comprehending the physical realm [1], [2], [3], [4]. This initiated a notable era of quantum information processing, characterized by the active research into the quantum revolution. Presently, global efforts such as the National Quantum Technologies Program of the United Kingdom, the Quantum Technology Flagship of the European Union, the National Quantum Initiative of the United States, and a multitude of quantum flagship programs by various nations showcase the potential of this thriving field [5], [6], [7], [8], [9]. According to projections, the quantum technology sector might reach $173 billion by 2040, propelled by enterprises eager to capitalize on its disruptive potential [10]. This will catalyze the emergence of new economic value chains [11], competitive advantages [12], and high-growth opportunities [13].

While global initiatives push the boundaries of quantum research, the computing industry simultaneously faces challenges with classical paradigms, particularly the impending limits of Moore's law [14], [15], [16], [17]. As transistor sizes approach atomic scales due to the advancements in lithographic techniques, continued scaling predicted by Moore's law has become challenging [15], [16]. This limitation in classical scaling demands a paradigm shift in computation, with quantum technologies offering a viable solution for the future.

To overcome the constraints currently hindering progress in achieving quantum advantage, quantum computers emerge as promising avenues for transformative advancement [18], [19], [20], [21]. These superposition-driven qubit-based computers exhibit broad applicability in domains that encompass computationally intensive processes that currently require the capabilities of high-performance computing resources [22], [23], [24], [25], [26], [27], [28], [29], [30]. The five foundational DiVincenzo criteria [31], [32], [33] define the essential requirements for a functional quantum computer. To illustrate how the DiVincenzo criteria translate into practical hardware requirements, Fig. 2 provides representative examples of engineering goals and system-level execution strategies used in practical system design.

Realizing functional quantum processors typically require stable control and readout mechanisms with defined temporal profiles to manipulate the quantum states [34], [35], [36], [37], [38]. The demands placed on this hardware infrastructure evolve significantly through successive evolutionary phases. In the current NISQ era, the objective is to maintain calibration stability and meet minimum error thresholds for gate and measurement fidelity, so that shallow-depth circuits can be executed reliably [10], [39]. The transition to QEC-assisted and early fault-tolerant systems introduces more rigid constraints [40], [41], [42]. Meeting these QEC-assisted requirements entails closing all control actions within the correction-cycle window, providing low-latency decoding in the classical stack, and enabling leakage mitigation to keep the logical error rate decreasing across rounds [43], [44], [45], [46], [47], [48], [49], [50]. Finally, reaching the utility-scale systems regime will shift the focus to achieving long-run system reliability and availability, requiring efficient orchestration of large computational workloads and mitigating superlinear growth in resource overhead [41], [51]. Thus, a technological evolution toward hardware-efficient systems and a synergistic co-design approach integrating qubit fabrication [52], control and readout circuits [53], signal propagation to qubits, and classical signal processing [34] are essential for large-scale computational potential.

FIGURE 1. (a) Table of contents for the survey. (b) Conceptual theme; from fundamentals to techniques, then state-of-the-art, and finally a roadmap.

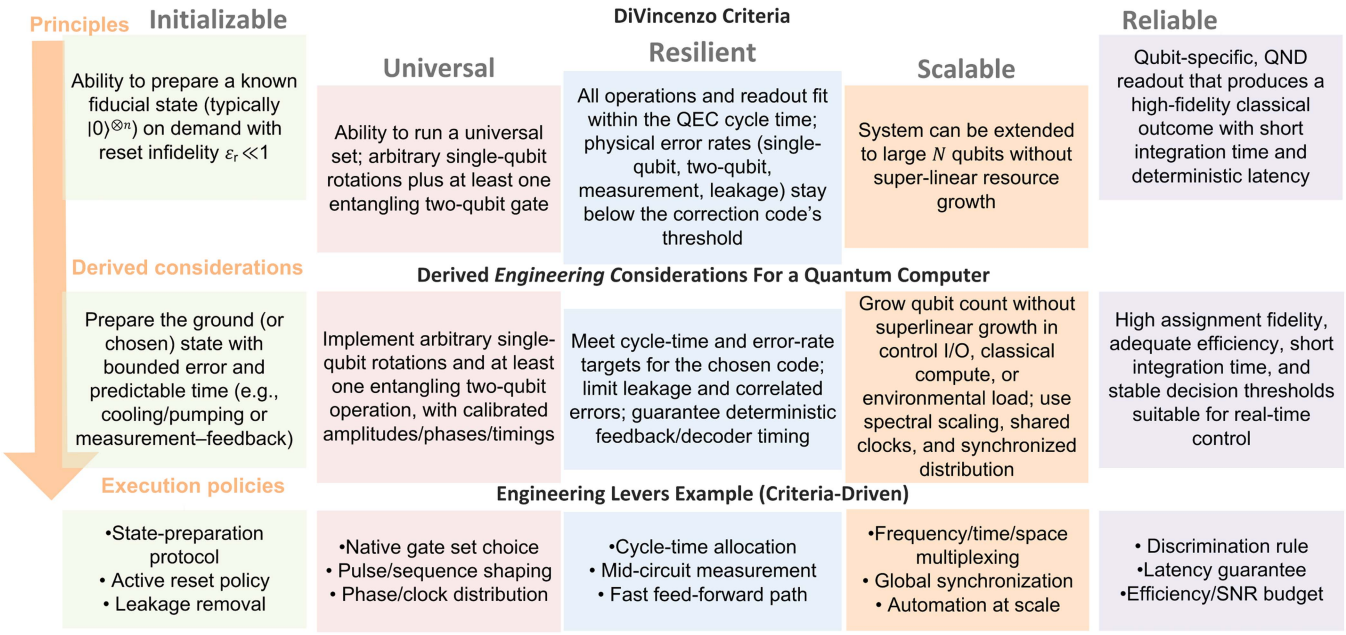

FIGURE 2. Mapping of DiVincenzo criteria to quantum engineering practice. The figure translates each fundamental criterion (Initializable, Universal, Resilient, Scalable, Reliable) into derived engineering considerations and concrete execution policies. Each criterion is linked to a design objective and to example mechanisms used in realization. Engineering-specific approaches often include state-preparation protocols, calibrated single-/two-qubit control, cycle-time and feedback closure for error correction, multiplexed and synchronized scaling, deterministic low-latency measurement, and others, as appropriate to the platform. Quantitative budgets for control and readout system design are summarized in Table 10.

Focusing on the prevalent use of resonant electromagnetic fields for control and readout, this survey presents a structured and comprehensive analysis of techniques employed in microwave-driven superconducting qubit systems. At present, superconducting qubits constitute a leading physical implementation for realizing near-term quantum algorithms [54], [55], [56]. By narrowing its scope to the hardware infrastructure of control and readout systems specifically designed for such implementations, this survey offers a focused examination of a key subsystem within the broader discipline of quantum computing. The overall organization and conceptual flow of this survey are summarized in Fig. 1. Fig. 1(a) provides a section-by-section roadmap, while Fig. 1(b) highlights the progression from fundamentals and key techniques to state-of-the-art systems and future research directions.

B. RELATED SURVEYS AND CONTRIBUTIONS

An examination of prior literature on superconducting qubit control and readout circuits is presented here to articulate the unique scope and focus of this survey.

Kjaergaard et al. [55] provide an overview of experimental advancements in superconducting qubits, covering hardware aspects, gate implementations, error correction, and high-fidelity readout capabilities. However, it primarily offers a broad overview of the state of the art without a dedicated focus on the detailed architectural strategies and hardware stacks for control and readout subsystems. Similarly, Anders et al. [30] survey Cryo-CMOS solutions for superconducting and spin qubits and highlight challenges in signal fidelity, thermal isolation, and scalability. Conversely, it limits itself to integrated circuit (IC) implementations without extending to cross-technological comparisons. Complementing this, Ahmad et al. [57] present a viewpoint on the integration of cryogenic-compatible classical electronics with quantum processors to enable large-scale quantum computing, with a focus on scalable cryo-electronics. However, this work primarily details integrated cryo-electronic solutions, without providing a broader comparative analysis of diverse control and readout architectural pathways and technologies.

The work by Krasnok et al. [58] focuses on superconducting microwave cavities with high Q-factors. The review includes bosonic encodings, material innovations, and the role of high-coherence resonators in qubit stabilization and readout. Nevertheless, the emphasis remains on device-level physics rather than system-wide architectural considerations. A broader survey by Yang et al. [59] surveys quantum protocols, algorithms, fundamentals of QML, hybrid quantum–classical systems, and network infrastructure, but omits a focused discussion on control and readout strategies for physical qubit modalities.

Finally, the work by Brennan et al. [60] presents and analyzes the leading methods for interfacing, highlighting limitations and opportunities for scalability. The survey explores emerging technologies and design strategies, including cryoelectronics and communication methods, essential for building scalable quantum systems. However, this article primarily discusses the limitations of the technologies and approaches for classical interfaces.

Despite the growing body of literature, the establishment of a comprehensive and unified taxonomy of hardware-level control and readout strategies, particularly in the context of superconducting qubit systems, remains an active area of research. This survey seeks to address this critical gap by providing a focused examination of classical control and readout stacks, cryogenic circuit pathways, wireless transceiver-based links, photonic interfaces, and thermal readout approaches.

Specifically, this exploration proposes a stratified classification encompassing architectural strategies for signal generation, routing, and analysis, alongside an analysis of platform-level implementations. It outlines diverse control and readout approaches categorized by frequency planning, signal conversion, pulse waveform synthesis, control architectures, spectral division, readout signal analysis, and software-hardware interface design. Furthermore, this work analyzes design tradeoffs in control and readout architectures from the literature, identifies key near-future research directions, and reviews recent developments and challenges. This work thus contributes to the development of a quantum hardware ecosystem and aims to serve as a valuable resource for academic research, as well as technology translation within the scalable quantum computing hardware landscape.

II. SUPERCONDUCTING QUBITS: PHYSICS, ARCHITECTURES, AND SYSTEM LIMITS

This section highlights the principles and engineering aspects of superconducting qubit hardware, analyzing the generation of qubit states and anharmonicity via Josephson junctions and Hamiltonian engineering. The discussion then transitions to addressing the theoretical and physical constraints (decoherence and noise) that compel the transition toward QEC as the architectural pathway toward fault tolerance and scalable computation.

A. QUBIT ENCODING, SUPERPOSITION, AND STATE ADDRESSABILITY

Qubits, the fundamental units of quantum information, enable quantum computation [61], [62], [63]. Classical bits assume two mutually exclusive states (0 or 1), whereas qubits can exist in a superposition of states. The arbitrary qubit state ($|\psi\rangle$) can be represented as a linear combination of the basis states (typically $|0\rangle$ and $|1\rangle$), as follows:

$$|\psi\rangle = \alpha|0\rangle + \beta|1\rangle \tag{1}$$

where α and β are complex numbers satisfying the normalization condition $|\alpha|^2 + |\beta|^2 = 1$. This property allows quantum bits to execute concurrent computational operations. Upon measurement, the superposition collapses to a classical outcome: $|0\rangle$ occurring with probability $|\alpha|^2$ and $|1\rangle$ occurring with probability $|\beta|^2$.

In superconducting qubit systems, the computational states are realized as the ground state ($H|0\rangle = E_0|0\rangle$) and the first excited state ($H|1\rangle = E_1|1\rangle$), with E_0 and E_1 representing the corresponding energy eigenvalues. The engineered nonlinear Hamiltonian of the system yields anharmonic energy spectrum where transition frequencies are distinct ($f_{01} \neq f_{12} \neq f_{23} \ldots$), enabling selective addressability and isolation of the computational subspace.

B. ANHARMONIC SPECTRUM GENERATION WITH JOSEPHSON JUNCTIONS

The linear and anharmonicity-induced characteristics of a quantum harmonic oscillator (*LC* resonant circuit) are depicted in Fig. 3(a). The quantum *LC* oscillator, composed of a linear inductor and capacitor, is governed by the Hamiltonian in the following equation [64]:

$$H = 4E_C n^2 + \frac{1}{2}E_L\phi^2 \tag{2}$$

where $E_C = \frac{e^2}{2C}$ is the charging energy and $E_L = \left(\frac{\Phi_0}{2\pi}\right)^2 / L$ is the inductive energy, with $\Phi_0 = \frac{h}{2e}$ denoting the superconducting magnetic flux quantum. The equidistant energy level structure of a harmonic oscillator and the proximity of the energy levels can make it challenging to isolate the desired two-level systems from higher energy eigenstates. To introduce nonlinearity to the system, a Josephson junction [65] is introduced, contributing a nonlinear potential. The modified Hamiltonian results in

$$H = 4E_C n^2 - E_J \cos(\phi) \tag{3}$$

where $E_C = \frac{e^2}{2C_{\text{sum}}}$, $C_{\text{sum}} = C_{\text{Junction}} + C_{\text{Shunt}}$, and $E_J = \frac{I_C\Phi_0}{2\pi}$. The inclusion of a nonlinear element enables nonequidistant energy levels, leading to a deviation from a purely linear energy response. These junctions induce anharmonic energy spectra that deviate from the ideal harmonic oscillator [66], [67]. Consequently, the application of narrowband excitation pulses characterized by their amplitude, duration, spectrum, temporal profile, and modulation envelopes allows for control over the computational states.

C. ENCODING IN SUPERCONDUCTING QUBITS AND ANHARMONICITY

Various modalities of superconducting qubits have been developed, each defined by their primary quantum degree of freedom in which information is encoded [55]. The modalities include charge (such as Cooper-pair box), magnetic flux (such as rf-SQUID), or macroscopic phase (such as Josephson phase qubit). These modalities originate from the quantization of Josephson-junction-based circuits incorporating capacitive (*C*), inductive (*L*), and nonlinear Josephson elements [68].

Among these, the transmon qubit, a widely adopted variant, emerges from the charge qubit architecture by operating in the highly shunted $E_J/E_C \gg 1$ regime [69]. Here, $E_J = \Phi_0 I_c/(2\pi)$ is the Josephson energy (where Φ_0 is the magnetic flux quantum and I_c is the junction critical current), and $E_C = e^2/(2C_\Sigma)$ is the charging energy (where e is the elementary charge and C_Σ is the total qubit capacitance). In this

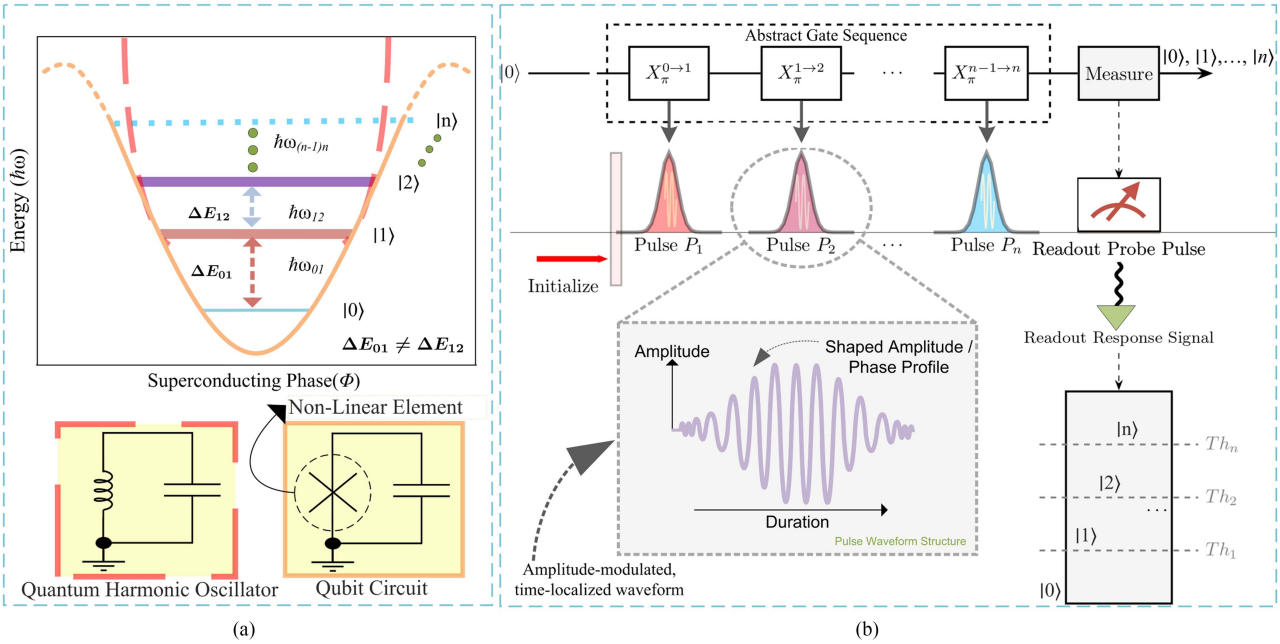

FIGURE 3. Overview of anharmonic energy levels and multilevel control/readout scheme in a superconducting quantum system. (a) Anharmonic potential, created by a Josephson junction (bottom right), results in nonequidistant energy levels ($\Delta E_{01} \neq \Delta E_{12}$). This key property, in contrast to a linear harmonic oscillator (bottom left), enables frequency-selective addressing of individual transitions. (b) Connection between abstract gates and their physical implementation. The abstract gate $X_{\pi}^{(k-1)\to k}$ is defined as a selective π-pulse. Here, X denotes an excitation or "bit-flip" operation between two adjacent levels, and the subscript π refers to the pulse area, which is precisely calibrated to drive a full Rabi rotation of angle π. This results in a complete 100% population transfer from the initial state $|k-1\rangle$ to the target state $|k\rangle$. The operation is selective because its frequency is tuned only to the $|k-1\rangle \leftrightarrow |k\rangle$ transition, leaving all other energy levels unaffected. This selectivity is achieved by tuning each physical microwave Pulse P_k to a unique transition frequency ($\omega_{k-1,k}$). The inset magnifies one such pulse, showing a high-frequency carrier shaped into a time-localized control pulse whose calibrated area implements the π rotation. Finally, to perform multilevel readout, a readout probe pulse is sent to a resonator coupled to the qubit. Due to the dispersive interaction, each qubit state ($|0\rangle, |1\rangle, \ldots, |n\rangle$) imparts a unique frequency shift on the resonator. This causes the readout response signal (the reflected or transmitted pulse) to have a state-dependent amplitude and phase. Finally, this analog signal is mapped to a digital state by comparing it against a series of precalibrated thresholds ($Th_1, \ldots, Th_n$).

convention, the effective charging energy for a Cooper pair is $4E_C$. This large ratio suppresses sensitivity to charge noise by effectively flattening the energy potential at the cost of reduced anharmonicity. Conversely, flux qubits encode information in persistent circulating supercurrents, representing distinct magnetic flux quanta states within a multiply connected superconducting loop [61]. Fluxonium qubits extend this concept by introducing a large shunting superinductance, resulting in low E_C (or equivalently, high E_J/E_L, where E_L is the inductive energy). This unique design enables large anharmonicity (>1 GHz) and extended coherence [70] with a suppressed zero-point energy. Table 1 offers a comparison of various types of superconducting qubit modalities.

D. JOSEPHSON-JUNCTION-DRIVEN SYMMETRIC AND ASYMMETRIC TRANSMON ARCHITECTURES

In a symmetric transmon, two identical Josephson junctions are employed to thread the entire loop with the magnetic flux, leading to a total Josephson energy

$$E_J^{\text{sym}}(\varphi_e) = 2E_J \left|\cos(\varphi_e)\right| \tag{4}$$

where φ_e is the normalized external flux, and E_J is the Josephson energy of an individual junction. Substituting this into the Hamiltonian yields

$$H = 4E_C n^2 - 2E_J \left|\cos(\varphi_e)\right| \cos(\phi)\,. \tag{5}$$

The Josephson energy E_J varies from zero to a maximum of $2E_J$. In a symmetric transmon, at flux bias points of odd half-integer multiples of the flux quantum $\Phi_0 = \frac{h}{2e}$, the Josephson inductance diverges, resulting in the transition energy vanishing [71]. Unlike a symmetric transmon, the asymmetric transmon avoids the complete suppression of transition energy at half-integer flux quantum points. The asymmetry ensures that the transmon qubit maintains a finite transition energy, leading to a twofold increase in the number of flux-insensitive spots. Furthermore, the energy dispersion curve becomes more linear, allowing better frequency tunability and faster gate operations [72]. The flux-dependent effective Josephson energy for this asymmetric SQUID is then given by

$$E_J(\varphi_e) = E_{J\Sigma}\sqrt{\cos^2(\varphi_e) + d^2\sin^2(\varphi_e)}. \tag{6}$$

Substituting this Josephson energy into the Hamiltonian, it becomes

$$H = 4E_C n^2 - E_{J\Sigma}\sqrt{\cos^2(\varphi_e) + d^2\sin^2(\varphi_e)}\cos(\phi) \tag{7}$$

TABLE 1. Comparison of Different Superconducting Qubit Modalities

Qubit type	Encoding variable	E_J/E_C Regime	Anharmonicity (α)	design features/Limitations
Charge qubit	Charge ($\hat{n}$)	$\ll 1$	High ($\sim E_C$)	High sensitivity to charge noise; largely historical
Transmon	Energy eigenstates (charge/phase)	$\gg 1$	Low ($\sim -E_C/10$)	Charge noise protected; weak nonlinearity; scalable
Flux qubit	Persistent current (flux)	$\gg 1$	Medium ($\sim$ GHz)	Requires precise flux bias; susceptible to flux noise
Fluxonium	Fluxon states (hybrid)	$\gg 1$ (high E_J, low E_L)	Tunable ($>$ GHz)	High coherence; complex fabrication; low frequency
Phase qubit	Phase (ϕ)	~ 1 (or high E_J/E_C)	Medium	Limited coherence; measurement backaction; less prevalent

whereas the flux-dependent total Josephson energy is given as follows [73]:

$$E_J(\Phi) = E_{J\Sigma}\left|\cos\left(\frac{\pi\Phi}{\Phi_0}\right)\right|\sqrt{1+d^2\tan^2\left(\frac{\pi\Phi}{\Phi_0}\right)}. \quad (8)$$

E. FLUX-ENHANCED SUPERCONDUCTING QUBIT ARCHITECTURES

By engineering three or more junctions into the qubit loop through utilization of more junctions, the design offers more flexibility in shaping the energy potential. To realize flux tunability, architectures such as asymmetric and C-shunted flux qubits incorporate multiple Josephson junctions and controlled asymmetry. This can lead to enhanced coherence and increased anharmonicity [64], [78], [79].

With N number of array junctions [80], [81], the Hamiltonian assumes the following approximate form:

$$H \approx 4E_C n^2 - E_J\cos(\phi+\varphi_e) + \frac{1}{2}E_L\phi^2 \quad (9)$$

where $E_L = \frac{\gamma}{N}E_J$ refers to the net inductance contributed by the array junctions (and γ is a parameter related to the junction properties). These modalities, illustrated in Fig. 4, represent key superconducting qubit designs, each employing distinct Josephson junction configurations. For a more mathematical analysis on Hamiltonian engineering, readers are encouraged to consult [64], [82].

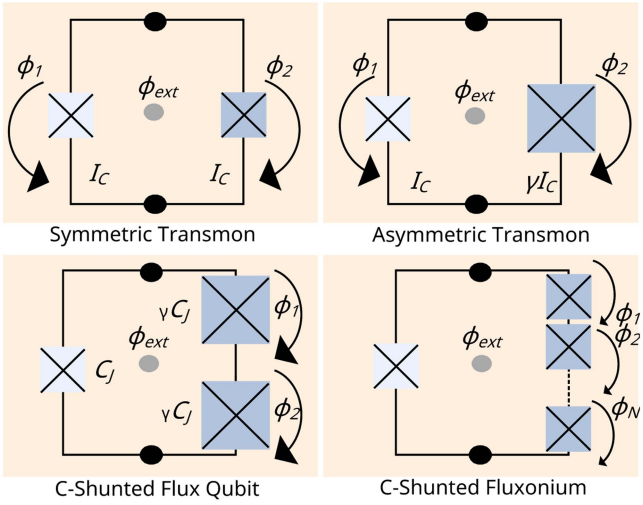

FIGURE 4. Schematic representations of different types of superconducting qubit modalities. These qubits leverage Josephson junctions (white and blue elements) and external flux to achieve distinct anharmonicity. The design of this figure has been inspired by the work in [64].

F. LIMITATIONS IN QUANTUM INFORMATION

Quantum computation, though offering many benefits, is subject to both theoretical and physical limitations that constrain its practical realization. Theoretical limits such as the no-cloning theorem and physical processes such as decoherence do not preclude quantum computation, but impose certain constraints on its practical implementation, shaping the approaches to fan-out, algorithm debugging, state distribution, and error-mitigation strategies. In what follows, we formalize the no-cloning constraint and its operational consequences.

1) THEORETICAL LIMIT: NO-CLONING THEOREM

The no-cloning theorem states that it is impossible to create an identical copy of an unknown quantum state. This theorem is a consequence of the linearity of quantum mechanics. Suppose that there exists a unitary operator U that could replicate an arbitrary quantum state $|\phi\rangle$ onto a blank state $|s\rangle$

$$U(|\phi\rangle\otimes|s\rangle) = |\phi\rangle\otimes|\phi\rangle. \quad (10)$$

However, this operation would contradict the linearity of quantum mechanics. Consider two distinct quantum states $|\phi\rangle$ and $|\psi\rangle$. If U is to clone these states, then

$$\begin{cases} U(|\phi\rangle\otimes|s\rangle) = |\phi\rangle\otimes|\phi\rangle \\ U(|\psi\rangle\otimes|s\rangle) = |\psi\rangle\otimes|\psi\rangle. \end{cases} \quad (11)$$

Therefore, there is no unitary/completely positive and trace-preserving (CPTP) map that performs perfect and deterministic cloning of an unknown quantum state [83]. This has the following operational consequences.

1) *No universal fan-out:* A unitary cloning operation, $U(|\psi\rangle\otimes|0\rangle^{\otimes(k-1)}) = |\psi\rangle^{\otimes k}$, is forbidden for an arbitrary state $|\psi\rangle$ when $k \geq 2$. Perfect cloning is restricted to states belonging to a known orthogonal basis [84], as demonstrated by the CNOT operation: CNOT $|x\rangle|0\rangle = |x\rangle|x\rangle$, for $x \in \{0, 1\}$.
2) *No copy-and-forward repeaters/noiseless amplification:* Classical-style repeaters that duplicate an

unknown input are not allowed; long-distance distribution must, therefore, rely on entanglement-based primitives and teleportation [85].

3) *No checkpointing/backup of unknown states:* A map $|\psi\rangle \mapsto |\psi\rangle \otimes |\psi\rangle$ for an unknown $|\psi\rangle$ is not physically realizable. Consequently, architectural strategies involving computational rollback must be designed to avoid duplicating the unknown quantum information.
4) *Redundancy via encoding, not replication:* Protection against noise cannot be obtained by making extra copies of an unknown quantum state, because universal cloning is forbidden. Instead, fault-tolerant schemes use an isometric encoding $V : \mathcal{H}_L \to \mathcal{H}_C \subseteq \mathcal{H}_P$ (e.g., stabilizer codes) and syndrome measurements that extract error information. The Knill–Laflamme condition [86] characterizes this: for the projector P onto the codespace and for errors $\{E_a\}$,

$$PE_a^\dagger E_b P = c_{ab} P$$

where c_{ab} is a Hermitian matrix of complex scalars. This means that, within the codespace, different error events remain distinguishable, while the logical state itself is not revealed. For a more mathematical analysis of Knill–Laflamme condition, readers are encouraged to consult [87], [88] or the original reference [86].

2) PHYSICAL LIMITS: DECOHERENCE AND NOISE MECHANISMS

Quantum systems couple to their environment and are, therefore, susceptible to decoherence and noise [89]. The dynamics of such open quantum systems are described using various mathematical frameworks, including Lindblad equations [74], Kraus operator representations [90], and stochastic differential equations [91]. A commonly encountered noise process in qubit systems is amplitude damping, which models energy relaxation from the excited state $|1\rangle$ to the ground state $|0\rangle$. A two-level system undergoing amplitude damping, for instance, may evolve as follows:

$$\frac{d\rho(t)}{dt} = \mathcal{L}_{AD}(\rho) = \frac{1}{T_1}\left(\sigma_- \rho \sigma_+ - \frac{1}{2}\{\sigma_+\sigma_-, \rho\}\right) \quad (12)$$

where $\rho(t)$ is the density matrix, $\sigma_\pm$ are the qubit ladder operators, and $\{A, B\} = AB + BA$ is the anticommutator. In parallel, phase damping (or dephasing) describes the loss of quantum phase information without energy loss. It can be modeled via the Kraus operator formalism [92] as

$$\mathcal{E}(\rho) = K_0 \rho K_0^\dagger + K_1 \rho K_1^\dagger \quad (13)$$

with K_0 and K_1 as Kraus operators, and characterized by T_2. Together, these two processes dominate decoherence in most current qubit platforms. Discrete noise events are modeled using the quantum channel formalism. The action of any noise channel can be described by a set of Kraus operators $\{K_k\}$ acting on the density matrix ρ

$$E(\rho) = \sum_k K_k \rho K_k^\dagger \quad \sum_k K_k^\dagger K_k = I. \quad (14)$$

This single framework captures various physical noise processes by defining the appropriate operators.

In addition, stochastic (time-fluctuating) noise effects further degrade quantum coherence. The noise modeling is usually done through stochastic equations, rather than deterministic equations. For semiclassical treatments, a Langevin-type description [93] can be used to model the fluctuating field or force.

Finally, non-Markovian dynamics can be modeled by more complex non-Markovian equations, like the Nakajima–Zwanzig equations (integro-differential equations) [94] or time-convolutionless approaches. A summary of major noise and decoherence mechanisms is provided in Table 2.

G. QUANTUM ERROR CORRECTION: A PATH TO FAULT TOLERANCE

QEC is an essential methodology for reducing the detrimental effects of noise and decoherence in quantum systems, enabling a path toward fault-tolerant quantum computation [95], [96]. The basic principle of QEC is to encode a logical qubit $|\psi\rangle_L$ in a larger Hilbert space, distributed across multiple physical qubits [97], [98], [99]. This redundancy allows the system to detect and correct errors without directly measuring the quantum state, thereby preserving coherence and avoiding the cloning constraint. The logical qubit resides in the subspace of states stabilized by a set of stabilizer operators [100].

In practice, various QEC codes have been developed, each offering different advantages for mitigating specific types of errors. The notable ones are listed as follows.

1) *Shor's code [116], [117]:* Shor's code was the first QEC code, proving that fault-tolerant quantum computing is theoretically possible. It protects a single logical qubit by encoding it across nine physical qubits, a structure created by combining a three-qubit bit-flip code with a three-qubit phase-flip code. This design allows it to correct a single-qubit error. The logical basis states, $|0_L\rangle$ and $|1_L\rangle$, are defined as

$$|0_L\rangle = \frac{1}{2\sqrt{2}}(|000\rangle + |111\rangle)^{\otimes 3}$$

$$|1_L\rangle = \frac{1}{2\sqrt{2}}(|000\rangle - |111\rangle)^{\otimes 3}.$$

2) *Calderbank–Shor–Steane (CSS) codes [118], [119]:* CSS codes generalize Shor's code by using two classical codes to correct bit-flip and phase-flip errors independently. The seven-qubit Steane code [120] is a well-known example. These codes underlie many modern stabilizer-code constructions.
3) *Surface codes:* Surface codes are topologically based and offer high error thresholds with local interactions,

TABLE 2. Quantum Noise and Decoherence Mechanisms: A Nonexhaustive Overview

Noise mechanism (Category)	Phenomenological description	Key impact on qubits	Physical origins and reduction
Environmental coupling(system-bath interaction)	Interaction of the quantum system ($\mathcal{S}$) with an external environment ($\mathcal{B}$) via an interaction Hamiltonian ($\mathcal{H}_{SB}$)	• Leads to decoherence through uncontrolled interactions • Evolution described by open quantum system dynamics (e.g., Lindblad master equation [74])	• Ubiquitous source of error • Reduced via shielding, isolation, dynamical decoupling
Decoherence (loss of coherence)	Irreversible loss of superposition and entanglement, leading to a transition from quantum to classical behavior	• Causes collapse of qubit states into classical mixtures • Affects algorithm accuracy	• Fundamentally linked to environmental coupling • Reduction using QEC, coherence protection techniques
Amplitude damping (energy relaxation)	Non-unitary evolution causing transitions from excited states to ground states due to energy dissipation	• Reduces qubit T_1, impacting gate fidelity and memory time	• Caused by spontaneous emission, dielectric loss; • Mitigated by cryogenics, low-loss materials
Phase damping (dephasing)	Random phase fluctuations in superposition states	• Reduces pure dephasing time (T_ϕ), which limits total coherence time (T_2), limiting interference-based quantum operations	• Driven by flux/charge noise • Mitigated using spin echo, noise filtering
Stochastic noise (random fluctuations)	Irregular external disturbances affecting system dynamics	• Introduces instability in gate operations and readout reliability • Described by stochastic differential equations (e.g., Langevin equation [75])	• Caused by thermal/electromagnetic noise • Reduced via fine control, filtering
Quantum channel noise (model representation)	Mathematical formalism describing the transformation of quantum states due to noise	• Captures bit-flip, phase-flip, depolarizing effects seen in real systems	• Basis for error correction design; • Mitigated via channel-specific corrections
Non-Markovian noise (memory effects)	Noise with time-correlated fluctuations, where past environmental states influence future qubit states	•Leads to unpredictable time-correlated errors difficult to model or correct • Described by non-Markovian master equations (e.g., Nakajima-Zwanzig equation [76], [77])	• Strong coupling or structured baths • Reduced through adaptive control, simulation
Readout noise	Errors and uncertainties introduced during the measurement of qubit states	• Causes misclassification of states, reducing measurement fidelity	• Limited detector SNR • Reduced through signal averaging, improved hardware

making them particularly attractive for large-scale quantum systems [121]. These codes require nearest neighbor interactions, making them suited for physical systems such as superconducting qubits [121], [122], [123]. Surface codes are defined on a 2-D lattice with qubits on edges. Stabilizers are local and consist of

$$A_v = \prod_{i \in \text{star}(v)} X_i \quad B_p = \prod_{i \in \text{boundary}(p)} Z_i$$

where A_v are vertex (star) operators and B_p are plaquette (face) operators. Logical operators span nontrivial cycles on the lattice. Surface codes have demonstrated robustness to errors and are currently one of the most studied QEC codes in the field [124].

4) *Toric codes:* Toric codes are another type of a topological QEC code defined on a torus [124], [125]. They use noncontractible loops for encoding and offer high error threshold. They are closely related to surface codes but operate in a different geometry.
5) *Color codes:* A family of topological codes defined on lattices where the faces are 3-colorable, which exist in both 2-D and 3-D geometries [126], [127]. Their advantage over surface codes is their capacity for transversal logical gates [126]. They offer a more efficient path to universal fault-tolerant quantum computation but at a cost of implementation complexity.
6) *Cat codes:* Cat codes are a type of bosonic code that encode a logical qubit into quantum superpositions of coherent states within a single harmonic oscillator (like a microwave cavity) [128]. The logical states are defined by their distinct photon number parity (even or odd). In cat codes, a single-photon loss event flips the photon number parity, projecting the state out of the logical subspace and enabling detection through syndrome measurements [129]. Cat codes are nontopological but are relevant for continuous-variable quantum systems.
7) *Low-density parity-check codes:* These codes are general-purpose error correction codes that have been

TABLE 3. Summary of Qubit Types, Typical Control Requirements, Readout Techniques, and Key Challenges

Superconducting qubits	
Physical realization	Persistent currents in superconducting loops [64]
Control requirement	Microwave pulses for transitions [101]; Operated in cryogenic environment [102]
Readout technique	Dispersive readout via coupled resonators [101]; Cryo-LNAs
Key challenges	Dilution refrigeration; Susceptibility to environmental noise
Realized scale	Realized at the thousand-qubit scale
Trapped Ion qubits	
Physical realization	Electronic states of trapped ions [103]
Control requirement	Laser beams or magnetic gradients for addressing [104]; Vacuum environment to minimize background gas [105]
Readout technique	State-dependent fluorescence [103]; Quantum logic spectroscopy [106]
Key challenges	Complex apparatus; Limited multi-ion scalability
Realized scale	Realized at the tens-to-hundreds-of-qubits scale, often with high connectivity
Neutral Atom qubits	
Physical realization	Electronic states of neutral atoms in optical lattices [107]
Control requirement	Laser system for trapping, cooling, and manipulating atoms [108]; Optical lattices or tweezer arrays [109]
Readout technique	Fluorescence imaging [110]; Rydberg excitation for entanglement/readout [108]
Key challenges	High laser stability; Experimental complexity
Realized scale	Realized at the thousands-of-qubits scale (e.g., 6,100-qubit arrays for simulation)
Semiconductor qubits	
Physical realization	Electron spin states in quantum dots [111], [112]
Control requirement	Electrical gating [111]; Microwave pulses [111]
Readout technique	Spin-to-charge conversion [113]; SET-based detection [114]
Key challenges	Charge noise; Fidelity of two-qubit gates
Realized scale	Realized at scales of several to tens of qubits
Photonic qubits	
Physical realization	Polarization or path of photons [115]
Control requirement	Optical elements for qubit manipulation; Nonlinear optical interaction for entanglement generation [115]
Readout technique	Photon detectors for detecting qubit states
Key challenges	Photon loss phenomena; Non-destructive detection
Realized scale	Realized at the hundreds-of-modes scale (boson sampling) and tens-of-qubits scale

adapted for quantum systems [130]. They are particularly useful for error detection and correction but still face challenges in practical implementation in quantum hardware.

Recent landmark results have demonstrated surface code operation below the threshold using a 72- and 105-qubit processor, showcasing a significant advance in the QEC scaling law [131]. Although we highlight representative QEC architectures and principles here, the design, implementation, and optimization of QEC constitutes an expansive research domain in itself. A full exposition, including decoding algorithms, syndrome extraction protocols, and hardware-adapted codes, is outside the scope of this survey.

H. CONTEMPORARY QUBIT IMPLEMENTATIONS

Diverse physical systems have been explored to encode the quantum information to realize a functional quantum computer. Each approach presents unique challenges and inherent advantages, influencing their suitability for specific quantum computing applications. Table 3 offers a comparison of prominent contemporary qubit technologies, highlighting their key characteristics and potential applications.

III. SYSTEMATIZING CONTROL AND READOUT DESIGNS

A diverse hardware ecosystem has developed, providing a range of possibilities suited to particular performance parameters. These design varieties balance size, complexity, and performance to support foundational research, educational angles, and the scalability of future quantum processors. As these platforms scale, the abstract features of quantum mechanics, such as superposition, entanglement, and coherence,

TABLE 4. Mapping Quantum Principles to Microwave Signal Generator Hardware Resources

Quantum principle	Hardware demand	Resource implication
Superposition	Precise amplitude/phase control	DAC resolution, ADC sampling rate
Entanglement	Synchronized pulse delivery	Multichannel DACs, timing precision
Coherence time	Rapid gate execution and readout	High DAC/ADC bandwidth, Low-latency control
State-space scaling	High qubit count I/O	Increased DAC/ADC channels/ N:1 multiplexing, Cryogenic power (mW/qubit)
Unitarity	Minimize signal distortion/noise	Low-noise figure amplifiers, Cryogenic power budget (mW-W)

become drivers of control precision and channel count, as outlined in Table 4.

The exponential scaling of state space imposes certain hardware demands. To maintain coherence and enable accurate state manipulation, high-precision control is required. As the number of qubits increases, hardware components, such as multichannel DAC, high-bandwidth ADC, and low-noise amplifiers, are necessary to manage the complexity of operations like superposition and entanglement, as highlighted in Table 4. The requirement for enhanced control precision and synchronization in quantum gate operations tends to drive a corresponding increase in the resource scaling of the quantum hardware stack.

A. ESSENTIAL REQUIREMENTS FOR CONTROL AND READOUT

Table 5 presents a focused overview of the essential control and readout requirements for superconducting qubit manipulation and state measurement. The requirements are structured across single-qubit, two-qubit, and readout functionalities. Researchers anticipate that ongoing research and technology translation will lead to further refinements and identification of new design criteria. The following discussion elaborates on the theoretical relationships and design dependencies summarized in Table 5. The analytical forms for fidelity loss and the associated modeling assumptions are primarily adapted from [134], with further refinements from recent experimental and system-level studies.

1) FREQUENCY AND PHASE STABILITY

Accurate frequency alignment between the control microwave source and the qubit transition frequency ω_{01} is essential for resonant single-qubit rotations. A detuning $\Delta\omega_{mw} = \omega_{mw} - \omega_{01}$ introduces an unwanted Z-axis component during an intended X or Y gate. For a rectangular pulse and small errors, the resulting fidelity degradation follows the second-order form reported in [134]:

$$F_{X,Y} \approx 1 - \frac{1}{2}\left(\frac{\Delta\omega_{mw}}{\omega_R}\right)^2 \left[1 - \cos(\theta)\right] \tag{15}$$

where ω_R is the Rabi rate and θ is the intended rotation angle. For MHz-scale Rabi rates, tens of kilohertz of carrier-frequency error already push single-qubit fidelities into the 10^{-3}–10^{-4} range, so tight frequency synthesis and stabilization are required [134]. While increasing the Rabi rate (by using higher drive amplitude and shorter pulses) improves tolerance to frequency and amplitude inaccuracies, this advantage is limited by the available qubit (Larmor) frequency and by the phase-noise performance of the LO, as noted in [134]. This imposes stringent requirements on frequency synthesis and stabilization, motivating phase-locked references and DDS-based fine tuning [152]. Phase accuracy is equally important because the microwave phase defines the rotation axis on the Bloch sphere; a random or systematic phase error $\Delta\phi$ leads to

$$F_{X,Y} \approx 1 - \frac{1}{2}\Delta\phi^2\left[1 - \cos(\theta)\right]. \tag{16}$$

Achieving 99.9% fidelity thus requires phase stability on the order of $\Delta\phi \approx 0.03$ rad (1.8°), which in turn demands low phase-noise LOs, careful I/Q calibration, and short-term coherence across channels in multiqubit systems [153].

2) AMPLITUDE ACCURACY AND PULSE SHAPE FIDELITY

The amplitude of the control microwave pulse (or, equivalently, the chosen pulse duration) determines the rotation angle $\theta = \omega_R T$, where T is the pulse duration. Additive amplitude noise with spectral density $S_{\mathrm{add}}(\omega)$ produces over- or underrotations on the Bloch sphere, leading to state-preparation errors and gate infidelity. Although analytical treatments of control-induced infidelity typically assume idealized rectangular pulse envelopes, the fundamental requirement is independent of waveform: relative amplitude fluctuations must be suppressed to a level where their contribution to gate error remains negligible compared to intrinsic decoherence mechanisms [142], [143]. Achieving single-qubit fidelities compatible with fault-tolerant thresholds thus demands control precision significantly exceeding that of conventional microwave electronics. Nonideal envelope generation or distortion by the microwave chain alters the spectral content of the drive and introduces off-resonant excitation or leakage into higher transmon levels. Path calibration compensates for cable dispersion, amplifier compression, and mixer imbalance to preserve the intended temporal and spectral pulse characteristics.

3) FREQUENCY NOISE, SPURIOUS TONES, AND THERMAL CONTRIBUTIONS

Time-dependent fluctuations in the control frequency, described by the PSD of phase noise $S_\phi(\omega)$, translate into frequency noise via $S_\omega(\omega) = \omega^2 S_\phi(\omega)$. These fluctuations lead to stochastic phase accumulation and effective dephasing,

TABLE 5. Selected Control and Readout Parameters Influencing Superconducting Qubit Fidelity and Architecture-Level Integration

Parameter	Requirement / Specification	Circuit / System design considerations
I. Single-qubit operations		
Microwave carrier frequency accuracy	Precise alignment with qubit transition frequency [132], [133], [134]	Frequency stabilization using a reference oscillator as master clock; direct digital synthesis (DDS) for fine frequency control [101], [135]
Microwave Carrier Phase Accuracy	High phase stability and accuracy for gate axis control [136], [137]	Low-phase-noise Local Oscillator (LO) design to minimize phase jitter; account for high-frequency phase noise and I/Q calibration errors [138]
Microwave carrier frequency noise	Low-frequency noise critical for stable Rabi oscillations [134]	Low-noise Phase-Locked Loop (PLL) and oscillators [139]; flicker and wideband noise filtering [140]; band-pass filtering [141]
Signal path bandwidth and flatness	Wide and flat response across control and readout chains to avoid pulse distortion and spectral filtering	Wideband amplifiers, mixers, and filters with minimal group delay; impedance matching; careful cable selection and equalization
Pulse Shape Fidelity	High fidelity of generated pulse shapes to minimize leakage and spectral broadening	Arbitrary Waveform Generator (AWG) limitations (resolution, sample rate); linear microwave chain and impedance matching; calibration of path-dependent distortions
Pulse shape selection	Balance gate speed (duration) against spectral leakage (shape) to minimize crosstalk and off-resonant errors	Control software defines envelope; AWG with sufficient memory and sample rate for complex shapes
Microwave Signal Amplitude Noise	Low amplitude noise to ensure accurate Bloch rotations and reproducible pulse areas [134]	Design of low-noise microwave generator output stage [142]; minimize thermal noise contribution and drift [143]
Spurious tones	Suppress spurious tones from nonlinearities and mixer leakage to prevent off-resonant excitation [134]	Harmonic rejection filtering, shielding, and control of nonlinearities in DACs and mixers [144], [145]
AC stark shift / Bloch–Siegert effect	Minimize or compensate for frequency shifts due to off-resonant driving fields	Use adiabatic pulses with optimized duration and power; pre-compensation via calibration or spectroscopy
Residual thermal noise	Minimize thermal noise coupled into the drive line to preserve idle fidelity [134]	Low-noise amplifier design with minimal back-action [146]; thermal anchoring and attenuation at cryogenic stages
II. Two-qubit operations		
Relative qubit frequency control	Stabilize qubit transition frequencies ($\omega_{0,A}$, $\omega_{0,B}$) for spectral isolation and reproducible gate timing	Filtering and shielding to suppress flux noise and cross-coupling; electronics for independent frequency tuning [147]
Tunnel coupling control	Precisely modulate interqubit coupling strength (t_0) for controlled entanglement	Fixed coupling: design of coupler element; tunable coupling: flux-tunable coupler architecture [148]
Qubit Parameter Inhomogeneity	Accommodate device-to-device variations in frequency, anharmonicity, and coherence across the processor	Wideband control electronics to address a range of qubit frequencies; flexible frequency planning software; robust, automated calibration routines for each qubit
Detuning control	Maintain accurate detuning between interacting qubits to avoid leakage and phase errors	Control electronics driving flux bias lines for independent frequency tuning [147], [149]
Pulse timing	Synchronize qubit and coupler pulses to maintain phase-aligned unitary evolution	Multi-channel AWGs with shared clock domains and sub-ps jitter; active skew compensation across coupler and qubit channels
III. Qubit readout		
Measurement chain Noise	Suppress additive and phase noise in readout chain to preserve qubit state contrast	Cryogenic LNAs with low T_{sys} and impedance matching [150], [151]; shielding, low-pass filtering, and thermal anchoring
Integration time	Optimize readout window to balance SNR, speed, and decoherence constraints	High-resolution ADCs with matched bandwidth; matched-filter processing for readout envelopes
Measurement-induced dephasing	Minimize back action on idle qubits due to measurement cross-talk	Optimize $\bar{n}$ and κ for minimal dephasing; isolation via directional couplers and temporal windowing

particularly during idle periods or long sequences [154]. The use of low-noise PLL and oscillators is, therefore, essential [139]. Filtering of flicker and wideband noise components in the baseband and RF paths further suppresses long-term drift and random phase jitter [140].

Nonlinearities in mixers, amplifiers, or DACs introduce spurious frequency tones that can resonantly drive neighboring transitions or parasitic modes [134]. To mitigate these effects, cryogenic shielding, harmonic rejection filters, and linear amplification stages are employed [144], [145]. Furthermore, residual thermal noise from higher temperature stages contributes broadband amplitude and phase fluctuations, which are visible in the measured noise spectral density and reduced through proper

thermal anchoring and attenuation at each temperature stage [146].

4) TWO-QUBIT INTERACTION AND TIMING CONTROL

Two-qubit entangling gates depend sensitively on the controlled exchange of energy between qubits (or between a qubit and a tunable coupler element). The interaction Hamiltonian typically includes a tunable coupling strength and detuning $\Delta\omega = |\omega_{0,A} - \omega_{0,B}|$. Errors in either parameter lead to deviations in the accumulated two-qubit phase and consequently reduce gate fidelity [148]. Variations cause over- or underrotation of entangling unitaries, while frequency drift modifies the resonance condition and induces unwanted single-qubit phases.

Flux-tunable coupler architectures mitigate this by allowing coupling strength to be dynamically adjusted via a shared superconducting loop, so the interaction can be turned ON only for the gate window. Precise synchronization of the drive pulses across multiple channels is required to ensure coherent timing between the qubit and coupler waveforms. Pulse misalignment results in relative phase errors, particularly for gates based on adiabatic or parametric modulation. Modern multichannel AWGs provide shared clock domains and subnanosecond jitter, while active skew compensation further aligns timing across channels [147].

5) READOUT CHAIN FIDELITY AND MEASUREMENT BACK ACTION

High-fidelity qubit readout relies on the ability to discriminate between resonator response states corresponding to $|0\rangle$ and $|1\rangle$ with minimal added noise. The effective SNR is set by the measurement chain noise spectral density $S_i(f)$ and the integration time T_{int}, where the effective noise bandwidth is approximately ENBW $= 1/(2T_{\text{int}})$. Longer integration improves SNR but may increase latency and reduce throughput. Cryogenic low-noise amplifiers, such as Josephson parametric amplifiers or traveling-wave parametric amplifiers, can be employed to achieve near-quantum-limited system noise temperature [150], [151]. Proper impedance matching and thermal anchoring minimize reflection and back action.

Measurement-induced dephasing of spectator or idle qubits arises from residual cross-Kerr coupling between their resonators and the measurement cavity. The associated phase shift per photon depends on the intracavity photon number and the cavity linewidth. Optimization of these parameters, together with isolation through directional couplers and temporal sequencing of readout pulses, can suppress unwanted dephasing while maintaining high measurement contrast.

B. PULSE ENGINEERING AND SIGNAL SHAPING STRATEGIES

Pulse shaping is essential for achieving unitary operations through the precise definition of the amplitude and phase evolution of control signals.

1) SINGLE-QUBIT CONTROL AND LEAKAGE SUPPRESSION

Single-qubit gate operations are realized through precisely engineered microwave pulse envelopes that drive transitions within the computational subspace $\{|0\rangle, |1\rangle\}$. These control pulses implement the desired unitary operation by applying a resonant microwave drive of the form

$$P(t) = A(t)\cos(\omega_{01}t + \phi(t)) \tag{17}$$

where ω_{01} is the qubit transition frequency. The corresponding complex envelope is

$$\mathcal{E}(t) = A(t)e^{i\phi(t)} \tag{18}$$

which defines the time evolution of both amplitude $A(t)$ and phase $\phi(t)$. A common choice is the Gaussian envelope

$$A_G(t) = A_{\max}\exp\left(-\frac{(t-t_0)^2}{2\sigma^2}\right) \tag{19}$$

where the standard deviation σ sets the spectral bandwidth. A simpler alternative is the square envelope

$$A_S(t) = A_{\max}, \quad 0 \le t \le T \tag{20}$$

which confines the pulse to a fixed duration T. For enhanced fidelity, DRAG shaping adds a quadrature component proportional to the time derivative of the in-phase envelope, giving

$$\mathcal{E}_{\text{DRAG}}(t) = A(t) + i\alpha_{\text{drag}}\frac{dA(t)}{dt} \tag{21}$$

where α_{drag} is a tunable coefficient. This term suppresses population transfer to higher transmon levels. In practice, the DRAG coefficient is initialized to the analytic value proportional to the inverse anharmonicity value and then fine-tuned empirically to minimize leakage and phase errors for the specific qubit and control chain. Gaussian envelopes, often combined with DRAG, are preferred because their smooth temporal profile yields a smooth spectral roll-off and reduced sidelobes. Higher order DRAG further extends leakage suppression by including higher derivatives

$$\mathcal{E}_{\text{HDRAG}}(t) = A(t) + i\sum_{k=1}^{n}\alpha_k\frac{d^kA(t)}{dt^k} \tag{22}$$

which improves fidelity for larger drive amplitudes or shorter gates [155].

2) TWO-QUBIT GATE PULSES

Pulse engineering for two-qubit gates, such as the cross-resonance (CR) gate, is widely used for implementing entangling operations [156], [157], [158], [159]. Unlike single-qubit gates driven by a single pulse, CR gates require a multitone pulse sequence with at least two microwave drives to achieve high fidelity [158], [160]. Spectral tailoring is essential to isolate the desired transition frequency difference while avoiding parasitic transitions near harmonic or subharmonic frequencies.

Operationally, the two drives function as a coordinated pair [147], [157], [161]. The primary (or alternatively called

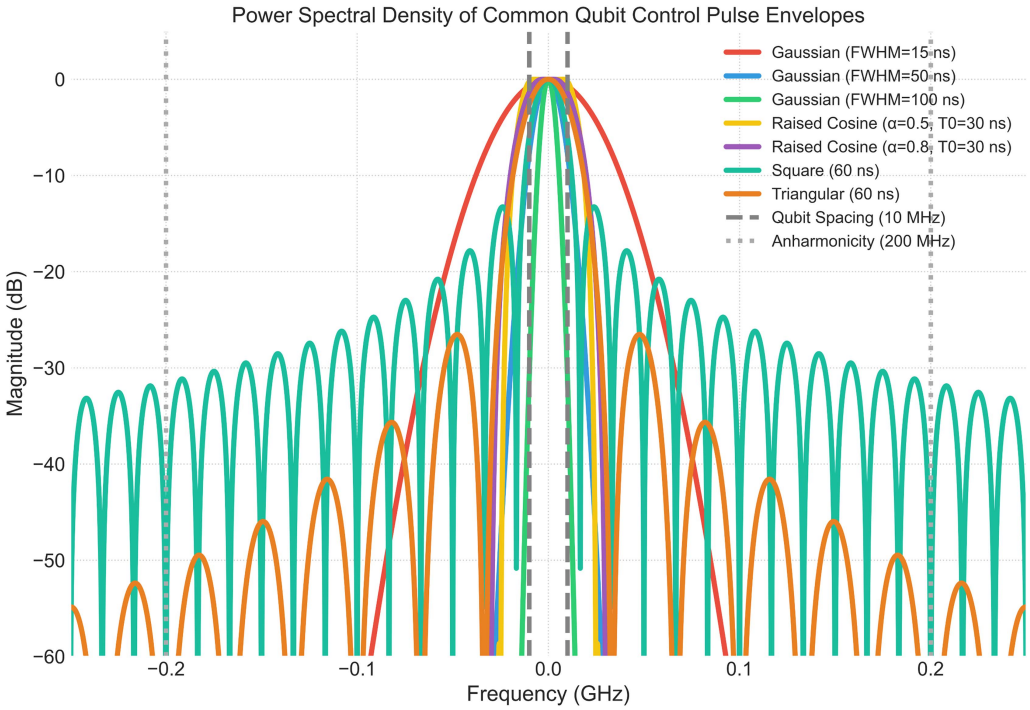

FIGURE 5. Normalized magnitude spectrum for various pulse types, using durations (Gaussian FWHM: 15, 50, 100 ns; square/triangular: 60 ns; and raised cosine: 30 ns with $\alpha = 0.5, 0.8$) representative of typical superconducting qubit control. These values are chosen to illustrate the tradeoff between pulse duration (affecting gate speed) and spectral purity. Vertical dashed lines highlight critical frequencies for superconducting qubits: qubit spacing (10 MHz) indicating potential interqubit crosstalk, and anharmonicity (200 MHz) showing the frequency offset for leakage to higher states.

as entangling) drive is applied to the control qubit at or near the transition frequency of the target qubit. The shape and amplitude of its envelope are calibrated to control the speed and strength of the desired entangling interaction while minimizing spectral leakage. A simultaneous secondary (compensation) drive is applied to the target qubit to cancel residual single-qubit rotations induced by the primary drive, thereby isolating the intended two-qubit interaction. This dual-drive approach, often embedded within an echo sequence, further suppresses static errors and ensures high-fidelity entanglement.

In broader superconducting qubit architectures, two-qubit gates can be realized through either tunable or fixed coupling mechanisms, depending on the system design [162], [163], [164]. In tunable-coupler architectures, a mediating element is coupled to both qubits, allowing the interaction strength to be dynamically varied. By controlling the bias waveforms applied to the coupler, the coupling can be varied, enabling the implementation of exchange-type gates such as the iSWAP. In contrast, fixed-frequency architectures achieve entanglement purely through microwave control, avoiding flux-tunable elements. With carefully calibrated amplitudes, durations, and pulse shapes, this method achieves the same computational effect as frequency-tuned gates [158]. Together, these two paradigms (tunable coupling and fixed-frequency) define the operational strategies for implementing two-qubit gates in modern superconducting quantum processors.

3) IMPACT OF ENVELOPE SHAPE ON PULSE SPECTRUM

To analyze the frequency content of $P(t)$, the Fourier Transform of the complex analytic signal $S(t) = A(t)e^{i(\omega_0 t+\phi(t))}$ is observed [165]

$$\tilde{S}(\omega) = \int_{-\infty}^{\infty} S(t)e^{-i\omega t}dt = \int_{-\infty}^{\infty} A(t)e^{i\phi(t)}e^{i(\omega_0-\omega)t}dt. \tag{23}$$

The magnitude of this spectrum, $|\tilde{S}(\omega)|$, indicates the strength of the frequency components at different frequencies ω. Concentrating the spectral power at the target transition frequency is important to minimize off-resonant excitations [155]. Gaussian envelopes produce narrowband spectra with minimal sidelobes, indicating a tradeoff between time-domain width σ and spectral selectivity. In contrast, square envelopes exhibit sinc-shaped spectra with significant leakage [166]. Cosine-shaped envelopes, characteristic of many window functions, reduce spectral splatter compared to square envelopes due to their smoother temporal profiles. Fig. 5 shows the frequency spectrum of some salient pulse envelopes.

4) SPECTRAL–TEMPORAL TRADEOFFS IN PULSE DESIGN

Residual imperfections remain unavoidable due to the finite spectral width $\Delta\omega$ of the control envelope. The spectral selectivity is constrained by the Fourier uncertainty relation

$$\Delta T\, \Delta\omega \geq \frac{1}{2} \tag{24}$$

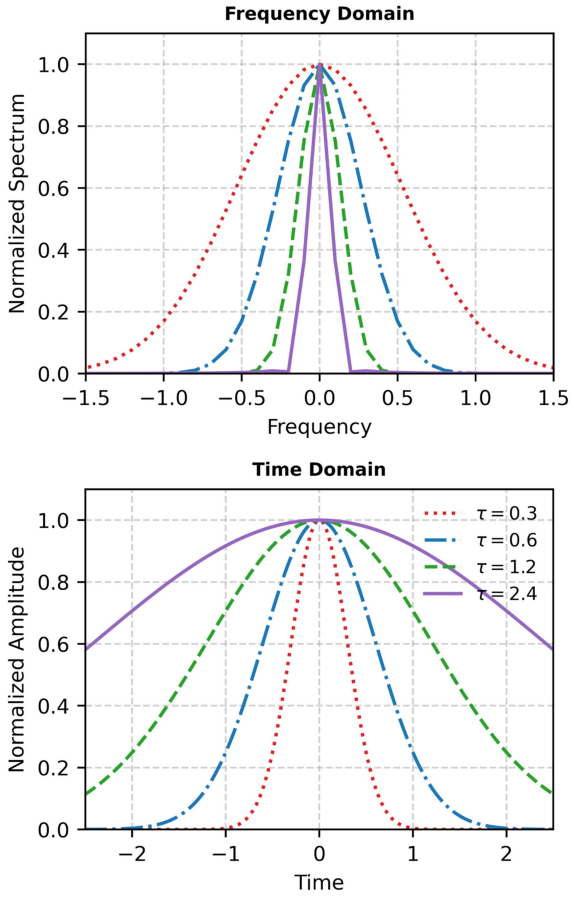

FIGURE 6. Illustration of the spectral–temporal tradeoff in qubit pulse design for pulses of different durations ($\tau = 0.3, 0.6, 1.2, 2.4$). The bottom panel shows the time-domain signals, while the top panel shows the corresponding normalized frequency spectra computed via the fast Fourier transform. Shorter pulses enable faster gate operations but produce broader spectra, increasing off-resonant excitation, whereas longer pulses are spectrally narrow and more selective.

where ΔT is the pulse duration and $\Delta\omega$ is the frequency spread. Shorter pulses ($\Delta T \to 0$) enable faster gate operations but broaden $\Delta\omega$, increasing off-resonant excitation risk. Conversely, highly selective (narrowband) pulses require longer durations, exposing the qubit to decoherence mechanisms. Thus, pulse engineering requires balancing gate speed, spectral leakage, and decoherence resilience within the constraints of qubit anharmonicity and available system bandwidth [167]. As shown in Fig. 6, using shorter pulses can enable faster gate operations but at the cost of broader spectra and higher risk of off-resonant driving; longer pulses improve spectral selectivity by narrowing the spectrum.

C. READOUT SIGNAL PROCESSING AND STATE DISCRIMINATION

Qubit state readout consists of two conceptually distinct stages: state projection and state discrimination. During the readout pulse, the qubit is coupled to a measurement resonator, and its quantum state is irreversibly projected onto the measurement basis, typically distinguishing between the $|0\rangle$ and $|1\rangle$ states. This physical measurement step imprints the

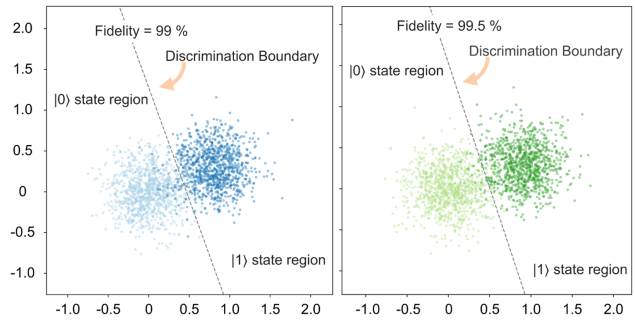

FIGURE 7. Simulated qubit readout in the in-phase–quadrature (IQ) plane for two representative readout fidelities (≈99% and 99.5%). Each panel displays two Gaussian clusters corresponding to the measured resonator responses for the qubit's ground ($|0\rangle$, light color) and excited ($|1\rangle$, dark color) states. The clusters are generated from 1000 simulated single-shot measurements for each state. The dashed line indicates a discrimination boundary used to assign classical state labels based on the measured IQ values. Increased separation between the clusters corresponds to a higher Signal-to-noise ratio (SNR), leading to improved state discrimination fidelity. The displayed fidelity values are estimated from the standard Gaussian detection relation $F \approx 1 - \frac{1}{2}\,\mathrm{erfc}(\mathrm{SNR}/\sqrt{2})$, which links readout fidelity to the effective SNR of the measurement channel. The plotted data are illustrative and based on simulated measurements.

outcome onto the resonator response, which is then amplified and digitized.

The subsequent state discrimination stage is purely classical signal processing. The recorded response is demodulated to extract the in-phase (I) and quadrature (Q) components, forming a complex value $I + iQ$ in the complex plane. Each qubit state corresponds statistically to a cluster in this plane. A discrimination threshold or decision boundary is defined to assign each measured point to one of the possible qubit states. The readout fidelity depends on the separation of these clusters, quantified by the SNR, which is determined by both the cryogenic amplification chain and the efficiency of the subsequent digital signal processing.

An illustrative example of this process is shown in Fig. 7, which depicts simulated single-shot readout outcomes in the IQ plane. Each point represents one measurement of the qubit state, forming two Gaussian-distributed clusters corresponding to the $|0\rangle$ and $|1\rangle$ states. The discrimination boundary shown in the figure separates these regions, demonstrating how classical state assignment is performed based on the measured IQ values. Larger cluster separation (i.e., higher SNR) reduces the overlap of the two distributions and thus increases the probability of correct state assignment.

IV. MAPPING MICROWAVE PULSES TO QUANTUM GATES

A. SINGLE-QUBIT CALIBRATION AND PERFORMANCE BENCHMARKING

Mapping microwave pulses to quantum gates involves a series of precise calibration and characterization steps to ensure accurate qubit operation. The procedure typically starts with frequency calibration. The calibration process begins with the resonator, where the resonant frequency of the readout resonator ω_r is determined by applying a frequency sweep

TABLE 6. Calibration and Characterization Steps for Single-Qubit Gates

Experiment	Description and procedure
Measure resonator frequency (calibration)	• Find the resonant frequency of the readout resonator ω_r. • Send a frequency sweep into the readout/resonator line. • Measure the amplitude on the readout line. • Plot the amplitude and identify the peak (or negative peak). • This measurement is stable and typically needs to be done only once per system turn-on.
Measure qubit frequency (calibration)	• Find the resonant frequency of the qubit transition ω_{01}. • Send a frequency sweep into the XY control line. • Measure the qubit response via the readout resonator. • Plot the amplitude and determine the qubit resonance peak. • This measurement can drift day-to-day due to environmental or bias fluctuations.
Rabi experiment (characterization)	• Calibrate the X_π pulse that rotates $\|0\rangle$ to $\|1\rangle$ (180° rotation). • Drive the XY line with a microwave pulse at ω_{01}. • Measure the qubit state using the resonator readout. • Repeat the experiment for a range of pulse lengths or amplitudes to record the probability of $\|1\rangle$. • Plot the probability versus pulse length to observe Rabi oscillations. • The X_π point is determined by fitting the measured oscillation data to a sinusoidal or damped sinusoidal function (or equivalent decaying oscillatory model) and identifying the pulse length corresponding to the first maximum.
Energy relaxation experiment (characterization)	• Prepare the qubit in the excited state $\|1\rangle$. • Wait a variable delay time τ, then measure the state. • Repeat the experiment many times to determine the probability of remaining in $\|1\rangle$. • Perform the measurement across a range of τ values. • Plot the resulting decay curve and fit to an exponential. • The decay constant corresponds to the energy relaxation time T_1.
Ramsey measurement (characterization)	• Apply an $X_{\pi/2}$ pulse to rotate the qubit to the equatorial plane. • Wait a time τ, then apply a second $X_{\pi/2}$ pulse. • In the absence of dephasing, the qubit returns to $\|1\rangle$; dephasing causes a reduction in the measured excitation. • Repeat over a range of τ values to obtain oscillations due to detuning and dephasing. • Fit the measured data to a decaying sinusoid to extract the dephasing time T_2^*. • When performed with a Hahn echo sequence, the extracted constant corresponds to T_2.

and measuring the amplitude on the readout line. This step is stable and typically requires only one measurement after power-up. For qubit calibration, the resonant frequency of the qubit ω_{01} is found by sending a frequency sweep into the XY line and measuring the readout response. Unlike the resonator, this quantity can drift over time and may require periodic recalibration [168]. After these frequency calibrations, the Rabi experiment is performed to calibrate the microwave pulse parameters for the fundamental X_π gate. This experiment characterizes the coherent Rabi oscillations of the qubit population between the $|0\rangle$ and $|1\rangle$ states. Because the total angle of rotation is determined by both the pulse amplitude (which sets the Rabi frequency) and its duration, the calibration can be performed in one of two ways. Most commonly, the pulse amplitude is held constant while its duration is swept to find the precise time required for a π-rotation. Alternatively, for a fixed pulse duration, the amplitude can be varied to achieve the same result. Fitting the resulting Rabi oscillations to a sinusoidal or damped-sinusoidal model identifies the pulse parameter corresponding to a π rotation. This yields a calibrated X_π pulse, from which $X_{\pi/2}$, Y_π, and $Y_{\pi/2}$ pulses are obtained by adjusting phase and duration.

Once the calibration is complete, device-level characterization is performed to quantify coherence. Energy relaxation characterization is performed by measuring the time-dependent decay of the qubit state, starting from the excited state $|1\rangle$ and allowing it to decay to $|0\rangle$. The probability of this decay is recorded over varying delay times, with T_1 representing the time constant of this exponential decay. In a Ramsey experiment, two $X_{\pi/2}$ pulses separated by a delay τ are applied; the resulting decaying oscillation reveals the dephasing time T_2^*, and with echo sequences, the homogeneous dephasing time T_2 can be extracted. These measurements define the physical coherence budget against which gate times must be chosen. Insights from characterization experiments, including gate fidelity and coherence times, inform the optimization of microwave pulse parameters to achieve precise unitary operations and quantum control. The experimental calibration and characterization workflow is summarized in Fig. 8 and Fig. 9. Fig. 8 shows resonator and qubit spectroscopy used to determine the operating frequencies, while

TABLE 7. Detailed Comparison Between Conventional Mixer-Based and Direct Digital (Mixerless) Architectures

Feature	Mixer-based architecture	Mixerless (Direct digital synthesis) architecture
Signal generation	Analog upconversion of baseband I/Q signals using an external LO and mixer	Direct digital synthesis of the final RF/microwave waveform without analog upconversion
Frequency range and bandwidth	Reaches high microwave frequencies via the LO; bandwidth limited by baseband filters and mixer linearity	Constrained by the DAC Nyquist frequency; Modern FPGAs can generate mulitple GHz frequencies
Signal purity	Prone to analog artifacts such as LO leakage, image sidebands, and intermodulation distortion; phase noise dominated by the LO source	Immune to analog mixing artifacts; residual spurs arise from digital effects (e.g., DAC clock feedthrough, quantization noise)
Calibration overhead	Requires frequent calibration to correct I/Q imbalance (amplitude/phase mismatch) and LO leakage (DC offsets)	No I/Q imbalance or mixer-specific errors; calibration focuses on pre-distorting digital waveforms to compensate the analog chain response
Phase coherence (Interchannel)	Challenging — requires phase-locked LO distribution networks; susceptible to thermal drift and cable length variations	Inherently high — all channels share a synchronized digital clock, improving deterministic and stable phase relationships
Form factor	Higher component count (DACs, mixers, LOs, filters) increases footprint and wiring complexity per channel	Reduced analog hardware enables compact, integrated implementations and high channel density
Flexibility and agility	Frequency agility limited by LO tuning; baseband amplitude and phase are digitally programmable	Fully agile — frequency, phase, and amplitude are digitally programmable on a sample-by-sample basis, supporting rapid chirps and frequency hops
Scalability	Scales poorly due to LO distribution, synchronization overhead, and per-channel calibration	Highly scalable — digital architecture allows straightforward parallelization of many DAC channels on a single ASIC or FPGA

Fig. 9 presents representative time-domain measurements (Rabi, relaxation, and Ramsey) used to tune control settings and extract coherence metrics. Table 6 outlines the practical workflow for single-qubit calibration, starting from resonator and qubit spectroscopy and followed by time-domain measurements used to tune pulse settings and extract coherence metrics.

While coherence times provide an upper bound on performance, gate quality in practice is assessed with randomized benchmarking. The standard method for this is randomized benchmarking [169], [170], [171], [172]. In randomized benchmarking, long sequences of randomly chosen Clifford gates are applied to the qubit, and the final state is measured. By observing the decay of the measurement fidelity as the sequence length increases, the average error per Clifford can be extracted. This technique has the advantage of being robust against state preparation and measurement errors, providing a reliable benchmark of the control hardware performance [173]. For a more exhaustive analysis, methods like gate set tomography can be employed to reconstruct coherent and stochastic error channels [174], [175].

B. TAXONOMIZING QUBIT CONTROL AND READOUT PARADIGMS

Given the architectural and technological diversity in existing implementations, a structured classification becomes essential to systematically address scalability and integration challenges. Accordingly, we categorize control and readout strategies into two complementary layers: 1) architectural approaches, encompassing aspects of frequency conversion, signal conversion, waveform management, control signal routing and logic architectures, readout and signal analysis, system infrastructure enhancements, and interface and usability considerations and 2) technology platforms, including COTS-based reconfigurable systems, Cryo-CMOS circuits, photonic interfaces and interconnects, wireless transceiver links, and thermal readout mechanisms. This categorization is intended to inform future efforts toward the scalable and efficient realization of quantum control and readout subsystems.

1) ARCHITECTURAL APPROACHES

Architectural approaches define the overall configuration for signal generation, transmission, and acquisition, aiming to support qubit manipulation and measurement. This classification is intended for a systematic evaluation based on their operational principles, scalability potential, and implementation complexity.

a) Frequency conversion

Specific types of qubits can operate up to 40 GHz and beyond [176], [177]. Frequency conversion is typically achieved through the mixer-based architectures, where an RF mixer combines low-frequency IF signal with an LO signal, generating the required control waveform at the desired qubit frequency. However, mixer-based designs suffer from nonlinearities [178], image frequencies, quadrature

TABLE 8. Organizing Qubit Control and Readout: Architectural Strategies From Single-Channel to Multiplexed and Feedback-Integrated Designs

Category	Technical description	Scalability potential [1]	Implementation complexity [2]
Frequency conversion techniques: Comparison of mixer-based and mixerless architectures			
Mixer-based designs	Mixers for frequency conversion.	Moderate	High
Mixerless architectures	Direct signal generation eliminating mixer noise.	Moderate	High
Signal conversion techniques: Methodologies for signal conversion in qubit control and readout			
Conventional Nyquist zone DAC/ADC	First Nyquist zone requiring external upconversion.	High	Low
Extended Nyquist zone operation	Utilizing higher Nyquist zones for direct synthesis.	High	High
Frequency multiplexed conversion	Multiplexing multiple control signals for scalability.	High	High
Waveform management techniques: Strategies for efficient storage, synthesis, and transmission of control waveforms			
Static waveform storage	Precomputed waveforms stored in memory for repeated execution.	Moderate	Low
Dynamic waveform synthesis	Real-time waveform synthesis based on experimental parameters.	Moderate	High
Compressed waveform techniques	Data compression techniques to optimize waveform storage and bandwidth usage.	Moderate	High
Control signal routing and logic architectures: Architectural approaches to qubit control signal routing and multiplexing			
Single-channel control	Dedicated per-qubit control lines for high-fidelity operations.	Low	Low
Spectral channelization	Single control line carrying multiple frequency-multiplexed signals.	High	High
Feedback-control integration	Real-time feedback mechanisms for dynamic qubit state correction.	Moderate	High
Readout and signal analysis techniques: Methods for accurate state readout and analysis.			
Matched filtering and template matching	Template-matching techniques for efficient state discrimination.	Moderate	Moderate
Real-time signal analysis	Real-time DSP-based processing of qubit readout signals.	High	High
Frequency-multiplexed readout	Combining multiple qubit signals into a shared readout channel.	High	High
System infrastructure enhancements: Foundational techniques that support scaling, synchronization, and modularity in quantum control systems			
Clock distribution and synchronization	Techniques for distributing reference clocks across multiple channels with deterministic latency (e.g., JESD204B/C, Multitile Synchronization (MTS), cryo-compatible PLLs).	High	High
Calibration and stability layer	Embedded calibration modules for IQ imbalance correction, clock drift compensation, and real-time stability monitoring.	High	High
Fault tolerance support	Support for mid-circuit measurement, real-time error-syndrome extraction, and dynamic pulse adaptation.	High	High
Modular hardware design	Plug-and-play modules enabling flexible control stack scaling and upgrade.	High	Moderate
Interface and usability: Enhancements in usability through software-hardware integration			
User-centric APIs	High-level APIs simplifying quantum programming.	High	Moderate
Open-source frameworks	Open-source frameworks providing modular and flexible architectures.	High	Moderate

[1]Scalability potential refers to a technique's capacity to support an increasing number of qubits—typically beyond 100—without exponential growth in control resources. High = broadly scalable with manageable overhead; Moderate = scalable with constraints (e.g., wiring and power); Low = limited to small-scale or prototype systems due to constraints.
[2]Implementation complexity quantifies the difficulty of practical deployment, signal integrity, calibration, usability, and maintenance. High = Custom hardware; Moderate = reflects moderate DSP effort, standard interfacing, or platform-dependent tuning; Low = minimal setup using standard components.

imbalance, DC offsets, and LO leakage. In contrast, mixerless architecture suppresses many of these limitations by generating control waveforms at desired qubit frequency. This approach avoids mixer-induced distortion at the cost of high-performance hardware. Table 7 compares mixerless and mixer-based designs.

b) Signal conversion

Conventional Nyquist-zone signal conversion is confined to the first Nyquist band (0 to $f_s/2$), requiring upconversion stages for gigahertz-range synthesis and downconversion stages for readout. In contrast, extended Nyquist-zone DACs/ADCs exploit higher order Nyquist bands, enabling signals in the gigahertz range. This approach demands more anti-aliasing, filtering, and higher data throughput.

Frequency-multiplexed conversion techniques enable multiple qubits to be controlled/measured by spectral division. This approach improves hardware utilization while maintaining throughput [179], [180]. However, it introduces additional challenges in spectral isolation and increases computational complexity.

c) Waveform management

Effective digital architectures and waveform management contribute to a lower power footprint and resource

TABLE 9. Cross-Platform Assessment of Qubit Control and Readout Systems (With Representative Examples)[1]

COTS-based reconfigurable systems	
Technical description	Uses reconfigurable hardware (FPGAs and AWGs) at room temperature, including both turnkey commercial platforms and flexible research-driven designs.
Scalability potential	High. This approach is used to control the largest existing processors (>1000 qubits) by tiling many parallel systems. Architecturally, a single controller cluster typically manages 10-100 qubits.
Precision (per qubit)	Moderate (∼99%).
Cryo-compatibility	Low.
Power efficiency	Low (> 1 W).
Representative examples / references	Commercial AWG/FPGA platforms (e.g. Zurich Instruments [186], Quantum Machines [187], Qblox [188], and Keysight [189]) and research platforms including QICK [190], SQ-CARS [191], ICARUS-Q [192], and COMPAQT [193].
Cryo-CMOS-based platforms	
Technical description	Cryogenic-temperature CMOS circuits for direct qubit control; reduces cabling overhead but limited by design complexity.
Scalability potential	High potential. Current demonstrations have controlled small-scale testbeds (e.g., 2–10 qubits) [157], [194], while controller chips with 64+ channels have been developed [195]. Projections aim for >1000 qubits.
Precision (per qubit)	High (> 99.9%).
Cryo-compatibility	High.
Power efficiency	High (∼4 mW or more).
Representative examples /references	Dual-channel RF AWG Cryo-CMOS [196], 28-nm Bulk CMOS based chip [197], 40-nm Bulk CMOS based controller [198]
Wireless-transceiver-based approaches	
Technical description	RF/microwave (or THz) transceivers for wireless cryogenic I/O; reduces cabling but challenged by noise and isolation.
Scalability potential	Conceptual. Current demonstrations have focused on single-qubit control/readout. Projections aim for 100 qubits.
Precision (per qubit)	Moderate (∼99%).
Cryo-compatibility	Moderate (still under adaptation).
Power efficiency	High (< 100 mW).
Representative examples /references	Wang et al. [199], Alarcón et al. [200]
Photonic interconnect and interface platforms	
Technical description	Optical interconnects and interfaces for modular communication and control; limited by microwave-to-optical transduction.
Scalability potential	High (conceptual stage). Demonstrations have shown control/readout of single qubits. Scalability is conditional on breakthroughs in transduction efficiency.
Precision (per qubit)	Moderate (optical control/readout under development).
Cryo-compatibility	Moderate.
Power efficiency	Moderate (∼500 mW).
Representative examples /references	Lecocq et al. [201]
Thermal readout architectures	
Technical description	Temperature-dependent state discrimination for readout; conceptually simple but slow and less sensitive.
Scalability potential	Low. Current demonstrations have been realized on single-qubit devices. Scalability beyond ten qubits is a projected to be a significant challenge.
Precision (per qubit)	Moderate (readout error > 1%).
Cryo-compatibility	Low.
Power efficiency	Low (> 1 W).
Representative examples /references	Early-stage readout experiments using thermal sensors in millikelvin regimes [202]

[1]Scalability potential reflects the architecture's indicative capacity to support larger qubit counts. It incorporates both demonstrated experimental realizations—which represent current technological maturity—and projected scalability trends reported in representative literature. These values should be interpreted as approximate and not directly comparable across platforms due to differing architectural assumptions and control constraints. Precision refers to typical control or readout fidelity. Cryo-compatibility denotes suitability for integration, with "High" implying operation at or near subkelvin stages. Power efficiency indicates the typical per-channel or module-level power demand at the relevant temperature stage.

consumption. Static waveform storage precomputes control signals for reuse, offering spectral purity but at the cost of memory overhead. The data movement, memory bandwidth, and energy consumption do not scale well [181]. The discrete representation of the sinusoidal waveform is given as

$$x[n] = A\cos\left(2\pi\frac{f}{f_s}n + \phi\right). \tag{25}$$

The sampling resolution is represented by $N_{\text{points per cycle}} = \frac{f_s}{f}$. Efficient storage techniques such as quarter-wave symmetry allow waveform compression with minimal fidelity loss. Only one-fourth of a sinusoidal cycle is stored, while the remaining three-quarters can be reconstructed [182]

$$x(t) = \begin{cases} \sin(t), & 0 \le t < \frac{\pi}{2} \\ \sin(\pi - t), & \frac{\pi}{2} \le t < \pi \\ -\sin(t - \pi), & \pi \le t < \frac{3\pi}{2} \\ -\sin(2\pi - t), & \frac{3\pi}{2} \le t < 2\pi. \end{cases} \tag{26}$$

TABLE 10. Typical Design and Performance Parameters for Superconducting Qubit Control and Readout Systems

Parameter	Mathematical / Empirical Formulation	Description	Typical Range (May Vary)
Signal Frequency (f_q)	$f_q \in [1, 10]$ GHz	Defines the resonant frequency of superconducting qubits; sets resonance for microwave control	1 GHz to 10 GHz
Gate Fidelity (F_G)	$F_G \geq 99.9\%$	Probability that the implemented gate reproduces the ideal state $F_G = \lvert\langle\psi_{\text{ideal}}\rvert\psi_{\text{actual}}\rangle\rvert^2$	$F_G \geq 99.9\%$
Gate Speed (t_G)	$t_G \sim 1/\Omega$, where Ω is the Rabi frequency	The time to execute a quantum gate. Faster gate operations reduce the impact of decoherence	10 ns to 300 ns
Error Rate (E_G)	$E_G = \frac{\text{Number of Errors}}{\text{Total Operations}}$	Fraction of erroneous operations relative to total gates applied. The goal is to minimize this error	$< 0.1\,\%$
IQ Mismatch Error (ϵ_{IQ})	$\epsilon_{\text{IQ}} = \sqrt{\frac{1}{2}(\Delta I^2 + \Delta Q^2)}$, where ΔI and ΔQ are RMS deviations from ideal I/Q components	Quantifies the error in complex modulation caused by amplitude and phase imbalances in I and Q components, leading to imperfect qubit rotations and leakage	$\epsilon_{\text{IQ}} < 3\%$
Spurious-Free Dynamic Range (SFDR)	$\text{SFDR} = 20\log_{10}\left(\frac{\text{Signal Power}}{\text{Spurious Power}}\right)$	Defines spectral purity of DAC output; limits harmonics and intermodulation products in microwave drive	SFDR > 40 dB
Phase Noise ($\mathcal{L}(f)$)	$\mathcal{L}(f) = 10\log_{10}\left(\frac{S_\phi(f)}{2}\right)$	Single-sideband phase noise power at frequency offset f; quantifies frequency stability and noise in control tones	$< -100\,\text{dB Hz}^{-1}$ at 1 MHz offset
Control Bandwidth (B_{ctrl})	Typically relates to the effective bandwidth of the waveform generator and the microwave upconversion chain $B_{\text{ctrl}} \propto 1/t_{\text{min\_feature}}$	Defines the maximum frequency content and modulation rate for arbitrary pulse envelope generation, enabling fast and precise shaping of control pulses. High bandwidth is critical for short gate times	>1 GHz
Signal Integrity (SNR)	$\text{SNR} = 10\log_{10}\frac{P_{\text{signal}}}{P_{\text{noise}}}$	Quantifies signal clarity during control and readout; higher values reduce errors	> 40 dB
Latency	$\tau_{\text{latency}} = T_{\text{response}}$	The time delay between command and signal delivery or response capture	$< 1\,\mu$s
Jitter (Δt_{jitter})	$\Delta t_{\text{jitter}} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(\Delta t_i)^2}$, where Δt_i are time deviations	Temporal instability in timing signals; affects synchronization of multi-channel control	< 15 ps
Power Consumption (P_{total})	$P_{\text{total}} = P_{\text{control}} + P_{\text{readout}}$	Total power consumed by the classical control and readout electronics, typically per qubit channel	Varies widely $\gg 5$ mW per channel
Readout Signal Type	State-dependent cavity frequency shift: $\Delta f_r \propto \chi$	Dispersive or resonant readout methods. The qubit state shifts the resonant frequency of resonator	Dispersive (typically)
Temperature Range	$T_{\text{operating}} \sim 10$ mK to suppress thermal noise and support coherence.	Superconducting qubits are typically operated at cryogenic temperatures near absolute zero	< 4 K

Another method for sinusoidal pulse generation is CORDIC, which uses predefined rotation angles and approximates any arbitrary rotation θ as

$$\theta = \sum_{i=0}^{N} z_i \theta_i, \quad \text{with} \quad d_i = \text{sign}(z_i). \tag{27}$$

CORDIC performs iterative vector rotations using only shift and add operations, eliminating the need for multipliers. This makes it easy for design synthesis on the hardware fabric. Future systems may involve the strategic consideration of sinusoidal waveform generation via polynomial approximations (e.g., Chebyshev and Taylor), recursive algorithms, and piecewise-linear interpolation to optimize waveform storage.

Dynamic synthesis offers flexibility at the cost of increased processing overhead. Compression techniques, in turn, enhance memory efficiency but require additional processing for waveform reconstruction. A hybrid approach integrating multiple strategies may offer the most efficient balance between performance and resource utilization.

d) Control signal routing and logic architectures

Traditional single-channel control architectures become impractical as system size increases, owing not only to wiring complexity but also to their indirect impact on qubit coherence. In a one-line-per-qubit scheme, each qubit requires a dedicated cryogenic control line, leading to dense wiring through the dilution refrigerator. This dense cabling increases the thermal load on the millikelvin stage and enhances electromagnetic crosstalk between lines, both of which can degrade qubit coherence times (T_1 and T_2) through elevated noise and correlated dephasing. To address these scalability and coherence challenges, spectral multiplexing of control and readout signals effectively reduces wiring density and per-line dissipation [183]. Complementary to

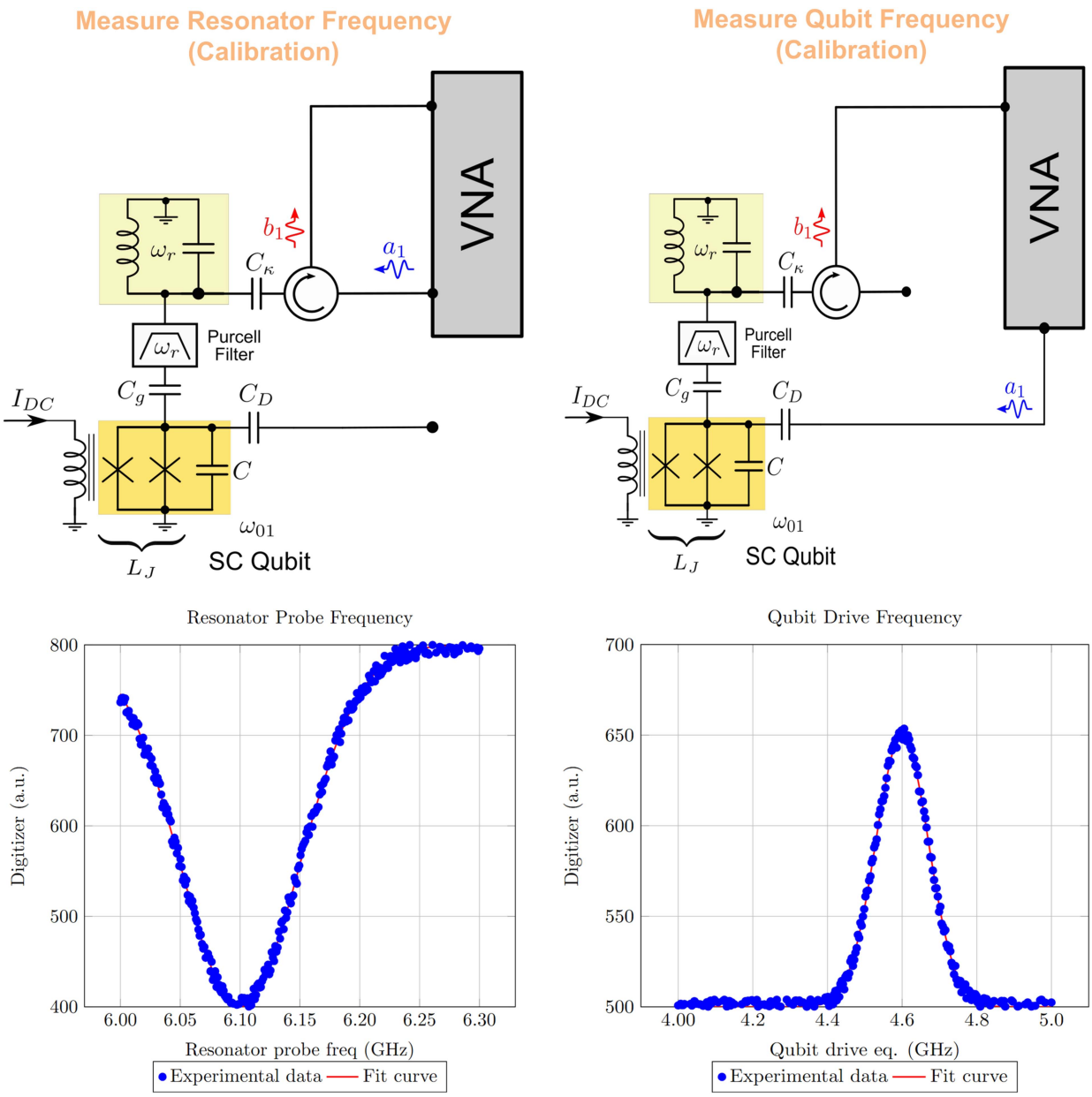

FIGURE 8. Experimental setup and representative data for resonator and qubit spectroscopy in a flux-tunable superconducting qubit system. (Left) One-tone resonator spectroscopy setup and data. The VNA measures a reflection dip, identifying the resonator frequency. (Right) Two-tone qubit spectroscopy setup and data. A fixed-frequency probe at ω_r measures the resonator's response, while a drive tone is swept. The resulting peak, caused by the dispersive shift, identifies the qubit's transition frequency at this flux bias. In both plots, blue dots represent experimental data and the red line is a fit to the data.

this, real-time feedback control utilizes qubit measurement outcomes to dynamically adjust subsequent control pulses or sequences, enabling fast state initialization and on-the-fly error correction [184], [185].

e) Readout and signal analysis

Matched filtering and template matching techniques enhance state discrimination by correlating received qubit signals with predefined reference templates. Real-time signal analysis enables data acquisition and time resolved measurements [203]. For scalable quantum systems, scaling via spectral division is achieved to aggregate multiple qubit signals into a single measurement channel. While this method enhances scalability, it introduces challenges in isolating individual qubit states.

f) System infrastructure enhancements

Deterministic clock synchronization can be used for phase-coherent signal delivery across multiple channels. However, this approach demands precision to suppress undesired signal leakage. Beyond synchronization, modularity is a key system infrastructure enhancement. This architectural approach involves structuring the control and readout system

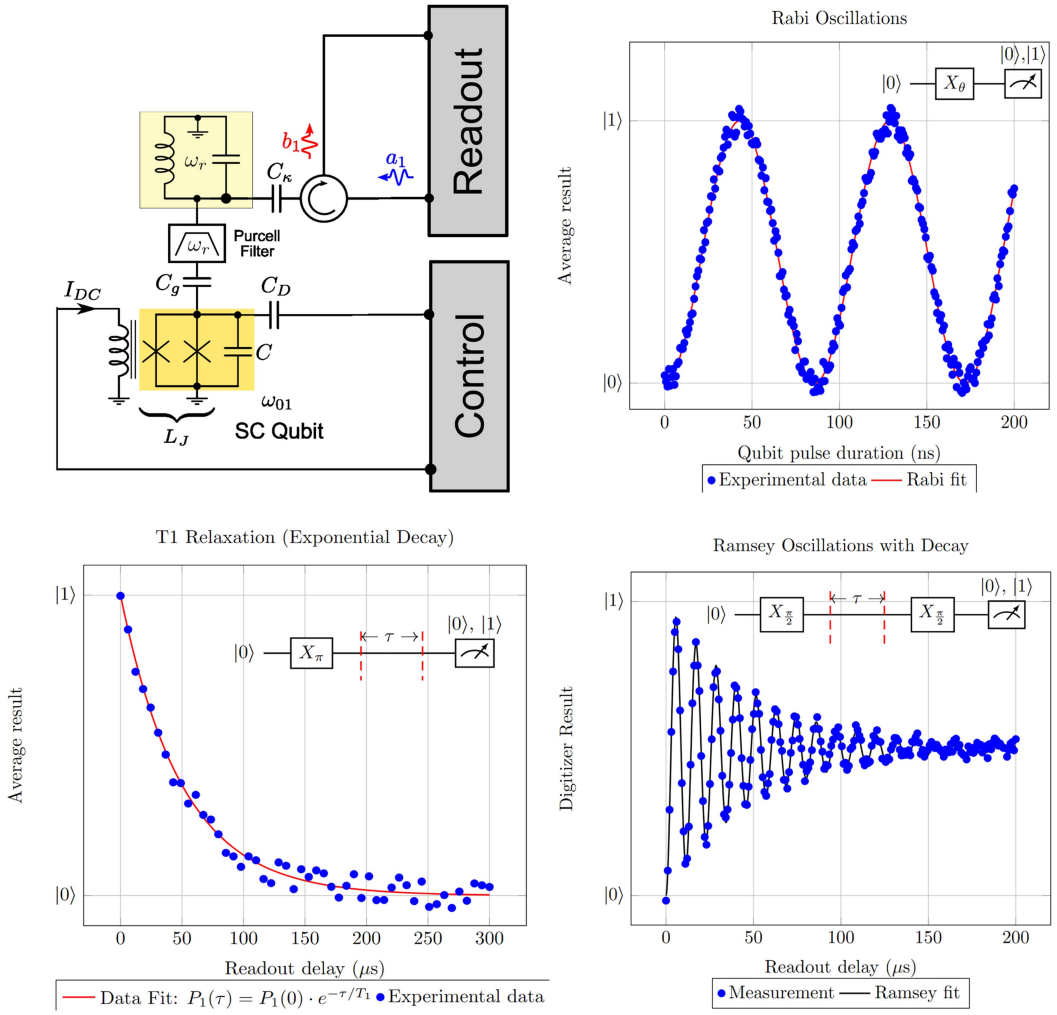

FIGURE 9. Experimental setup and coherence characterization of a superconducting qubit. (Top left) Schematic of the flux-tunable qubit, coupled to a readout resonator (Purcell filter) for measurement and a control line for driving. (Top right) Rabi oscillations, showing coherent population transfer between $|0\rangle$ and $|1\rangle$ as a function of drive pulse duration. This is used to calibrate π and $\pi/2$ pulse lengths. (Bottom left) T_1 relaxation measurement. The population in the $|1\rangle$ state is measured after a variable delay τ, revealing an exponential decay (red fit) from which the energy relaxation time T_1 is extracted. (Bottom right) Ramsey oscillations. A Ramsey experiment (two $\pi/2$ pulses separated by τ) measures the decay of phase coherence, characterized by T_2^* (from the black fit envelope), and the qubit's frequency detuning (from the oscillation frequency).

into standardized and interchangeable modules. Such modularity facilitates flexible scaling, simplifies system upgrades, and eases maintenance through plug-and-play components.

g) Interface and usability

User-centric API simplify quantum programming, while open-source frameworks offer extensible platforms that accelerate development and community-driven innovation [204], [205]. Therefore, this characteristic of "openness" can be considered as a choice for categorization. Table 8 shows the architectural strategies and its technical description.

2) TECHNOLOGICAL APPROACHES

The classification of physical technology platforms is based on their underlying implementation modalities. Table 9 highlights various technology platforms and their scalability outlook.

a) Reconfigurable COTS-based systems

Reconfigurable COTS platforms offer flexibility and programmability for adaptive quantum operations. However, they require wiring to interface with cryogenic environments.

b) Cryo-CMOS platforms

Cryo-CMOS platforms offer high integration feasibility by enabling direct qubit interfacing, significantly reducing interconnect complexity. However, their precision and scalability remain moderate due to cryogenic design constraints till date.

c) Wireless and photonic technologies

Wireless transceiver-based links, utilizing RF/microwave devices, address physical interconnect limitations and enhance deployment flexibility. In parallel, photonic platforms encompass both interconnects for high-speed long-range signal transmission and emerging interfaces for qubit-level control

and readout via electrooptic or optomechanical coupling. Integration feasibility remains challenging due to coupling constraints with superconducting qubits.

d) Thermal readout architectures

Thermal schemes leverage temperature-sensitive mechanisms such as bolometric effects for nonelectrical state readout. Thermal readout architectures face limited scalability, low integration feasibility, and power inefficiencies, restricting their widespread adoption.

C. PERFORMANCE BENCHMARKS AND PRACTICAL RANGES

Table 10 provides a concise compilation of the typical design and performance parameters that are important for the effective control and readout of superconducting qubits. Typical parameter ranges often reflect isolated or small-scale performance. However, scaling toward fault-tolerant quantum computing with QEC imposes more system-wide requirements. Many of these parameters are directly influenced by pulse shaping strategies, signal integrity considerations, and the spectral engineering approaches discussed earlier. Examining the parameters, we observe that operational frequencies lie in the 1–10 GHz range, gate fidelities above 99.9% are essential, and sub-300-ns gate times enable more operations. Control precision is upheld through low phase noise ($<-100\,\text{dB/Hz}$), sub-15-ps jitter, and tight IQ calibration ($<3\%$). Power constraints, typically below 5 mW per qubit, remain a bottleneck under cryogenic load to this date. To minimize distortion, systems demand SFDR $>$ 40 dB, and sub-1-μs latency. The typical range values presented in this table are indicative of current technological capabilities and can vary depending on the specific qubit modality, design process, and experimental setup employed.

While Table 10 summarizes representative device-level benchmarks, scaling these parameters toward fault-tolerant quantum computing introduces additional system-wide constraints. Fault tolerance places stringent requirements on every layer of the control stack, since overall reliability is ultimately limited by the weakest component in the quantum–classical feedback loop (in accordance with Amdahl's law for system reliability [206], [207]).

QEC codes are not passive overhead; they are active resource-intensive processes that dictate the entire architecture of a quantum computer [44], [208], [209]. The successful implementation of a QEC code hinges on solving several interconnected engineering problems.

1) *Meeting the error threshold:* QEC codes function if the error rate of the underlying physical operations is below a certain "error threshold." This translates to a requirement for uniformly high gate fidelity across the entire processor. A few poorly performing qubits can render the error correction scheme useless.
2) *Managing qubit overhead:* QEC achieves robustness through massive redundancy, requiring several physical qubits to encode a single protected logical qubit. Each of these physical qubits needs control and readout connection.
3) *Closing the feedback loop:* QEC is an active process that operates in a real-time feedback loop. This cycle, ranging from measuring the error syndrome from ancilla qubits, sending the data to a classical decoder, calculating the most likely error, and sending a corrective pulse back to the processor, must be completed much faster than the logical qubit decoherence time. Any delay in this classical feedback loop allows errors to accumulate faster than they can be corrected.
4) *System survival and holistic robustness:* True QEC success depends on the entire system's survival under continuous operation, accounting for thermal, bandwidth, latency, and noise injection constraints. It is not sufficient for individual qubits or gates to meet specifications in isolation: the cryogenic stack, control electronics, interconnects, and real-time decoding must all maintain performance simultaneously over long runs. Any subsystem that drifts, injects excess noise, or cannot keep up with the QEC cycle can become the bottleneck that breaks the logical error suppression.

D. THERMAL BUDGETING AND SYSTEM INTEGRATION AT MILLIKELVIN SCALES

Cryogenic operation below 20 mK imposes severe thermal load constraints on the dilution refrigerator's base stage, where available cooling power is typically limited to below 2500 μW. Excessive cabling, high-power amplifiers, or inefficient signal routing can cause thermal loading, leading to temperature drift, degraded coherence times (T_1, T_2), and increased crosstalk between qubits. System integration must, therefore, prioritize power-efficient signal generation, cryo-optimized cabling, and thermal anchoring to maintain fidelity and scalability.

E. SCALABILITY AND INNOVATIONS FOR HIGH-DENSITY QUBIT CONTROL

A variety of architectures that optimize signal conversion pipelines, waveform synthesis strategies, and cryogenically compatible hardware platforms are available. Advancements in digital synthesis and direct microwave DAC are anticipated to simplify signal chains and reduce spurious distortion. Cryo-optimized readout chains with integrated feedback, waveform caching, and low-noise amplification will be essential for real-time discrimination.

Scalability beyond 1000 qubits will require precision packaging, high-density interconnects, and hybrid stacks combining cryo-CMOS, memory elements, and adaptive firmware. Integrated platforms minimizing I/O overhead and deterministic timing synchronization are already an active area of research and are expected to receive increased attention in the future.

V. RECONFIGURABLE COTS PATHWAYS TOWARD SCALABILITY

COTS hardware platforms enable the development of control and readout systems based on self-contained units, thereby facilitating system integration and potential scalability. For clarity, COTS pathways in the present context can be broadly classified into two categories.

1) *Commercially integrated systems:* Complete hardware–software control and readout platforms designed, manufactured, and supported by vendors. These systems (for example, the Zurich Instruments SHFQA [186], Quantum Machines OPX+ [210], and Qblox cluster platforms [188]) are distributed as ready-to-deploy instruments with dedicated interfaces, synchronization frameworks, and software ecosystems.
2) *Research-driven COTS implementations:* Architectures proposed and demonstrated in academic or open-source research that leverage reconfigurable platforms such as field-programmable gate array (FPGA) or radio-frequency system-on-chip (RFSoC) evaluation boards to design modular control and readout systems. Representative examples include QICK [190], SQ-CARS [191], ICARUS-Q [192], and Compressed Waveform Memory Architecture for Scalable Qubit Control (COMPAQT) [193]. These frameworks leverage commercially available hardware to prototype scalable and configurable quantum controllers, typically prioritizing flexibility, rapid reconfiguration, and accessibility over turnkey operation.

The distinction is conceptual rather than absolute. Several research-oriented COTS implementations have influenced commercial instrument design and vice versa. For instance, open-source initiatives like QICK have demonstrated low-cost modular control architectures that align closely with vendor-provided solutions such as the SHFQA or OPX+, reflecting a gradual convergence between research-grade and commercial-grade COTS development. Hence, *COTS pathways* in this work collectively refer to both commercially integrated and research-derived systems that utilize available reconfigurable hardware as a foundation for scalable quantum control and readout. Together, they represent complementary trajectories toward scalable quantum architectures, bridging prototype experimentation and deployable quantum computing infrastructure. Recent research activities have focused on employing the inherent flexibility of configurable hardware, notably FPGA and SDR platforms, for the implementation of control and readout loops [205], [210]. The forthcoming subsections detail the design paradigms and architectural solutions for superconducting qubit control and readout systems documented within the current body of literature.

A. BENEFITS AND TRADEOFFS OF COTS ARCHITECTURES

Architectural modularity has emerged as a key architectural strategy, with numerous research groups and hardware ventures proposing modular design approaches in literature [101], [190], [191], [192], [193], [211], [212], [213], [214], [215], [216]. This approach aims to streamline system deployment and reduce the setup complexity of quantum experiments. Modular and commercial architectures often integrate spectral division to enhance scalability, enabling a single control or readout line to address multiple qubits [36], [217].

While commercial offerings and more broadly modular architectures enable room temperature precision control and the prospect for system scalability, prominent drawbacks persist. These often include a considerable physical footprint ("bulkiness"), challenges associated with managing high-density interconnects, and significant power consumption. Nevertheless, these systems significantly accelerate the development of prototype-to-intermediate-scale platforms and provide accessible tools for establishing experimental capabilities.

Beyond these shared characteristics, the two COTS pathways present distinct tradeoffs. Commercially integrated systems prioritize reliability and ease of use, offering specifications and vendor support that accelerate experimental timelines. This approach typically involves a closed-ecosystem, where the hardware is abstracted, limiting deep customizability. Research-driven systems, in contrast, offer architectural transparency and reconfigurability, ideal for novel prototyping, but demand in-house development expertise and integration effort.

B. GENERALIZED ARCHITECTURE AND DESIGN CONSIDERATIONS

A typical system architecture for COTS pathways is illustrated in Fig. 10, which depicts a common heterodyne architecture. This paradigm is widely adopted because it allows a reconfigurable module (typically an FPGA or RFSoC) to perform all complex pulse-shaping and real-time processing using high-resolution DACs and ADCs. The diagram demonstrates a reconfigurable module for real-time digital signal processing, which drives DACs and IQ mixers for modulated XY control, while Z control is achieved by a dedicated current-biasing circuit for frequency tuning. This hardware topology is one design paradigm: variations, such as superheterodyne architectures that use a two-stage mixing process via an IF, are also proposed in the literature [186]. Beyond the mixing scheme, a complete system design must address further operational and engineering challenges. Key issues include robust cryogenic interfacing, maintaining signal integrity, and precise multitone synthesis. Compensating for component imperfections through calibration, such as converter dynamic range limits and IQ mixer imbalances, is also required.

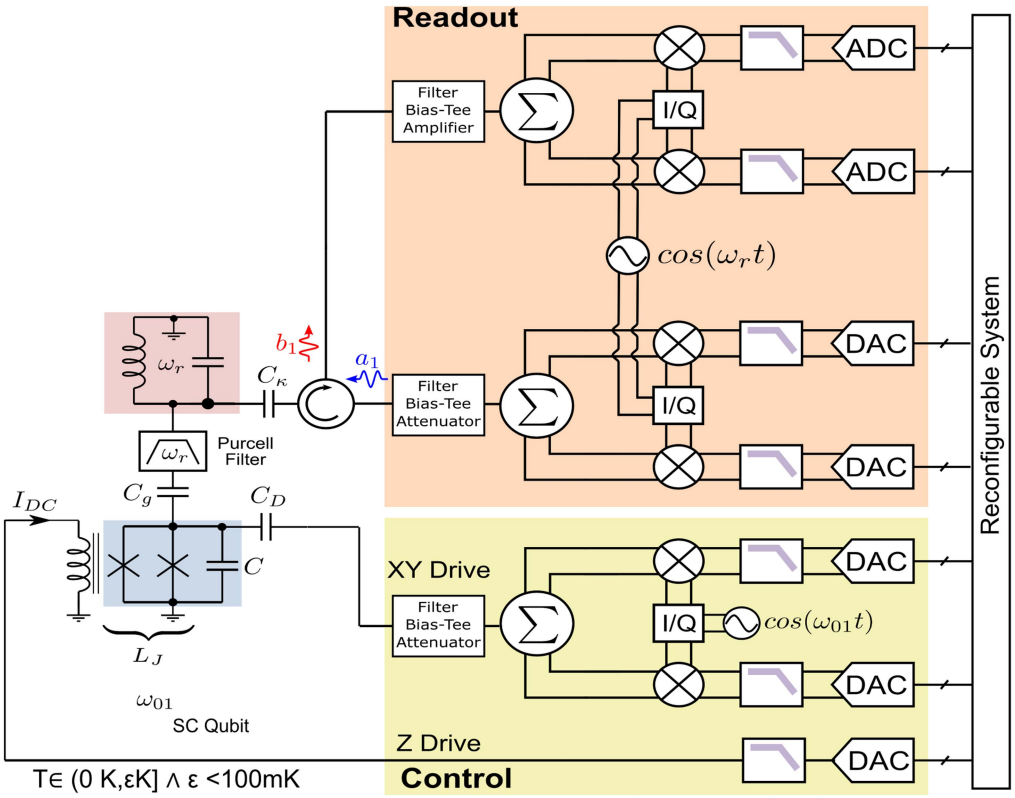

FIGURE 10. Modular system implementation for a superconducting qubit, showcasing a control and readout loop with an FPGA/reconfigurable module, data converters, and IQ mixers. This diagram illustrates a common heterodyne (IQ-mixing) architecture, a design adopted in both commercial and research-driven COTS systems.

C. STATE-OF-THE-ART COTS SYSTEMS: A CRITICAL EVALUATION

As mentioned earlier, the development of control and readout architectures is notably addressed in the literature through the development of diverse COTS systems. Consistent with this trend, recent publications detail a variety of innovative platforms. The COMPAQT [193], uses discrete cosine transform (DCT) for waveform compression, enabling the storage of compressed waveforms in memory. The real-time decompression is achieved through a dedicated hardware pipeline incorporating a run-length encoding decoder and an inverse discrete cosine transform engine. Real-time decompression may not always maintain ideal performance at high qubit counts, potentially leading to small synchronization offsets and timing errors. Furthermore, while memory power dissipation is reduced by 2.5 times compared to static storage, the tradeoff between compression ratio and real-time processing speed still poses a bottleneck, especially when trying to scale beyond the current limits. Adaptive compression algorithms could be integrated, dynamically adjusting the tradeoff between compression efficiency and latency based on real-time system requirements. Fig. 11 illustrates the COMPAQT compressed waveform memory workflow, where pulses are compressed in software and decompressed on the control hardware before conversion to analog signals.

A further example of a research-driven COTS implementation built on commercial evaluation boards is the scalable quantum control and readout system (SQ-CARS) [191]. The proposed system introduces a synchronization framework of multiple channels for multiqubit operations. Designed for multiqubit quantum processors, the SQ-CARS integrates control and readout functionalities within a modular architecture. Operating in the second Nyquist zone, the SQ-CARS, based on the ZCU111 RFSoC platform, provides microwave pulse synthesis spanning the frequency range of 4–9 GHz. The SQ-CARS incorporates direct digital synthesis of microwave pulses, maintains phase synchronization of all channels, and provides a programming interface to configure the described features. It maintains phase synchronization by leveraging the MTS capability of the RFSoC. Employing this clocking architecture, the standard deviation of interchannel jitter is minimized to approximately 0.6 ps. While phase synchronization and timing jitter are managed for current qubit counts, scaling to thousands of qubits poses a challenge. Fig. 12 shows the end-to-end control and readout signal paths in SQ-CARS, from waveform generation and digital processing to conversion and acquisition. Small jitter can accumulate across channels, leading to degraded interchannel synchronization. Managing signal routing and real-time signal processing becomes increasingly difficult, as system complexity and resource utilization grow, potentially limiting scalability.

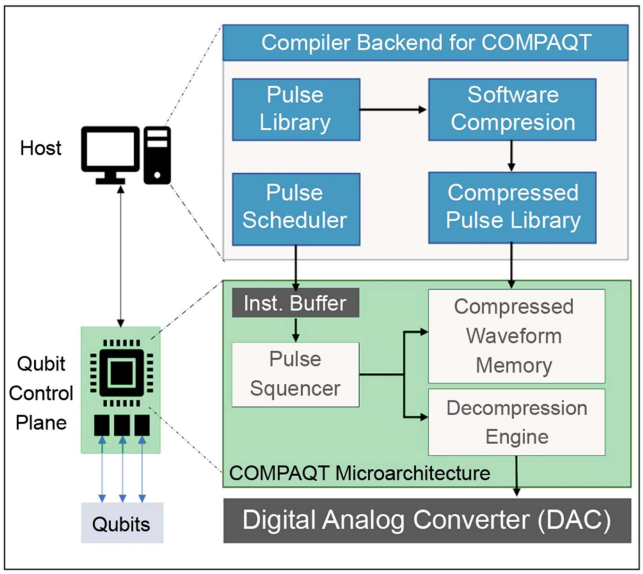

FIGURE 11. COMPAQT compressed waveform memory architecture. A host-side compiler backend performs software compression on a pulse library, which is then loaded onto the qubit control plane. An efficient on-chip decompression engine reconstructs the waveforms in real-time before they are sent to the DAC for qubit control. This figure has been reproduced from [193].

Similarly, the ICARUS-Q system [192] represents another research-driven implementation that aims to enable scalable control. The ICARUS-Q system, based on the HTG-ZRF16 RFSoC platform, provides scalability and synchronization for large-scale quantum processors. The authors characterize the direct RF output power in its normal (NRZ) mode, reporting an average of -23.1 ± 1.8 dBm in the 7–9 GHz range, noting that power deviation at higher frequencies is attributable to the balun's 8-GHz bandwidth limit. In terms of resource requirements, the authors report their implementation utilized approximately 50% of the FPGA logic blocks and 75% of its available Block RAM, with each channel supporting waveform segments of up to 65 536 samples. Intraboard interchannel synchronization uses MTS with an integrated PLL to align channel outputs to a common reference clock. For interboard synchronization, a master oscillator distributes the reference clock across interconnected boards, enhancing timing alignment during waveform generation and sampling. Synchronized multidevice data converters and waveform generators face routing complexity, potentially impacting signal purity via crosstalk and interboard communication, especially at microwave frequencies.

Prominent examples of research-driven, open-source COTS implementations include the Quantum Instrumentation Control Kit (QICK) [190] and Qubit Control (QubiC) [212]. Both were developed to provide flexible lower-cost control and readout architectures for scalable multiqubit processing. The QICK system was initially based on the Xilinx ZCU111 (Gen 1 RFSoC), featuring eight DAC channels (up to 6.5 GSa/s) and eight ADC channels (up to 4 GSa/s) [190]. More recent work utilizes newer hardware such as the ZCU216 (Gen 3 RFSoC), which offers 16 DACs (up to 9.85 GSa/s) and 16 ADCs (running at 2.5 GSa/s) [218]. QICK leverages the RFSoC's capabilities for direct digital synthesis of control pulses, achieving mixer-free operation up to 6 GHz on Gen 1 and potentially up to 10 GHz on Gen 3 hardware, using appropriate Nyquist zones. The system maintains phase coherence across channels and frequencies, crucial for protocols like parametric gates, and reports a feedback latency (readout-to-action) in the range of 184–211 ns. Fig. 13 depicts the QICK multiplexed signal-generation chain, where buffered timing data and register settings drive synthesizer channels that are combined, scaled, and converted to analog output. The newer hardware also enables features like high time resolution (100 ps on ZCU216) for pulse shaping, multiplexed readout, and predistortion for fast flux pulses [218]. QubiC, conversely, utilizes a more traditional FPGA approach, featuring real-time pulse shaping and multichannel synchronization for phase coherence across qubits. The recent QubiC 2.0 [219] upgrades the system to the Xilinx ZCU216 (Gen 3 RFSoC) platform, enabling key features such as mid-circuit measurement and feedforward. This new version, which uses 16 DACs at 8 GSa/s and two ADCs at 2 GSa/s, adopts a scalable multicore distributed processor architecture (one core per qubit) within the FPGA to handle commands on-the-fly. This contrasts with the original QubiC 1.0 [212], which utilized a more traditional FPGA approach.

Reference [211] is another research-driven COTS platform built upon the third-generation Xilinx RFSoC, named Presto. It utilizes either the ZCU208 (8 DAC/8 ADC) or ZCU216 (16 DAC/16 ADC) evaluation board. Presto utilizes direct digital synthesis for the generation of signals up to 9-GHz frequency without external mixers, leveraging the RFSoC's integrated numerically controlled oscillators (NCOs) and digital upconversion. Presto features two continuous-wave outputs for synthesizing frequencies up to 15 GHz, 16 DC-bias outputs, four inputs, and four outputs for digital triggers. The system incorporates real-time signal analysis capabilities, including template matching (matched filtering) and low-latency feedback with a reported round-trip latency between 184 and 254 ns. Multitone signal generation in pulsed mode is achieved by digitally superimposing multiple waveform templates within the FPGA before sending the composite signal to a single DAC channel, rather than consuming multiple physical outputs. While efficient, managing the computational resources for complex multitone waveforms within the FPGA could present scaling considerations.

Wang et al. [213] propose an AWG-based system for controlling and reading out a ten-qubit superconducting quantum processor, showing its capability for multiqubit control, readout, and feedback with a reported latency of 178.4 ns. High synchronization between control channels is ensured by a central clock board distributing clock and trigger signals. Characterization of six gates, each with a 50-ns operation time, using the system proposed in [213] yielded an

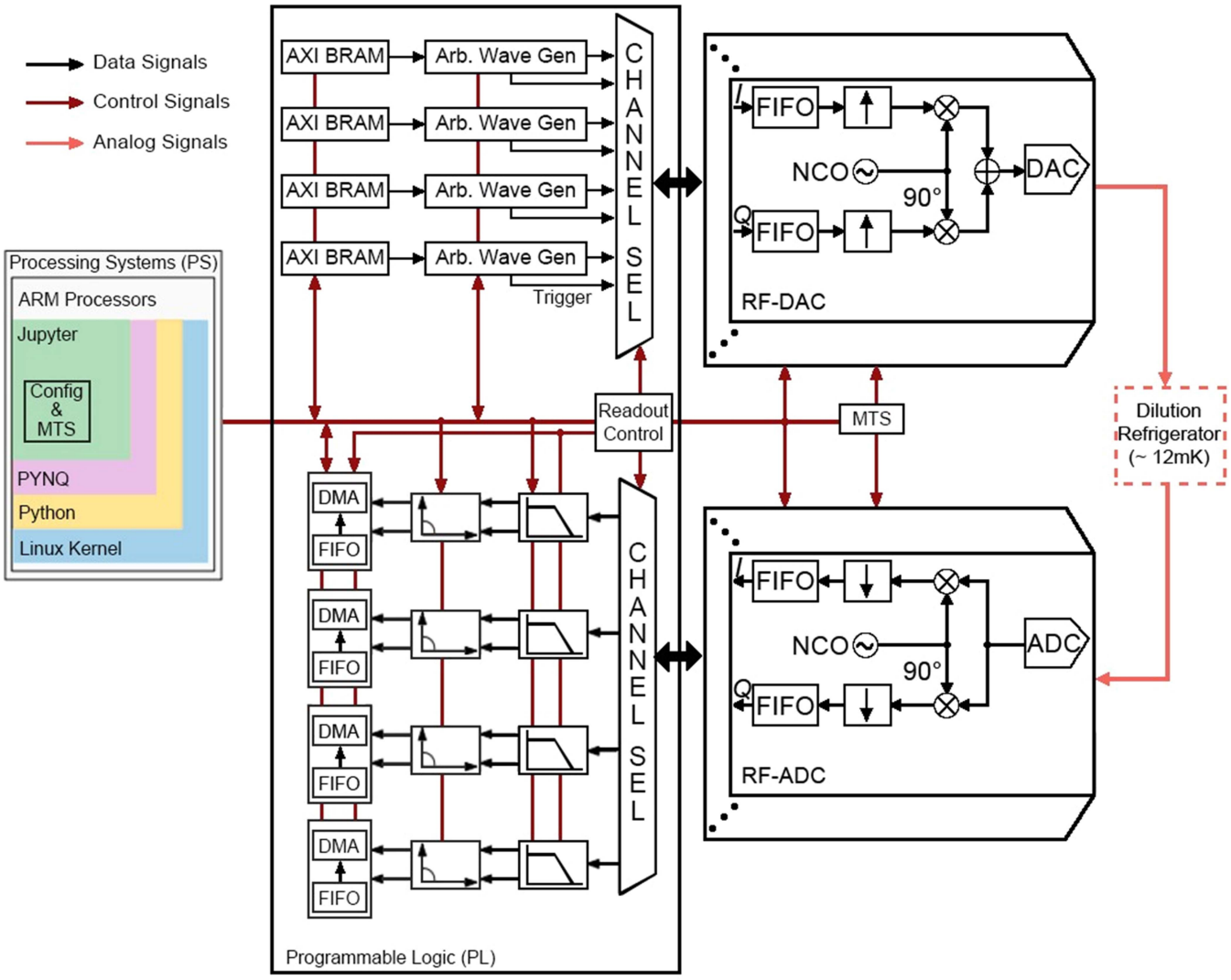

FIGURE 12. Control and readout signal paths in the SQ-CARS architecture. For quantum control (top flow), arbitrary waveforms are generated in the programmable logic (PL), upconverted by the RF-DAC, and sent to the qubits. For readout (bottom flow), analog signals are received by the RF-ADC, then digitized, downconverted, and filtered in the PL before being transferred via direct memory access (DMA) to the processing system for analysis. This figure has been reproduced from [191].

average gate fidelity greater than 99.68% . Utilizing a VPX-6 U chassis, the system integrates data converters, DC sources, and AWGs, demonstrating a modular design for flexible expansion and maintenance. While the modular design is suited for small-scale setups, scaling to control and read out thousands of qubits will require overcoming resource bottlenecks, including data throughput, signal routing, and power dissipation.

Within the research-driven COTS pathway, a distinct approach emphasizing the minimization of feedback latency was demonstrated by Yang et al. [221]. The proposed system implements a low-latency AWG based on a modular PXI 3 U architecture, integrating a Xilinx Kintex FPGA with four 14-bit DAC channels operating at 2 GSa/s. This configuration achieves an analog bandwidth of approximately 500 MHz for IF signal generation. The proposed system has a low response time with total AWG latency of only 55 ns (from trigger input to pulse output). Such performance is realized through deliberate architectural optimizations, including the use of a high-speed parallel low-voltage differential signaling (LVDS) interface between the FPGA and DACs (in place of the conventional JESD204B serial link), and the deployment of on-chip BRAM for waveform lookup operations, thereby eliminating the latency associated with external double data rate (synchronous dynamic random-access memory (DDR) memory access.

Sharing the objective of providing scalable control for superconducting qubits, and employing a modular architecture, Gebauer et al. [216] introduce an RFSoC-based qubit control system with high-level programmability for microwave pulse generation and readout. The modular design utilizes digital unit cells (QiCells), integrating signal generators, an RISC-V sequencer for 4-ns timing precision, and FDM to optimize channel usage. The system supports Python-based

TABLE 11. Features of Notable Quantum Control and Readout Systems at a Glance

COMPAQT [193]	
User interface	Python-based software system integrated with Qiskit Pulse
Processes	Compressed waveform generation via DCT at runtime
Scalability	Supports up to 5× qubits via DCT compression (IBM-Guadalupe)
Unique feature	Compressed memory with DCT for scalability and efficient storage in high-dimensional systems
SQ-CARS [191]	
User interface	Python framework
Processes	Phase synchronization, direct microwave synthesis with low jitter
Scalability	Supports 4 qubits per board, expandable to larger systems with increment in data converters
Unique feature	Phase synchronization enables scalability, reducing decoherence and enhancing qubit operation fidelity
ICARUS-Q [192]	
User interface	Python API
Processes	Hierarchical Synchronization: Intra-board with PLL, MTS with distributed triggers and D-type flip-flops
Scalability	Multi-board synchronization via distributed triggers enables high qubit addressability
Unique feature	Mixerless operation, high Nyquist zone sampling for efficient signal processing at GHz frequencies with synchronous pulses
QICK [190]	
User interface	Python API
Processes	Direct microwave synthesis for precise qubit manipulation
Scalability	Supports eight channels, stackable architecture for multichannel configurations
Unique feature	Open-source framework, low-cost design, applicable for research and educational setups
Presto [211]	
User interface	Python API
Processes	Low-latency feedback with frequency-multiplexed qubit operations, synchronous channels
Scalability	Supports multiple channels, stackable architecture for multichannel configurations
Unique feature	Synchronous multiple channels, template matching feature, applicable for research and educational setups
QubiC [212]	
User interface	Python based open-source interface
Processes	Platform to explore real-time feedback with closed-loop pulse synthesis for qubit manipulation
Scalability	Supports multiple channels, modular design with expandability options for multiqubit systems
Unique feature	Open-source, flexible pulse control architecture allowing precise control over multiqubit operations
SPulseGen [215]	
Processes	Pulse generator architecture simplifies both the generator circuit and the waveform of the RF pulse
Scalability	Aims to enhance scalability by reducing circuit cost and simplifying RF pulse generation
Unique feature	This architecture eliminates the requirement for power and cost-intensive AWGs
QiCells [216]	
User interface	Python API
Processes	Signal generation in unit cells for targeted qubit addressing; each cell has logic for single-qubit control
Scalability	Modular design with unit cells enabling scalable qubit control
Unique feature	Digital unit cells (QiCells), each with a custom RISC-V-based sequencer, and utilizing a star-point structure for synchronization
SHFQA+ [186]	
User interface	Controlled through LabOne, LabOne Q, or APIs for Python, C, MATLAB, LabVIEW™ and. NET
Processes	Real-time signal processing including matched filters (up to 16 complex filters per channel, depending on model/options)
Scalability	Integrates into the QCCS framework with other Zurich Instruments devices
Unique feature	Provides a modular and expandable solution for growing quantum computing setups
Quantum Machines (OPX+) [187]	
User interface	QUA (a pulse-level Python-based language)
Processes	Real-time pulse-level classical processing via PPU ; IF signal generation
Scalability	Modular system, scales by adding OPX+ modules; requires external mixers (e.g., Octave) for RF signal generation
Unique feature	QUA language allows complex real-time logic (loops, branching) with low latency (sub-400 ns)
Qblox (Cluster) [188], [220]	
User interface	Python APIs (JSON-based)
Processes	Heterodyne (IQ-mixing) up to 18.5 GHz; each module has its own sequence processor
Scalability	Modular 19" chassis (Cluster) holds stackable QCM-RF/QRM-RF modules
Unique feature	Distributed sequencer architecture; deterministic intermodule sync; low latency ($\tilde{3}$00–400 ns)
Keysight (QET) [189]	
User interface	Python API; HVI framework
Processes	FPGA-based real-time sequencing (HVI) on modular PXIe cards (AWGs, Digitizers)
Scalability	Industry-standard PXIe chassis allows mixing high-performance modules
Unique feature	Leverages PXIe standard; HVI framework for deterministic sequencing (below 10-ns resolution)

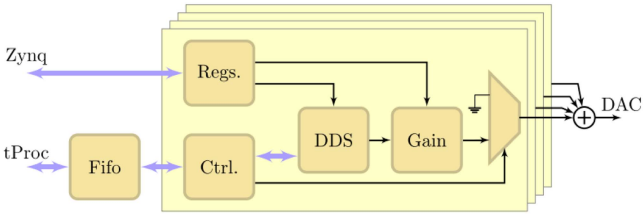

FIGURE 13. Block diagram of the multiplexed signal generation architecture of QICK. Data from the Zynq timing processor (tProc) is buffered in first in, first out control. Control logic (Ctrl.) uses these data and parameters from the Registers (Regs.) to drive one or more direct digital synthesizer channels. The synthesized signals are combined, scaled by a Gain block, and then converted to an analog signal by the DAC. This figure has been reproduced from [218].

high-level programming (QiCode) for flexible experiment definition and automated execution. The system employs IQ signals for pulse shaping, flexible FDM-based signal routing, and high-speed data acquisition. Adaptive channel routing algorithms can dynamically optimize channel allocation to enhance signal integrity and minimize interference as the system scales. Fig. 14 shows the hierarchical architecture of the QiCells system.

This architectural paradigm is further reflected in numerous commercial ventures, such as Zurich Instruments [186], Quantum Machines [187], Qblox [188], and Keysight [189]. Zurich Instruments offers a complete Quantum Computing Control System (QCCS) [222] built from modular rack instruments. The ecosystem is coordinated by the programmable quantum system controller (PQSC). This central controller uses ZSync—a proprietary, low-latency, and deterministic (sub-100-ns) link—to distribute timing, triggers, and coordinate all specialized instruments. The system is supported by several key instruments.

1) The SHFQA [186] integrates 14-bit data converters and real-time matched filters, enabling multiplexed readout of up to 64 qubits over a 1-GHz bandwidth.
2) The SHFQC [223] provides an integrated control and readout solution for up to six qubits. It is designed for algorithms requiring fast, conditional logic, featuring an internal feedback path with low latency from measurement to conditional pulse emission—a key metric for quantum error correction.
3) The SHFSG+ (SHF Signal Generator) [224] variant is available for systems with higher-frequency qubits, offering a direct microwave synthesis range of up to 16 GHz using a double superheterodyne technique.

For high-channel-count systems, the architecture scales using the Quantum System Hub (QHub). This infrastructure device forms the center of a star-topology QCCS, providing automated synchronization and a powerful central processor. With 56 ZSync ports, the QHub can coordinate up to 56 instruments, enabling the control of systems with as many as 448 microwave channels or up to 300 fixed-frequency qubits. The entire architecture is programmed via the LabOne Q software, which provides a high-level Python API for system-level control. The block diagram of the Zurich Instruments QCCS is shown in Fig. 16 .

Quantum Machines centers its architecture on the OPX+ platform, which is controlled by a dedicated, FPGA-based real-time processor called the pulse processing unit (PPU). This processor executes a pulse-level programming language (QUA), designed to integrate complex quantum operations (like pulse generation and acquisition) with classical processing (like loops and branching). This architecture allows for complex, real-time logic and feedback with latencies reported in the sub-400-ns range. The OPX+ modules feature 16-bit 1-GSa/s DACs and 12-bit 1-GSa/s ADCs, with integrated direct digital synthesis capable of generating control signals at an IF, which are then typically upconverted to microwave frequencies using external analog mixers (such as those integrated into the companion Octave module [225]).

Adopting a distinctly modular approach, Qblox provides a scalable solution with its Cluster platform [220], a 19-inch chassis that holds compact and stackable modules. The system is built using QCM-RF (Qubit Control) and QRM-RF (Qubit Readout) modules, each containing its own internal sequence processor for real-time sequencing. Fig. 15 shows a detailed schematic of the QCM-RF module internal architecture. This architecture supports a wide frequency range via heterodyne (IQ-mixing) up to 18.5 GHz. The modules integrate 16-bit 1-GSa/s DACs and 12-bit 1-GSa/s ADCs, enabling low-latency feedback (reported in the 300–400 ns range) and deterministic intermodule synchronization.

Keysight's Quantum Engineering Toolkit (QET) is built on the industry-standard PXIe (PXI Express) modular instrumentation platform [189]. This architecture leverages Keysight's portfolio of high-performance modules, such as the M3202A AWG (1 GSa/s, 14-bit) and the M3102A Digitizer (500 MSa/s, 14-bit). For applications requiring fast feedback, Keysight also provides integrated "combo" modules like the M3302 A, which combine AWG and digitizer functions on a single card and specify an input-to-output latency of less than 400 ns. The platform's real-time performance is driven by on-board Xilinx Kintex-7 FPGAs programmed with Keysight's Hard Virtual Instrument (HVI) technology. This HVI framework enables deterministic sequencing with a timing resolution below 10 ns and orchestrates the low-latency feedback required for quantum control protocols.

Calibration can improve the operational fidelity of modular quantum systems. It involves optimizing gate parameters, qubit frequencies, and pulse shapes, to reduce errors and ensure high-fidelity operations. Modular platforms may simplify this process by integrating calibration workflows into their control-readout architectures. C3 (control, calibration, and characterization) [226] provides automated calibration routines that can integrate with modular systems like SQ-CARS and QICK. By incorporating machine learning algorithms, C3 fine-tunes pulse parameters to achieve gate fidelity exceeding 99.9% . Similarly, open-source tools like QuTiP [227] and Qiskit Aer [228] offer simulation

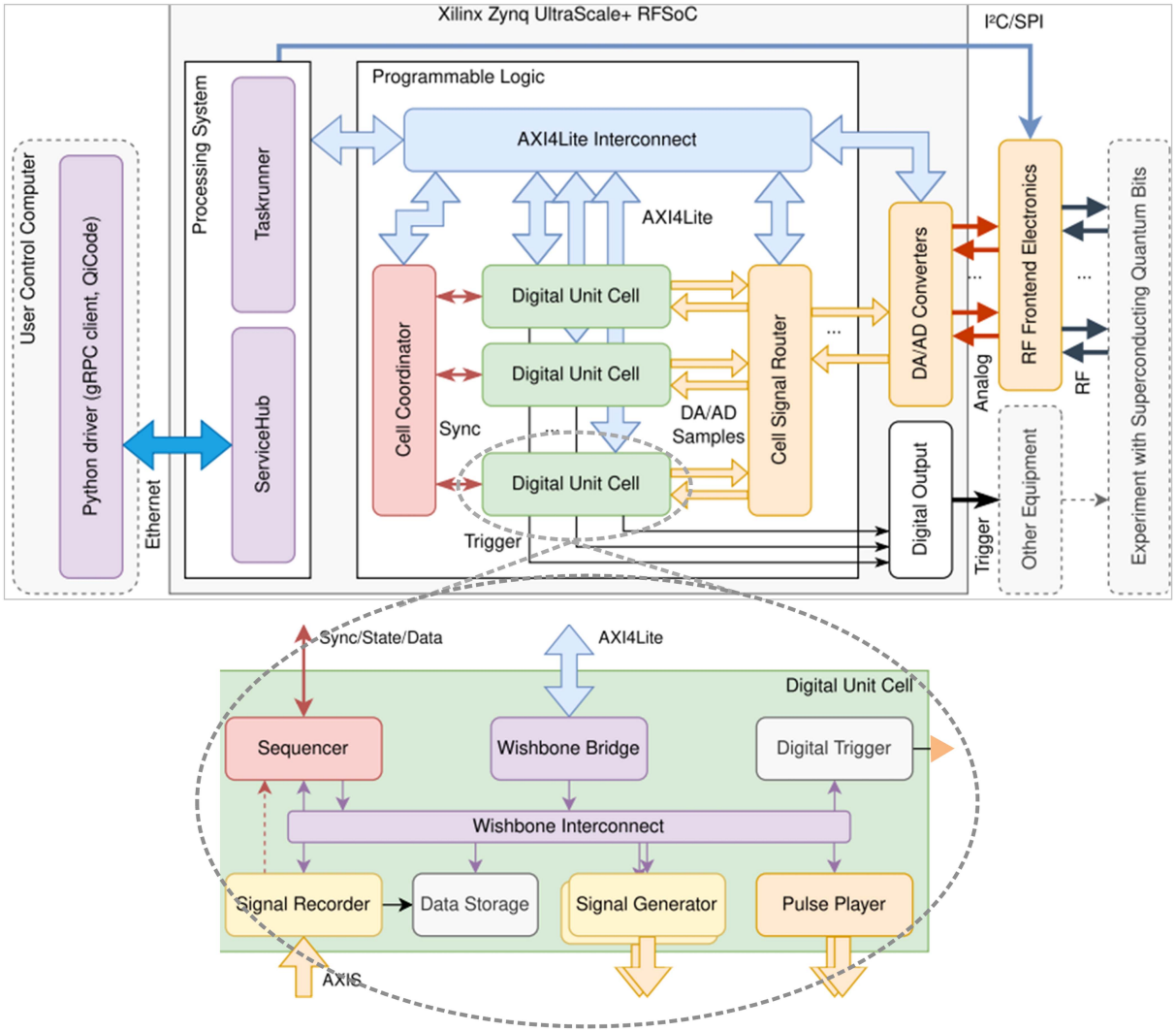

FIGURE 14. Hierarchical architecture of the QiCells system. The platform is split between a user control computer for high-level Python-based programming (QiCode) and a Xilinx RFSoC for real-time execution. The RFSoC's processing system manages tasks, while the programmable logic contains the modular hardware. A "cell coordinator" dispatches commands to multiple "digital unit cells" (QiCells). The magnified view details a single QiCell, which integrates a sequencer, signal generator, and pulse player for autonomous pulse generation. This figure has been reproduced from [216].

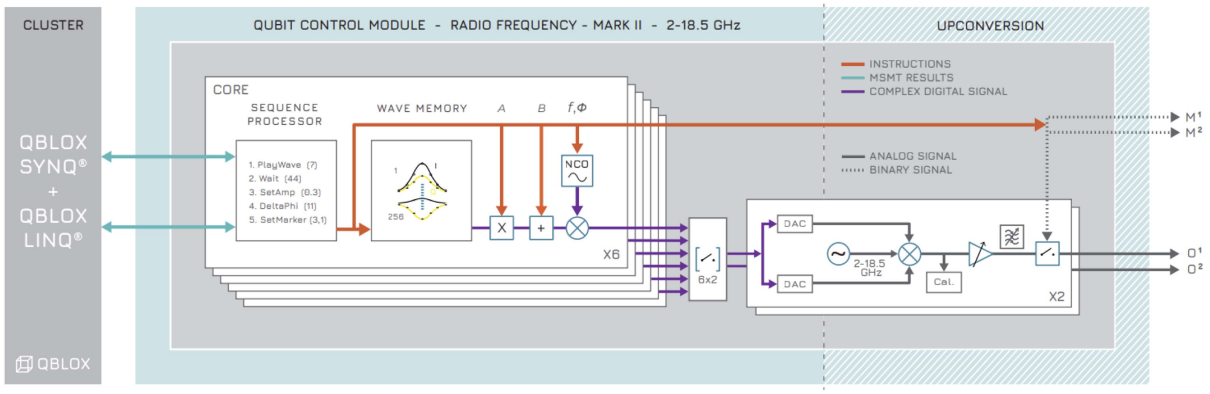

FIGURE 15. Signal flow within the Qblox QCM-RF module. A sequence processor orchestrates the playback of I/Q waveforms from wave memory, which are modulated by an NCO. This complex baseband signal is then upconverted using an IQ-mixer and a 2–18.5 GHz LO to produce the final RF drive pulses. The figure has been reproduced from [220].

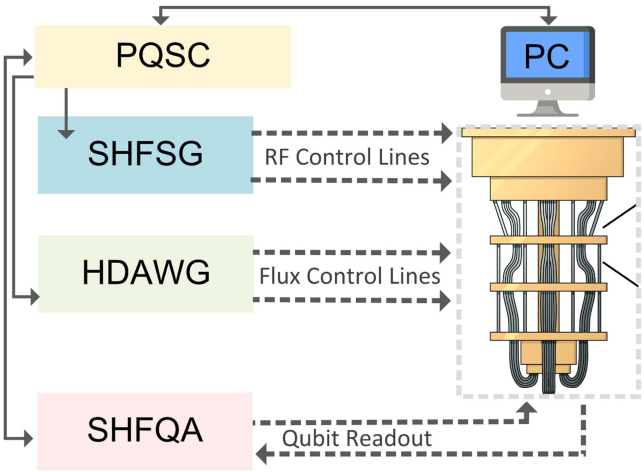

FIGURE 16. Block diagram of the Zurich Instruments QCCS. The central PQSC controller coordinates the SHFSG (RF control) and HDAWG (flux control) signal generators. Qubit readout is processed by the SHFQA, which sends feedback to the PQSC, while high-level control is managed by a PC.

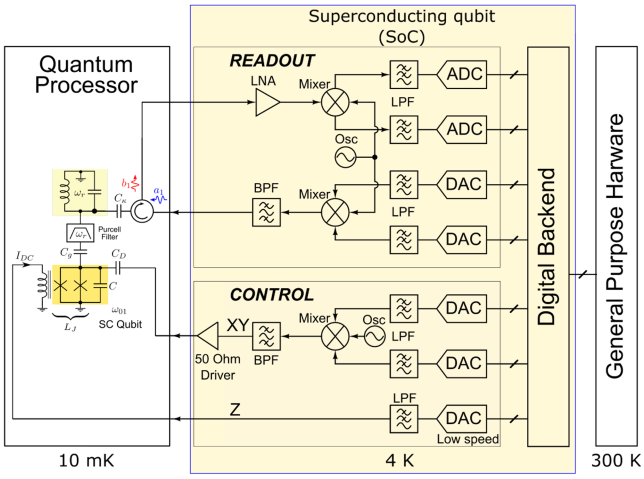

FIGURE 17. Multistage Cryo-CMOS architecture for superconducting qubit control and readout, integrating ADCs, DACs, LO, mixers, and amplifiers.

frameworks, enabling researchers to validate and optimize calibration routines before deployment.

D. COMPARATIVE ANALYSIS OF COTS SYSTEMS

The commercial and modular systems discussed in the preceding sections offer a variety of approaches to quantum control and readout, each aimed to achieve the scale necessary to realize fault-tolerant quantum computers capable of executing complex algorithms. Currently, fault-tolerant quantum computers capable of executing complex algorithms have not been realized [41].

RFSoC-based platforms, such as QICK, SQ-CARS, ICARUS-Q, and Presto, are built to leverage the tight integration of FPGAs with high-speed data converters on a single chip. This enables mixer-free direct microwave synthesis and feedback latencies in the sub-300-ns range. Other platforms target specific bottlenecks. COMPAQT, for instance, focuses on solving the waveform memory challenge through real-time compression, while QiCells demonstrates a cell-based approach to distributed control. Table 11 provides an overview of their distinctive user interfaces, processes, scalability aspects, and unique features.

The platforms listed in Table 11 adopt diverse strategies to address issues of resource overhead. SQ-CARS achieves scalability by employing phase synchronization across multiple boards, with the capacity to expand by adding more data converters. ICARUS-Q utilizes a multiboard synchronization scheme based on distributed triggers, enabling the control of a large number of qubits. Modular architectures, as seen in QICK, Presto, QubiC, and QiCells, offer a pathway to increased channel counts and thus greater qubit addressability through the stacking or interconnection of individual units. Table 12 compares selected commercial and off-the-shelf quantum control and readout systems in terms of hardware platform, converter specifications, frequency coverage, and reported latency.

A trend can be observed in the leading commercially integrated systems. Platforms from Zurich Instruments, Quantum Machines, Qblox, and Keysight all adopt a modular rack-based approach for scalability. Keysight leverages the industry-standard PXIe chassis and its HVI framework for FPGA programming. In contrast, Zurich Instruments and Qblox use proprietary 19” chassis with high-speed backplanes (e.g., ZSync, SYNQ/LINQ) for ultralow-latency intermodule synchronization. Quantum Machines employs a centralized PPU running the pulse-level language QUA, while Qblox distributes this intelligence by embedding an RISC-V processor in each module. Finally, the SHFQA+ from Zurich Instruments offers a modular and expandable solution that integrates into a broader QCCS framework, highlighting its suitability for growing quantum computing setups.

Common to nearly all modern platforms is the adoption of high-level Python APIs. This convergence simplifies experiment design, allowing researchers to use familiar tools to define complex pulse sequences, while the underlying hardware (PPU, HVI, or RISC-V sequencers) handles the microsecond-level real-time execution.

E. KEY RESEARCH TOPIC: OVERCOMING SCALING BOTTLENECKS

Further research is anticipated in real-time feedback mechanisms, improved pulse shaping techniques, and more efficient use of control resources. From the literature, we analyze that scaling introduces significant technical roadblocks, notably concerning data throughput rates and power dissipation associated with interconnects. Signal integrity is affected with increased interconnect density and the complexity of routing signals across multiple boards. As the number of qubits increases, the latency and bandwidth requirements across control, readout, and feedback channels will

TABLE 12. Representative COTS Quantum Control and Readout Systems (Selected Examples)

System	Core hardware	DAC / ADC Specs	Freq. range / bandwidth	Latency (feedback)
COMPAQT [193]	RFSoC	4.54 GSa/s (DAC) (platform dependent)	platform dependent	(platform dependent) Readout $<$ 500ns
SQ-CARS [191]	Xilinx ZCU111 (Gen-1 RFSoC)	14-bit, 6.144 GSa/s (DAC) 12-bit, 4.096 GSa/s (ADC)	4–9 GHz (2nd Nyquist zone reported)	sub-50 to 250 ns (For different operations)
ICARUS-Q [192]	HTG-ZRF16 (Gen-3 RFSoC)	14-bit, 6.144 GSa/s (DAC) 12-bit, 1.966 GSa/s (ADC)	Up to $\sim$8 GHz	N/R
QICK [190]	Xilinx ZCU111 / ZCU216	Generation dependent (see source)	Gen-1: up to $\sim$6 GHz Gen-3: up to $\sim$10 GHz	184–211 ns (reported total latency)
Presto [211]	Xilinx ZCU208 / ZCU216 (Gen-3 RFSoC)	Uses board DACs/ADCs	Up to $\sim$9 GHz (DDS); CW outputs to $\sim$15 GHz (reported)	184–254 ns (reported)
QubiC 2.0 [219]	Xilinx ZCU216 (Gen-3 RFSoC)	14-bit, 8 GSa/s (DAC) 14-bit, 2 GSa/s (ADC)	N/R	mid-circuit feed-forward capable (reported)
Yang et al. [221]	Xilinx Kintex FPGA + PXIe	14-bit @ 2 GSa/s (reported for their AWG)	$\sim$500 MHz (IF)	55 ns (trigger-to-output, reported)
Zurich Inst. SHFQA / SHFQC [186], [223]	Commercial Integrated Systems	14-bit, 6 GSa/s (DAC) 14-bit, 4 GSa/s (ADC)	Up to 8.5 GHz (vendor)	$<$300 ns (vendor/leaflet reports)
Quantum Machines (OPX+) [187]	Commercial integrated platform (OPX+)	16-bit, 1 GSa/s (DAC) 12-bit, 1 GSa/s (ADC)	IF: DC–400 MHz	224–272 ns (reported)
Qblox (Cluster) [188], [220]	Commercial integrated cluster (19" chassis)	16-bit, 1 GSa/s (DAC) 14-bit, 5 GSa/s (ADC)†	Up to $\sim$18.5 GHz (via IQ mixing, vendor)	$\sim$350–400 ns (reported)

Latency values refer to the interval from readout to conditional pulse, or from trigger to action, as reported by the cited sources; measurement methodology (trigger placement, processing path, and start/stop definitions) varies across vendors.

increasingly challenge current hardware capabilities. Adaptive algorithms for dynamic routing and optimized signal integrity protocols may help overcome some challenges, but real-time feedback mechanisms and low-latency synchronization still require further development to handle more complex systems beyond the NISQ era.

VI. CRYO-CMOS PATHWAYS FOR DENSE QUBIT ARRAYS

A. OVERVIEW OF CRYO-CMOS SYSTEMS

Cryo-CMOS systems are integral enablers for current and future quantum computing technologies. Operating at temperatures typically below 4 K, Cryo-CMOS systems lead to: 1) a significant reduction of thermal noise; 2) the facilitation of high-density shorter interconnects with potentially reduced parasitic capacitance and inductance; and 3) precise and coherent control of quantum gates. The challenging nature of the cryogenic environment mandates the development of power efficient, thermally stable, and scalable electronic systems designed for reliable operation within a temperature range of 10 mK to 4 K.

B. OPERATIONAL CHALLENGES IN CRYOGENIC ENVIRONMENTS

1) DEVICE-LEVEL CHALLENGES AT CRYOGENIC TEMPERATURES

Meeting the operational demands of superconducting qubits, Cryo-CMOS systems must not only withstand these near absolute-zero conditions but also support the low-noise control and readout mechanisms. Unique challenges are faced at this temperature regime, including but not limited to evolved transistor behavior [229], carrier freeze-out [230], kink effect [231], modified threshold voltages [232], [233], performance degradation of passive components [234], and subthreshold swing degradation [235].

2) SYSTEM-LEVEL CHALLENGES FOR QUBIT CONTROL AND READOUT

To address system-level operational constraints, the architectural design of electronic systems for cryogenic environments takes space and wiring constraints into account to enable compact, scalable, and thermally efficient integration. As the system is in periphery with the qubits, Cryo-CMOS allows for reducing the complexity and latency associated with the qubit control [236]. Therefore, various research initiatives are exploring effective architectures, leveraging these advantages to scale systems for practical applications.

3) SIGNAL MODULATION STRATEGIES IN CRYOGENIC ENVIRONMENTS

IQ modulation facilitates to dynamically modify the control signals to satisfy the requirements of various qubit modalities. SSB modulation is commonly employed to optimize bandwidth utilization, enabling the efficient transmission of

high-frequency qubit control signals. Although SSB modulation does not directly minimize thermal noise (which is primarily addressed by the cryogenic environment), the narrower bandwidth can lead to a reduction in the total noise power within the signal band [237], potentially improving the SNR. The typical cryogenic control and readout system architecture, illustrated in Fig. 17, outlines a multitemperature stage design for quantum computation for efficient qubit manipulation and measurement.

C. KEY DESIGN CONSIDERATIONS FOR CRYO-CMOS SYSTEMS

Designing Cryo-CMOS systems presents multifaceted challenges spanning device, circuit, and system levels. Critical aspects include stringent power dissipation limits, noise and nonideality management, precise device modeling at cryogenic temperatures, and sophisticated packaging and integration techniques.

1) DESIGN CONSTRAINTS: POWER DISSIPATION AND THERMAL MANAGEMENT

Power dissipation (P) within the constrained thermal budget of dilution refrigerators ($\dot{Q}_{\text{cool}}$) poses a design limitation at each stage. To maintain the desired operating temperature, thermal analysis must verify that the power dissipation does not exceed the cooling power ($P \ll \dot{Q}_{\text{cool}}$). Exceeding this thermal limit can lead to decoherence in nearby qubits and degrade system performance. Efficient power management strategies, including low-power circuit architectures, dynamic power scaling, and localized thermal isolation techniques, can be used for minimizing thermal impacts in scalable cryogenic quantum systems. In [144], cryogenic controllers are divided into two broad categories: those with restricted and reduced power functionality and those with moderate/high power and comprehensive functionality. Thus, power dissipation is an important factor of categorizing Cryo-CMOS circuits.

2) CIRCUIT-LEVEL NONIDEALITIES AND NOISE SOURCES

Although thermal noise is lessened at cryogenic temperatures, control and readout operations may be hampered by additional noise sources as flicker noise [239], random telegraph noise [240], and intermodulation distortions [241]. Furthermore, issues such as image artifacts, SFDR, and LO leakage present addition challenges [36], since they introduce unwanted signals or degrade the spectral purity of the generated waveforms.

3) DEVICE BEHAVIOR AND MODELING AT CRYOGENIC TEMPERATURES

Cryogenic temperatures significantly alter the behavior of the semiconductor devices. Phenomena such as threshold voltage shifts, incomplete dopant ionization, and changes in carrier mobility [36], [242], [243], [244] are needed to be incorporated in simulation models. Researchers have developed empirical and physics-based models to address these gaps, but further refinements are needed to capture the precise behavior at temperatures near 4 K for faithful system-level performance predictions.

4) PACKAGING, INTEGRATION, AND ELECTROMAGNETIC COMPATIBILITY

Extending beyond individual circuit design, the packaging and interconnect technologies employed in Cryo-CMOS systems are also an area of research. This enables multilevel integration with cryogenic quantum processors, addressing aspects such as signal routing, impedance matching, and thermal conductance between different temperature regimes. State-of-the-art packaging techniques, such as flip-chip bonding [245] and through-silicon vias [246], have been explored to reduce parasitic effects and maintain signal fidelity. In addition, the physical proximity of control electronics to quantum processors introduces the risk of electromagnetic coupling and crosstalk [247], which can degrade qubit performance. Innovations in 3-D integration and heterogeneous integration techniques are being explored to address these challenges [248], [249].

D. STATE-OF-THE-ART CRYO-CMOS SYSTEMS: A CRITICAL EVALUATION

In the literature, various Cryo-CMOS solutions have been developed to advance control and readout architectures [196], [197], [238], [250], [251], [252]. For instance, Le Guevel et al. [238] present a Cryo-CMOS controller particularly used for fluxonium qubits. Fluxonium qubits are a type of superconducting qubits characterized by lower operating frequencies and higher anharmonicity compared to transmon qubits, which make them preferred for low-power and spectrally relaxed control [253]. The proposed Cryo-CMOS controller, fabricated in a 22-nm fully depleted silicon-on-insulator (FD-SOI) technology, consumes less than 1.2 mW per active qubit and generates spectrally controlled microwave pulses with durations ranging from 1 to 255 ns. It achieves phase accuracy better than 0.5° and amplitude accuracy within 0.55% through a pulse shaping circuit with programmable amplitude and duration. Quantum experiments demonstrate its capability to perform high-fidelity single-qubit operations, achieving gate error rates as low as 0.22%. However, thermal isolation requirements and potential electromagnetic interference in dense multiqubit systems have not been addressed. Crosstalk, dynamic timing synchronization, and the impact of scaling the controller to larger quantum arrays remain open technical challenges. Future research could focus on extending the controller architecture to support multiqubit control with synchronized and low-error operations.

Yoo et al. [250] propose a Cryo-CMOS IC designed for Sycamore quantum processor unit cell [254], providing complete RF and baseband control of transmon qubits. The architecture integrates two RF pulse generators for XY qubit control and three current generators for Z line (qubit frequency

control via flux bias). In addition, the architecture features a qubit-qubit coupling rate (g) controller, supporting multilevel signal generation. Each generator employs a direct-conversion scheme, with DACs summing current pulses of varying duty cycles, allowing for precise waveform synthesis. The IC demonstrates integration efficiency, consuming 7.4 mW while achieving gate error rates as low as 0.17%, validated on a two-qubit patch of the Sycamore processor. Future research may focus on mitigating crosstalk, spurious signal generation, and dynamic range limitations in scaled qubit systems.

Chakraborty et al. [196] presents a dual-channel qubit state controller optimized for cryogenic operation at 3.5 K. The controller incorporates a custom domain-specific processor to semiautonomously execute qubit control sequences. Its architecture includes 10-bit IQ DACs, an SSB mixer, and a programmable baseband filter, enabling RF pulse generation with noise floors below −80 dBc/MHz at 5 K. The current-mode design minimizes power consumption by reusing bias currents across the analog datapath. Experimental results demonstrate Rabi oscillations and coherence times comparable to conventional room temperature controllers, with a power dissipation of 23.1 mW at 5 K. The controller relies on external sequencing and coordination for complex multiqubit operations or feedback-based adaptive control. Extending the controller architecture toward multichannel and multiqubit support with synchronized clock domains and coordinated pulse generation would represent a step toward scalable cryogenic quantum systems.

Guo et al. [197] introduce a Cryo-CMOS chipset for quantum computing, integrating a phase-detection-based reflective readout ASIC (ASIC-1) and a phase-shifter-based controller ASIC (ASIC-2). The readout ASIC employs a quadrature upconversion transmitter, an N-path filter-based receiver, and phase-detection using TDC. It supports simultaneous two-qubit state readout with a power consumption of 11 mW. The controller ASIC, based on a polar architecture, integrates XY and Z drivers, which can also generate DRAG pulses. The chipset demonstrates high readout fidelity ($\sim$ 94.8%) and efficient qubit manipulation, consuming 4.3 mW per qubit for active control. Future research may explore enhancing the chipset to support dense multiplexed readout and control architectures with robust calibration and drift-compensation schemes.

Furthermore, Patra et al. [251] present a scalable Cryo-CMOS controller operating at 3 K, designed for frequency-multiplexed qubit control. The architecture features 32 NCOs with a frequency resolution of 0.2 kHz for FDM, enabling multiqubit control using a single external LO. A polar modulator generates IQ pulses for high-fidelity qubit operations over a 2–20 GHz frequency range. Key innovations include a digitally intensive instruction-based controller with an integrated SRAM for pulse shaping, which reduces data transfer requirements to $\sim$ 1 kb/s. The analog front-end employs a current-steering DAC, a quadrature Gilbert-cell mixer, and a wideband amplifier for signal conditioning. One important open question is whether the polar modulation technique and wideband analog front-end can maintain high-fidelity performance across diverse qubit modalities and broad frequency ranges. Robust analog front-end design, encompassing current-mode DACs and wideband mixers, is essential for preserving signal quality; scaling to larger qubit arrays will demand enhanced linearity, noise suppression, and thermal robustness.

Kang et al. [198] introduces an efficient cryogenic pulse modulator IC, operating within a frequency range of 2–7 GHz. The IC employs a nonlinear DAC coupled with a linear interpolating DAC to enhance hardware compactness. The nonlinear DAC translates a triangular waveform into a sinusoidal output using custom-defined steps, providing a fine effective resolution despite limited input bits. In addition, the pulse modulator supports advanced shaping techniques, including raised-cosine and rectangular pulse shaping, achieved through a shunt-based amplitude modulation method. To explain the use case, experiments involving Rabi and Ramsey oscillations with a superconducting transmon qubit at 77 K are performed. The modulation scheme is mathematically characterized by representing the output signal as $y(t) = x(t)\sqrt{1+\alpha^2}\sin(\omega_0 t + \tan^{-1}(\alpha))$, where $x(t)$ is the baseband signal, ω_0 is the carrier frequency, and α is an amplitude weighting factor. This formulation enables dynamic control over both amplitude and phase. The reliance on custom nonlinear DAC mappings may present challenges for scaling to high-fidelity multiqubit control, where process variation and drift could impact waveform accuracy and spectral purity. Future work could focus on adapting the nonlinear DAC architecture for enhanced calibration and self-correction to compensate for fabrication and thermal drifts. Table 13 shows the technologies at a glance.

E. COMPARATIVE ANALYSIS OF CRYO-CMOS SOLUTIONS

The analysis of Cryo-CMOS technologies for qubit control and readout proposed in the literature highlight their applications, challenges addressed, integration levels, experimental validations, and utilization scope. Each solution targets a specific paradigm of quantum control and readout, from single-qubit operation to large-scale processors. For instance, the 22-nm FD-SOI controller for fluxonium qubits [238] demonstrates a low-frequency and scalable approach with low power consumption, making it suitable for single-qubit research setups. In contrast, the 28-nm Bulk-CMOS IC [250] for Sycamore processor showcases its capability to address lightweight data handling while maintaining low error rates. Similarly, solutions like the scalable 2–20 GHz controller [251] utilize FDM to efficiently manage high channel counts, positioning it as a candidate for multiqubit control along a single cable.

While the surveyed Cryo-CMOS architectures demonstrate substantial progress, several capabilities remain largely unaddressed across the surveyed literature. Native support

TABLE 13. Comparison of Representative Cryo-CMOS Implementations for Qubit Control and Readout

[238]	
Technology node:	22-nm FD-SOI
Power consumption:	< 1.2 mW per active qubit
Operational temp:	4 K
Error metrics:	Gate error: $\sim 0.22\%$
Scalability:	Single qubit, scalable with additional qubits (Multiqubit control not yet demonstrated)
Key features:	Direct pulse synthesis, phase interpolator for 0.5° resolution
Innovation/advancements:	Reduced power consumption and direct low-GHz signal generation
Challenges addressed	Power efficiency, signal fidelity, low frequency control
Utilization scope:	Suitable for fluxonium qubits in research environments, emphasizes low-power control systems
[250]	
Technology node:	28-nm Bulk-CMOS
Power consumption:	7.4mW total
Operational temp:	3 K
Error metrics:	0.17% single-qubit gate error
Scalability:	Two qubit control unit-cell
Key features:	Integrated RF pulse generators for *XY*, *Z*, and *g*
Innovation/advancements:	Compact instruction set for lightweight data handling, optimized for Sycamore Processor
Challenges addressed	Efficient data handling, low-power signal generation for qubit control
Utilization scope:	Suitable for superconducting qubits requiring compact, low-power unit-cell control; highly adaptable
[196]	
Technology node:	14-nm FinFET
Power consumption:	23.1mW (max)
Operational temp:	3.5 K
Error estimation metrics:	0.08% per Clifford gate
Scalability:	Supports two qubits per chip
Key features:	Dual-channel RF AWG, semi-autonomous operation
Innovation/advancements:	Low power operation with AWG flexibility
Challenges addressed	Low power for cryogenic stages
Utilization scope:	Semi-autonomous operation in superconducting qubits, with a focus on compact scalability
[197]	
Technology node:	28-nm Bulk CMOS
Power consumption:	11-mW readout, 4.3mW per *XY* driver
Operational temp:	3.5 K
Error estimation metrics:	94.8% and 92.6% fidelity
Scalability:	Supports two qubits per chip
Key features:	Phase-detection based readout, DRAG pulse generation
Innovation/advancements:	Low-power readout and pulse generation, inclusion of DRAG Pulse
Challenges addressed	Power efficiency in readout and multiqubit control
Utilization scope:	Versatile for XY control and qubit readout in superconducting quantum processors; supports experimental setups
[251]	
Technology node:	22-nm FinFET
Power consumption:	~ 1.7mW per qubit
Operational temp:	3 K
Error estimation metrics:	Gate fidelity: 99.99
Scalability:	128 channels (32 per TX)
Key features:	FDMA, arbitrary IQ pulse generation
Innovation/advancements:	Wide frequency range, scalable FDMA architecture, IQ correction
Challenges addressed	Wide frequency operation, FDMA implementation
Utilization scope:	Optimized for large-scale spin-qubit systems using FDMA; supports frequency multiplexing
[198]	
Technology node:	40-nm Bulk CMOS
Power consumption:	5.5mW/channel
Operational temp:	77 K
Scalability:	Six independent pulse modulators
Key features:	Sinusoid-shaping nonlinear DAC, raised cosine filtering
Innovation/advancements:	Energy-efficient direct synthesis
Challenges addressed	Scalable pulse generation with low power
Utilization scope:	Suitable for high-frequency superconducting qubits requiring energy-efficient modulation with minimized power

FDMA: frequency-division multiple access.

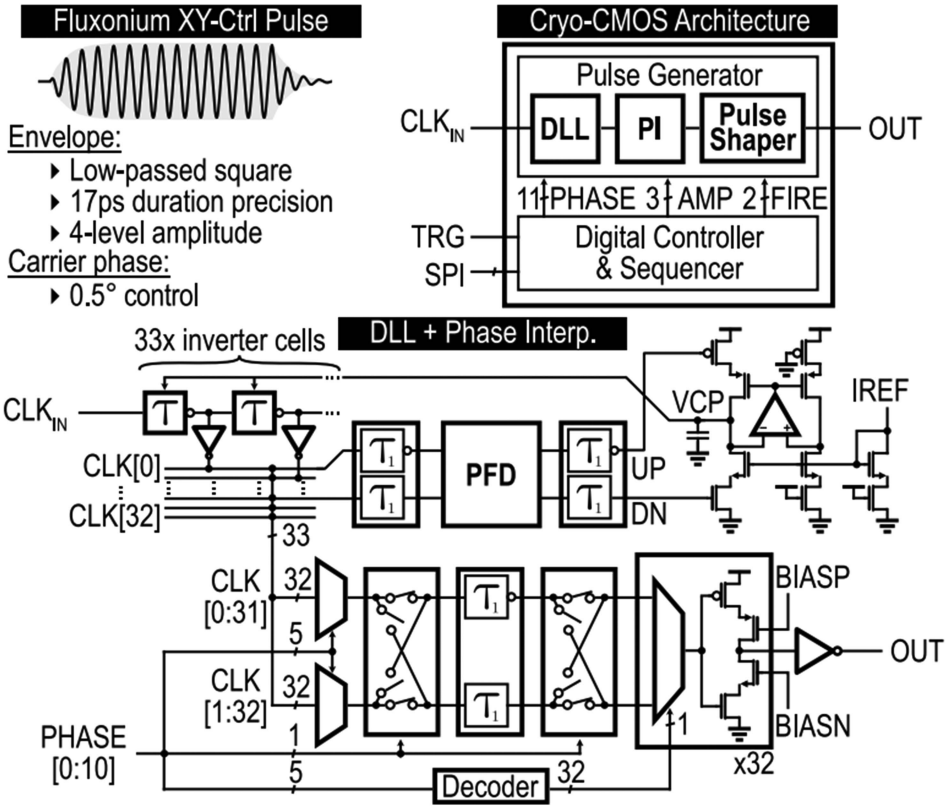

FIGURE 18. Block diagram of the AWG-free cryo-CMOS controller architecture. The system generates fluxonium XY-control pulses by combining a DLL and phase interpolator (PI) for carrier phase control with a separate pulse shaper for the envelope. A digital controller and sequencer manage the gate operations. Figure reproduced from [238].

for real-time error correction, closed-loop feedback mechanisms, fully autonomous cryogenic control, adaptive calibration and drift compensation, and flexible signal generation are generally absent. This survey of recent advancements in Cryo-CMOS technology reveals the dynamic potential for innovation.

Despite the challenges at cryogenic temperature, the experimental validations emphasize the growing maturity of Cryo-CMOS technologies, with metrics such as SFDR, readout fidelity, and gate error rates illustrating their potential for real-world deployment. Representative cryogenic CMOS based quantum control and interface architectures are illustrated in Figs. 18, 19, 20, 21, covering on chip pulse generation and shaping, integrated controller microarchitecture, and complete cryogenic control and readout interface chipsets.

VII. EMERGING PATHWAYS FOR QUANTUM INSTRUMENTATION: NEW FRONTIERS

A. ADDRESSING INTERCONNECT LIMITATIONS

Among the prominent emerging technologies are wireless transceiver-based approaches [255], [256], temperature-sensing-based readout technologies [257], and optical interfaces [258]. In a direct comparison, optical fibers offer vastly lower thermal conductivity than conventional coaxial cables, a property that reduces the heat load by two orders of magnitude [259]. Furthermore, they feature low signal loss (approximately 0.2 dB $\cdot$ K $\cdot$ m^{-1}), a stark improvement over the significant losses (approximately 3.0 dB $\cdot$ m^{-1}) of coaxial cables at gigahertz frequencies [260]. While still experimental, these technologies enable a shift from brute-force wiring to the integrated architectures required for large-scale, fault-tolerant quantum computation.

B. OVERVIEW OF EMERGING PATHWAYS

This article surveys three major technology directions: wireless microwave and terahertz links, optical interconnects/interfaces, and thermometry-based readout techniques. Fig. 22 illustrates these distinct approaches, all sharing the common goal of reducing thermal load, improving scalability, and enabling high-fidelity operations. Wireless approaches replace physical wiring with electromagnetic wave transmission between cryogenic and room temperature stages. Optical technologies, which leverage components like EOMs and lasers to transfer data via optical fibers, offer high bandwidth and reduced thermal load. In addition, a novel approach has been proposed in the literature [257] for thermometry-based readout of qubit states, enabling state discrimination based on thermal signatures. Thus, the limitations imposed by conventional electrical interconnects underscore their role as a significant impediment to achieving high-density qubit control [261].

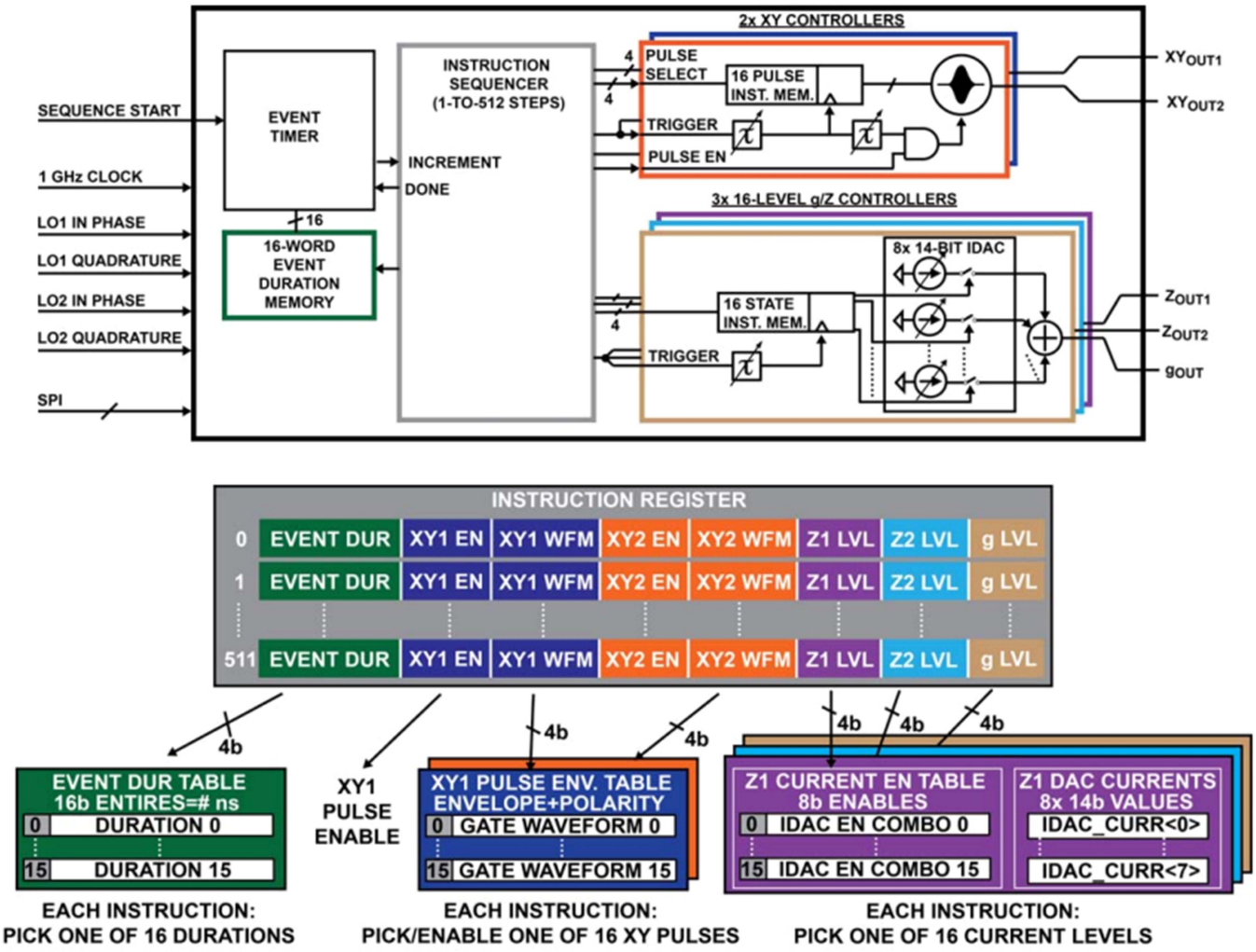

FIGURE 19. Architecture of the integrated cryo-CMOS controller for full qubit unit-cell control. The system combines RF (*XY* Controllers) and baseband (*g*/*Z* controllers) signal generation. An Instruction Sequencer executes a 512-step sequence. Each instruction specifies an event duration and selects pre-programmed waveforms and current levels from 16-element lookup tables, as detailed in the Instruction Register breakdown. Figure reproduced from [250].

1) WIRELESS MICROWAVE AND TERAHERTZ LINKS

In wireless microwave and terahertz links, directional transmit (TX) and receive (RX) antennas are coupled to a quantum circuit housed inside a dilution refrigerator [262]. A cryogenic interface module facilitates microwave signal generation for qubit control and enables qubit state interrogation.

As a heuristic for link performance, the theoretical data transmission limit is commonly estimated using the Shannon channel capacity formula [263]

$$C_c = B \log_2 \left(1 + \frac{P_r}{N}\right) \tag{28}$$

where C_c is the channel capacity (bits $\cdot$ s^{-1}), B is the bandwidth, P_r is the received power, and N is the noise power. The power dissipation budget at cryogenic temperatures constrains circuit design, often limiting components to milliwatt-level consumption to avoid heating the quantum device [264]. This constraint favors modulation schemes such as onoff keying (OOK), frequency-shift keying (FSK), phase-shift keying (PSK), and pulse-amplitude modulation (PAM), which can be implemented with power-efficient nonlinear circuits [265]. Conversely, spectrally efficient schemes like quadrature amplitude modulation (QAM) and orthogonal frequency-division multiplexing (OFDM) are generally reserved for the higher temperature classical layers, as their strict requirements for high-linearity amplifiers and complex digital signal processing result in prohibitive power consumption for the cryogenic stage. To minimize the probability of bit errors, these methods can be used alongside forward error correction schemes, provided that the hardware stack can accommodate the complexity of the modulation. Methodologies spanning directional RF front ends, channel modeling, modulation schemes, and robust error correction are currently the subject of research and development efforts [200], [266], [267], [268].

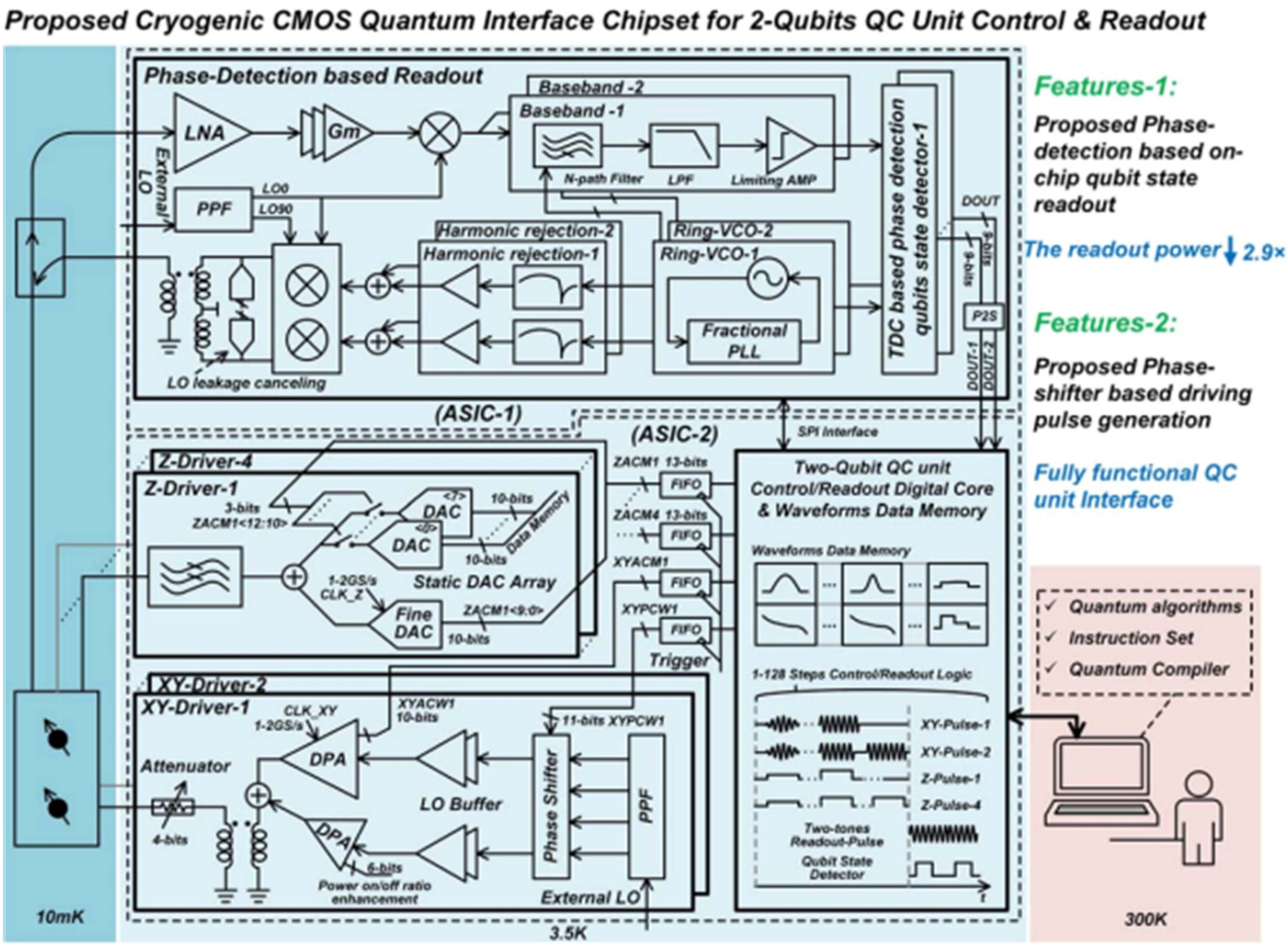

FIGURE 20. System architecture of the complete quantum interface. A room temperature (300 K) computer provides the quantum algorithm to the "Digital Core" on ASIC-2 (at 3.5 K). This core controls the *Z*-Drivers and *XY*-Drivers to send pulses to the qubits (at 10 mK). The return signal from the qubits is received by ASIC-1, processed by the "Phase-Detection based Readout" chain, and the resulting state is sent to the digital core on ASIC-2 for feedback. Figure reproduced from [197].

At cryogenic temperatures, antenna characteristics are expected to deviate due to thermal contraction of structural materials and changes in dielectric properties; however, to date, experimental characterization of these effects remains largely unexplored. The anticipated shifts include variations in the effective electrical length, input impedance, and radiation pattern of the antenna. A temperature-dependent impedance mismatch inevitably arises from these changes, resulting in significant signal reflection loss. This phenomenon not only reduces the absolute power delivered to the quantum device but also has the potential to distort the control pulses, degrading the fidelity of qubit operations.

Electromagnetic fields inside a dilution refrigerator may also induce surface currents on conducting surfaces, leading to parasitic dissipation or unintended coupling. As a boundary condition (in the quasi-static limit), the surface current density can be expressed as

$$\mathbf{J_s} = \mathbf{n} \times \mathbf{H} \tag{29}$$

where $\mathbf{n}$ is the unit normal to the conducting surface and $\mathbf{H}$ is the tangential magnetic field intensity. This relation is a simplified representation; a full assessment requires numerical electromagnetic simulation that includes skin-depth effects, material conductivity at low temperature, and geometry-dependent resonances.

In summary, wireless and terahertz links present a potentially attractive route to reduce wiring density and thermal load, but their practical suitability for qubit control and readout is an open question that calls for targeted experimental studies, refined cryogenic device models, and system-level tradeoff analyses.

2) OPTICAL INTERCONNECTS AND INTERFACES

Optical interconnects may offer a power-efficient and low-latency platform for control and readout in quantum computing architectures [269]. Electrooptical modulators, characterized by their half-wave voltage V_π, can, in principle, encode control information onto optical carriers through

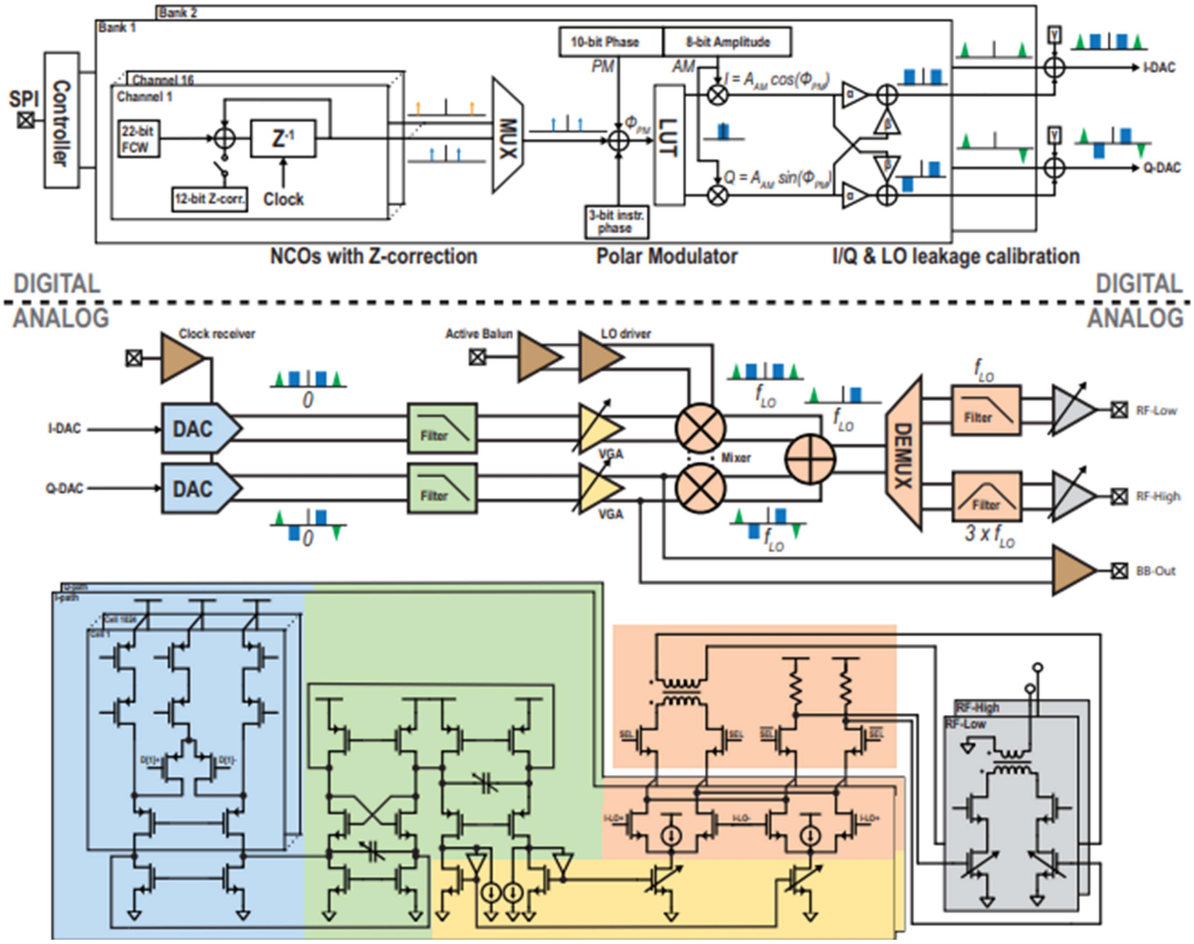

FIGURE 21. Functional diagram of the Cryo-CMOS controller IC. The system is split into a digital section and an analog/RF front-end. The digital section uses an instruction set to drive 32 NCOs into a polar modulator. The analog section consists of current-steering DACs, a gm-C reconstruction filter, a VGA for gain control, and a Gilbert-cell active mixer for upconversion. The output path is split into two bands (RF-Low and RF-High) to cover the full 2–20 GHz range. Figure reproduced from [251].

temperature- and voltage-dependent variations of the refractive index in a nonlinear crystal. The extent to which these modulation techniques can be made compatible with cryogenic environments remains an open area of active research, with ongoing efforts to optimize insertion loss, modulation efficiency, and thermal stability. The propagation of optical signals through single-mode fibers is typically modeled by an attenuation coefficient $\alpha(\lambda, T)$, which depends on the optical wavelength λ and the operating temperature T. The transmitted optical power $P(d)$ over a distance d can be approximated as

$$P(d) = P_0 e^{-\alpha(\lambda,T)d} \tag{30}$$

where P_0 is the launched optical power. In practice, minimizing $\alpha(\lambda, T)$ at cryogenic temperatures is desirable to reduce insertion losses and associated thermal dissipation, although direct measurements of fiber attenuation in deep-cryogenic regimes remain relatively limited in the literature. Laser sources for these systems are often required to exhibit high coherence, quantified by a narrow linewidth to maintain phase stability and enable precise qubit control. The practical feasibility of achieving such coherence while maintaining low heat load at subkelvin temperatures is a subject of continuing experimental investigation. Consequently, while optical interconnects present a compelling pathway for scalable quantum systems, their full integration into cryogenic control and readout stacks will depend on future demonstrations that confirm thermal, optical, and electronic compatibility under operational conditions.

3) THERMOMETRY-BASED QUBIT READOUT

Thermometry techniques in quantum systems have traditionally been focused on measuring the temperature of devices operating at low temperatures [270], [271], [272]. Pahl and Oliver [257] first suggested the potential of employing thermal detectors for the measurement of qubits in their publication in *Nature Electronics*. Expanding upon this initial proposition, the literature survey reveals that single-shot readout of superconducting qubits using a thermal detector is a recent and underexplored area of research. The temperature change ΔT induces a change in electrical resistance R of the

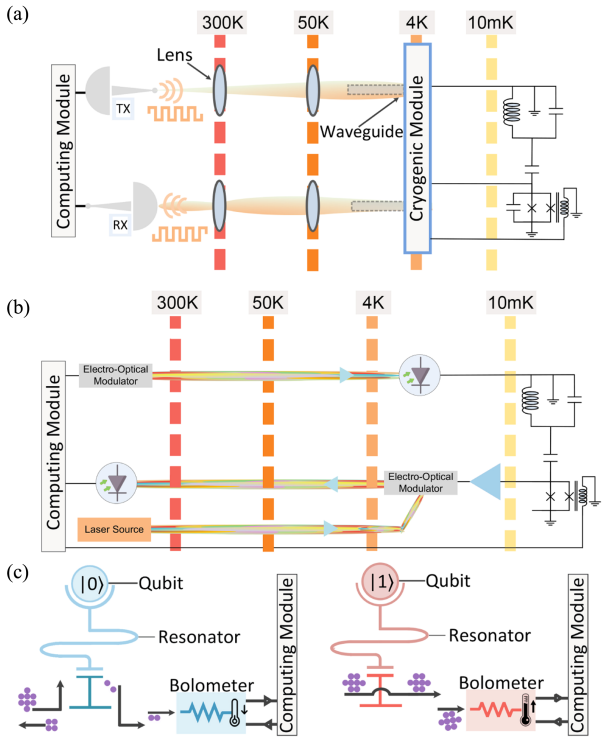

FIGURE 22. Diverse and emerging quantum control/readout methodologies. (a) Wireless transceiver based links via *TX* and *RX* lines coupled to a cryogenic quantum device. (b) Optical interconnect to cryogenic device via laser and electrooptical modulators. (c) Thermometry-based. The layout of this figure is inspired by the presentation in [257].

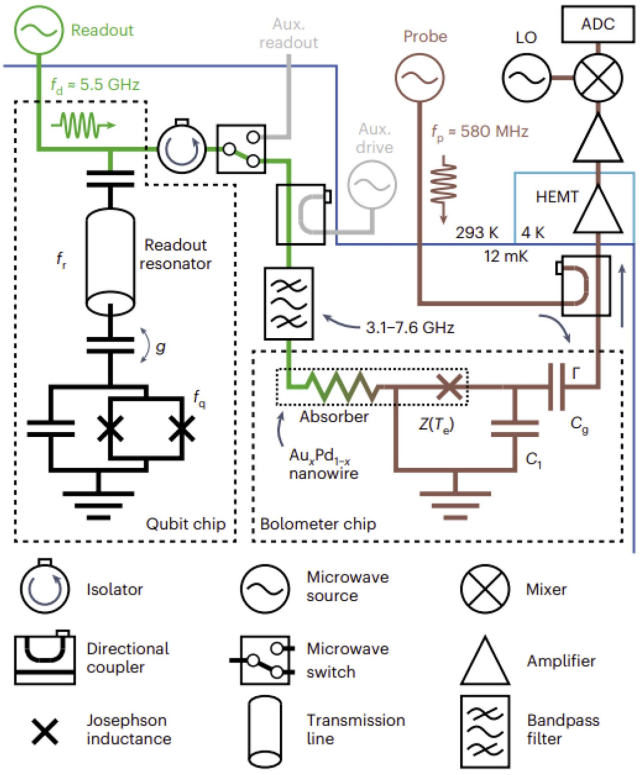

FIGURE 23. Experimental setup for qubit readout using a bolometer. The figure is reproduced from the work of Gunyhó et al. [202].

bolometric material, described as follows:

$$\Delta R = \left(\frac{dR}{dT}\right) \Delta T. \tag{31}$$

This resistance change can be converted into an electrical voltage signal ΔV. Thus, the bolometric detector transduces absorbed photon energy into a measurable electrical signal, enabling qubit state discrimination based on thermal signatures. However, the strength and fidelity of this correlation depend sensitively on material properties, device geometry, and thermal relaxation dynamics, which remain active subjects of investigation. Fig. 23 shows an example experimental setup for qubit readout using a bolometer-based detection chain. Following a thorough analysis of the literature, this rigorous effort revealed a notable scarcity, with only one publication [202] demonstrating this specific capability to the best of our current knowledge. This result is presented with an understanding of the inherent limitations of any literature survey, including the possibility of oversights or variations in search methodologies.

C. STATE-OF-THE-ART SYNERGISTIC APPROACHES: A CRITICAL EVALUATION

Recent literature documents both experimental demonstrations and conceptual proposals that target the principal bottlenecks of qubit control and readout. Some approaches (bolometric readout [202]) have laboratory demonstrations, while others (e.g., hybrid wireless Qcore concepts [200]) remain largely architectural proposals requiring experimental validation. For instance, Wang et al. [199] presented a terahertz Cryo-CMOS link operating at 260 GHz designed for cryogenic quantum processors. The CMOS compatibility enables the architecture to overcome classical data transmission heat loads. Key performance parameters include data rate of 2 Gb/s, BER of less than 10^{-6} for binary phase-shift keying (BPSK) modulation, and SNR of 52.5 dB at a 100-kHz resolution bandwidth. The passive backscatter technique contributes to minimizing power dissipation at the cryogenic stage. However, future work must address challenges associated with extending passive backscatter schemes to high-density quantum processors. Similarly, Alarcón et al. [200] envision distributed quantum cores (Qcores) interconnected by quantum-coherent microwave cavities and classical wireless links within a cryogenic package. The architecture aims to balance and reconfigure tradeoffs between computation and communication, emphasizing architectural flexibility, quantum coherence preservation, and wireless management of quantum states. While promising, this proposal is conceptual and requires experimental validation.

Gunyhó et al. [202] introduced a superconducting qubit readout method employing a thermal nanobolometer at millikelvin temperatures. The bolometer, constructed from a

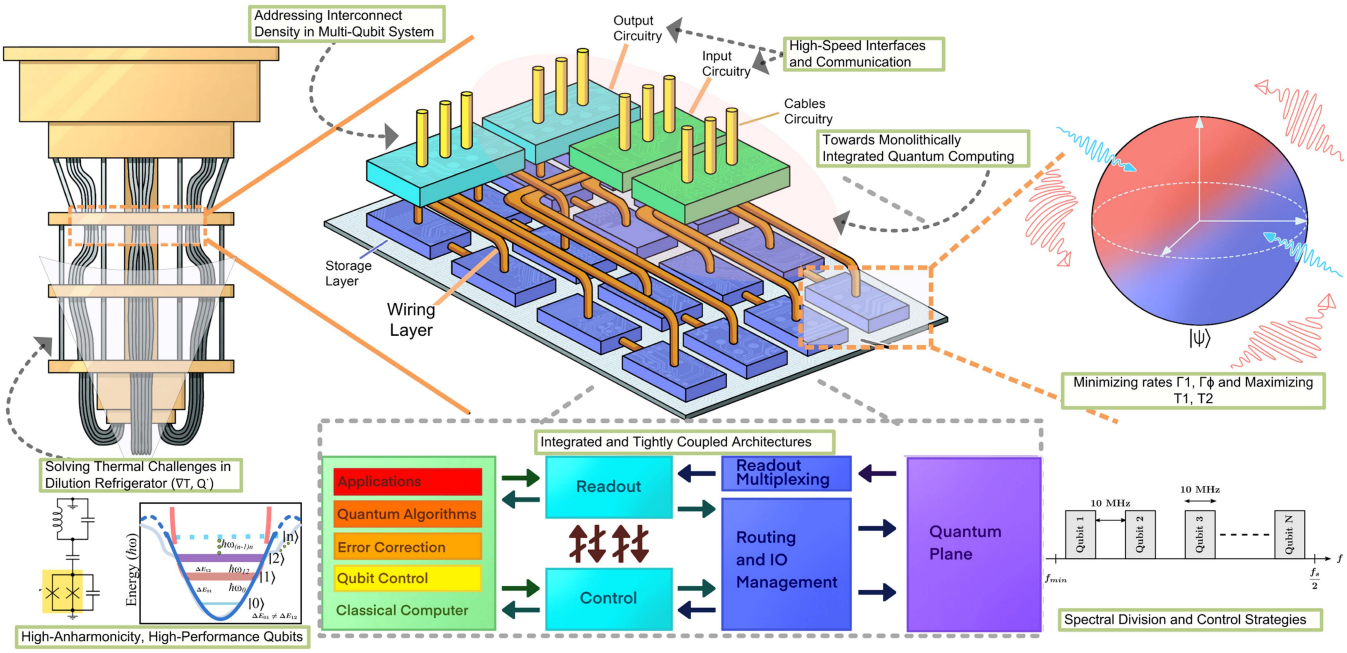

FIGURE 24. **(a) Potential architecture for tightly integrated next-generation quantum Systems. This diagram represents a potential future layout, showcasing tightly integrated components such as classical layer, control and readout layer, and quantum plane. The design highlights key elements like monolithic integration, minimized wiring complexity, and thermal management. In addition, many other innovative approaches are envisioned to complement this architecture. The layout of this diagram is inspired by the design presented in [275].**

resistive AuPd nanowire, demonstrated single-shot readout; however, the fidelity was 0.618, limited mainly by qubit energy relaxation. This approach offers key advantages, including reduced quantum noise compared to parametric amplifiers and the elimination of bulky microwave isolation components, though these benefits depend on detector performance and integration tradeoffs. Nevertheless, its technical limitations include a relatively long readout duration of 13.9 μs and moderate fidelity, necessitating continued material and device development. This initial demonstration used a slower bolometer, which limited the readout duration. While promising, these results indicate that device-level improvements (bolometer absorber materials, thermal time constants) and tighter integration with qubit lifetimes are necessary to approach competitive readout latency and fidelity.

Lecocq et al. [201] demonstrated a photonic link for interfacing superconducting qubits with room temperature electronics. This approach employs cryogenic photodetectors and optical fibers to enable coherent microwave qubit control and readout below 20-mK environment. The unique features include its capacity to achieve shot-noise-limited performance, reduced passive heat load, and multiplexing capabilities. Scalability is limited by active optical power dissipation at cryogenic temperatures and the inverse relationship between the number of supported qubits and the qubit driving duty cycle. Furthermore, this approach introduces system complexity due to the integration of optical components with cryogenic systems, and further optimization of hardware and protocols is necessary for practical application.

Beyond passive optical fiber links, active electrooptic modulators offer an alternative pathway to integrate optical control within cryogenic quantum systems. Youssefi et al. [273] demonstrated cryogenic electrooptical readout of a superconducting electromechanical circuit using a commercial titanium-doped lithium niobate (Ti:$LiNbO_3$) modulator at temperatures near 800 mK. Future research direction may explore the fabrication of integrated cryogenic electrooptic modulators that achieve both low insertion loss and high modulation efficiency. Identifying alternative materials or device geometries that outperform Ti:$LiNbO_3$ at low temperatures remains an important open challenge. Moreover, while the use of commercial modulators demonstrates feasibility, custom-designed devices explicitly optimized for cryogenic conditions will likely be necessary to minimize thermal load and enhance optical efficiency.

Warner et al. [274] achieved coherent optical control of superconducting qubits via a cavity electrooptic transducer exhibiting a conversion efficiency of $\eta \approx 1.18\%$, with a single-photon coupling rate of $g_{eo}/2\pi \approx 945$ Hz and cooperativity $Co \approx 1.16$, while maintaining $\bar{n}_{add} < 0.12$ added microwave photons. Complementarily, Arnold et al. [53] showcase an all-optical readout approach with state-assignment fidelity $F_{oo} = 0.82 \pm 0.01$, implemented without cryogenic microwave components, reinforcing the role of telecom-compatible optics in qubit interfacing. Improving electrooptic transduction efficiency toward near-unity requires advances in cavity design, material quality, and optical-microwave mode overlap to minimize losses and enhance coherent energy transfer.

TABLE 14. Selected Emerging Modalities for Quantum Control and Readout: Key Features and Challenges

Bolometer qubit readout [202]	
Key features	Nanobolometer for single-shot qubit state measurement
Advancements	Single-shot fidelity: 0.618, improved to 0.927 after error correction from finite qubit lifetime
Challenges addressed	Replaces parametric amplifiers, reduces thermal load
Scalability	High-fidelity readouts for large qubit arrays (conceptual layout)
Unique features	Thermal readout, no parametric amplification
Hybrid quantum-coherent wireless networks [200]	
Key features	Wireless communication between quantum processors
Advancements	Conceptualization of Qcore quantum networking architecture
Challenges addressed	Reduces wiring complexity and supports intercore communication
Scalability	Supports 10^6 qubits across Qcores (under conceptualization)
Unique features	Hybrid quantum-coherent links
THz Cryo-CMOS transceivers [199]	
Key features	CMOS-based THz transceivers (260 GHz) with passive backscatter communication
Advancements	Data rates up to 4 Gbps with low power
Challenges addressed	Avoids active THz generation; reduces thermal load
Scalability	Suitable for large qubit systems (conceptual layout)
Unique features	Passive backscatter communication
Photonic link for qubit control [201]	
Key features	Optical fibers and EOM for qubit control
Advancements	High-fidelity control at T $\approx$ 4 K
Challenges addressed	Solves thermal load using optical links
Scalability	Scalable to millions of qubits with low heat dissipation (conceptual layout)
Unique features	High-fidelity optical control with minimal thermal impact ((Heat load significantly lower than conventional wiring))
Electro-optic interconnect for microwave control [273]	
Key features	Microwave control using EOM
Advancements	Coherent control via optical signals
Challenges addressed	Reduces thermal load; supports fast qubit control
Scalability	Scalable to large systems (conceptual layout)
Unique features	Coherent microwave-optical interaction
Microwave-optical transducers [274]	
Key features	Electrooptic transduction via thin-film lithium niobate (TFLN)
Advancements	Conversion efficiency of 1.18%, enables optical-microwave interfacing
Challenges addressed	Interfaces microwave and optical domains to reduce thermal impact
Scalability	Enables scalable quantum networking (conceptual layout)
Unique features	Bidirectional transduction
Cryogenic photonic readout [53]	
Key features	Photonic readout at cryogenic temperatures
Advancements	Achieves high-fidelity readout
Challenges addressed	Minimizes heat load and quantum decoherence
Scalability	Scalable for large quantum systems (conceptual layout)
Unique features	Optical readout with minimal heat impact

D. ANALYSIS OF EMERGING SOLUTIONS

Table 14 synthesizes a selection of contemporary quantum computing technologies focused on overcoming current bottlenecks in qubit control and readout. Emphasizing cryogenic operation, the presented pathways explore novel methodologies for achieving high-fidelity measurements and efficient manipulation of quantum states. From the literature, photonic links and readout interfaces reduce heat constraints through fiber-based interconnects, which outperform conventional coaxial lines in both scalability and dissipation. Electrooptic interconnects and microwave-optical transducers may further enable coherent bidirectional conversion between microwave and optical domains, critical for modular quantum architectures and networking. Terahertz Cryo-CMOS transceivers and hybrid wireless networks present alternatives by eliminating wired interconnects altogether, introducing backscatter-based and quantum-coherent wireless schemes. Furthermore, bolometer-based readout, though still in its initial stage, is challenged by lower fidelity without correction.

The conceptual layouts mentioned for scalability represent initial steps, and future research will need to address emergent challenges related to crosstalk, control line density, and maintaining fidelity across scaled quantum circuits. These initial technological pathways, while promising, are foundational and necessitate continued innovation to realize fault-tolerant and large-scale quantum computation.

TABLE 15. Challenges and Opportunities in Quantum Systems

Challenges	Opportunities
	
Resource optimization	Read-time quantum control
Cryo-compatibility	Direct synthesis and filtering
Power efficiency	
Interconnect complexity	High-throughput processing
Thermal dissipation in cryogenic systems	Integrated heat dissipation and noise filtering
Noise propagation in signal pathways	Noise-resilient signal amplifiers
Thermal isolation	Thermal management algorithms
Power budgeting	Localized thermal stabilization
Integration of cryo-classical components	Adaptive quantum control
Maintaining signal integrity	Scalable cryogenic signal processing architectures
Power dissipation in cryogenic systems	Control through on-chip processing
Robustness to environmental fluctuations	Cryo-resilient pulse shaping and modulation
SerDes at cryogenic temperatures	Quantum-optimized data compression and encoding
Synchronization in quantum–classical systems	High-fidelity data conversion
Thermal isolation and noise in data links	Dynamic bandwidth allocation for division
Power-quality issues in cryogenic interconnects	Error correction
Decoherence and qubit–bath interactions	Superconducting materials for low-loss circuits
Qubit coupling and connectivity	Improved hybrid quantum–classical systems
Materials science for low-loss circuits	Quantum coherence enhancement techniques

VIII. POTENTIAL FUTURE OUTLOOK AND TRENDS

As deduced from the current body of literature, the evolution of scalable control and readout systems points toward a convergence of highly integrated control architectures, cryo-compatible systems, and mixed-signal interfaces designed for operation at the edge of quantum noise limits. For sample rates, the challenge now extends beyond single-channel bandwidth to ensuring multichannel synchronization and the capacity to render the complex and overlapping pulse sequences required for multiqubit algorithms [30], [276]. In parallel, the requirement for high SFDR has scaled from single-tone purity to maintaining a low noise floor across the entire operational spectrum, mitigating the cumulative spectral contamination from dozens or hundreds of parallel control lines operating simultaneously [277], [278]. Emerging directions include monolithic integration, cryogenic signal processing, high-throughput communication and interfacing, and system-on-chip approaches, all incorporating noise management and power-aware design, with aspirational power consumption targets often set below 1 mW per channel. Identified herein are a number of prominent research domains expected to shape the field in the coming decade. Fig. 24 provides a forward-looking view of tightly integrated quantum systems, emphasizing co-design across qubits, control and readout, interconnects, and thermal management to enable scalability.

A. INTEGRATED AND TIGHTLY COUPLED ARCHITECTURES

Highly integrated and tightly coupled control and readout architectures aim to optimize quantum computation through several key approaches. Monolithic Integration seeks to minimize latency and wiring length, while maximizing SNR, by fabricating control and readout circuitry directly in close proximity to the qubits. This creates a complex co-design challenge, requiring researchers and designers to balance these competing objectives against the fundamental constraints of fabrication technology.

On-chip signal processing at cryogenic stages offers an additional pathway for enhancing quantum control fidelity. It involves performing on-chip transformations to control signals and measurement outcomes, such as pulse shaping for qubit manipulation, low-latency real-time feedback based on measurement results, and error correction decoding. Executing these processing operations in close proximity to the qubit array minimizes signal propagation delays and dissipative power delivery losses. Promising implementation approaches include specialized signal processing units and cryo-optimized CMOS processes. This enables the deployment of low-latency feedback loops.

B. DIGITAL AND FPGA INNOVATIONS

Currently, most qubit controllers employ RFSoC-based system-on-chip (SoC) architectures for managing control, readout, and signal processing tasks at room temperature, given their integrated RF and digital processing capabilities. The optimization of the FPGA design for direct RF synthesis is a multiobjective problem, offering a tradeoff between the signal integrity of the analog output and the end-to-end latency of the digital pipeline required to generate it. For example, adding more pipeline stages may ease timing closure on the critical path and allow for higher clock frequencies, but at the cost of increased latency and higher lookup table (LUT)/flip-flop utilization. Similarly, implementing complex digital filters utilizes DSP slices, which increases dynamic power dissipation and can lead to routing congestion during the place-and-route stage.

Advances in cryo-compatible FPGA architectures, lightweight IP cores, direct synthesis capabilities, and hybrid

TABLE 16. Mapping DiVincenzo Criteria to Control and Readout Design for Microwave-Driven Superconducting Quantum Systems

DiVincenzo Criterion	Relevant control and readout design aspects
Scalability	• **Density and integration:** High-channel count, compact classical electronics, heterogeneous integration [280] • **Power dissipation:** Low power architectures, efficient thermal management (especially for cryo-electronics) [281] • **Interconnects:** Miniaturized, low-loss, high-density wiring and routing solutions [282] • **Modularity:** Expandable control / readout system architectures [192]
Initialization	• **Pulse generation fidelity:** High-fidelity, low-noise, spectrally pure AWG with relevant settling times [283] • **Temporal precision:** Synchronization and phase coherence across multiple control channels [191] • **Reproducibility:** Stable performance across environmental variations [201] • **Calibration:** Hardware support for rapid and accurate state preparation and calibration [226]
Coherence and resilience	• **Noise mitigation:** Low-noise design, effective electromagnetic shielding and isolation [284] • **Thermal management:** Precision temperature control and isolation from the qubit environment [285] • **Crosstalk suppression:** Multi-channel phase / amplitude control, active cancellation techniques [286] • **Quasi-static field control:** Stable and precise DC / low-frequency field generation for qubit tuning [287]
Universality (gate set)	• **Waveform flexibility:** Reconfigurable and arbitrary waveform generation for complex pulse sequences [212] • **Fidelity and precision:** Relevant amplitude, phase, and frequency resolution in generated signals [177] • **Speed and latency:** Fast gate execution relative to T_1 and T_2, low latency feedback loops [288] • **Resource management:** Efficient allocation and synthesis of microwave / RF and DC control signals [289]
Measurement capability	• **Sensitivity and SNR:** Low noise, high-gain amplification chains at the qubit operating frequency [290] • **Readout speed:** High-bandwidth acquisition and rapid state discrimination [202] • **Data processing:** Digital signal processing for state extraction, error detection, and feedback [212] • **Back-action minimization:** Design for minimal measurement-induced perturbation of qubit states [291]

analog-digital designs are anticipated to significantly extend quantum processor scalability. Several FPGA and SoC advancements are underway, with notable releases like Xilinx's Versal SoC in 2026 [279], offering enhanced processing power and signal processing for quantum applications. Furthermore, Microchip's radiation-hardened FPGAs are being developed for future deployment in extreme environments, offering the reliability needed for quantum technologies in harsh conditions.

C. HIGH-SPEED INTERFACES AND COMMUNICATION

High-speed low-latency interfaces provide the communication channel between the classical control hardware and the quantum processor. These interfaces are responsible for delivering precisely timed control signals to the qubits and retrieving readout signals from the cryogenic environment. As quantum systems scale, future developments will likely focus on addressing key challenges related to cryo-compatible serialization/deserialization (SerDes), clock-data recovery, noise coupling in data lines, and thermal isolation to ensure efficient data transfer. Furthermore, the integration of high-precision data converters for facilitating bidirectional signal conversion between quantum and classical domains is a novel area of exploration.

D. POWER EFFICIENCY AND NOISE MANAGEMENT IN ELECTRONIC DESIGN

Minimizing power dissipation is fundamental to the viability of large-scale cryogenic quantum systems. Future electronic designs are expected to incorporate power-aware circuit techniques, low-noise amplification strategies, electromagnetic shielding, and thermal optimization frameworks. Dilution refrigerators maintain ultralow temperatures, offering limited cooling capacity at their base stage (typically a few microwatt). Due to the complex mechanical and thermodynamic management required for their operation (a detailed discussion of which is beyond the scope of this analysis), these refrigeration systems are needed be carefully integrated into the overall design to balance cooling efficiency with quantum system performance, respecting the thermal budget constraints. The challenges and opportunities discussed in this entire section are summarized in Table 15.

E. SOLVING OPEN QUESTIONS IN PHYSICS: ENABLING NEW PARADIGMS

The development of new quantum architectures is linked to solving fundamental open questions in physics. Breakthroughs in quantum mechanics, condensed matter physics, and thermodynamics will likely address the limitations of

current quantum systems. The following are key areas of focus for enabling these advancements.

1) *Decoherence mitigation:* Suppressing environmental coupling requires refining open quantum system models to understand and engineer qubit-bath interactions, minimizing rates Γ_1, Γ_ϕ and maximizing T_1, T_2.
2) *Materials science for low-loss circuits:* Developing new materials and interface engineering to minimize dielectric loss, reduce two-level system participation, and suppress $1/f$ noise is factor for increasing quality factor.
3) *High-fidelity quantum measurement:* Optimizing dispersive readout schemes requires understanding and controlling the photon-qubit interaction in resonators to extract state information with high SNR and minimal back action.
4) *Thermodynamics of complex cryogenic systems:* Managing heat dissipation across dense electrical interconnects and components at millikelvin temperatures is essential to maintain the low-entropy environment required for quantum coherence.
5) *Scalable electrical integration:* Engineering multilayer superconducting circuits and packaging solutions that ensure low-loss signal propagation and minimize parasitic crosstalk are crucial manufacturing and physics challenges for large qubit arrays.

The preceding technological survey now converges on a central synthesis: grounding these engineering advances in the foundational principles of quantum information. This connection is made explicit in Table 16, which methodically aligns the novel approaches to qubit control and readout with the DiVincenzo criteria for a functional quantum computer.

This framework reveals a powerful narrative: the abstract requirements for universal quantum computation are being systematically addressed by tangible progress in the physical layer. It demonstrates that the path toward fault-tolerant systems is paved not only by theoretical breakthroughs but also by relentless innovation in the classical hardware forming the interface to the quantum world.

IX. CONCLUSION

In summary, this survey provides a comprehensive consolidation and contextualization of methodologies for superconducting qubit control and readout. By detailing the co-design required across analog–digital paths, cryogenic electronics, and precise waveform control, it highlights how engineering choices impact qubit performance. The work identifies key challenges like interconnect bottlenecks and thermal constraints and explores several architectural strategies and emerging technologies, linking engineering solutions to the requirements for advancing quantum systems

The central sections offer a cohesive framework encompassing pulse generation, signal synthesis, readout analysis, and related performance metrics. This framework categorizes systems based on their architectural control schemes and enabling hardware technologies. The survey then evaluates the tradeoffs inherent in these categories, assessing their impact on system complexity, integration depth, and scalability. By evaluating these approaches, the work highlights the engineering challenges—such as interconnect bottlenecks, calibration overhead, and cryogenic thermal management—that must be overcome to achieve scalability. It highlights crucial emerging trends, offering a consolidated foundation essential for advancing scalable quantum hardware.

Building on this foundation, the survey concludes with future outlook and trends. This final section explores key directions anticipated to shape the next generation of scalable quantum systems. It details prospective innovations, including monolithic integration, cryogenic signal processing, power-aware circuit design, and interface engineering. Furthermore, it considers open questions in physics crucial for introducing new architectural paradigms. Collectively, these insights serve as both a vision for the future and a strategic map for researchers and engineers navigating the evolving landscape of quantum control infrastructure.

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