

The Electronics of the EUSO-Balloon UV camera

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Abstract: The JEM-EUSO collaboration is currently developing the EUSO-BALLOON instrument, a pathfinder of the JEM-EUSO mission. Such an effort is led by the CNES, the French space agency, and involves several French institutes as well as several key institutes of the JEM-EUSO collaboration. The EUSO-Balloon instrument consists of an UV telescope and of an Infrared Camera. The UV telescope will operate at an altitude of 40 km, collecting background and possibly signal photons in the (290-430 nm) fluorescence UV range, the one in which the UV tracks generated by high energetic cosmic rays propagating in the earth's atmosphere are observed. The balloon experiment will be equipped with electronics and acquisition systems, as close as possible to the ones designed for the UV telescope of the main JEM-EUSO instrument. The past year has been devoted to the design, the fabrication and the tests of the prototypes of the optics, of the Photo Detector Module (PDM), of the digital processor and of the IR Camera of the EUSO-Balloon. In this contribution we focus on the PDM, the core element of the JEM-EUSO focal surface. We first describe all key items of the PDM, from the photo-detectors to the FPGA board of the first stage of the digital processing. We then report on the tests carried out on the prototypes to assess their functionality and their suitability for a balloon mission.

Keywords: JEM-EUSO, balloon, electronic, photo-detection

1 Introduction

The EUSO-Balloon experiment [1, 2] is a pathfinder of the ISS mission JEM-EUSO [3] whose goal is to observe the Extensive Air Showers (EAS) produced in the atmosphere by the passage of the high energetic extraterrestrial particles with energy higher than 10^{19} eV. The particles of the showers generate a UV light track, observable in the 290-430 nm wavelength range, because of the fluorescence emission of Nitrogen molecules excited by collisions with secondary particles of the cascade. The detection of these UV photons is the base of the JEM-EUSO observational technique. In the EUSO-Balloon, a set of Fresnel lenses is used to focus the UV photons on the 2304 pixels of the Photo detector Module (PDM), the core element of the JEM-EUSO detection system and the focal surface of the Balloon instrument, as shown on figure 1.

The main instrument of the EUSO-Balloon can be con-

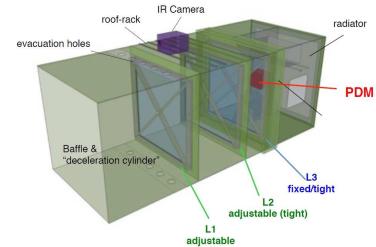


Fig. 1: 3D view of the EUSO-Balloon instrument. The 36 MAPMTs (bottom left part) and the ASIC boards (top right part) are visible.

sidered as an UV camera taking pictures every $2.5 \mu\text{s}$ (the size of a gate time unit, GTU). It will serve as a technological demonstrator of the JEM-EUSO mission, since they share similar parts and concept elements, not only for the PDM

electronics but also for the mechanics and the data processing system (acquisition and monitoring).

The EUSO-Balloon experiment will be also essential to test the technologies selected and developed in a severe environment. In fact the EUSO-Balloon will work at 40 km of altitude where the pressure is at 3 mbar, worse than in space conditions.

The science goals of the experiment are the study of the UV background below 40 km (the main contribution is known as nightglow) and the test of the trigger algorithms selectivity and rate.

2 The PDM electronic

2.1 Overview

The PDM (see figure 2) is composed by nine elementary cells (ECs) which are made of four Multi-Anode Photo-Mulitpliers (MAPMT [4], R11265-M64 from Hamamatsu) and their associated electronics. The EC unit electronics (see section 2.2) is very compact due to restrictive dimensions of the global mechanic. A set of small boards were designed to be placed in the shadow of the photomultipliers (MAPMT) used to detect the photons. Three different boards are used to supply 14 different high voltages and to collect the analog signals from the 64 channels of each MAPMT.

These signals are sent to a fourth board (see section 2.3) containing the SPACIROC ASICs, which perform single photon counting and the estimate of the charge of the signal. The digitized data are sent to the PDM board (described in section 2.4) which controls up to six ASIC boards with an FPGA. The PDM contains the high voltage power supplies (see 2.5) which provide the high voltages and is equipped with a system of switches to protect the MAPMTs from intense light flux.

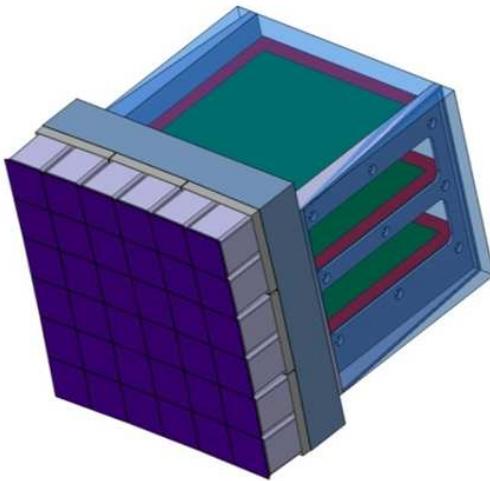


Fig. 2: PDM 3D view.

2.2 Elementary Cell unit

Each EC unit is composed by four MAPMTs and a stack of three types of boards (see figure 3):

- One EC-DYNODE board, which distributes the high voltage to the four MAPMTs
- Four EC-ANODE boards, which collect the analog signals and transmit them to the next stage of the electronic

chain

- One EC-HV, which interfaces the HVPS with the EC-dynode, transmitting the high voltage

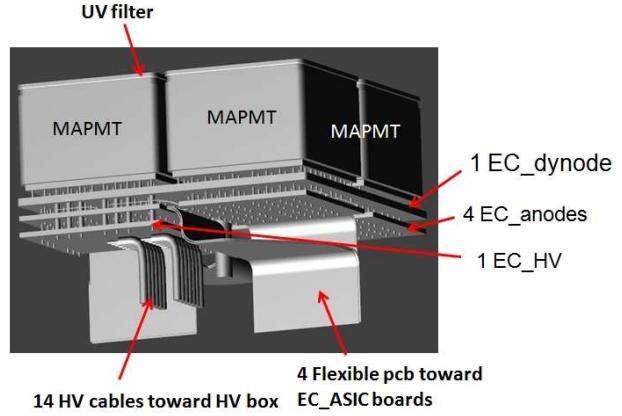


Fig. 3: 3D view of an EC unit.

Special care must be taken in the assembly of each EC unit to secure a firm montage in the mechanical structure. Because of the severe conditions of pressure, they have to be potted to protect them against destructive sparking induced possibly by high voltage. The figure 4 shows a potted EC unit. Only the cables, a fixation screw and the UV filters are coming out of the potting.



Fig. 4: Picture of a potted EC unit.

2.3 ASIC boards

To collect the analog signals coming out from the 36 MAPMTs (or EC-ANODE boards), six ASIC boards are fixed perpendicularly to the mechanical frame which welcomes the nine EC units. Figure 5 illustrates this connection.

These six ASIC boards (also called EC-ASICs) welcome six ASICs, as well as six connectors toward the EC units and one connector toward the PDM board (section 2.4). Figure 6 shows the top and bottom views of the first EC-ASIC produced and assembled. There are three packaged SPACIROC ASICs [5] on each side. The ASIC performs photon counting for each pixel of the 36 MAPMTs, as well as an estimate of the charge of the gathering of eight pixels. Before integrating the ASIC on the board, its performances were checked successfully alone and coupled to a MAPMT.

The configuration (in a daisy chain mode) of the ASICs and the powers are sent through a connector by the PDM board, which also collects the digital data produced by the 36 ASICs.

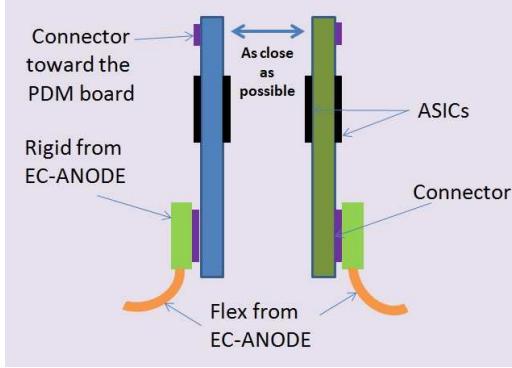


Fig.5: Connection between EC-ANODE and EC-ASIC boards.

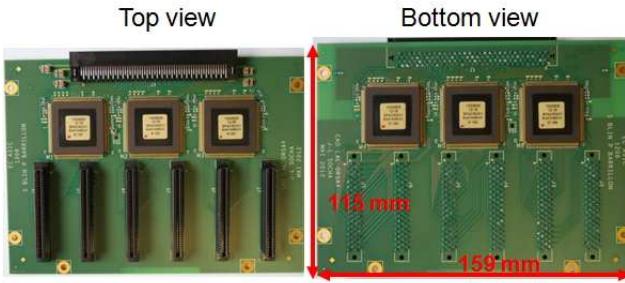


Fig.6: Top and bottom views of the prototype of the EC-ASIC board.

2.4 FPGA board

As shown in figure 7, which presents the PDM electrical architecture, the PDM board is a central element which is connected to several components not only of the PDM but also of the Digital Processor system. It communicates with the LVPS-PDM (providing the power), and with the Cluster Control Board (the next stage of the data processing and trigger) [6], the housekeeping board which distributes the necessary commands and collects relevant operational parameters, and one of the HVPS (high voltage power supply, see section 2.5).

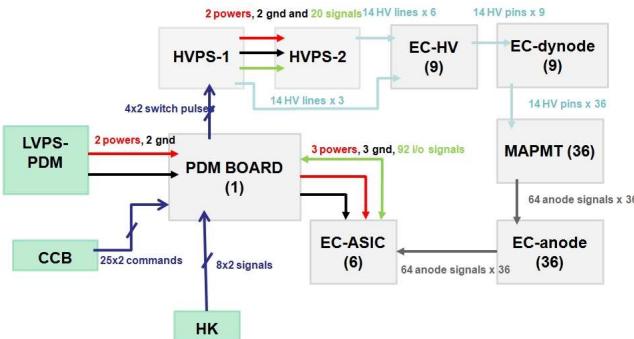


Fig.7: Electrical architecture of the PDM. CCB: Cluster Control Board. HK: Housekeeping. LVPS-PDM: Low voltage power supply.

All the features needed for the interfaces but also for the data processing, such as the first level trigger algorithms, are integrated in the firmware of an FPGA (from Xilinx Virtex 6 family), the key element of the PDM board. The

figure 8 represents different views of this board, as well as its integration in the mechanical structure. In addition to the FPGA, this board is equipped with DC-DC converters and regulators to provide the different voltage sources required, the connectors toward the other boards and passive components.

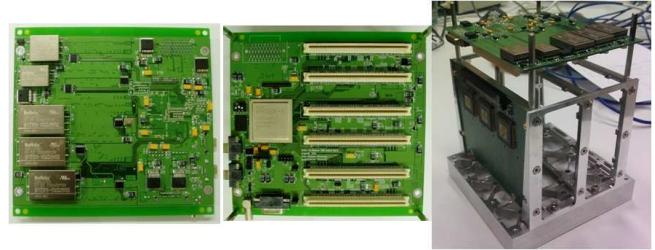


Fig.8: Top and bottom views of PDM board (left). PDM and EC-ASIC board fixed on the mechanical structure(right).

2.5 High voltage power supply

There are two HVPS (see figure 9), whose roles are to provide the 14 high voltage levels needed by each MAPMT. These voltages are generated by a Cockcroft-Walton (CW) system from a 28V power source. This system was preferred to the classical voltage divider because of its very low power consumption (50 times less). The first and second HVPS produce the high voltage levels respectively for three and six EC units.

The HVPS also includes a system of switches which allows to cut the powering of all the MAPMTs in less than a GTU in case of strong light events.

Based on the charges estimated by the ASICs and FPGA logic, the PDM board produces a switch control signals sent to the first HVPS, which transmits it to the second one. A variant option is to check for a current increase on one of the last dynodes at the level of the HVPS.

The first HVPS interfaces the housekeeping board, which provides it with monitoring signals.

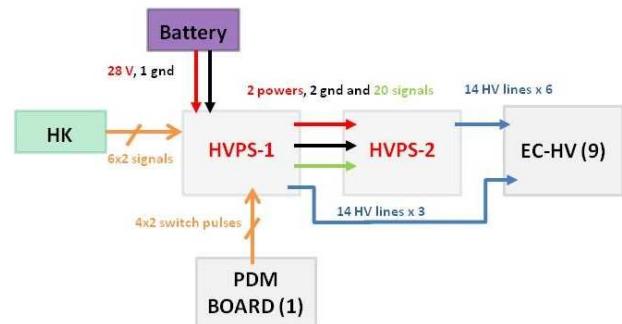


Fig.9: Schematic of the two HVPS with their signals and interfaces.

3 Prototype tests

In order to assess each board before starting the flight model production, prototypes were produced and tested in 2012.

Two prototypes of the EC units were assembled: a pure

mechanical version and an electrical one. The first one was used to check the dimensions of the boards, the assembly sequence and the potting process. The second one (assembled later), while allowing finalising these aspects, permitted to check the performances. It was tested in a black box with a light source together with the prototype of the HVP-S powering the EC unit up to 1100 V. The analog signals coming out from the MAPMTs were found as expected, proving that the system was working properly. Low pressure and temperature tests were carried out and no problem was noticed.

In parallel, a prototype of the ASIC board was tested with a dedicated test board (see figure 10). The latter has its own FPGA used to manage the ASICs configuration, data read-out and communication protocole with a computer running Labview software. All the features were tested with a test bench that included multimeters, used to check the pedestal levels and the linearity of the threshold voltage, and a pulse generator which allowed injecting a MAPMT-like signal into the board. The measurements showed nice performances validating the design of the board as it was.



Fig. 10: Picture of the ASIC prototype board connected to a dedicated test board.

After standard individual tests to check the consumption and the signal levels, the PDM board was tested together with ASIC boards with a set-up similar to the previous one (see figure 11). The interface between these two elements was checked by sending configuration to the ASICs and reading out data. Despite few minor adjustments in the firmware, all tests were successful proving that communications performed as expected.

In addition, the rest of the data processing chain was tested successfully with the PDM board, an ASIC board and an EC unit. These tests were carried out in Riken institute for the project TA-EUSO (Telescope Array) [7], which also constitut in a complete PDM that will be installed on the ground in Utah to perform similar and complementary measurements to the ones of EUSO-Balloon.

4 Conclusion

The 18th of December 2012, the results of all these prototype tests were presented to CNES during a review of the phase B of the EUSO-Balloon project. The conclusions from this review were that the flight model production of all the boards should start early 2013. The assembly of the EC units would follow on and then the individual tests of

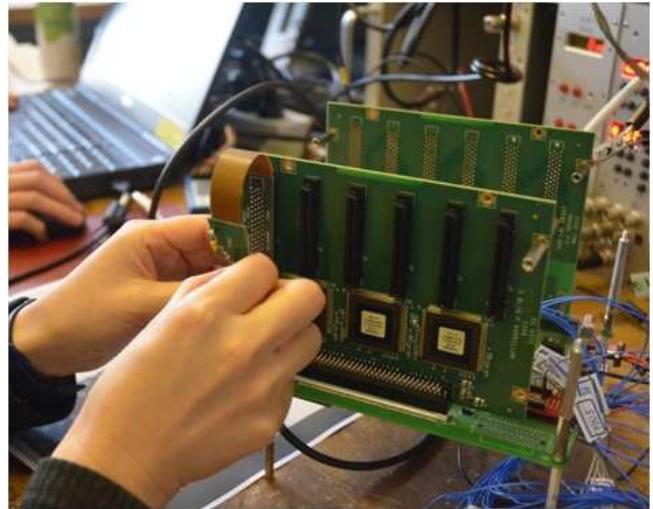


Fig. 11: Picture of the PDM board with two ASIC boards connected during prototype tests.

each element before the assembly and integration tests of the whole PDM. The goal is to provide a full instrument by the end of the year 2013 to be ready for the first balloon flight in 2014.

5 Acknowledgment

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