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Abstract

Superconducting qubit based on superconducting circuits consist of a superconducting capacitor and a Josephson junction with the transmon geometry is extensively used in advanced quantum processors, pursuing scalable quantum computing. The tuning of the qubit frequency of the transmon relies on magnetic flux-dependent interference between the supercurrents of two superconductor-insulator-superconductor (S-I-S) Josephson junctions in a superconducting loop. Josephson junction based on superconductor-semiconductor-superconductor (S-Sm-S) materials opens up a possibility to the gate-tunable transmon, referred to as the "gatemon", in which the qubit frequency can be tuned by electrostatic mean. Recent realizations of gatemons on III-V material platforms show impressive development on the alternative to the transmon, yet still leave a big question on the scalability. The silicon-germanium (SiGe) heterostructure is one of the potential platforms to host hybrid devices due to its high hole mobility and the low Schottky barrier at the Ge-metal interface. Additionally, the compatibility with the silicon-based semiconductor industry is a capable advantage for the scaling-up qubit platform.

In this thesis, we develop gatemons based on the Al-Ge-Al Josephson junction in the SiGe heterostructure. Firstly, the robust fabrication recipe, found on a top-down approach, for Josephson Field Effect Transistors (JoFETs) is established. We perform measurements exhaustively on the JoFETs to study their properties as a function of the gate voltage, temperature, and magnetic field. The devices show gate-tunability of the critical current (I_C) and the normal state resistance (R_N). The devices are estimated to have a high-transparency superconductor-semiconductor interface, as demonstrated by the high $I_C R_N$ product on the SiGe heterostructure. In the finite-voltage regime, the features corresponded to multiple Andreev reflections (MARs) are observed. Then, we fabricate and characterize niobium nitride (NbN) superconducting resonators on SiGe heterostructure. We measure the resonators in the transmission mode and extract the resonant frequency (f_r), internal quality factor (Q_i), and coupling quality factor (Q_c) from the transmission coefficient (S_{21}). Following that, we develop the fabrication process to integrate Al-Ge-Al junctions shunted with capacitors, or, in other words, gatemon, into the resonator scheme and perform the fabrication according to the design. We demonstrate the anticrossing feature in one of the fabricated gatemons. The resonant frequency of the gatemon is mapped using the two-tone spectroscopy technique and is found to be gate-tunable. The qubit has large spectral linewidth, implying a low coherence time. Additionally, we conduct the current-phase relationship (CPR) measurement on the junctions in the Superconducting QUantum Interference Device (SQUID) geometry. We can demonstrate that the junctions pose non-sinusoidal CPR. Further, the integer and half-integer Shapiro steps are observed in the current-voltage characteristic curves of irradiated junctions. This indicates that our junctions have the $\cos 2\varphi$ element, which can open up another possibility toward protected qubits.

Résumé

Le qubit supraconducteur basé sur des circuits supraconducteurs se compose d'un condensateur supraconducteur et d'une jonction Josephson avec la géométrie transmon est largement utilisé dans les processeurs quantiques avancés, à la recherche d'une informatique quantique évolutive. L'accord de la fréquence du qubit du transmon repose sur l'interférence, en fonction du flux magnétique, entre les supercourants de deux jonctions Josephson S-I-S dans une boucle supraconductrice. Les jonctions Josephson basées sur des matériaux S-Sm-S ouvrent une possibilité alternative au transmon accordable par la porte, appelée "gatemon", dans laquelle la fréquence du qubit peut être accordée par une moyenne électrostatique. Les réalisations récentes de gatemons sur des plates-formes de matériaux III-V montrent un développement impressionnant de l'alternative au transmon, mais laissent encore une grande question sur l'extensibilité. L'hétérostructure SiGe est l'une des plateformes potentielles pour accueillir des dispositifs hybrides en raison de sa grande mobilité des trous et de la faible barrière de Schottky à l'interface Ge-métal. En outre, la compatibilité avec l'industrie des semi-conducteurs à base de silicium est un avantage certain pour la plateforme de qubits à grande échelle.

Dans cette thèse, nous développons des gatemons basés sur la jonction Josephson Al-Ge-Al dans l'hétérostructure SiGe. Tout d'abord, nous établissons une recette de fabrication robuste, basée sur une approche descendante, pour les transistors à effet de champ Josephson (JoFET). Nous effectuons des mesures exhaustives sur les JoFET afin d'étudier leurs propriétés en fonction de la tension de grille, de la température et du champ magnétique. Les dispositifs présentent une adaptabilité à la grille du courant critique (I_C) et de la résistance à l'état normal (R_N). On estime que les dispositifs ont une interface S-Sm transparente, comme le montre le produit $I_C R_N$ élevé. Dans le régime de tension finie, les caractéristiques correspondant aux réflexions multiples d'Andreev sont observées. Ensuite, nous fabriquons et caractérisons des résonateurs supraconducteurs en NbN sur une hétérostructure SiGe. Nous mesurons les résonateurs en mode transmission et extrayons la fréquence de résonance (f_r), le facteur de qualité interne (Q_i), et le facteur de qualité de couplage (Q_c) du coefficient de transmission (S_{21}). Ensuite, nous développons le processus de fabrication pour intégrer des gatemons, dans le schéma du résonateur et effectuons la fabrication conformément à la conception. Nous démontrons la caractéristique d'anticroisement dans l'un des gatemons fabriqués. La fréquence de résonance du gatemon est cartographiée à l'aide de la technique de spectroscopie à deux tons et il s'avère qu'elle peut être réglée par la porte. Le qubit a une grande largeur de ligne spectrale, ce qui implique un faible temps de cohérence. En outre, nous mesurons la relation courant-phase (CPR) sur les jonctions dans la géométrie du SQUID. Nous pouvons démontrer que les jonctions présentent une CPR non sinusoïdale. En outre, les pas de Shapiro entiers et demi-entiers sont observés dans les courbes caractéristiques courant-tension des jonctions irradiées. Cela indique que nos jonctions ont l'élément $\cos 2\varphi$, ce qui peut ouvrir une autre possibilité vers des qubits protégés.

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Contents

Introduction

Since the establishment of the field of quantum mechanics in the late 19th and early 20th centuries, knowledge development in the field has led to various applications. One of those that draws a lot of attention, both from academic research and industrial investing, in this era is quantum computing.

First proposed by Feynman in 1981 [1], the quantum computer is expected to be able to simulate quantum systems requiring polynomial time and resources compared with the exponential growth in time and resources demanding for the standard computer, facilitating research in the fields of material science, chemistry, biology, and pharmacy. Further, it has been predicted theoretically that the quantum computer can outperform the classical computer for some algorithms such as prime number factorization, proposed by Shor [2], and the search algorithm, proposed by Grover [3]. This is expected to have applications in the fields of cryptography, big data, and other information technology.

However, quantum bits, the building blocks of the quantum computer, in the real world are suffering significantly from noise, which reduces the fidelity of the result. One approach to overcome the noise is the error-correcting surface code [4], where a number of physical qubits are connected together and behave as one logical qubit to improve logical qubit fidelity. To give an idea of the numbers, we give an example in the case of Shor's algorithm. To begin with, the most widely used encryption system nowadays is 2048-bit RSA encryption. With this number of bits, it implies that no standard classical computer can factorize this prime number in a realizable time scale. On the other hand, a quantum computer is expected to crack this encryption in the order of hours or days with 2048 logical qubits. Nevertheless, for the 2048 logical qubits, one needs at least about 15 million physical qubits, each with 1% error tolerance, to realize the algorithm [5].

Since a number of qubits are required, scalability is clearly one of the main

research axes in the field of quantum computing. There are many quantum systems that can host the qubits, e.g., trapped ions [6], quantum dots [7], superconducting circuits [8], nitrogen vacancies in the diamond lattices [9], and photons based on boson sampling [10]. Amongst them, one with the notable level of engineerability and scalability, with the largest solid-state-based quantum processor up to date (433-qubit IBM Quantum Osprey [11]), is the superconducting qubit based on circuit quantum electrodynamics (cQED) theory of the superconducting circuit. This makes it a promising candidate for a scalable platform for qubits.

A superconducting qubit is made of superconducting elements, mainly capacitors and Josephson junctions. There are various models of superconducting qubits with different approaches. One of the widely used models is the transmon, which was first proposed theoretically by Koch in 2007 [12]. It is composed of two Josephson junctions in a superconducting loop shunted by a large capacitor. The Josephson junctions are usually tunnel junctions that exploit the Al/Al_2O_3 technology. The transmon is insensitive to the charge noise and has a qubit transition energy that can be tuned by modulating the magnetic flux inside the superconducting loop. However, the disadvantages of the transmon are the power load in the case of many qubits and the crosstalk between neighbor bits.

In 2015, another model of the superconducting qubit was realized by de Lange [13] and Larsen [14] with the bottom-up fabrication of InAs nanowires. In this geometry, two superconducting contacts are connected through a semiconductor weak link, and an electrostatic gate allows for tuning the carrier density of the semiconductor material, similar to a standard transistor. When the semiconductor channel is fully proximitized by the superconductor contacts, a gate-tunable supercurrent can flow through the device. This geometry of the device is known as the Josehpson Field Effect Transistor (JoFET). In this case, a qubit only requires one Josephson junction, again shunted by a large capacitor. This qubit has the nickname "gatemon", shortened from gate-tunable transmon, reflecting its capability to be tuned by electrostatic gate voltage. This advantage makes the gatemon a promising alternative to the transmon. Later, the gatemon based on 2DEG in InAs were demonstrated by Casparis in 2018 [15] using top-down fabrication, which offers better reproducibility and scalability.

In the gatemon, the device operates based on the proximity effect within the S-Sm-S junction. Supercurrent can flow through the junction via the Andreev reflection process. According to the Octavio-Blonder-Tinkham-Klapwijk (OBTK) theory [16, 17], the rate of Andreev reflection, which contributes to the supercurrent, depends on the strength of the barrier at the interface. In practice, this barrier at the interface can result from factors such as oxide layers, defects, and surface imperfections. Therefore, from a fabrication perspective, it is crucial to achieve a clean superconductor-semiconductor contact.

From a physical point of view, germanium is a material that can establish a good ohmic contact with p-type metals due to the pinning of the Fermi level at the valence band [18]. This phenomenon results in a low Schottky barrier across the metal-semiconductor interface. Moreover, germanium is known for its high

hole mobility [19]. This characteristic implies less scattering within the semiconductor region, leading to the potential for higher supercurrent. The JoFETs based on germanium heterostructure were first demonstrated in our group in 2019 by Vigneau [20].

From an engineering point of view, germanium is the material that is already compatible with the semiconductor industry and CMOS technology, so when talking about scalability, germanium is the material that has been widely used in large-scale processes. Thus, it would be easier to develop a scalable process based on germanium.

These considerations lead to the motivation behind the work presented in this thesis: to explore hybrid superconductor-semiconductor devices on the SiGe heterostructure platform with the ambition of realizing the Ge-based gatemon. This thesis is organized into six chapters.

In Chapter 1, we review the fundamental concepts of circuit quantum electrodynamics (cQED), which forms the foundation of superconducting qubits. We also justify the suitability of Ge as the material for this project.

Chapter 2 discusses the fabrication of the devices using a top-down approach. We provide a brief overview of the SiGe heterostructure, the material platform we work with. Then, we present the fabrication recipe for achieving high yields and high transparency Al-Ge-Al junctions, along with insights into the optimization of the process to develop this recipe.

Chapter 3 focuses on the characterization of S-Sm-S junctions as JoFETs. We present the result of the exhaustive study of the properties of the JoFETs as a function of gate voltage, temperature, and magnetic field.

Chapter 4 is the story about superconducting resonators. Initially, we study superconducting resonators in the co-planar waveguide geometry through electromagnetic simulations. We use this information to design and implement the fabrication of niobium nitride (NbN) resonators on the SiGe heterostructure. Furthermore, we characterize the resonators through transmission measurements and extract relevant parameters, such as internal quality factor, coupling quality factor, and resonant frequency.

Chapter 5 is particularly exciting as it combines our know-how in JoFETs and resonators to design the gatemon. This "qubit" is realized by shunting a JoFET with a capacitor and is coupled to a superconducting resonator, which, in turn, couples to a transmission line. We demonstrated the qubit-resonator coupling with anticrossing behaviors and mapped the resonant frequency of the qubit using the two-tone spectroscopy technique.

In Chapter 6, we present a complementary study on the current-phase relationship (CPR) and the AC radiation response of the junctions. The aim of this study is to justify the presence of two Cooper-pairs cotransport, a critical element for the $\cos 2\varphi$ qubit, offering an alternative approach to address the challenges of the Noisy Intermediate Scale Quantum (NISQ) era.

Lastly, we will discuss the final overview of the results, and the further perspectives of the project.

CHAPTER 1

Why are we interested in Ge-based hybrid superconductor-semiconductor devices?

Quantum computing and quantum information technology have been developed a lot in the past few decades. The field of study is based on a building block called a "quantum bit" or a "qubit". On the theory aspect, there is the development of algorithms for a certain task to achieve quantum supremacy; Shor's factorization algorithm [2] is one of the best-known examples. The challenges from an experiential point of view are to fabricate, control, and measure the robust qubit. There are several material platforms on which the qubit has been realized, for example, trapped ions [6], quantum dots [7], nitrogen vacancies in diamonds [9], and photons [10]. Arguably, one of the most developed solid-state-based platforms is the superconducting qubit based on the circuit quantum electrodynamics (cQED) system. Transmon [12] is a commonly used design of a superconducting qubit where the logic gate operation relies on tuning qubit energy with applied magnetic flux. In the past few years, gate-tunable transmon [13–15, 21] has been explored as an alternative to tune the qubit energy with electrostatic means to put away concerns about crosstalk and Joule heating effects. Nevertheless, gatemon is based on a superconductor-semiconductor-superconductor (S-Sm-S) junction. Thus, choosing the material wisely would greatly facilitate future progress on the study. Here, we consider germanium the semiconductor of choice for our gatemon, as it offers several advantages for the gatemon device. Additionally, germanium is compatible with the current CMOS technology [22], and it could benefit the scaling-up architecture of the gatemon in the future.

1.1 Quantum computing with cQED

Circuit quantum electrodynamics (cQED) is the study of an interaction between a photon and an artificial atom. Typically, in cQED, the photon is represented by the oscillation mode confined in a superconducting resonator [23], and the artificial atom is based on a non-linear superconducting circuit.

In this section, we present several superconducting circuits that are related to our work in this thesis. First, we describe the superconducting LC circuit, which is a quantum harmonic oscillator. Then, we discuss the superconducting circuit of a transmon qubit, where the Josephson junction is integrated into the circuit to provide anharmonicity to the system. Then, we show two approaches, split transmon and gatemon, for implementation to be able to tune qubit frequencies, which is necessary for quantum logic gate operations. Later, we discuss the situation where a transmon is attached to an LC oscillator, which provides a basic understanding of the qubit readout.

1.1.1 Quantum harmonic oscillator

One of the simplest superconducting circuits is a superconducting LC oscillator. As stated in its name, it consists of a superconducting capacitor with a capacitance C, and a superconducting inductor with an inductance L. Here, we consider them lumped elements, as shown in Figure 1.1(a). Firstly, we treat the circuit with the classical approach of the linear LC oscillator, where the energy is stored in the inductor and the capacitor.

The energy stored in an element at a certain time is given by:

$$E(t) = \int_0^t I(t')V(t')dt', \tag{1.1}$$

where, $I(t')$ is the current passing through an element, and $V(t')$ is the voltage across the element. Note that we assume that the system is at rest at $t = 0$. To determine the Lagrangian of the system, we need to define the "position" variable of the system and its conjugate momentum in terms of the circuit variable. Here, we use the flux of the system as a position variable. The flux is defined as:

$$\Phi(t) = \int_0^t V(t')dt', \tag{1.2}$$

where, Φ is the magnetic flux through the inductor.

Then, we express the associated kinetic energy stored in the capacitor $\mathcal{T}_C$, and the associated potential energy stored in the inductor $\mathcal{U}_L$, using the classical current-voltage relation $V = L\ dI/dt$, and $I = C\ dV/dt$ and the definition of energy and flux given in Equations 1.1, and 1.2, as:

$$\mathcal{T}_C = \frac{C\dot{\Phi}^2}{2}, \tag{1.3}$$

$$\mathcal{U}_L = \frac{\Phi^2}{2L}. \tag{1.4}$$

Then, we can write the Lagrangian of the system as:

$$\mathcal{L} = \mathcal{T}_C - \mathcal{U}_L = \frac{C\dot{\Phi}^2}{2} - \frac{\Phi^2}{2L}, \tag{1.5}$$

and the conjugate momentum as:

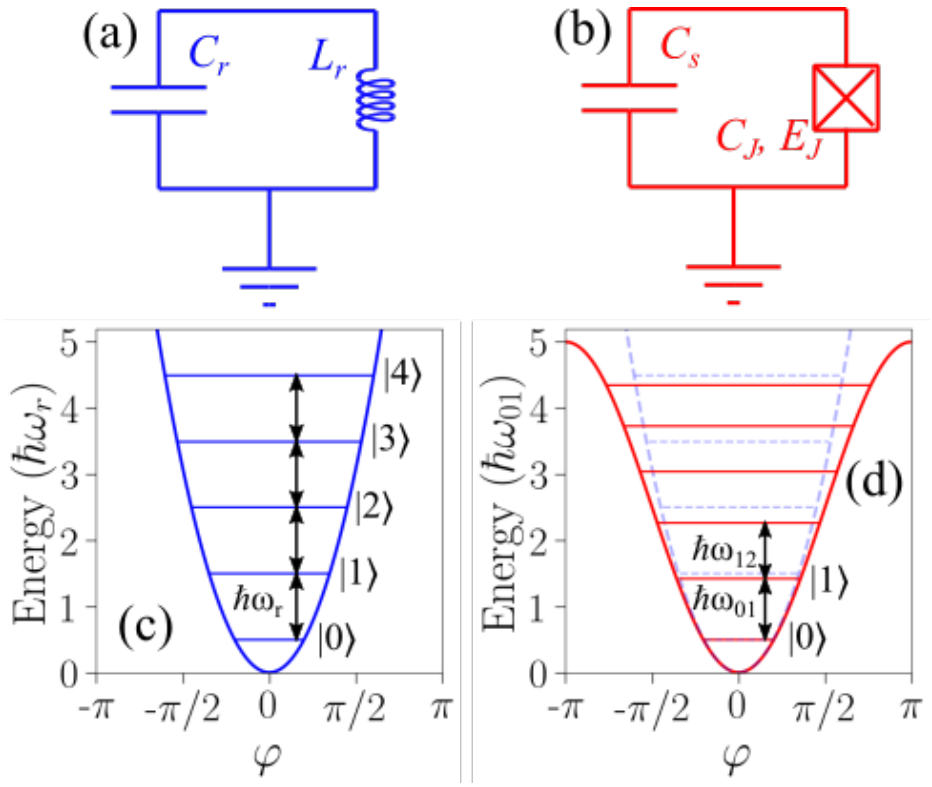

Figure 1.1 – Lumped element representation of: (a) Quantum harmonic oscillator as LC oscillator, and (b) Transmon as a Josephson junction in parallel with a capacitor. The circuit in (a) has the Hamiltonian that gives quadratic potential well results in a quantum harmonic oscillator with an equally spaced energy level. The non-linearity provided by the Josephson junction causes the potential well to deviate from the quadratic function. This gives rise to the anharmonicity in the energy level, as shown in (d). The ability to drive the transition between each energy state separately makes the transmon can be used as a qubit while the LC oscillator cannot. Nevertheless, the LC oscillator has an application in cQED as a resonator. The figure has been adapted from [24].

$$Q = \frac{\partial \mathcal{L}}{\partial \dot{\Phi}} = C\dot{\Phi}. \tag{1.6}$$

Effectively, the Hamiltonian H of this LC oscillator can be written as:

$$H = Q\dot{\Phi} - \mathcal{L} = \frac{Q^2}{2C} + \frac{\Phi^2}{2L}. \tag{1.7}$$

In an analogy with the case of the Hamiltonian of the mechanical oscillator $H = p^2/2m + m\omega^2 x^2/2$, one can imply the resonant frequency of the system to be $\omega = 1/\sqrt{LC}$ [24].

Then, we turn this to the Hamiltonian of the quantum LC circuit by replacing Φ and its conjugate momentum Q with quantum operators $\hat{Q}$, and $\hat{\Phi}$, respectively. Thus, we obtain [24]:

$$H = \frac{\hat{Q}^2}{2C} + \frac{\hat{\Phi}^2}{2L}, \tag{1.8}$$

with the commutation relation:

$$[\hat{\Phi}, \hat{Q}] = \hat{\Phi}\hat{Q} - \hat{Q}\hat{\Phi} = i\hbar, \tag{1.9}$$

where $\hbar$ is the reduced Planck's constant.

We can express the Hamiltonian to represent the superconducting circuit by rewriting Equation 1.9 in terms of superconducting effect-related variables; Cooper pair number $\hat{n} = \hat{Q}/2e$, and the phase $\hat{\varphi} = 2\pi\hat{\Phi}/\Phi_0$, where $\Phi_0 = \hbar/2e$. This give:

$$\hat{H} = 4E_C\hat{n}^2 + \frac{E_L}{2}\hat{\Phi}^2, \tag{1.10}$$

where, $E_C = e^2/(2C)$ is the charging energy, and $E_L = (\Phi_0/2\pi)^2/L$ is the inductive energy.

The Hamiltonian in Equation 1.10 is similar to the Hamiltonian describing a particle in a quadratic potential well $\hat{H} = \hat{p}^2/2m + m\omega^2\hat{x}^2/2$, so we can sketch the potential well and the energy levels of eigenstates of the system as shown in Figure 1.1(c) [25]. Likewise, this has an infinite number of eigenstates $|n\rangle$ for $n = (0, 1, 2, ...)$, and the eigenenergies of these eigenstates are equally spaced by $E_{n+1} - E_n = \hbar\omega_r$, where $\omega_r = \sqrt{E_C E_L}/\hbar$. By making an analogy with the Hamiltonian of a particle in a quadratic potential well, we can deduce the lowering $(\hat{a})$, and raising $(\hat{a}^\dagger)$ operators in terms of $\hat{\varphi}$ and $\hat{n}$ as:

$$\hat{a} = \left(\frac{E_L}{32E_C}\right)^{1/4}\hat{\varphi} + i\left(\frac{2E_C}{E_L}\right)^{1}/4\hat{n}, \tag{1.11}$$

$$\hat{a}^\dagger = \left(\frac{E_L}{32E_C}\right)^{1/4}\hat{\varphi} - i\left(\frac{2E_C}{E_L}\right)^{1/4}\hat{n}, \tag{1.12}$$

with, $\hat{a}\,|i\rangle = \sqrt{i}\,|i-1\rangle$, $\hat{a}^\dagger\,|i\rangle = \sqrt{i+1}\,|i+1\rangle$, and $[\hat{a}, \hat{a}^\dagger] = 1$.

Following that, the Hamiltonian in Equation 1.10 can be simply written as:

$$\hat{H} = \hbar\omega_r(\hat{a}^\dagger\hat{a} + \frac{1}{2}). \tag{1.13}$$

While the quantum states can be created by the superconducting LC oscillator, their application as a qubit is not possible. To define a qubit, we need to define the two energy states and be able to address the transition between them without exciting other energy transitions. Since all of the energy levels are equally spaced in this system, we cannot choose a frequency ω_r to selectively drive a particular transition. Nevertheless, the LC circuit can be used as the superconducting resonator for applications in mediating the qubit states, qubit readout, and qubit manipulation [26].

1.1.2 Transmon: anharmonic oscillator

To introduce an anharmonicity in the system, we add a non-linear element to the superconducting circuit, as shown in Figure 1.1(b). Here, the linear inductance in the LC oscillator can be replaced by a Josephson junction, which is a non-linear and non-dissipative element. In practice, the Josephson junction can be formed by two superconducting leads separated by a non-superconducting layer. One of the commonly used Josephson junctions for the superconducting qubits is the superconductor-insulator-superconductor (S-I-S) junction, where the non-superconducting layer is a thin layer of oxide. For this kind of junction, the first Josephson relation can be written as [27]:

$$I_s = I_C \sin(\varphi) = I_C \sin\left(2\pi\frac{\Phi(t)}{\Phi_0}\right), \tag{1.14}$$

where I_s is the supercurrent passing through the junction, I_C is the critical current, the maximum non-dissipative current the junction can hold, and φ is the phase difference across the junction.

The second Josephson relation describing the evolution of the phase as a function of the voltage dropped V across the junction is given by [27]:

$$\frac{\mathrm{d}\varphi}{\mathrm{d}t} = \frac{2eV}{\hbar}. \tag{1.15}$$

Note that we treat the Josephson junction as a non-linear inductor with flux-dependent inductance [28]:

$$L(\Phi) = \left(\frac{\partial I_s}{\partial \Phi}\right)^{-1} = \frac{L_J}{\cos\left(2\pi\frac{\Phi}{\Phi_0}\right)}, \tag{1.16}$$

with $L_J = \Phi_0/2\pi I_C$ as the Josephson inductance.

Using Equation 1.1, we can derive the energy stored in a Josephson junction to be:

$$E(\varphi) = \int_0^t I(t')V(t')dt' = \int_0^t I_s \frac{\hbar}{2e}\frac{\mathrm{d}\varphi}{\mathrm{d}t'}dt' = \int_0^{\varphi} \frac{I_C\hbar}{2e}\sin(\varphi')d\varphi' = E_J[1-\cos(\varphi)], \tag{1.17}$$

where $E_J = I_C\Phi_0/2\pi = I_C\hbar/2e$ is the Josephson energy. As we treat this expression as potential energy, we omit the constant term, which is just a potential offset, and use $\mathcal{U}_J = -E_J\cos(\varphi)$.

Likewise, we can write the Lagrangian of the circuit in Figure 1.1(c) to be:

$$\mathcal{L} = \mathcal{T}_C - \mathcal{U}_J = \frac{C\dot{\Phi}^2}{2} + E_J\cos(\varphi), \tag{1.18}$$

which then gives the Hamiltonian:

$$\hat{H} = 4E_C\hat{n}^2 - E_J\cos(\hat{\varphi}). \tag{1.19}$$

Effectively, the phase dependent of the potential well of this system is a cosine function, as plotted in Figure 1.1(d). The deviation from the quadratic potential gives rise to the anharmonicity between each transition between eigenstates. The ground state ($|0\rangle$) and the first excited state ($|1\rangle$) can then be used as a two-level system of a qubit.

Here, we define the anharmonicity of the system by $\alpha = \hbar\omega_{12} - \hbar\omega_{01}$, where ω_{12}, and ω_{01} are the resonant frequencies that correspond to the transition between the states $|1\rangle$ to $|2\rangle$ and $|0\rangle$ to $|1\rangle$, respectively.

To compute the anharmonicity of the system, we expand $\mathcal{U}_J$ using the Taylor series of cosine to obtain:

$$\mathcal{U}_{\mathcal{J}} = -E_J + \frac{E_J}{2}\hat{\varphi}^2 - \frac{E_J}{24}\hat{\varphi}^4 + \dots. \tag{1.20}$$

Typically, a transmon is designed to be operated in the "transmon regime", where $E_J/E_C \approx 50$, to suppress the charge noise [12]. By drawing an analogy with a pendulum of mass m attaching to a string of length l at the center of rotation under a gravitational field g as shown in [12], the Hamiltonian of the rotor can be expressed as $H_{rot} = \frac{\hat{L}_z^2}{2ml^2} - mgl\cos\hat{\varphi}$, where $\hat{L}_z \leftrightarrow \hat{n}\hbar$ is the angular momentum, $E_J \leftrightarrow mgl$, and $E_C \leftrightarrow \hbar^2/8ml^2$. When the gravitational field is significantly strong, such that $E_J \gg E_C$, the dynamic favors the small-angle oscillation around $\hat{\varphi} \approx 0$. Thus, we neglect terms with an order higher than four. Additionally, the constant term $-E_J$, corresponding to a potential offset, can be omitted. Then, Equation 1.19 can be expressed approximately as:

$$\hat{H} \approx 4E_C\hat{n}^2 + \frac{E_J}{2}\hat{\varphi}^2 - \frac{E_J}{24}\hat{\varphi}^4. \tag{1.21}$$

We can treat this as a perturbation of $\hat{H}_0$ by the potential $V'(\hat{\varphi})$ as [29]:

$$\hat{H} = \hat{H}_0 + V'(\hat{\varphi}), \tag{1.22}$$

where, $\hat{H}_0 = 4E_C\hat{n}^2 + \frac{E_J}{2}\hat{\varphi}^2$ with $\omega_J = \sqrt{E_J E_C}/\hbar$, and $V'(\hat{\varphi}) = -\frac{E_J}{24}\hat{\varphi}^4$.

From the definition of ladder operators in Equation 1.11, and 1.12, we can express the phase operator as:

$$\hat{\varphi} = \left(\frac{2E_C}{E_J}\right)^{1/4}(\hat{a} + \hat{a}^\dagger). \tag{1.23}$$

Then, the perturbation is equal to:

$$V'(\hat{\varphi}) = -\frac{E_C}{12}(\hat{a} + \hat{a}^\dagger)^4 \approx -\frac{E_C}{2}(\hat{a}^\dagger\hat{a}^\dagger\hat{a}\hat{a} + 2\hat{a}^\dagger\hat{a}). \tag{1.24}$$

Note that the approximation in Equation 1.24, keeping only the resonant terms with the same number of raising and lowering operators, is based on the rotating wave approximation with an assumption $\omega_J \gg \alpha/\hbar$. From this assumption, in the rotating frame at ω_J, all the non-resonant terms oscillate with the angular frequency ω_J much larger than α. Thus, on the time scale of α, the average of these non-resonant terms over the time scale of α is approximately zero [29].

We can compute the expectation value E_i, which corresponds to the eigenenergies of the first three states $|0\rangle$, $|1\rangle$, and $|2\rangle$, using $\langle i|\,\hat{H}\,|i\rangle = E_i$ as follows:

$$\langle 0|\,\hat{H}\,|0\rangle = \langle 0|\,\hat{H}_0\,|0\rangle + \langle 0|\,V'(\hat{\varphi})\,|0\rangle = \frac{1}{2}\hbar\omega_J, \tag{1.25}$$

$$\langle 1|\,\hat{H}\,|1\rangle = \langle 1|\,\hat{H}_0\,|1\rangle + \langle 1|\,V'(\hat{\varphi})\,|1\rangle = \frac{3}{2}\hbar\omega_J - E_C, \tag{1.26}$$

$$\langle 2|\,\hat{H}\,|2\rangle = \langle 2|\,\hat{H}_0\,|2\rangle + \langle 2|\,V'(\hat{\varphi})\,|2\rangle = \frac{5}{2}\hbar\omega_J - 3E_C, \tag{1.27}$$

which give the anharmonicity:

$$\alpha = E_{12} - E_{01} = \hbar\omega_J\left(\frac{5}{2} - \frac{3}{2}\right) - 2E_C + \hbar\omega_J\left(\frac{3}{2} - \frac{1}{2}\right) - E_C = -E_C. \tag{1.28}$$

In practice, transmon qubits are usually designed to have $E_C \approx$ 200-300 MHz for the qubit resonant frequency, $\omega_{01}/2\pi$ in the range between 4 and 8 GHz [30–33].

1.1.3 Flux-tunable transmon

One of the commonly used approaches to performing computation on qubits is to apply the quantum logic gate. In practice, the logic gate operations are based on tuning the qubit frequencies to bring them in and out of resonance with others to exchange energy states [34]. Experimentally, one way to implement the frequency tuning of the qubit is by replacing a single Josephson junction with two Josephson junctions in parallel, forming a loop of the Superconducting

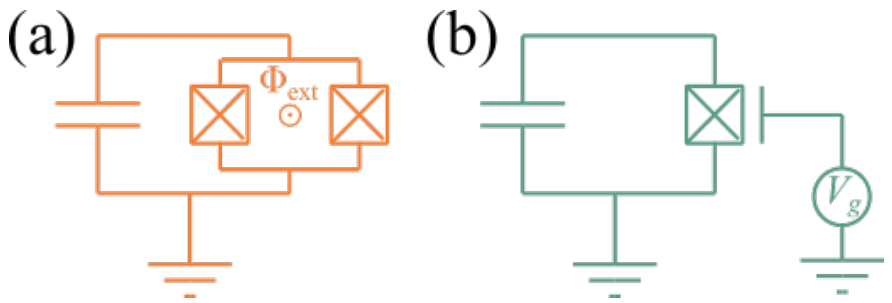

Figure 1.2 – Schematics of the lumped circuit models of: (a) Flux-tunable transmon, and (b) Gate-tunable transmon

QUantum Interference Device (SQUID) as shown in the schematic of the flux-tunable transmon, sometimes also called split transmon, in Figure 1.2(a).

Given this configuration and assuming that both junctions are identical, the Hamiltonian of the system is as follows:

$$\hat{H} = 4E_C\hat{n}^2 - E_J(\cos(\varphi_1) + \cos(\varphi_2)), \tag{1.29}$$

where, φ_1, and φ_2 are the phases across the first and the second junction, respectively.

When a magnetic field is applied to the SQUID loop, there is a magnetic flux due to an external magnetic field (Φ_{ext}) trapped inside the loop. To satisfy the condition of flux quantization, the condition [27]:

$$\varphi_1 - \varphi_2 + \frac{\pi\Phi_{ext}}{\Phi_0} = 2n\pi, \tag{1.30}$$

where, $n = (0, 1, 2, \ldots)$, must be met.

With trigonometric identities $\cos(A)+\cos(B) = 2\cos((A+B)/2)\cos((A-B)/2)$, we can rewrite the Hamiltonian of the flux tunable transmon as:

$$\hat{H} = 4E_C\hat{n}^2 - 2E_J\cos\left(\frac{\pi\Phi}{\Phi_0}\right)\cos(\hat{\varphi}) = 4E_C\hat{n}^2 - E'_J\cos(\hat{\varphi}), \tag{1.31}$$

where $E'_J = 2E_J\cos\left(\frac{\pi\Phi}{\Phi_0}\right)$ is the flux-dependent effective Josephson energy, and $\varphi = (\varphi_1 - \varphi_2)/2$ is the average phase between two junctions.

Effectively, Equation 1.31 indicates that the effective Josephson energy of the flux-tunable transmon can be tuned by external magnetic flux. This results in tuning the qubit energy $\hbar\omega_{01} \approx \sqrt{8E'_J E_C} - E_C$ with the applied magnetic field.

1.1.4 Gate-tunable transmon

While flux-tunable transmon is one of the most used transmon nowadays, with an impressive record of a coherence time of 503 µs [33], one of the drawbacks of flux-tunable transmon is that it relies on an applied magnetic field. This can

lead to cross-talk to the adjacent qubits and the possible issues of large currents ($\approx 10^{-3}$A per transmon $\times 10^6$ physical qubits) in the flux line when the number of qubits is scaled up. The estimation based on the statement that we may need millions of physical qubits for 4000 logical qubits for the widely used RSA (Rivest–Shamir–Adleman) encryption [35]. Recently, gate-tunable transmons have been proposed and demonstrated [13–15, 21, 36]. In this model, the single S-I-S Josephson junction in the transmon is replaced by a superconductor-semiconductor-superconductor (S-Sm-S) Josephson junction. In the S-Sm-S junction, the supercurrent can be transported through the junction by a process called "Andreev reflection" [37, 38]. In the mechanism, an electron at the Sm-S interface can be retroreflected as a hole and transfer one Cooper pair to the superconducting lead. In another direction, a hole can also reflect back as an electron and absorb one Cooper pair. This is also called the proximity effect, which is the phenomenon when the sign of superconductivity is observed in the non-superconducting material in contact with a superconductor. In other words, the semiconductor channel is proximitized by the superconducting leads. The rate of the Andreev reflection process depends on several factors, including carrier density. As a result of changing the carrier density in the semiconductor by the gate voltage, the critical current and, consequently, the qubit frequency are gate-tunable. This qubit model has the nickname "gatemon", in short for gate-tunable transmon [39].

Since the gatemon is a variation of the transmon, in a simple demonstration, one can understand that the tuning of qubit frequency is the tuning of E_J in the transmon Hamiltonian (Equation 1.19) as:

$$\hat{H} = 4E_C\hat{n}^2 - E_J(V_g)\cos(\hat{\varphi}) = 4E_C\hat{n}^2 - \frac{\hbar}{2e}I_c(V_g)\cos(\hat{\varphi}), \tag{1.32}$$

which may be enough to perceive the basic idea of gatemon. Nevertheless, substituting the S-I-S junction with the S-Sm-S junction is not as simple as that. In fact, not all of the S-Sm-S junctions have the simple energy phase relation of $\mathcal{U}(\varphi) = -E_J\cos(\varphi)$. If we assume that the junction is sufficiently short, in the short junction limit where the junction length is much less than the junction coherence length (ψ), quasiparticles can go on Andreev reflection multiple times before losing the coherence. This leads to the formation of the Andreev bound states of a Cooper pair with the energy states of $\pm\Delta\sqrt{1 - T_i\sin^2(\hat{\varphi}/2)}$, where Δ is the superconducting gap and T_i is the transparency of the transport channel i [40, 41]. In an S-Sm-S junction with multiple transport channels, the potential energy can be found by summing the energy of all the ground-state energy of the Andreev bound states. This gives:

$$\mathcal{U}_J(\hat{\varphi}) = -\Delta\sum_i \sqrt{1 - T_i\sin^2(\hat{\varphi}/2)}, \tag{1.33}$$

and the new gatemon Hamiltonian as:

$$\hat{H} = 4E_C\hat{n}^2 - \Delta\sum_i \sqrt{1 - T_i \sin^2(\hat{\varphi}/2)}. \tag{1.34}$$

In fact, this led to one of the consequences that could be considered a drawback of the gatemon as it could potentially reduce the anharmonicity of the qubit. To elaborate on that, we expand $\mathcal{U}_J$ up to the order of four as [36]:

$$\begin{aligned}\mathcal{U}_J(\hat{\varphi}) &= -\Delta\sum_i \sqrt{1 - T_i \sin^2(\hat{\varphi}/2)} \\ &\approx \frac{\Delta}{4}\sum_i \left[\frac{T_i}{2}\hat{\varphi}^2 - \frac{T_i}{24}\left(1 - \frac{3}{4}T_i\right)\hat{\varphi}^4\right] \\ &= E_J\frac{\hat{\varphi}^2}{2} - E_J\left(1 - \frac{3\sum T_i^2}{4\sum T_i}\right)\frac{\hat{\varphi}^4}{24},\end{aligned} \tag{1.35}$$

where $E_J = \frac{\Delta}{4}\sum T_i$. Then, we do the same trick as in Equation 1.22 by considering the perturbation term $V'(\hat{\varphi})$ as:

$$V'(\hat{\varphi}) = -E_J\left(1 - \frac{3\sum T_i^2}{4\sum T_i}\right)\frac{\hat{\varphi}^4}{24} = -\frac{E_C}{12}\left(1 - \frac{3\sum T_i^2}{4\sum T_i}\right)(\hat{a} + \hat{a}^\dagger)^4. \tag{1.36}$$

Following that, we apply the rotating wave approximation and calculate the eigenenergies of the first three states as:

$$\langle 0|\,\hat{H}\,|0\rangle = \langle 0|\,\hat{H}_0\,|0\rangle + \langle 0|\,V'(\hat{\varphi})\,|0\rangle = \frac{1}{2}\hbar\omega_J, \tag{1.37}$$

$$\langle 1|\,\hat{H}\,|1\rangle = \langle 1|\,\hat{H}_0\,|1\rangle + \langle 1|\,V'(\hat{\varphi})\,|1\rangle = \frac{3}{2}\hbar\omega_J - E_C\left(1 - \frac{3\sum T_i^2}{4\sum T_i}\right), \tag{1.38}$$

$$\langle 2|\,\hat{H}\,|2\rangle = \langle 2|\,\hat{H}_0\,|2\rangle + \langle 2|\,V'(\hat{\varphi})\,|2\rangle = \frac{5}{2}\hbar\omega_J - 3E_C\left(1 - \frac{3\sum T_i^2}{4\sum T_i}\right), \tag{1.39}$$

which, again, gives the anharmonicity that can be expressed as:

$$\begin{aligned}\alpha &= E_{12} - E_{01} \\ &= \hbar\omega_J\left(\frac{5}{2} - \frac{3}{2}\right) - 2E_C\left(1 - \frac{3\sum T_i^2}{4\sum T_i}\right) + \hbar\omega_J\left(\frac{3}{2} - \frac{1}{2}\right) - E_C\left(1 - \frac{3\sum T_i^2}{4\sum T_i}\right) \\ &= -E_C\left(1 - \frac{3\sum T_i^2}{4\sum T_i}\right).\end{aligned} \tag{1.40}$$

Equation 1.40 shows that the anharmonicity of the gatemon depends on the transparency of the conducting channels. In the case of a very high-transparency S-Sm-S junction ($T_i \approx 1$), α can be reduced up to the factor of 4. This is in contrast to the preference to have high anharmonicity in practical applications of transmon. The effect of a reduction in anharmonicity in the high-transparency junction has been confirmed experimentally in the study by A. Kringhøj [36].

From the fabrication point of view, the complexity of the fabrication process can be considered another major drawback of the gatemon, as it involves more steps than that of the transmon. This could result in more surface residue and, consequently, qubit decoherence. Additionally, the top-down fabrication approach of the gatemon is usually based on two-dimensional gas in the heterostructure [15]. This kind of material platform generally has more dielectric loss than standard oxide materials like silica or sapphire. On the other hand, the bottom-up approach based on semiconductor nanowires has the problem of scalability instead.

1.1.5 Dispersive readout

Having access to the qubit states is a crucial requirement to make use of quantum computing. Dispersive readout is a non-disruptive method to read the qubit state [23, 42], which is widely used in the cQED community. The method relies on measuring the state of a resonator coupled to the qubit. The data from the resonator measurements gives access to information about the state of the qubit. Although we did not perform the dispersive readout of our gatemon in this thesis, we made use of the dispersive shift to map the gatemon resonant frequency in Chapter 5. Thus, it is worth discussing the basic principle of the dispersive readout.

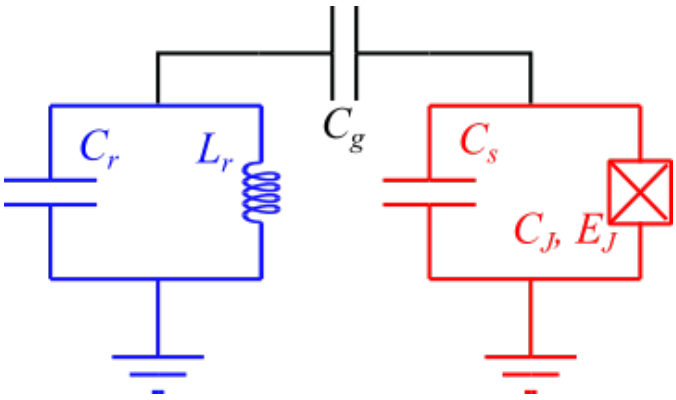

Figure 1.3 – Schematic of a transmon coupled to a resonator via a capacitor C_g. The Josephson junction in the transmon is shunted by a capacitor with a capacitance much larger than the junction capacitance ($C_s \gg C_J$). Coupling interaction causes a dispersive shift in the resonator's frequency depending on the state, $|0\rangle$ or $|1\rangle$, of the transmon.

First, we consider the transmon qubit coupling to an LC oscillator via a capacitance C_g as shown in the circuit diagram in Figure 1.3. Here, we treat the LC oscillator as the resonator with a capacitance C_r, an inductance L_r, and a resonant frequency $\omega_r = 1/\sqrt{L_r C_r}$. Note that, typically, transmon is designed to have C_J much smaller than the shunt capacitance C_s. From the figure, we define $C_\Sigma = C_J + C_s$, and $E_C = e^2/2C_\Sigma$. The model can be described by the Hamiltonian [12]:

$$\hat{H} = 4E_C\hat{n}^2 - E_J\cos(\hat{\varphi}) + \hbar\omega_r\hat{a}^\dagger\hat{a} + 2\beta eV_{rms}^0\hat{n}(\hat{a} + \hat{a}^\dagger), \tag{1.41}$$

where $\beta = C_g/C_\Sigma$, and $V_{rms}^0 = \sqrt{\hbar\omega_r/2C_r}$ denotes the root mean square voltage of the resonator. Here, the first and second terms in the Hamiltonian describe a bare transmon, as discussed in Subsection 1.1.2. The third term represents the resonator as the quantum harmonic oscillator, and the fourth term describes the coupling between the qubit and the resonator.

Equation 1.41 can be expressed in terms of the uncoupled transmon states $|i\rangle$ with the transition frequency ω_i in the form of the generalized Jaynes-Cummings Hamiltonian [12]:

$$\hat{H} = \hbar\sum_j \omega_j |j\rangle\langle j| + \hbar\omega_r\hat{a}^\dagger\hat{a} + \hbar\sum_{i,j} g_{i,j}|i\rangle\langle j|(\hat{a} + \hat{a}^\dagger), \tag{1.42}$$

where $g_{ij} = 2\beta eV_{rms}^0\langle i|\hat{n}|j\rangle/\hbar$ denotes the coupling strength between the states $|i\rangle$ and $|j\rangle$. From Equations 1.11, and 1.12, the number operator $\hat{n}$ can be expressed in terms of ladder operators as:

$$\hat{n} = -i\left(\frac{E_J}{8E_C}\right)^{1/4}(\hat{a} - \hat{a}^\dagger), \tag{1.43}$$

which yields:

$$\langle j+1|\hat{n}|j\rangle \approx \sqrt{\frac{j+1}{2}}\left(\frac{E_J}{8E_C}\right)^{1/4}, \tag{1.44}$$

$$\langle j+k|\hat{n}|j\rangle \approx 0, \tag{1.45}$$

for $|k| > 1$, and $E_J/E_C \to \infty$. We use Equations 1.44 and 1.45, along with the rotating wave approximation, to simplify Equation 1.42 to be [12]:

$$\hat{H} = \hbar\sum_j \omega_j |j\rangle\langle j| + \hbar\omega_r\hat{a}^\dagger\hat{a} + \hbar\sum_{i,j} g_{i,j}(|i\rangle\langle j|\hat{a}^\dagger + |i+1\rangle\langle i|\hat{a}). \tag{1.46}$$

We define the detuning Δ_i as $\Delta_i = \omega_{i,i+1} - \omega_r$. In the dispersive limit where $|\Delta_i| \gg g_{01}$, and $|\Delta_i + \alpha| \gg g_{01}$, one can apply the second-order perturbation on Equation 1.46 [43] to obtain the effective Hamiltonian [12]:

$$\hat{H} = \frac{\hbar\omega'_{01}}{2}\hat{\sigma_z} + (\hbar\omega'_r + \hbar\chi\hat{\sigma_z})\hat{a}^\dagger\hat{a}, \tag{1.47}$$

where $\sigma_z = |1\rangle\langle 1| - |0\rangle\langle 0|$ is the Pauli's spin operator, $\omega'_r = \omega_r - \chi_{12}/2$, $\omega'_{01} = \omega_{01} + \chi_{01}$, $\chi = \chi_{01} - \chi_{12}/2$, and $\chi_{ij} = g_{ij}^2/(\omega_{i,j} - \omega_r)$. In principle, the main message from Equation 1.47 is that the resonant frequency of the resonator ω'_r will be shifted for $\pm\chi$ according to the state of the transmon.

By applying $\hbar\omega_{12} = \hbar\omega_{01} + \alpha$, and $g_{12} = \sqrt{2}g_{01}$ [42], we can also express χ in term of α as:

$$\chi = \frac{g_{01}^2}{\Delta_0} - \frac{g_{01}^2}{\Delta_0 + \alpha/\hbar}, \tag{1.48}$$

which indicates that large anharmonicity is more favorable in the dispersive readout application as it yields a larger dispersive shift on the resonator, making it easier to be observed experimentally.

1.2 Germanium for scalable quantum computing

If we want to build scalable quantum processors based on a certain material platform, there are two main things to consider: first, can we really make a qubit on that platform, and second, is it scalable? Therefore, for the superconductor-semiconductor-based material platforms, choosing the right semiconductor materials is the crucial first step. For instance, silicon (Si) is the material that has dominated the semiconductor industry for decades. The technology for fabricating Si-based devices is very mature and scalable, as we have seen in modern electronics nowadays. Additionally, we can include the advantage that Si is the second most abundant material (27.2 percent by weight in the Earth's crust) [44]. However, when it comes to hybrid S-Sm devices, fabricating robust Si-based JoFET devices is found to be challenging due to low Si-superconductor interface transparency [45]. On the other hand, III-V materials are favorable for hybrid S-Sm devices due to their high mobility [46, 47] and superior S-Sm interface quality [47–49]. These result in several realizations on indium-arsenide (InAs)-based gatemon [13–15, 21, 50–54]. Nevertheless, scaling up could be more of a problem for III-V materials.

Considering the information above, germanium (Ge) can be a promising candidate for scalable quantum computing. Standing from a technological point of view, Ge has already been used in several complementary metal-oxide semiconductor (CMOS) devices with mature technology built around it. From a physics point of view, Ge has several advantages for realizing good S-Sm-S junctions: having high hole mobility and a low Schottky barrier, for instance. In this section, we elaborate on our interest in Ge as a potential material platform to host gatemons.

Germanium in CMOS industry

Transistors are one of the most important inventions of the 20th century. They are crucial components in all modern electronic devices. Historically, the first breakthrough in working transistors was realized on Ge [55]. However, the native oxide of germanium (germanium dioxide, GeO_2) is unstable and can be dissolved in water. This makes it harder to process and fabricate high-quality transistors. On the contrary, silicon dioxide (SiO_2) has superior material properties, which facilitate the design of metal-oxide semiconductor-field-effect transistors (MOSFET) [56] and CMOS technology widely used nowadays. This led to the shifting of the material choice for transistors from Ge to Si. The scalability of the technology has improved drastically since then, and the size of transistors has been reduced significantly to the scale of a few nanometers. Nevertheless, at the scale of nanometers, it reaches the point where scaling up by reducing transistors' sizes further can be very challenging, as the phenomenon at the atomic level can have a significant effect on transistors. This leads to finding an alternative for scaling up the electronic devices. Then, Ge-based transistors gain interest again due to their high hole mobility. This has the potential to build faster and lower-power microelectronic devices [57, 58]. Further, the development of the technology to grow high-κ dielectrics on Ge helps to get rid of the problem of Ge's native oxide and draw more attention to the material [59]. Additionally, Ge is compatible with growing on Si substrates, helping reduce the cost of Ge-based devices.

Material properties of germanium

From a physics point of view, Ge poses several advantages for applications in quantum information technology. First, Ge has the highest hole mobility among semiconductors. It sets the record for the hole mobility of 4.3×10^{6} cm^2/Vs [19] in epitaxial growth silicon-germanium (SiGe) heterostructure on Si substrate. While having high hole mobility is a kind of more favorable property in the quantum dot qubit-based community, it is observed that the higher hole mobility may result in a higher $I_C R_N$ product, the figure of merit of the S-Sm-S junction quality as well. This could be due to the fact that the high mobility implies fewer scatterings, and the scatterings can degrade the S-Sm interface [49]. Secondly, it has been found that the metal/Ge contacts show the Fermi level pinning close to the valence band for every metal [18]. This results in a low Schottky barrier at the metal/Ge interface, which facilitates the Andreev reflection and the proximity effect. Moreover, this helps make realizing good ohmic contacts on metal-Ge-metal less complicated [22].

Hybrid superconductor-semiconductor devices based on germanium

Ge is an appealing material for making a gatemon. The first step to achieving the gatemon is to make a gatetunable S-Sm-S junction, i.e., Josephson field effect transistor (JoFET). Several works have been published in recent years in an at-

tempt to realize and comprehend Ge-based JoFET devices. The first realization was made in Ge/Si nanowire (NW), which has been contacted with aluminum (Al) leads [60]. The device exhibits very high transparency with an impressive $I_C R_N$ product ($\approx$ 200 µV) almost in the same order as the superconducting gap. The recent development of well-controlled diffusion by thermal annealing also opens up the possibility of realizing a very short Al-Ge-Al junction [61, 62]. Additionally, one of the most recent advancements in hybrid Ge-NW devices would be the realization of a Ge-NW-based gatemon with a coherence time of 180 ns [63].

Nevertheless, in this thesis, we base our fabrication on the top-down approach of SiGe heterostructure, as it offers higher reproducibility with less constraint on device design. The demonstrations of JoFET on SiGe heterostructure have been progressing in recent years [20, 64] on SiGe heterostructure with a strained-layer Ge quantum well. While the first realization on this platform has the $I_C R_N$ product significantly lower than that of NW-based JoFET, the most recent study on Ge JoFET on SiGe heterostructure shows significant improvement on the $I_C R_N$ product ($\approx$ 50 µV for Al-Ge-Al and $\approx$ 360 µV for Nb-Al-Ge-Al-Nb) [65]. Further, several JoFET-related devices, i.e., SQUIDs [20, 65] and superconducting quantum point contacts [66], have been demonstrated on the heterostructure platform as well.

In conclusion, the material properties—high hole mobility and low Schottky barrier, for instance—of Ge, as well as its CMOS compatibility, draw interest in developing hybrid S-Sm devices based on Ge for quantum information applications. There have been several remarkable advancements in recent years, yet there is still a lot of room for study and improvement. One of the main goals of this thesis is to realize Ge gatemon on the SiGe heterostructure platform.

CHAPTER 2

Device fabrication

We cannot do an experiment if we do not have a device. In fact, device fabrication took a large portion of time and effort in this thesis work. In this chapter, I will present hands-on practical work to realize the devices: aluminum-germanium-based Josephson Field Effect Transistors (JoFETs) and superconducting quantum interference devices (SQUIDs), to be specified. The chapter will begin by reviewing our material platform, which is a silicon-germanium (SiGe) heterostructure. Then, I will discuss each step of cleanroom fabrication, starting from the bare wafer to the final devices. Lastly, I will explain how to prepare the final devices to be ready for the experimental setup.

2.1 Silicon-Germanium heterostructure

The devices have been realized on the SiGe heterostructure platform [67]. The heterostructures are grown at **Laboratoire d'électronique et de technologie de l'information (LETI), CEA Grenoble** on 200-mm wafers. A schematic of the cross section of the heterostructure is shown in Figure 2.1. The heterostructure has been grown by the plasma-enhanced chemical vapor deposition (PECVD) technique. The first step of growth has been done on a silicon (Si) (001) substrate at 850 °C, and starts by the linear-grading technique to gradually increase the percentage of germanium (Ge) in the $Si_{1-x}Ge_x$ compound at a rate of 10% Ge/micron. When the Ge concentration reaches the designated value of x, the growth continues at the constant concentration for another 2.5 microns. The change in lattice

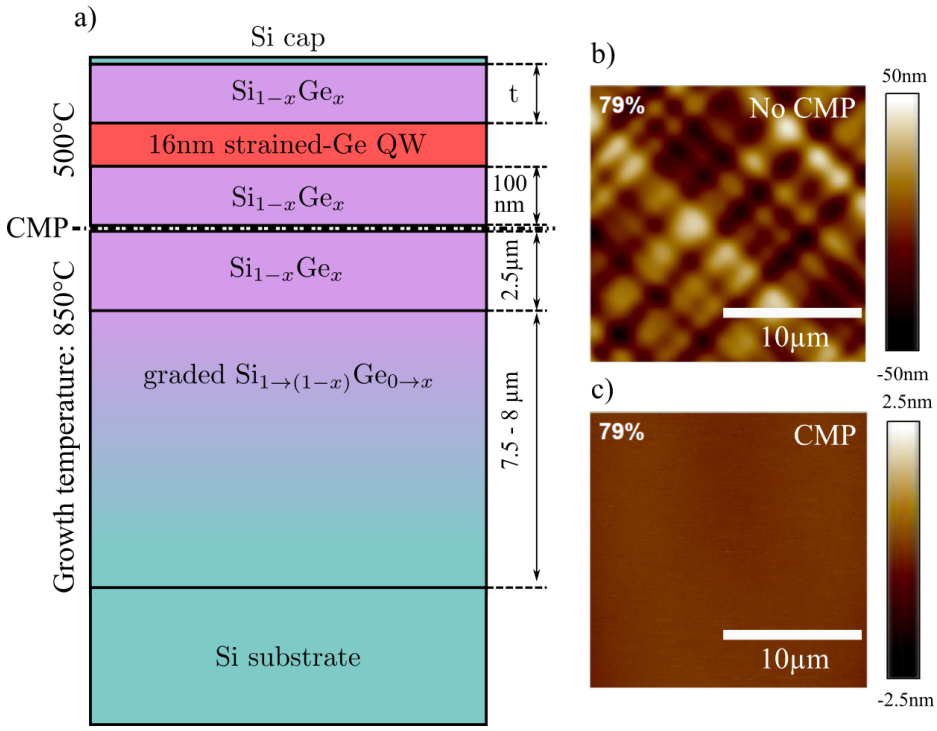

Figure 2.1 – **a**, Schematic diagram of the cross-section of the SiGe heterostructure grown on the Si substrate. The thickness of the upper SiGe layer is labeled as t and the concentration of the Ge in the SiGe layer is labeled as x. **b (c)**, AFM image of the surface of $Si_{0.21}Ge_{0.79}$ after the first step growth at 850 °C **without (with)** a chemical mechanical polishing (CMP) step. Subfigures (b) and (c) are reproduced from [67].

constant causes strain to accumulate in the growth layer. This results in a cross-hatch pattern observed on the surface. For this reason, a chemical and mechanical polishing (CMP) has been implemented on the wafer to reduce the surface roughness and get rid of the cross-hatch pattern. The atomic force microscoping (AFM) images in the subfigures on the right show the disappearance of the cross-hatched pattern after the CMP.

Following that, the wafer is moved to the PECVD machine for the second-step growth at 500 °C following the CMP. During this stage, an under layer of $Si_{1-x}Ge_x$ of around hundreds of nanometers in thickness is grown on the surface. Following that, 16 nm of a pure Ge layer is deposited. Over the Ge layer, the upper layer is grown to form the quantum well heterostructure. The Ge quantum well is compressively strained due to the mismatch in lattice constant between the Ge (5.66 Å) and the SiGe (5.61 Å). Finally, the heterostructure is capped by the 2 nm of the Si layer to prevent the formation of a complex oxide of SiGe.

In terms of electronic properties, Figure 2.2 shows the hole mobility as a func-

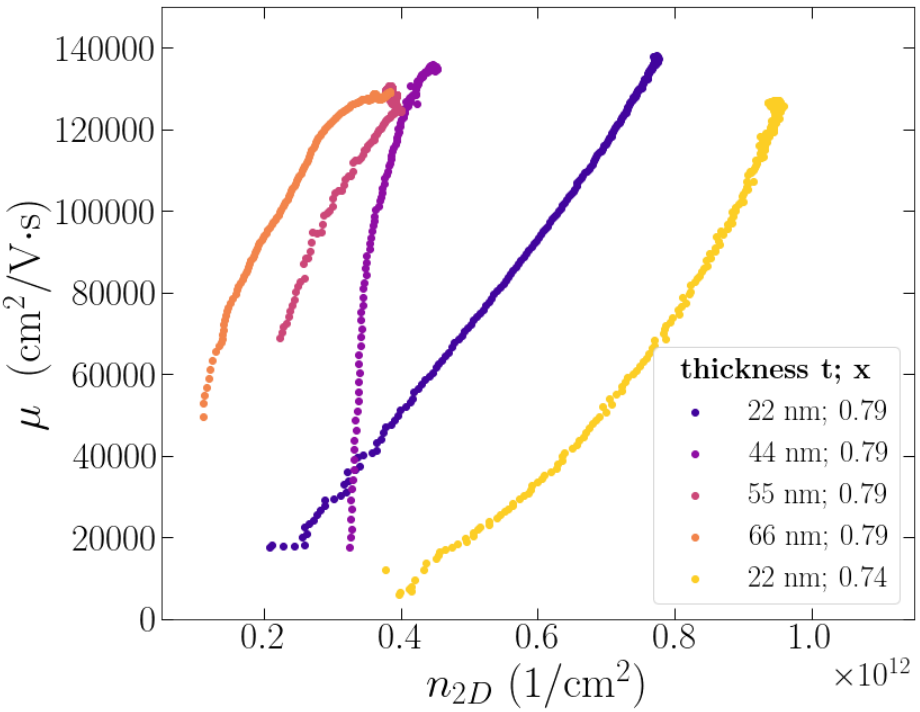

Figure 2.2 – Hole mobility (μ) as a function of the two-dimensional carrier density (n_{2D}) obtained from the Hall measurement. The plot shows the data from the Hall bars made in the wafers of the SiGe heterostructures with the different concentrations (x) and the different thicknesses (t) [E. Kiyooka, a doctoral student in the lab].

tion of the carrier density of the SiGe heterostructure with different upper layer thicknesses t, and Ge concentration x, measured at 4.2 K [E. Kiyooka, a doctoral student in the lab]. The devices studied in this thesis are fabricated from the heterostructure with $t = 22$ nm and $x = 0.79$, which has a hole mobility of 140000 cm^2/Vs at the carrier density of $8\times\ 10^{11}$ cm^{-2}. To give an idea, the state-of-the-art reported value of the hole mobility in Ge/SiGe heterostructures is around 4300000 cm^2/Vs [19].

2.2 Device fabrication

Fabrication plays an important role in this thesis, and our goal is to obtain a reproducible fabrication recipe of working devices. The first step in the fabrication is to make a design of the devices. Then we create create the lithography pattern with the corresponding cleanroom processes. The lithography pattern is created in the Graphic Design System (GDS) format with multiple layers. The main cleanroom processes can be broken down as follows:

1. Sample preparation and alignment marker
2. Mesa etching
3. Ohmic contacts
4. Insulating layer deposition
5. Gate deposition

An example of a GDS file for fabricating JoFETs and SQUIDs is shown in Figure 2.3. The design has been made to fit a chip with a size of 1×1 cm^2.

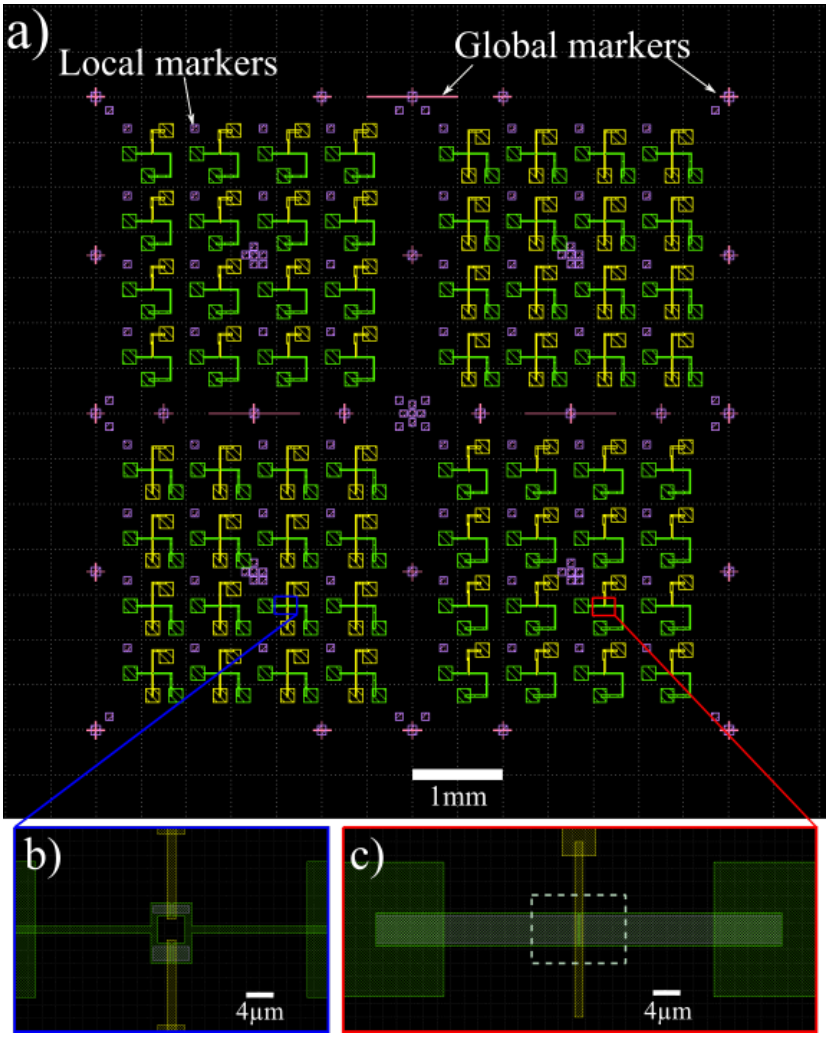

Figure 2.3 – **a**, GDS design contains global markers, local markers, and devices (JoFETs and SQUIDs). Global markers are on the side and are used for associating the chip coordinate with the GDS coordinate. Local markers are located next to each device. **b**, an example of SQUID's design with two junctions in parallel. **c**, an example of JoFET's design with one junction

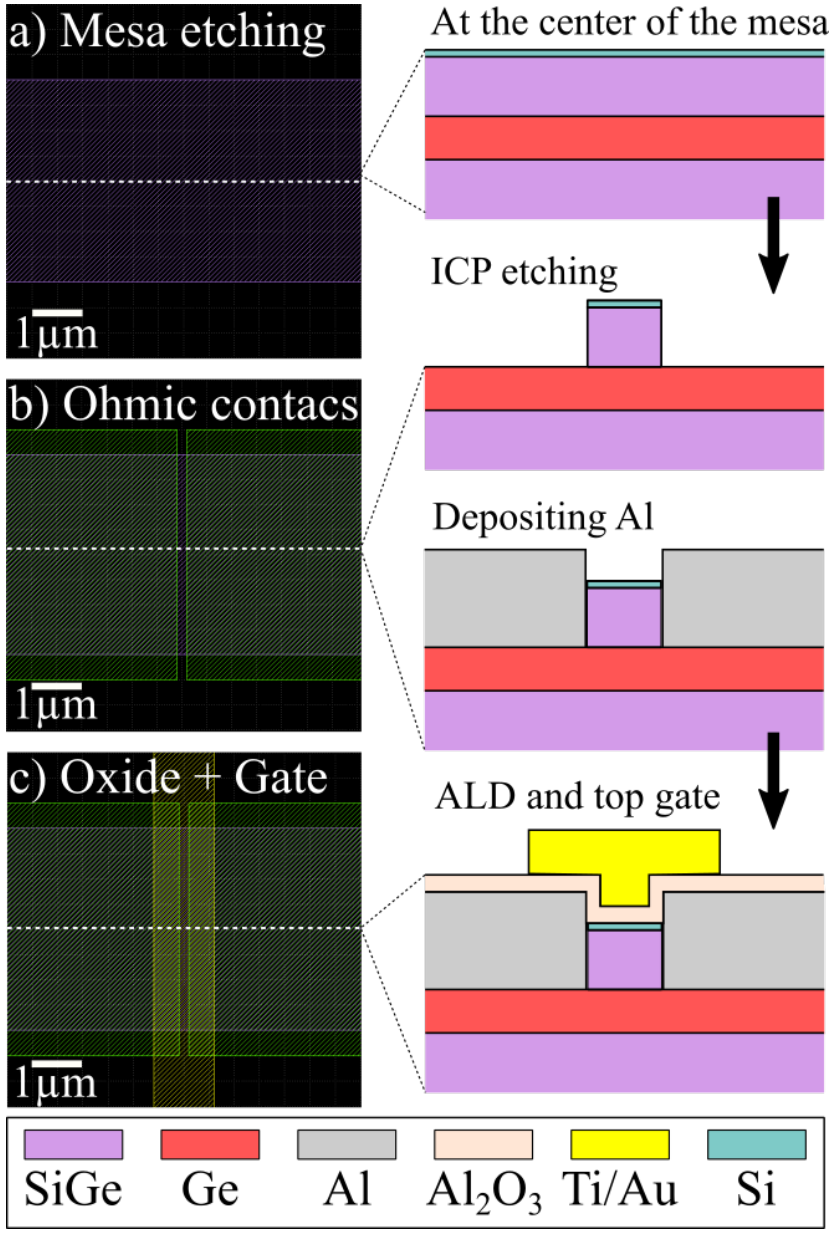

Figure 2.4 – Schematic diagram of the process flow of the fabrication. The white dashed lines represent the line-cut of the schematic of the cross section. The color box at the bottom shows the color representation of the material in the cross section. The process flow consists of: **a)** mesa etching, **b)** ohmic contacts, and **c)** depositing oxide and gate.

Generally, we leave an empty space a few millimeters inward from the 1×1 cm^2 border as the lithography resist is not uniform there. There are two sets of markers:

global markers are for locating the center of the chip, and local markers are for performing the fine alignment for each device. The figure shows the design of 32 JoFETs and 32 SQUIDs with four lithography layers.

Figure 2.4 shows schematics of the device fabrication. First, the mesa pattern is exposed with a negative resist, and the heterostructure is etched down to below the Ge QW. In the second step, the ohmics are defined using a positive resist that is used for both the etching of the upper SiGe layer and the Al deposition and lift-off. The entire chip is then covered by a thin insulating layer grown by the ALD technique. Lastly, the patterning and metal deposition of the gates comprise the final fabrication steps.

The fabrication has been done and characterized with academic cleanroom facilities in **Plateforme Technologique Amont (PTA), CEA Grenoble** and **Plateforme Nanofab, Institut Néel**.

2.2.1 Cleaving and markers

Usually, I make a GDS design for the lithography mask with a size of either 1×1 cm^2 or 2×1 cm^2. We process the fabrication steps on a chip with a size that is slightly bigger to avoid the resist non-uniformity around the corners. The chip is cleaved from the 200-mm wafers using a diamond pen or a diamond wafer scriber. For preparing the clean surface, we put the cleaved sample into a beaker filled with acetone in an ultrasound bath for 5 minutes. Following that, we transfer the chip to a beaker filled with isopropanol (IPA) in an ultrasound bath for another 5 minutes. After that, we blow dry the chip with a flow of nitrogen gas. Then, we check the surface with an optical microscope. If the surface is clean, we apply PMMA 4% electron beam resist to the sample and expose the sample with electron beam lithography techniques. Then we deposit gold, with titanium as an adhesion material [68], (Ti/Au) as a marker layer. The thickness of the marker layer affects the signal intensity for marker detection. We found that 3 nm of titanium (Ti) sticking layer and 77 nm of Au are enough for marker detection. Generally, we keep the metal thickness under 1/3 of the resist thickness (270 nm) to make the lift-off easy to do. The left optical microscoping image in Figure 2.5 shows an example of a clean surface with markers. Sometimes, if the surface of the cleaved chip is not cleaned after we apply the cleaning processes, we implement the cleaning steps again. If it does not improve, we consider discarding the chip as it may affect the devices' performance (especially big devices like resonators). The right image in Figure 2.5 shows an example of a surface we considered not clean. There are several black spots on the surface. These can be due to wafer defects, damage from cleaving, or scratches from chip handling. From our experience, we try to avoid using the edges of the wafer since these regions are most likely to have a greater density of visible black spots.

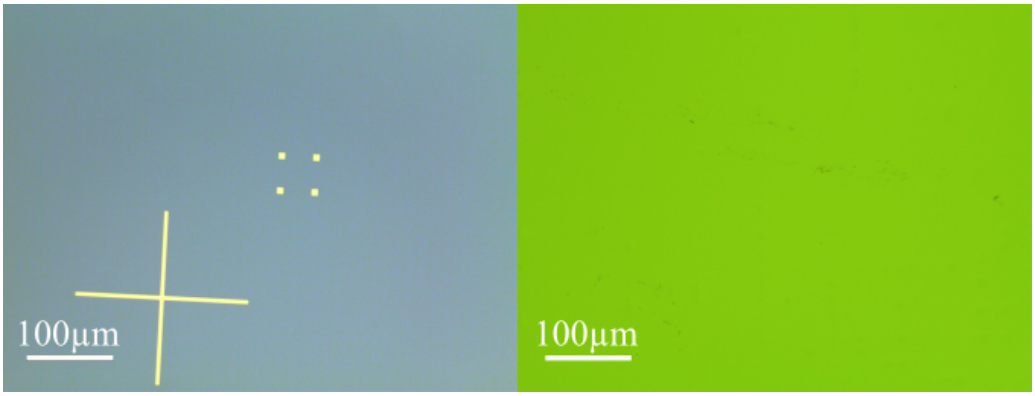

Figure 2.5 – **(left)** Optical images of the surface of the chip with marker. **(right)** An example of "unclean" surface. If we observe this kind of surface during this step, we try to re-clean or discard the chip.

2.2.2 Mesa etching

Mesa etching is a step to etch structures in the shape of mesas. The purpose of this step is to prevent conduction in two-dimensional hole gas (2DHG) between each device. The etching depth (the mesa height) has to be greater than the total thickness of the upper layer (22 nm) and the quantum well (16 nm). At the same time, when the etching depth is higher, we will need a greater thickness of the gate layer to overcome the mesas without discontinuity. In this thesis, we aim for an etching depth of 55 nm to make sure that the 2DHG layer outside the device is completely etched. This thickness is decided while taking into account the variation of the thickness on the etching and measuring the thickness with a profilometer. In the beginning, we made an attempt at this step with the wet etching method. Later, we switched to the dry etching approach and used this technique to realize the devices. Between the two techniques, we found that dry etching was more suitable for our work in terms of controllability and reproducibility. Please note that some of the etching optimization I show in this subsection has been done on a 4-inch wafer of $Si_{0.2}Ge_{0.8}$ heterostructure grown at TU Delft [69]. The wafer has an upper layer of 22 nm and a quantum well of 16 nm, similar to the wafer that we used for realizing the devices. The main difference in the growth process is that this wafer employs a reverse grading technique to grow the buffer layer. Nevertheless, we found similar results on the dry etching in terms of the etching depth and the surface profile, at least in the etching range of our interest (under 100 nm).

Wet etching

Wet etching utilizes chemical solutions as etchants. In the wet etching method, the wafer with the patterned resist is placed in a beaker of etching solution and

agitated for a fixed amount of time. In general, wet etching gives an isotropic profile. However, anisotropic wet etching is possible with a certain selection of etchants with respect to the material and crystal plane of the wafer. We performed the wet etching with a solution of HF:HNO_3:H_2O [70] in the proportion of 20:52:40. The solution mixture is prepared at least one day before the etching and is used within one week after the preparation. This etching recipe has been used for realizing JoFETs in our group previously [20]. In the etching process, three beakers are prepared. The first beaker is filled with the solution mixture. The other two are filled with deionized water. The process starts by patterning the photoresist on a sample. Then, the sample is put in the first beaker for a certain amount of time. The time the sample staying in the first beaker defines the etching thickness. After that, the sample is moved to the second beaker and the third beaker for 15 seconds and 120 seconds, respectively, to stop the reaction. To finish the process, we make the sample dry with a flow of N_2.

Here, we show the result of a wet-etched sample of a 1×1 cm^2 piece of $Si_{0.2}Ge_{0.8}$ heterostructure. The sample was coated with Man2403 photoresist, and patterned with electron beam lithography technique. The lithography pattern is an array of mesas of various sizes. The etching was performed by leaving the sample in the first beaker for 90 seconds. The rest of the process is as mentioned in the previous paragraph. The surface morphology of two mesas fabricated by wet etching is shown in Figure 2.6. The lithography mask of the mesa in the left (right) figure is expected to be 500 nm (3 µm). From the figure, we assume that the central lines are the etched mesa. It indicates that the width of the mesa done by the wet etching is less than the designed width. Further, bands of debris are observed on both sides of the mesa.

As a result, there are approximately 300–400 nm variations between the final and the designed width of the mesa. This can be a problem if we want to define the junction precisely. Further, it can be complicated to realize the junction with

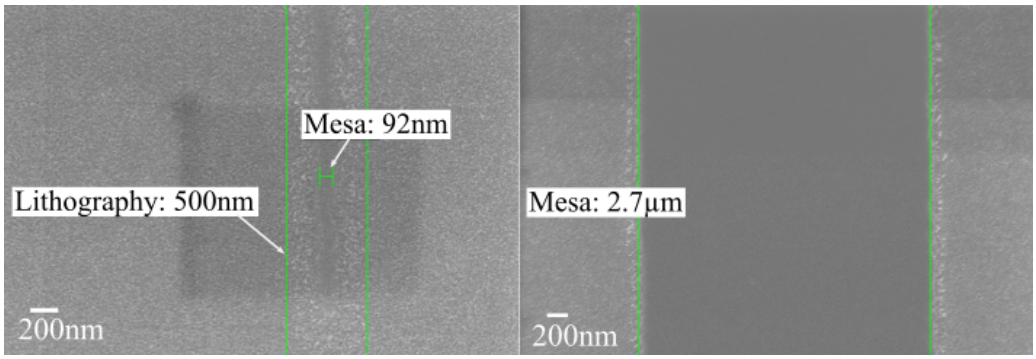

Figure 2.6 – SEM images of the mesa fabricated by the wet etching using a solution of HF:HNO_3:H_2O in the proportion of 20:52:40. The mesa in the **left (right)** image is desiged to be **500nm (3µm)** wide.

a junction length shorter than 500 nm. Additionally, the reproducibility of this method also depends on the person who performs the etching, the condition of preparing and storing the etchants, and many other factors. For these reasons, we decided to study the mesa etching with another approach, which will be shown in the following section.

Dry etching

Dry etching technique removes layers of materials from a wafer by bombardment with ions or plasma. The dry etching technique used in this thesis is reactive-ion etching (RIE), where the plasma of the reactive gases is generated by inductive coupling of the plasma to the radio frequency [71]. For this reason, this etching technique is also called inductively coupled plasma (ICP) etching.

The goal of the etching optimization is to obtain a reproducible etching recipe with an acceptably clean surface. In Figure 2.7, we show the result of several different etching recipes we used in the thesis.

- Initially, there was an etching recipe based on Cl_2:O_2:N_2 with a flow rate of 50:5:12 sccm. This recipe was used in our group to etch $Si_{0.2}Ge_{0.8}$ at a rate of 42 nm per minute [72]. We performed the etching with this recipe on a patterned chip with a size of around 1×1 cm^2 for 2 minutes. However, we found that the etching depth is around 20 nm, which is much lower than we expected. We took the same chip into the chamber and continued the etching for another 2 minutes, and the etching depth was still at 30 nm. From the tilted-angle SEM image (Figure 2.7(a)), the surface morphology shows many pillar-like structures. The pillar heights are comparable to that of the mesa. Our explanation is that the 2 nm Si top layer is oxidized, and this recipe does not etch the SiO_2 smoothly. It results in partially etched SiO_2 by the mechanical means of the plasma. Then the unetched SiO_2 acts as a hardmask for the layer underneath.
- Following that, we add another step of CF_4 gas into the process since the fluorine-based plasma is known for its SiO_2 etching ability [73, 74]. Figure 2.7(b) shows the cross section of the etching result using two-step etching with 10s of CF_4 followed by 5 minutes of Cl_2:O_2:N_2. We observed pyramid-like structures on the etched surface.
- Then we tried to simplify the etching process by using only one etching step. The result shown in Figure 2.7(c) is obtained from etching with 10 s of CF4 at an ICP power of 1000 W and a bias power of 100 W. We noticed a smoother surface with the etching depth in the good range ($\approx$ 100 nm). However, the issue with this recipe is the too-high etching rate (approximately 10 nm/s). This can lead to difficulty controlling the etching depth under $\pm$20 nm precision.
- We used the etching with CF_4 as a starting point. To obtain lower etching rate, we dilute the CF_4 with Ar, and reduce the ICP power and bias power.

Figure 2.7(d) shows the result of the heterostructure etched by 10 sccm of CF_4 and 40 sccm of Ar with an ICP power of 200 W and bias power of 25 W for 30 seconds. From the image, it shows the etching profile and the etched surface comparable to previous recipe. Nevertheless, the etching rate become lower (approximately 2.3 nm/s).

The etching recipe used on the sample in Figure 2.7(d) is the recipe that we use in etching layer of the heterostructure for fabricating the devices in this thesis, both in the mesa etching and the ohmic contacts steps.

2.2.3 Ohmic contacts

This fabrication step is performed to make contact between superconductor materials and the germanium quantum well. S-Sm-S junctions are formed in this step. First, we perform the lithography using a positive ZEP520A resist. The choice of this resist is motivated by the fact that it can withstand a few seconds of

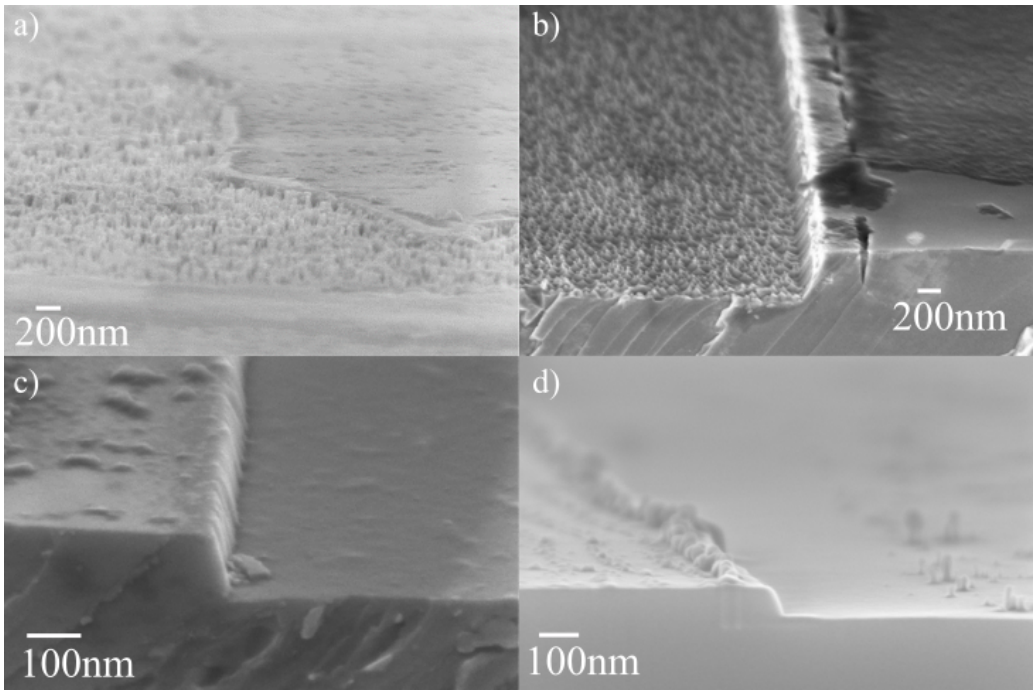

Figure 2.7 – Tilted-angle SEM images. **a**, Gas: 50 sccm Cl_2, 5 sccm O_2, 12 sccm N_2. ICP power 50 W/ bias power 20 W. Etching time: 2+2 minutes. **b**, Step 1) Gas: 50 sccm CF_4. ICP power 1000 W/ bias power 100 W. Etching time: 10 s. Following by step 2) Gas: 50 sccm Cl_2, 5 sccm O_2, 12 sccm N_2. ICP power 50 W/ bias power 20 W. Etching time: 5 minutes. **c**, Gas: 50 sccm CF_4. ICP power 1000 W/ bias power 100 W. Etching time: 10 s. **d**, Gas: 10 sccm CF_4, 40 sccm Ar. ICP power 200 W/ bias power 25 W. Etching time: 30 s.

ICP etching while leaving sufficient resist thickness for the lift-off process. After that, we perform an ICP etching step to expose the Ge quantum well layer. After several attempts, we found that it gives the best result if we stop the etching just above the quantum well layer. Following this step, we transfer the chip from the ICP chamber to a metal evaporator. The transfer process should be fast (typically less than 5 minutes) to minimize the oxidation of the etched surface. Additionally, we perform an in-situ etching with Ar plasma in the deposition chamber prior to the metal deposition. The in-situ etching is for removing the native oxide and the residue forming on the Ge surface. The metal deposition is made by evaporating the metal target with a high-energy electron beam. The metal is then evaporated and deposited on the sample. The deposition angle is set to be zero. In other words, the metal target is facing directly at the sample. The sample is rotating during deposition to compensate for the inhomogeneity due to a possible small angle deviation. Then, the metal outside the designated area has been removed by the lift-off process. Finally, the remaining resist residue has been removed by applying oxygen plasma to the sample.

2.2.4 Oxygen plasma

ICP etching can cause burned resist that is difficult to be removed by chemical solvents (acetone, and IPC). Applying oxygen plasma to the sample is an effective method to remove the remains of the burned resist. Figure 2.8(a) and (b) show optical images of the same sample after the mesa etching step. In the figure (a), there are several resist remains seen on the mesas as the dark patches. These patches are removed after 6 minutes of oxygen plasma, as shown in the figure (b). SEM images in Figure 2.8(c) and (d), taken after the ohmic contacts step before (c) and after (d) applying the oxygen plasma, show the disappearance of the black dirt around the junctions and deposited Al. It demonstrates that the method is effective in removing the remaining of ZEP520A after etching and lift-off as well. However, we notice that there are black dots present on Al after applying the plasma. We think that these are the etching residues covered by Al. They became more visible due to the heat generated by the oxygen plasma.

2.2.5 Carrier wafer for etching

There is one important remark on the ICP etching step, relating to both mesa etching and ohmic etching. The ICP machines in the PTA cleanroom are compatible with a 4-inch wafer platform. Since our samples are a few cm^2 in size, we need a carrier wafer. There are two approaches we would like to discuss.

Wafers with holes With this approach, we cut holes in a 4-inch unpolished Si wafer using laser cutting techniques. The holes match the size of the sample. We glued the wafer with holes to another unpolished 4-inch Si wafer by using Crystalbond on a hot plate at 65 °C. Then we remove the wafers from the hot plate and wait until they are cooled off. To perform the etching, we put the

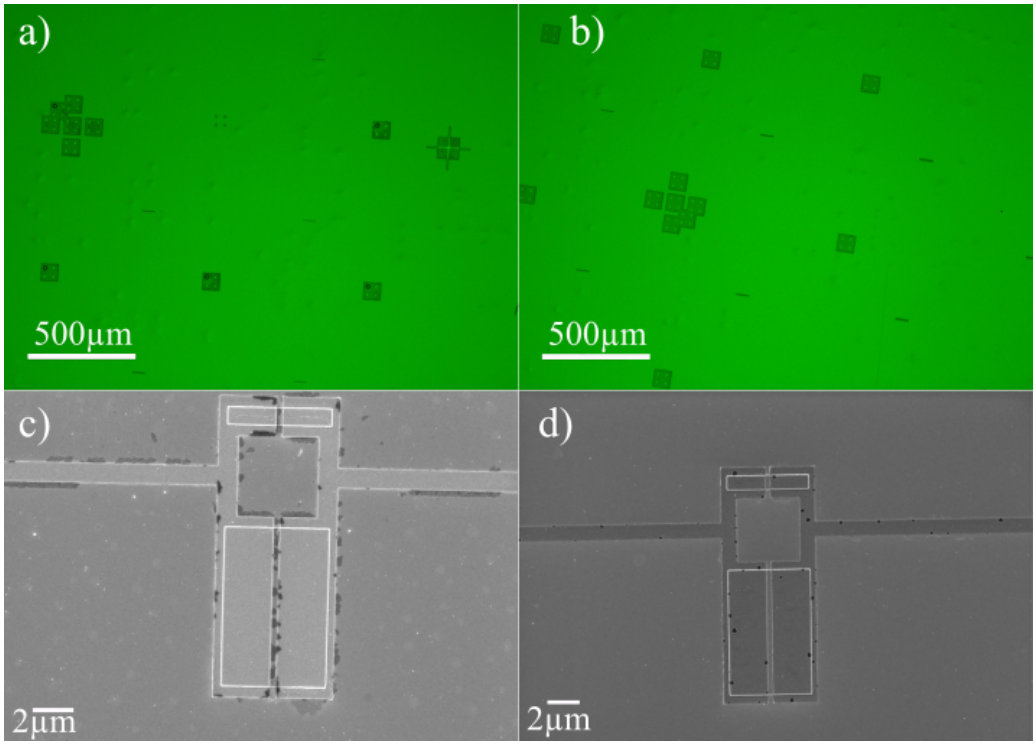

Figure 2.8 – The figure shows an effect of applying 6 minutes of oxygen plasma to the sample. **a (b)** Optical image of the sample, after the mesa etching step, taken **before (after)** applying the oxygen plasma. **c (d)** SEM image of the sample, after the ohmic contacts step, taken **before (after)** applying the oxygen plasma. They show the removal of the black patches and dirt.

samples in the holes. The sample will be kept in place during the pumping and loading of the etching machine. This approach makes it simple to load and unload the sample. However, the main drawback of this approach is thermal regulation. To give an explanation, the etching temperature during the process is maintained by a flow of helium on the back side of the carrier wafer. Putting the sample without an adhesion layer will not give good thermal contact between the sample and the carrier wafer. This results in variations in the etching rate and the final etching depth. It is crucial to have reproducible etching depth for making good ohmic contacts.

Adhesion layer Alternatively, we can adhere the sample to a 4-inch unpolished Si wafer, a carrier wafer, with an adhesive material. We test the fabrication on two kinds of glue: **Crystalbond**, and **Cool-Grease (CGR7016)**. Figure 2.9 shows SEM images of the junction part in two devices taken after the ohmic contacts step. During the etching, the sample in the left image was glued by Crystalbond, while the sample in the right image was glued by CGR7016. From the images, qualitatively, we found that using CGR7016 as

an adhesive material to glue the etching sample to a Si carrier wafer results in less dirt and a cleaner overall surface of the chip. We did several etching tests with CGR7016, and they yielded reproducible results.

As it produces a reproducible result with an acceptably clean etched surface, the CGR7016 is used in the final fabrication recipes for every etching step of the devices present in this thesis (JoFETs, SQUIDs, resonators, and gatemon).

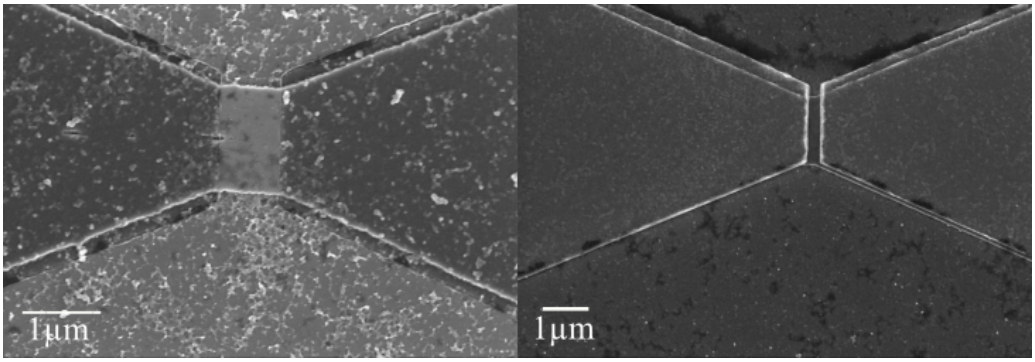

Figure 2.9 – SEM images of the devices, zooming at the junctions, taken after the ohmic contacts step. The junction in the **left (right)** image has been etched by gluing the sample to a Si carrier wafer using **Crystalbond (CGR7016)** as an adhesive material. The rest of the etching process is similar.

2.2.6 Insulating layer deposition

The insulating layer has been grown by the plasma-enhanced atomic layer deposition (ALD) technique. In my thesis, we grow 10 nm of Al_2O_3 as an insulating layer. Before the ALD growth, the sample is pre-treated with 10 minutes of O_2 plasma in the growth chamber. The growth has been done over 108 cycles. Each growth cycle consists of a pulse of trimethylaluminium (TMA, $Al(CH_3)_3$) precursor followed by an exposure to oxygen plasma. The growth temperature during all the processes is 280 °C, which is the limit of the ALD machine. Due to the growth temperature, we expect to have a thermal annealing effect between Al and Ge during this growth process [20, 64], which which can favor the ohmic behavior of the Al contacts in our junctions. We have not observe oxide leakage in the range of the gate voltage of ± 4 V in our devices fabricated with this ALD recipe.

2.2.7 Gate deposition

Gate is a component used for accumulating or depleting hole carriers in 2DHG by electrostatic means. We use the top gate approach by depositing a metal strip on the Al_2O_3 layer right over the S-Sm-S junction. This metal strip is connected to a bond pad in the same layer. The challenge of this step is finding the right thickness for the gate. We need to have enough thickness for the gate to crawl

up the mesa. In the same time, the thickness has to be thin enough to be able to perform the lift-off. In the final fabrication recipe, we deposit 10 nm of Ti and 130 nm of Au as a top gate layer.

2.2.8 Proximity effect in electron beam lithography

We observe a difference in the size of the fabricated devices with respect to the design. Generally, we found that the dimension of the exposed area was larger than the design. One possible explanation is the proximity effect in electron beam lithography [75] (not to be confused with the superconducting proximity effect). The proximity effect is due to the scattering of the electron beam outside the area of exposure. It causes the resist to be exposed slightly outside of the designed area. Figure 2.10 shows SEM images of two junctions. The mesa of the first junction is designed to be 4 µm wide. The junction separation is expected to be 200 nm. In the right image, the junction is designed to have a 150-nm separation. The widths of the Al and the mesa are designed to be 9 and 8 µm, respectively. As we use the negative resist for the mesa etching and the positive resist for the ohmic contacts step, it shows the increase in size of the structure with respect to the area of exposure in the design, and matches the explanation of the proximity effect. Quantitatively, we find an extra 40 nm increase in size. From this information, it can be complicated to make a junction under 100 nm separation reproducibly.

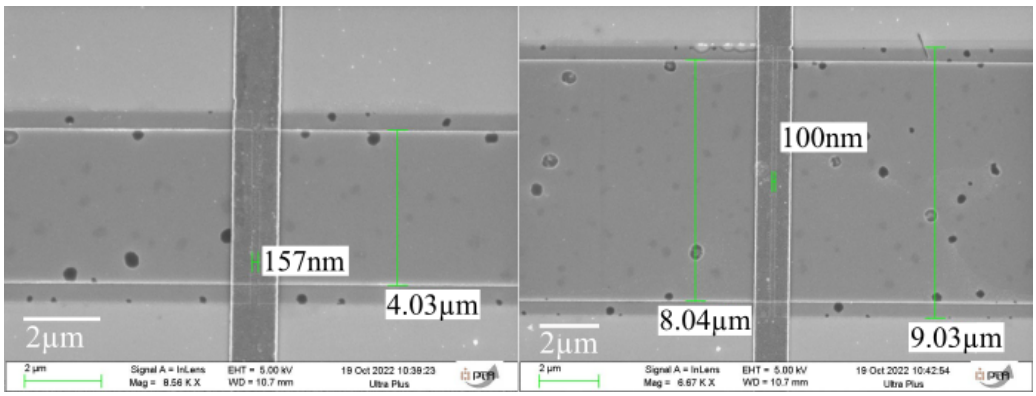

Figure 2.10 – SEM images of the junctions in the fabricated devices. The left junction is designed to be 4 µm wide with a 200-nm separation. The right junction is designed to be 8 µm wide with a 150-nm separation. 40 nm mismatches between the measured and the designed size are observed.

2.3 Sample preparation for measurements

After the fabrication, we need to prepare the devices for the measurement. In the measurement, the sample is attached to a daugtherboard PCB. The daugtherboard is connected to a motherboard, which is connected to the loom in the measurement setup. Figure 2.11 shows the step of preparing the sample to be ready for cooling down. Following the letter labeling, the steps consist of:

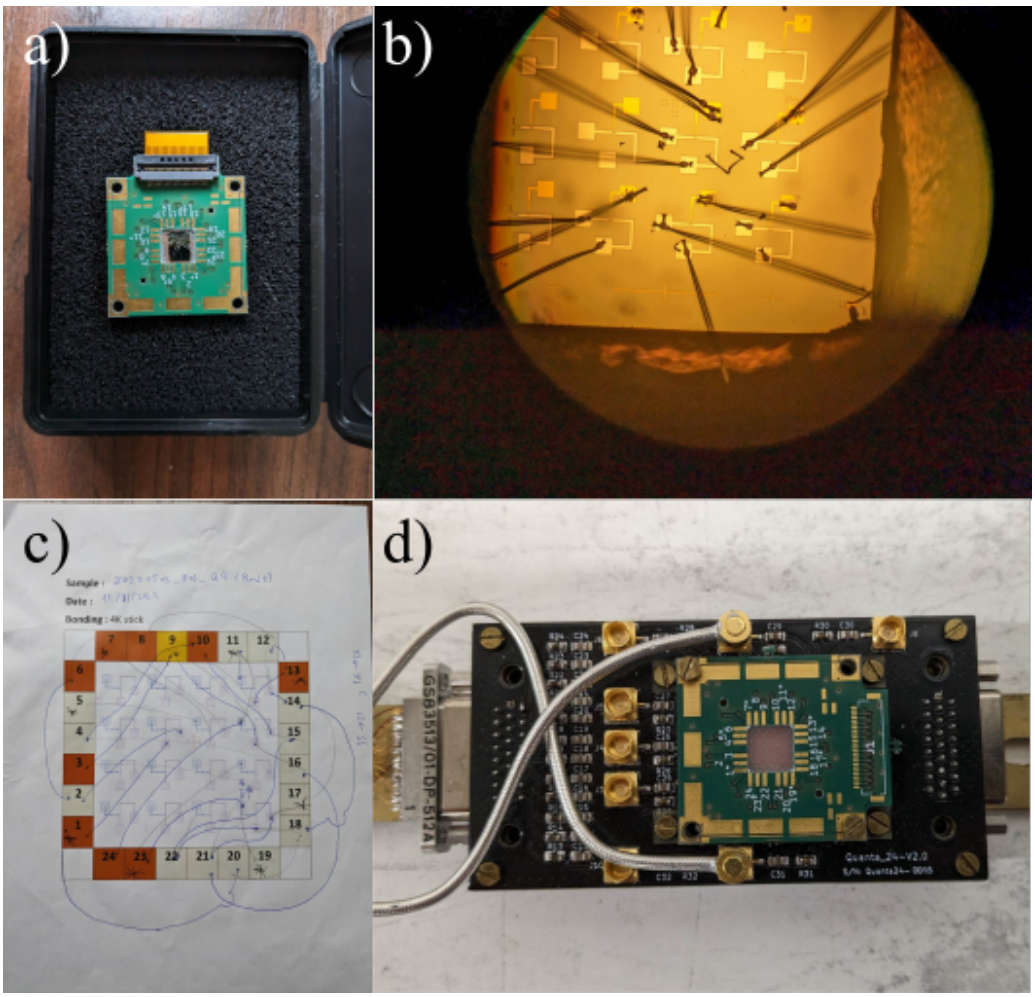

Figure 2.11 – The figure shows the sample at each step of preparation for cooldown: **a,** sample glued to a daugtherboard PCB. **b,** wire bonds between the sample and the PCB through the bond pads. **c,** a bonding schematic, **d,** a PCB mounted on a motherboard.

a, Cleave the fabricated chip into a size that can fit on a daugtherboard. Glue the back of the sample to an adhesive material (silver paint or epoxy), and put it on the daugtherboard. Wait for the glue to dry for an hour.

b, Make bonds between the bond pads on the chip and the bond pads on the PCB using ultrasonic wire bonding technique.

c, Make a schematic of the device bonding.

d, Mounting the daugtherboard (green) to a motherboard (black) in the setup.

Then, we encapsulate the motherboard in a vacuum chamber of the setup, and the sample is ready to be cooled down and measured at a low temperature.

The final fabrication recipes of the devices are presented in Appendix A.

CHAPTER 3

3

Josephson Field Effect Transistors

In this chapter, we focus on studying Josephson Field Effect Transistors (JoFETs). In principle, a JoFET is a transistor with superconducting leads and a sufficiently short junction length. Above the critical temperature (T_C) of the metal leads, it behaves as a normal transistor. At a lower temperature, the semiconductor channel is proximitized by the superconducting leads, which allows the transport of the supercurrent through a process called Andreev reflection. We start this chapter by reviewing the basic concepts of Andreev reflection and supercurrent. For the experimental part, firstly, we presented the results of basic transistor characterizations at 4.2 K. Then, we cooled the devices down below T_C, and studied the critical current-related effects, including gate dependency, temperature dependency, and Fraunhofer diffraction. Following that, we investigated the devices in the non-dissipative regimes, where we observed subgap features. In the section, we presented the study of the temperature dependency of the subgap features leading to the estimation of the superconducting gap. We also presented our attempt at studying the junction length dependency and magnetic field dependency of the subgap features.

3.1 Basic theoretical concepts

3.1.1 Superconducting gap, S-N interface, and Andreev reflection

A superconductor is a material that can conduct a current with zero resistance when it is cooled down below the critical temperature (T_C). First, when the

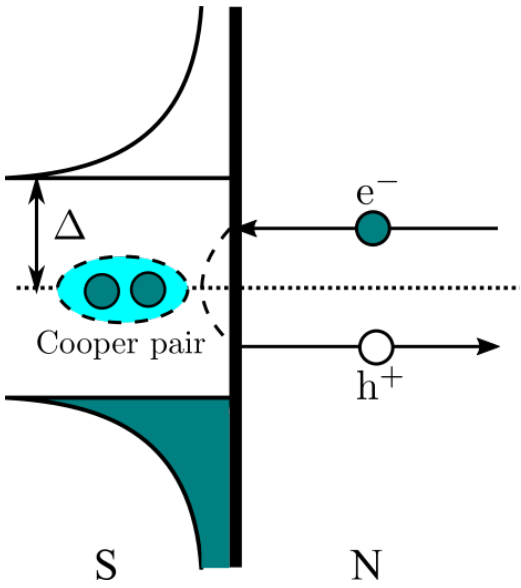

Figure 3.1 – Schematic of the energy band diagram of a superconductor-normal (S-N) interface. The figure shows the superconducting gap (Δ) in the density of states of the superconducting lead that open below T_C, and the quasiparticles (Cooper pairs, electrons, and holes) participating in the Andreev reflection process.

temperature drops below T_C, a superconducting gap (Δ) opens in the density of states of the superconducting leads, and charge carriers condensate into Cooper pairs at the Fermi level (left side, Figure 3.1) [27]. A Cooper pair consists of two coherent electrons that carry a non-dissipative supercurrent. When a normal semiconductor (N) is connected to a superconductor (S), an S-N junction is formed. When a carrier (an electron or a hole) inside the semiconductor travels to the interface inside the gap, the normal transmission is greatly reduced due to the non-existence of the energy state for single quasi-particles inside the gap. We might expect that the incident carrier can only be reflected back as the **"normal reflection"** of the quasiparticles with the potential barrier. In fact, there exists a second-order process called **"Andreev reflection"** [37, 38] that allows converting two charge carriers in the normal part into a Cooper pair in the superconductor. In this process, the electron is reflected as a hole at the interface. The charge is conserved, and a Cooper pair is added to the superconductor (see Figure 3.1).

3.1.2 The Blonder-Tinkham-Klapwijk formalism

In the real world situation, not every incident carriers leads to Andreev reflection. In 1982, Blonder, Tinkham, and Klapwijk proposed a theory to model imperfection of S-N interface and the effect on the transport event in the junction [16].

In the model of Blonder-Tinkham-Klapwijk (BTK) formalism (Figure 3.2), we

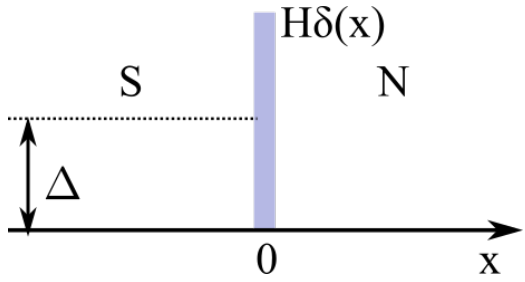

Figure 3.2 – Schematic diagram of the S-N interface according to the BTK model. The potential barrier of the barrier strength H describes the quality of the interface.

introduce a repulsive potential $H\delta(x)$ at the S-N interface, which represent real world effect that could degrade the interface, for example the oxide layer, the Schottky barrier, and the disorder at the interface. For simplicity, the barrier strength can be rewritten in the form of a dimensionless Z-parameter as:

$$Z = \frac{H}{\hbar v_F}, \tag{3.1}$$

where v_F is the Fermi velocity.

When an incident electron travels from the N side to the barrier, we consider three possible consequences: Andreev reflection, normal reflection, and transmission.

The expressions of $A(E)$, $B(E)$, and $T(E)$ derived from BTK formalism are shown in Table 3.1, and plotted in Figure 3.3.

Table 3.1 – Table lists the probability of Andreev reflection ($A(E)$), normal reflection ($B(E)$), and transmission (T). Here, $\gamma^2 = [u_0^2 + Z^2(u_0^2 - v_0^2)]^2$, and $u_0^2 = 1 - v_0^2 = \frac{1}{2}[1 + \sqrt{(E^2 - \Delta^2)/E^2}$. u_0, and v_0 are probability amplitudes of electrons and holes in a wave function of a superconducting state, respectively [16].

	A(E)	**B(E)**	**T(E)**
$E < \Delta$	$\frac{\Delta^2}{E^2+(\Delta^2-E^2)(1+2Z^2)^2}$	$1 - A$	0
$E > \Delta$	$\frac{u_0^2 v_0^2}{\gamma^2}$	$\frac{(u_0^2-v_0^2)^2 Z^2(1+Z^2)}{\gamma^2}$	$1 - A - B$

The barrier parameter is related to the parameter "τ" by the equation $\tau = 1/(1 + Z^2)$. The upper left panel in Figure 3.3 shows the probability of each event when there is no barrier ($Z = 0$) and the transparency is equal to unity. In

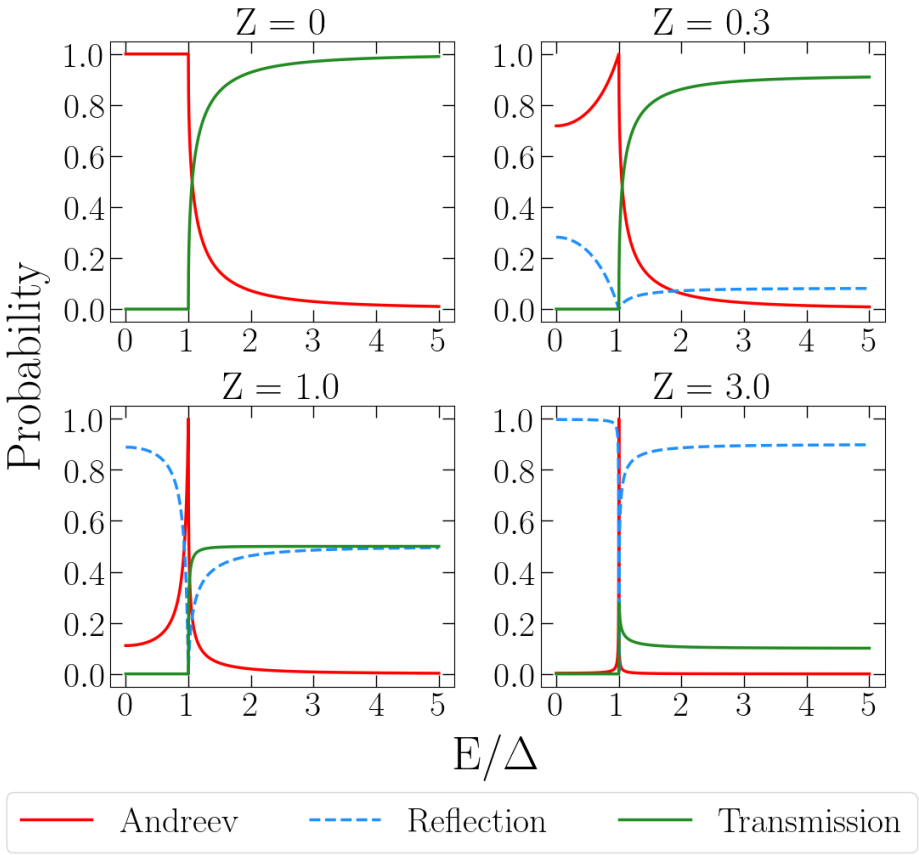

Figure 3.3 – Probability of the Andreev reflection (red), the Normal reflection (blue), and the Transmission (green) as a function of energy of an incedent particle with respect to the gap Δ at different values of the barrier parameter Z.

this case, all of the incident electrons inside the superconducting gap go through the Andreev reflection process without any normal reflection or transmission ($A = 1, B = 0, T = 0$). For incident electrons with energy above Δ, the probability of the Andreev reflection decreases as the energy of the incident electrons increases. On the contrary, in the case of the high barrier and low transparency limit ($Z = 3.0$ in the figure, for instance), the probability of the Andreev reflection is greatly suppressed, and most of the incident electrons are normally reflected inside the superconducting gap. Outside the superconducting gap in the non-zero barrier limit, the particle is partially reflected and partially transmitted, depending on the strength of the barrier. In every case, the total probability is conserved as $A(E) + B(E) + T(E) = 1$.

3.1.3 Andreev Bound States and supercurrent

Now, when the two superconductors are connected on both sides of the normal part as in Figure 3.4, an S-N-S junction is formed. In the figure, an incident electron is reflected as a hole on the right N-S interface. The reflected hole travels to the left S-N interface and is reflected as an electron traveling in the opposite direction. A cycle of this process removes one Cooper pair from the superconductor on the left and adds a Cooper pair to the superconductor on the right. This allows the transport of the Cooper pair through the S-N-S junction, which results in the non-dissipative supercurrent and zero-resistance state which can be observed in the measurement.

In the case of a short junction in the ballistic limit, the cycle of Andreev relections described above leads to the formation of the Andreev bound states that the energy depends both on the transparency τ and on the phase difference between the two superconducting contacts φ as [40, 41]:

$$E_A = \pm\Delta\sqrt{1 - \tau\sin^2\frac{\varphi}{2}}, \tag{3.2}$$

The supercurrent is then derived from these energy levels as [41]:

$$I_s = \frac{2e}{\hbar}\frac{dE}{d\varphi} = \frac{e\Delta}{2\hbar}\frac{\tau\sin\varphi}{\sqrt{1 - \tau\sin^2(\varphi/2)}} \tag{3.3}$$

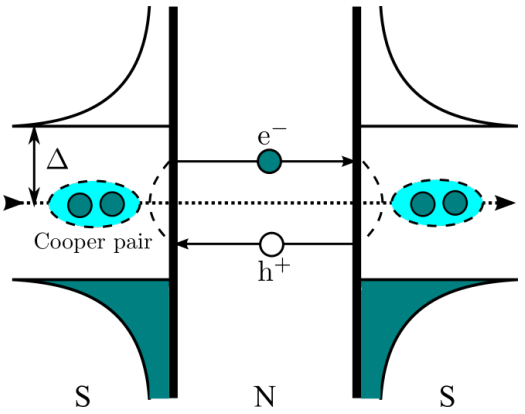

Figure 3.4 – Schematic of the energy band diagram of a superconductor-normal-superconductor (S-N-S) junction. The figure shows the superconducting gap (Δ) in the density of states of the superconducting leads that open below T_C, and the quasiparticles (Cooper pairs, electrons, and holes) confining in the Andreev bound states.

3.2 Devices description

We fabricated sets of JoFETs and SQUIDs using the lithography mask shown in Figure 2.3(a). Figure 3.5(a) is an optical microscope image of the fabricated chip, while Figure 3.5(b) displays a false-colored SEM image of a JoFET device. In the figure, two ohmic contacts made of Al are separated by a junction length denoted as "L." Beneath the Al layer, there is a 16-nm layer of Ge quantum well, acting as a proximitized layer. The width of the mesa of the Ge quantum well defines a junction width marked as "W." The schematic in Figure 3.5(c) illustrates the cross-section of the device along the green dashed line in Figure 3.5(b). The junction is formed by the deposited Al leads on top of the etched Ge quantum well. We conducted TEM analysis on one of the measured devices (labeled as "B2", see below). Figure 3.5(d) shows the TEM image of the contact interface in a fabricated device, revealing the direct contact between Al and Ge. Figure 3.5(e) presents TEM analysis of the device at the gate stack, where we measured L to be 169 nm, deviating from the intended design of 200 nm. We attribute this discrepancy to the electron beam proximity effect on the positive resist (ZEP520A). Figure 3.5(f) provides a zoomed-in image of the area within the maroon box in Figure 3.5(e). We confirmed the materials in each part of the stacks using the energy-dispersive spectroscopy (EDS) technique (see the Appendix C). Unexpectedly, we observed a layer of Al-O beneath the Si-O layer, indicated by the red arrow in Figure 3.5(f). We suspect that the Al from the Al leads diffused underneath the Si-O layer during the ALD process at 280°C. All the TEM images presenting here have been taken by J. L. Lábár and I. Levente at Institute for Technical Physics and Materials Science, Centre of Energy Research (EK MFA), Budapest, Hungary.

The lithography mask in Figure 2.3(a) comprises four quarters. In this study, we characterized devices in the upper-left and bottom-right quarters of the chip, which were cleaved separately. Each quarter contains JoFETs with various junction lengths. Both quarters were designed to be nearly identical. For ease of reference, we will refer to the set of devices in the bottom-right quarter as "Set A" (A1, A2, A3, and A4) and the top-left quarter as "Set B" (B1, B2, B3, and B4). The junction parameters of the measured devices are listed in Table 3.2.

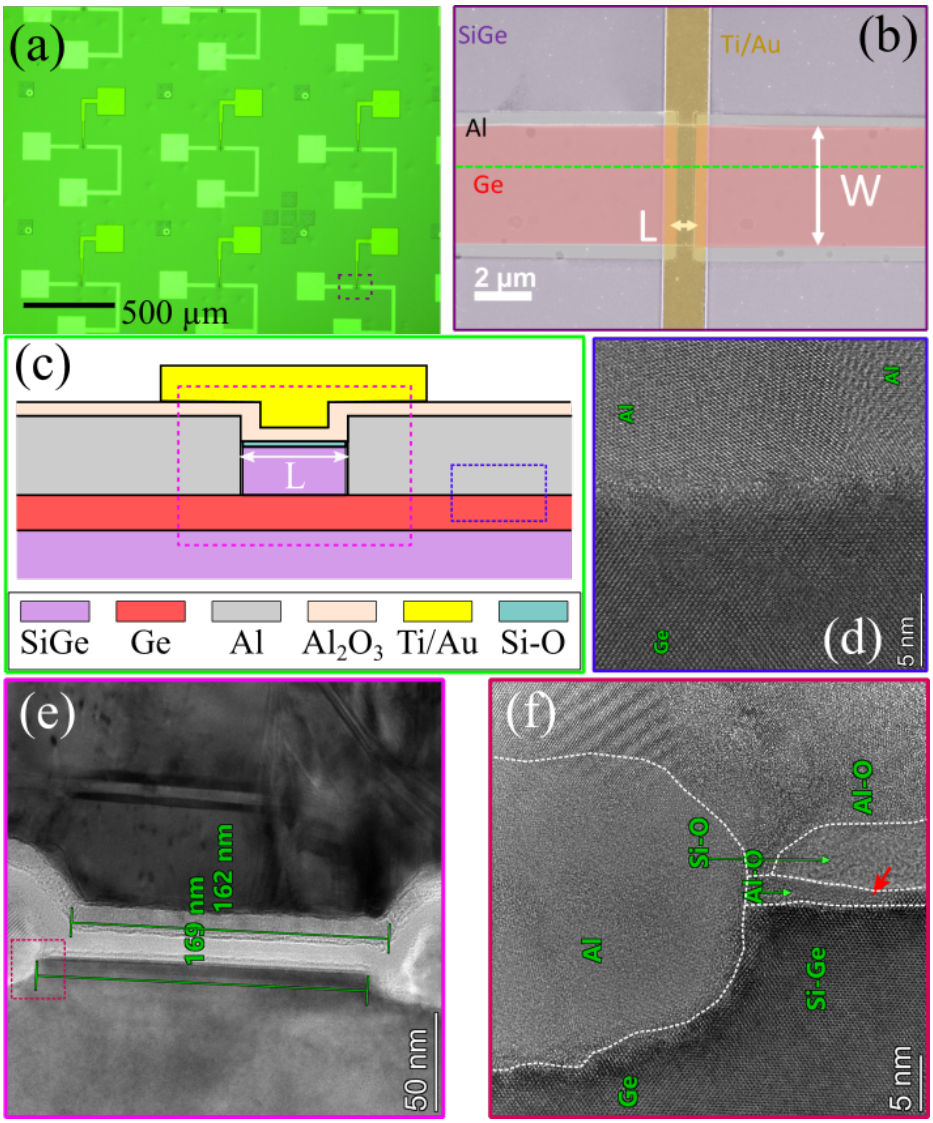

Figure 3.5 – (a) An optical microscope image of the chip we measured (b) a false-colored SEM image of a JoFET device at the junction showing Al leads on a Ge channel with a Ti/Au top gate. The junction length is defined by the space between two ohmic contacts (L), and the junction width (W) is defined by the lateral dimension of the mesa. (c) Schematic of the device A germanium quantum well (QW) (red) is capped between two barriers of SiGe layers (purple). The source and drain aluminum contacts (gray) are connected to the QW. (d) a TEM image of the area in the blue box in (c) showing direct contact between Al and Ge. (e) a TEM image of the area in the magenta box in (c) showing the gate stack. (f) a TEM image showing the zoom-in of the area in the maroon box in (e) showing the components of the gate stack. Subfigures (d), (e), and (f) are produced by J. L. Lábár and I. Levente [EK MFA, Budapest, Hungary].

Table 3.2 – Table lists the junction parameters (device labels, junction lengths (L), and junction widths (W) of the measured devices.

Device	**L (nm)**	**W (µm)**
A1	200	4
A2	300	4
A3	500	4
A4	150	8
B1	150	4
B2	200	4
B3	300	4
B4	500	4

3.3 Josephson FET as a transistor

3.3.1 Transistor characterization

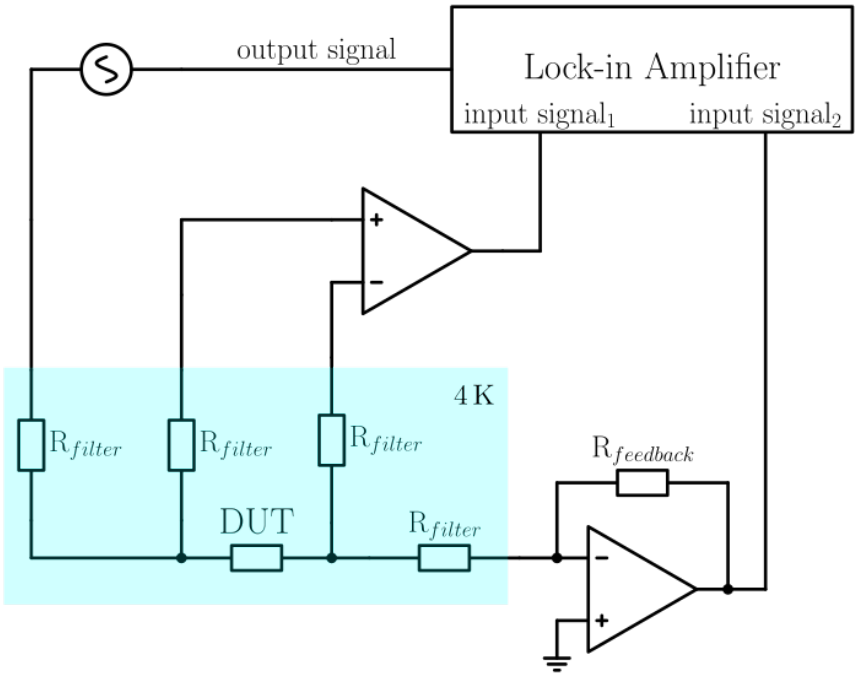

Figure 3.6 – Schematic diagram of the measurement set-up. The device under test (DUT) is connected to low-temperature low-pass filters. Each filter has a resistance of 2k Ω. The device has been measured with four-point measurement set-up with a lock-in amplifier by applying an alternating signal to the DUT and measuring the voltage drop across the device (input signal$_1$) and the current passing through the device (input signal$_2$) with a differential amplifier and a current-to-voltage converter, respectively.

To characterize the transistor characteristics, we have measured the conductance and the resistance of the device at 4.2 K which is above the critical temperature of aluminum. To measure the conductance at the zero source and drain DC bias voltage, we have used a lock-in amplifier operating at a low frequency (typically below 400Hz). From the lock-in amplifier, a small AC voltage is applied to the source contact of the device under test (DUT). The induced AC current (dI) passing through the filters and the DUT is recorded by a current-to-voltage converter, and the voltage drop (dV) across the DUT is measured by a differential amplifier. The conductance and the resistance are calculated from the measured dI and dV.

In this section, four JoFET devices ("B1", "B2", "B3", and "B4") with different junction lengths have been studied. These devices have been designed to have

junction lengths of 150 nm, 200 nm, 300 nm and 500 nm while having the same junction width of 4 μm. Figure 3.7 shows the conductance of the devices with respect to the gate voltage. From this figure, we observe that the conductance increases when the gate voltage becomes more negative. This indicates an accumulation of holes as carriers in these transistors. The drop of the conductance at a gate voltage close to 2 V shows that the transistors can be fully depleted with a threshold voltage around 2 V. Nevertheless, although the heterostructure is undoped, it has been noticed that the conductance of all the devices is finite at the gate voltage equal to zero. This positive threshold voltage in the devices has not been fully understood yet, but we attribute this to the surface charges. We have noticed that this effect depends strongly on the details of the process flow and is rather reproducible.

Figure 3.7 also shows that there is a slight difference in the threshold voltage on each device. This threshold voltage is determined by the method represented in Figure 3.8. First, the minumum of the numerical derivative of the conductance as a function of the gate voltage determines the reference point (the black cross in the figure). This value is reported to the conductance curve, and the line from that point is drawn with the slope equal to the value of the minima. The threshold voltage is defined by an interception between this and the horizontal axis.

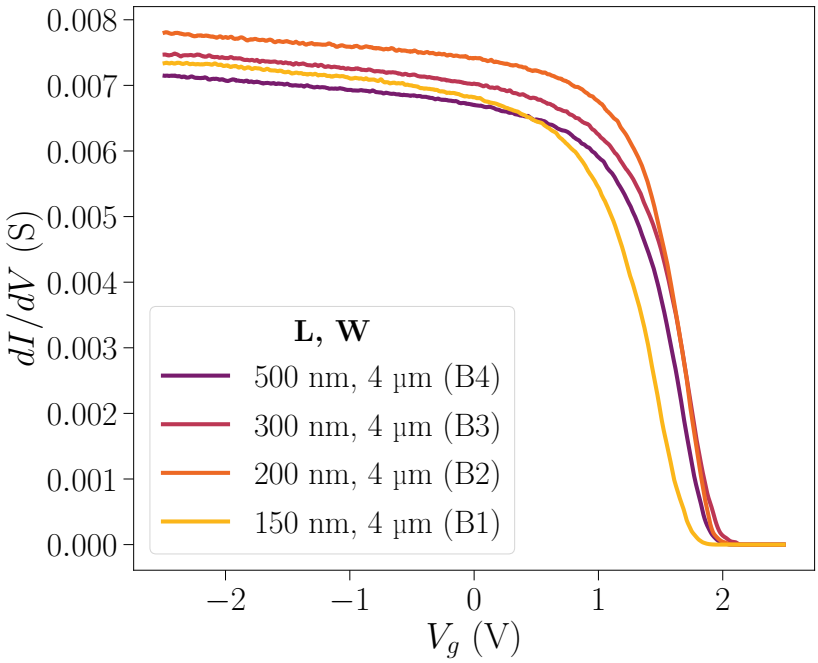

Figure 3.7 – The conductance (dI/dV) of four JoFETs with L= 150 nm, 200 nm, 300 nm and 500 nm as a function of the gate voltage (V_g) at low temperature (4.2 K). This data is obtained at the zero DC voltage applied. The AC voltage applies to the device is 0.5 mV at 77 Hz.

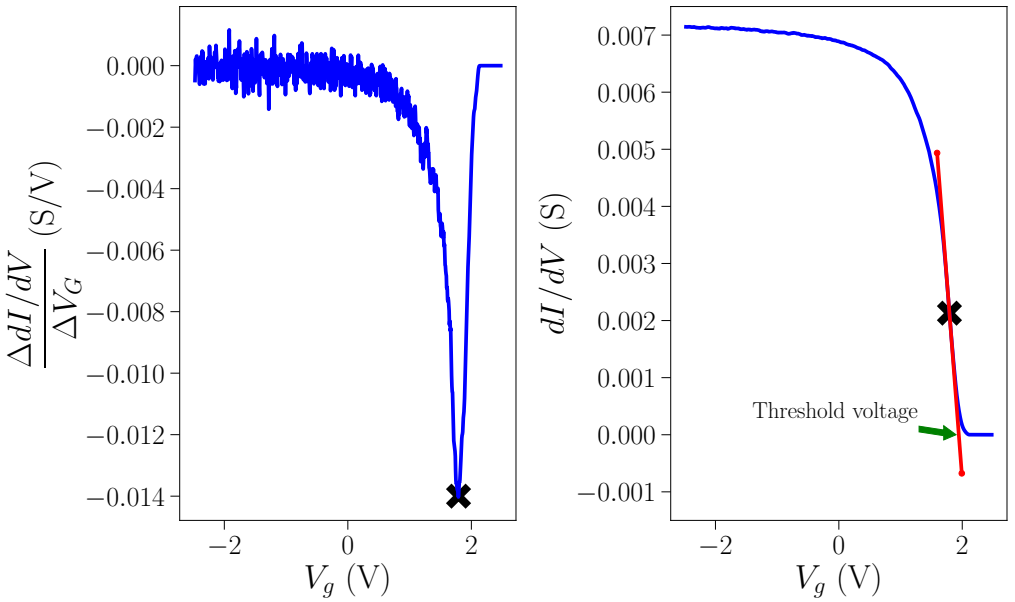

Figure 3.8 – **Left:** Numerical differentiation of the conductance of the device with $L = 500$ nm with respect to the gate voltage. The black cross marks the point with the minimum derivative value. **Right:** The conductance as a function of the gate voltage of the same device. The black cross is locating at the same spot on the horizontal axis. The red line has the same slope as the value in the vertical axis of the figure on the left. The threshold voltage is marked by the green arrow.

Additionally, the mobility in each device has been estimated with the Drude model of electrical conduction. Based on an assumption that the conduction is in the 2D hole gas (2DHG) and the change in the mobility is neglegible in the region of interest, from the Drude model of electrical conduction: $\sigma = ne\mu$ [76], the mobility of the carriers in the device can be written as:

$$\mu = \left(\frac{\Delta dI/dV}{\Delta V_G}\right)\left(\frac{W}{L}\right)\left(\frac{d_{AlOx}}{\varepsilon_{AlOx}\varepsilon_0} + \frac{d_{SiGe}}{\varepsilon_{SiGe}\varepsilon_0}\right). \tag{3.4}$$

where μ is the mobility of carriers, $\frac{\Delta dI/dV}{\Delta V_G}$ is the derivative of the conductance as a function of the gate voltage, W is the junction width, L is the junction length, d_{AlOx} and d_SiGe are the thicknesses of the aluminum oxide layer and the silicon-germanium capping layer, ε_{AlOx} [77] and ε_{SiGe} [78] are the relative permittivity of the aluminum oxide and the silicon-germanium, and ε_0 is the permittivity of free space.

From the equation, the mobility can be determined by the slope calculated from the curve in Figure 3.8, the geometrical shape of the device, and the permittivity of materials. The mobility of the devices calculated from this equation is: 895×10^3, 839×10^3, 503×10^3 and 295×10^3 cm^2/V·s at the gate voltage around 2 V

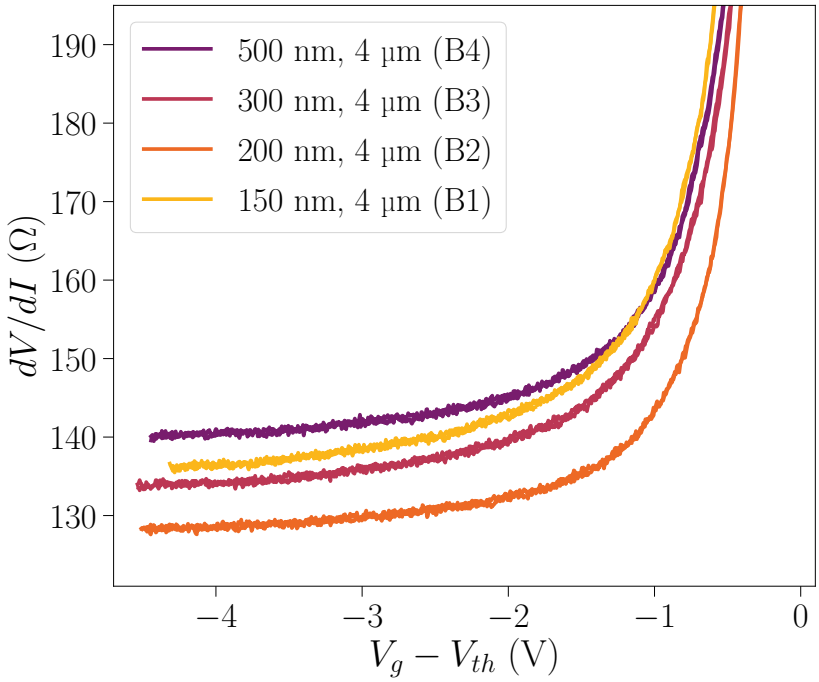

Figure 3.9 – Resistance as a function of the gate voltage with respect to the threshold. The colors and the labels in the legend indicate the junction lengths of the device by the lithography design.

(where the values of the derivative $\frac{\Delta dI/dV}{\Delta V_G}$ are at their maximum) for the device with junction lengths of 150 nm, 200 nm, 300 nm and 500 nm, respectively. The calculated mobility from this method varies strongly with the devices, which is not physically reasonable. Also, by comparing with the mobility caculated with the data from the Hall effect measurement (140×10^3 cm^2/V·s), the values calculated from the Drude model are off by a factor of between 2 and 7. The possible explanation is that the conducting channel length for the normal state is, in fact, equal to an effective length which is longer than the junction length. Combining with the fact that the etching for the ohmic contact is aimed at the depth of the middle of the quantum well, this explanation can describe the mismatch of the mobility calculated by the Drude model. This will be discussed later, at the end of this section.

After the data processing, Figure 3.9 shows the resistance of the devices with respect to the gate voltage from the threshold. Apart from the data obtained from the device with L =150 nm, the figure shows that the longer the device, the larger the resistance. It is not clear yet why the resistance of the JoFET with a junction length of 150 nm does not follow this trend.

The data are analyzed with a simple model assuming that the total resistance is the contribution of two components as stated in the equation:

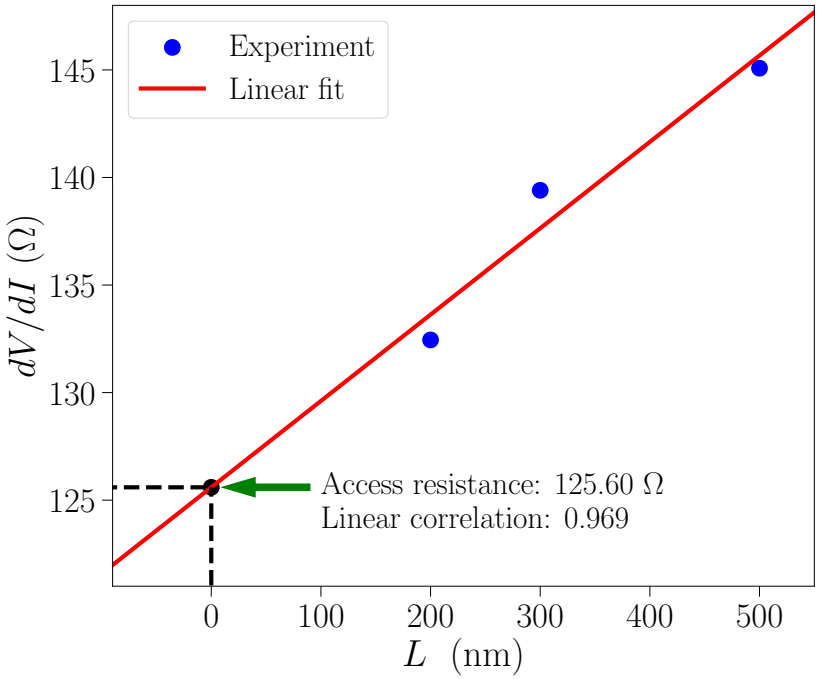

Figure 3.10 – The fitting method corresponds to the equation 3.5. The blue scattered points represent the resistance data from Figure 3.9 at the $V_g - V_{th}$ = -2 V. It has been assumed that the junction lengths follow the lengths in the lithography design. The linear regression of the data is shown by the red line, and the access resistance is represented by the black dot in the figure.

$$R_{total} = 2R_{access} + R_{square} \times \frac{L}{W}, \tag{3.5}$$

where R_{total} is the total resistance measured, R_{access} is the contribution of the aluminum pads and the Al-Ge contact interface, R_{square} is the square resistance of the Ge, L is the junction length and W is the junction width of the device. For this analysis, we have excluded the data from the device with a junction length of 150 nm.

From this equation, we expect a linear dependence of the measured resistance as a function of the length L. The data observed at the $V_g - V_{th}$ equal to -2 V are plotted in Figure 3.10 and confirm this linear behavior. The square resistance is determined by the slope of the linear fit multiplied by the width of the junction (4μm) and the access resistance is defined by the interception of this line with the vertical axis (125.60Ω).

The analysis is repeated for the data for all gate voltage values and the square resistance and the access resistance with respect to the gate voltage are shown in Figure 3.11. The figure shows that the square resistance of the conducting channel decreases as the gate voltage becomes more negative. This indicates an

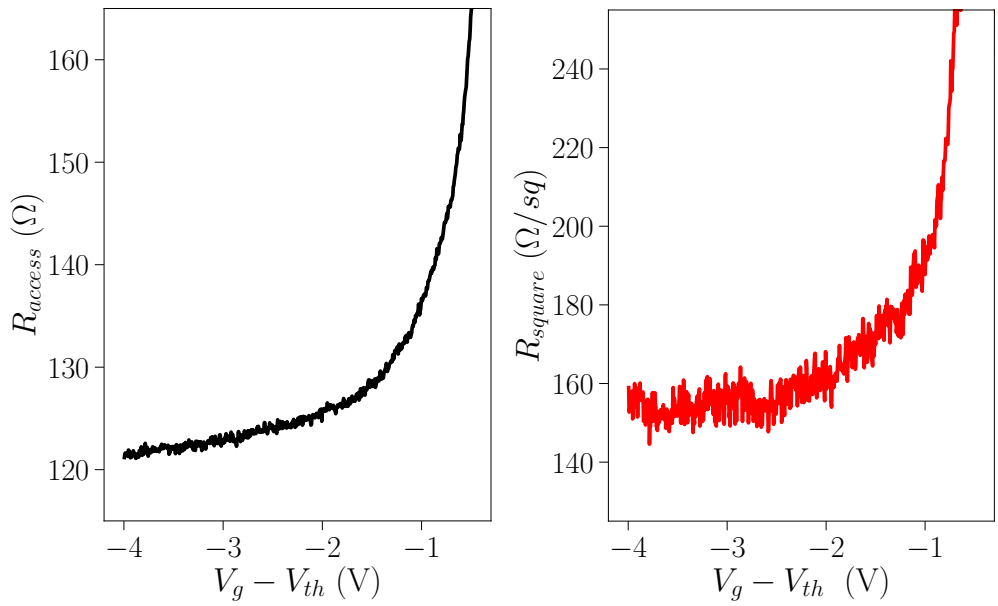

Figure 3.11 – Access resistance of the devices (**Left**), and square resistance of the germanium 2DHG (**Right**) extracted from the data of the resistance as a function of the gate voltage obtained from the devices with junction lengths of 200 nm, 300 nm and 500 nm using linear regression method.

accumulation of the holes as the carriers in the conducting channel by the gate voltage. The decreasing trend is also observed for the access resistance. Since the aluminum contacts should not be affected by the gate voltage, this can be attributed to the decrease of the Schottky barrier at the Al-Ge interface as well as the accumulation of the carriers in the channel close to the contacts.

Additionally, we observed the saturation of the square resistance when the gate voltage is more negative than -3 V from the threshold. We give a possible explanation in Figure 3.12. In this figure, the energy band diagrams of the device is shown. When the metal, the oxide, and the semiconductor are separated, their energy bands are not related to each other. When they are connected, the Fermi level (E_F) in the metal, the oxide, and the semiconductor are aligned at a constant energy level. Consequently, the energy bands in the oxide and the semiconductor are bent toward the energy level of the metal with respect to the Fermi level (E_{FM}). At a certain gate voltage V_{G_1} below the threshold voltage, the carriers accumulated in the quantum well have energy above the Fermi level and contribute to the conduction. The number of carriers accumulated causes the square resistance to drop. When the E_{FM} is lifted further to the gate voltage V_{G_2} in the figure, there are energy levels at the SiGe-Al_2O_3 interface, that have lower energy than the energy levels in the quantum well. The carriers in the quantum well can tunnel to these energy levels and start to accumulate there. This causes the accumulation of the carriers in the quantum well to level off. Since the carriers that have built

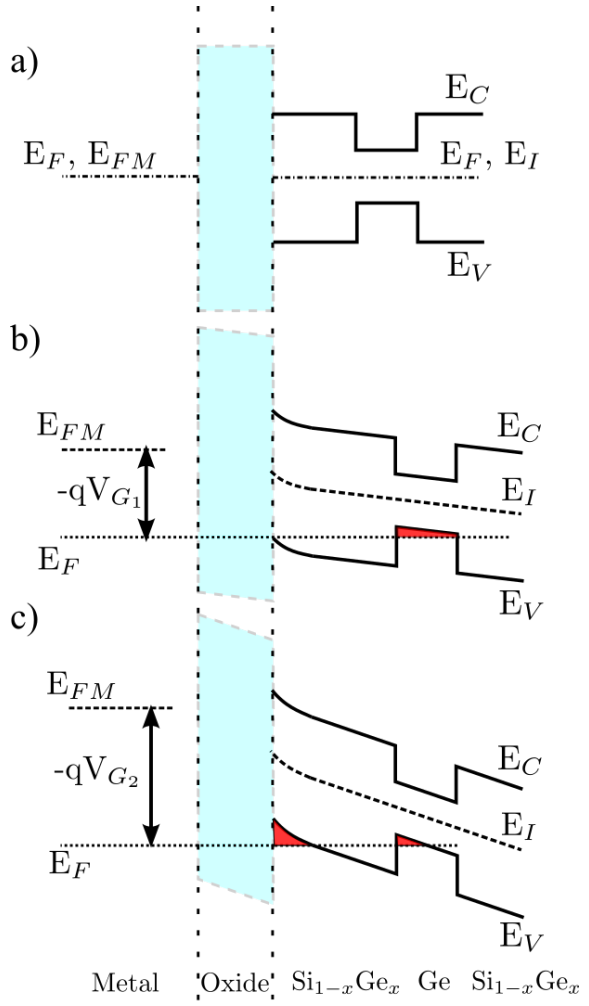

Figure 3.12 – Schematic of the band diagram of the device in three different situations. **a) Not connected:** The Fermi level of the metal and the semiconductor are independent. There are confinement energy levels in the conduction band and the valence band of the quantum well due to the band gap difference. **b) Accumulation:** The energy band of the oxide and the semiconductor are bent due to the voltage applied on the metal. There are carriers above the Fermi level confined in the quantum well participating in the conduction. **c) Saturation:** When the negative voltage is applied on the gate until a certain point, the energy levels at the interface due to the band bending start to become lower than those in the quantum well. Hence, the carriers can tunnel from the quantum well and be accumulated at these energy levels. Since the carriers confined in these levels are not participating in the conduction, the carrier density is saturated and the square resistance measured start to level off. (**From the diagram:** E_F is the Fermi level of the device, E_{FM} is the energy level of the metal with respect to the Fermi level, E_I is the Fermi level in the intrinsic semiconductor, E_C and E_V are the conduction band and the valence band of the semiconductor, and $V_{G_{1,2}}$ are the gate voltages applied on the metal.)

up in the energy states at the interface are not contributing to the conduction, we observe the plateau in the square resistance when the gate voltage becomes more negative than -3 V.

The simple model from the equation 3.5 can be extended further by assuming that the access resistance consists of the contact resistance between the aluminum and the germanium and the resistance of the aluminum leads. Then, the contact resistance depends on the interface resistance and the bulk resistance of the germanium channel underneath the contact. Schematic diagram in Figure 3.13(a) introduces the effective contact length of the transport ($\mathcal{L}$), the full quantum well thickness (t) and the etched quantum well thickness (d). The equation of the contact resistance can then be written as:

$$\frac{R_{access} - R_{Al}}{2} = R_{contact} = \frac{R_{interface}}{W\mathcal{L}} + \frac{\mathcal{L}}{W}\left(\frac{t}{d}R_{square}\right), \tag{3.6}$$

where $R_{contact}$ is the contact resistance, R_{Al} is the resistance of the aluminum leads connecting to the bonding pads, $R_{interface}$ is the interface resistance which depends on the effective area of the contact and $\left(\frac{t}{d}R_{square}\right)$ is the square resistance of the germanium quantum well under the effective contact area, assuming that the square resistance scales with the remaining quantum well thickness. It is noted that, to simplify Equation 3.6, the resistance of the parts of the aluminum leads just above the germanium quantum well has been neglected. It is justified by the fact that the square resistance of the Ge channel is between 160 and 240 Ω/□ (see Figure 3.11) and is much larger than that of the Al estimated to less than 1 Ω/□ (see the paragraph below).

The system will have the minimum value of the contact resistance when:

$$\mathcal{L} = \sqrt{\frac{R_{interface}}{2\left(\frac{t}{d}R_{square}\right)}} \quad \text{and,} \quad R_{interface} = \frac{2W^2{R_{contact}}^2}{9\left(\frac{t}{d}R_{square}\right)}. \tag{3.7}$$

From the design, the aluminum lead has a thickness of 50 nm and consists of approximately 45 squares. This contributes to the resistance of 23.85 Ω (for $\rho_{Al} = 2.65 \times 10^{-8}$ Ω·m [79]). The TEM image in Figure 3.5(d),(e) and (f) suggest that the etching depth in the quantum well ($t - d$) is relatively low. We estimate the effective length ($\mathcal{L}$) for two cases at the value of d of 8 and 16 nanometers, as an upper bound and the lower bound. To avoid the disorder of the conduction close to the pinch-off voltage, the effective length $\mathcal{L}$ in the region of the gate voltage from -1 V to -4 V has been calculated (Figure 3.13(b)) and yields an average in the range of 209 to 419 nanometers. If this effective length has been taken into account to the mobility calculation with the equation 3.4, the mobility becomes less dependent on the junction length (which is more physically reasonable) and the value of the mobility is calculated to be in the range of $135 \times 10^3 - 220 \times 10^3$ cm^2/V· s, which is in better agreement with the value obtained from the Hall effect measurement. Nevertheless, this model may oversimplify the real device in some aspects, for example by ignoring the screening effect of the contact that can cause the gradient

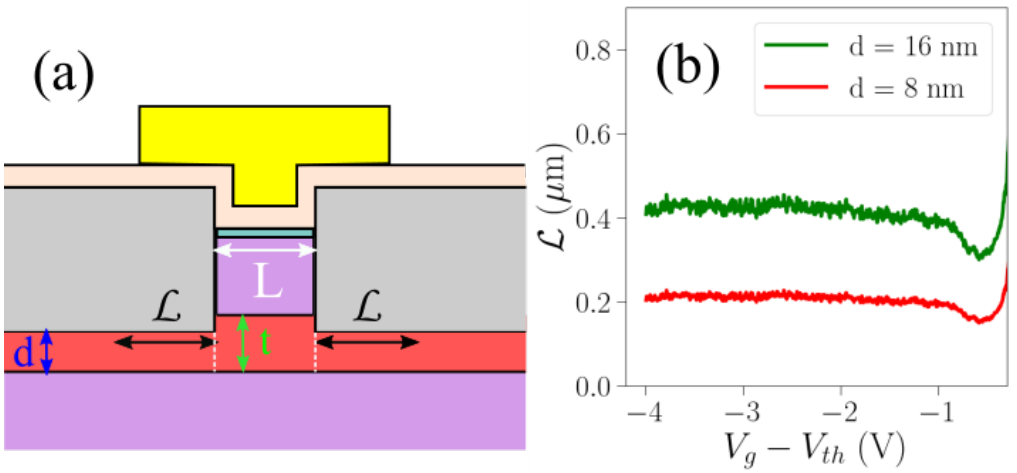

Figure 3.13 – Schematic diagram of the contact resistance model depicts the side view of the device and labels the junction length (L), the effective contact length ($\mathcal{L}$) and the quantum well thickness (full: t and etched: d).

in the square resistance. This can lead to an inaccuracy in estimating the effective length and the mobility. However, the explanation that the actual effective length that contributes to the conduction is longer than the junction length should still be valid.

3.4 Josephson FET: low-temperature characterization

3.4.1 Superconducting transition at low temperature

To study the transport properties of the devices at low temperatures, specifically below the critical temperature of aluminum (T_C), measurements were conducted using a dilution refrigerator with a base temperature of 60 mK. The schematic diagram of the measurement setup is depicted in Figure 3.14.

To measure the device under test (DUT), a signal is applied to the DUT through a DC voltage source connected to a resistor (R_2, typically 1 MΩ). The voltage drop across the device is then measured using a differential amplifier, while the current passing through the device is measured by a current-to-voltage converter. The signals from the differential amplifier and the current-to-voltage converter are recorded using digital multimeters (DMMs). After a few calibrations, we opted to use the internal ammeter of the voltage source for current measurements and replaced the current-to-voltage converter with a ground connection. In the low-temperature section of the dilution refrigerator, several low-pass filters are connected in series with the measurement line to filter out noise during measurements. Additionally, in some measurements, we have measured the differential resistance of the DUT. To do so, an AC current at a low frequency (below a few

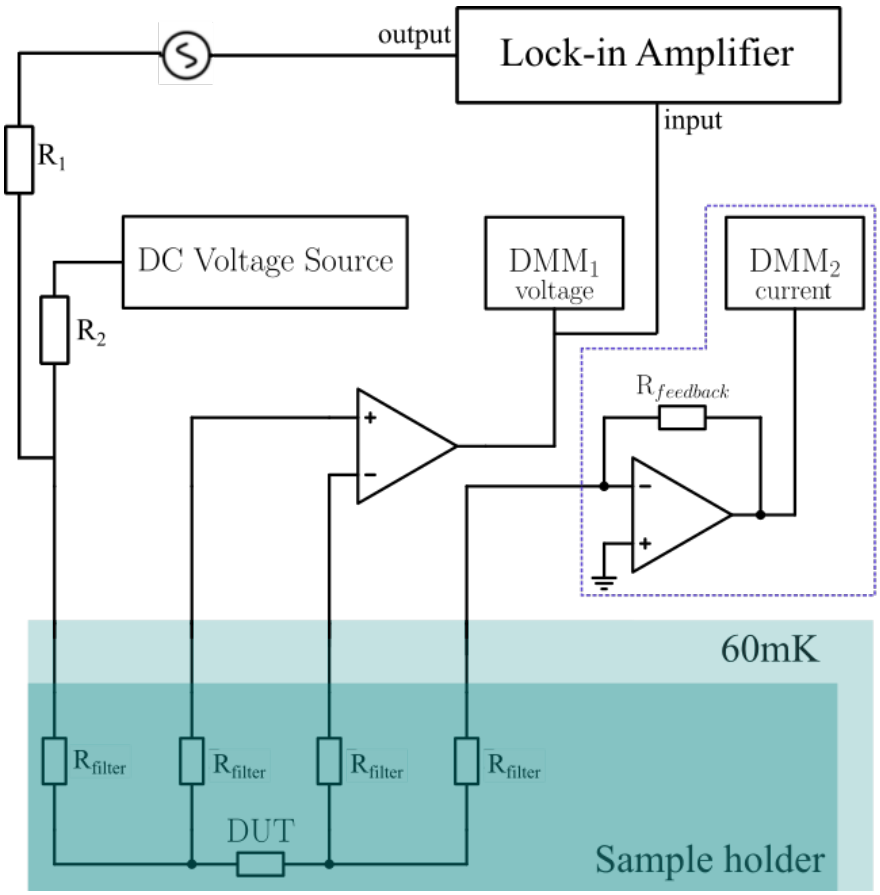

Figure 3.14 – Schematic diagram of the measurement set-up in the dilution refrigerator The device under test (DUT) is connected to low-temperature, low-pass filters. Each filter has a resistance of either 2k or 20k Ω, and is on the sample holder connecting to the device. The device has been measured with a four-point measurement setup by applying a signal from the direct signal source to the DUT and measuring the voltage drop across the device (DMM_1) and the current passing through the device (DMM_2) with a differential amplifier and a current-to-voltage converter, respectively. We can use a lock-in amplifier to improve the signal-to-noise ratio of the measured voltage. In some measurements, we used the internal ammeter at the direct signal source and shunted the current-to-voltage converter to ground instead. The DC voltage line connecting to the gate has not been shown in the figure.

hundred Hz) was sent in addition to the DC current. The resulting AC voltage was analyzed with a lock-in amplifier.

The inset in Figure 3.15 shows the conductance of the device "A1" as a function of gate voltage. We observed a small shift ($\approx$ 10 mV) in threshold voltage with respect to the direction of gate voltage ramping. We attribute this to the effect

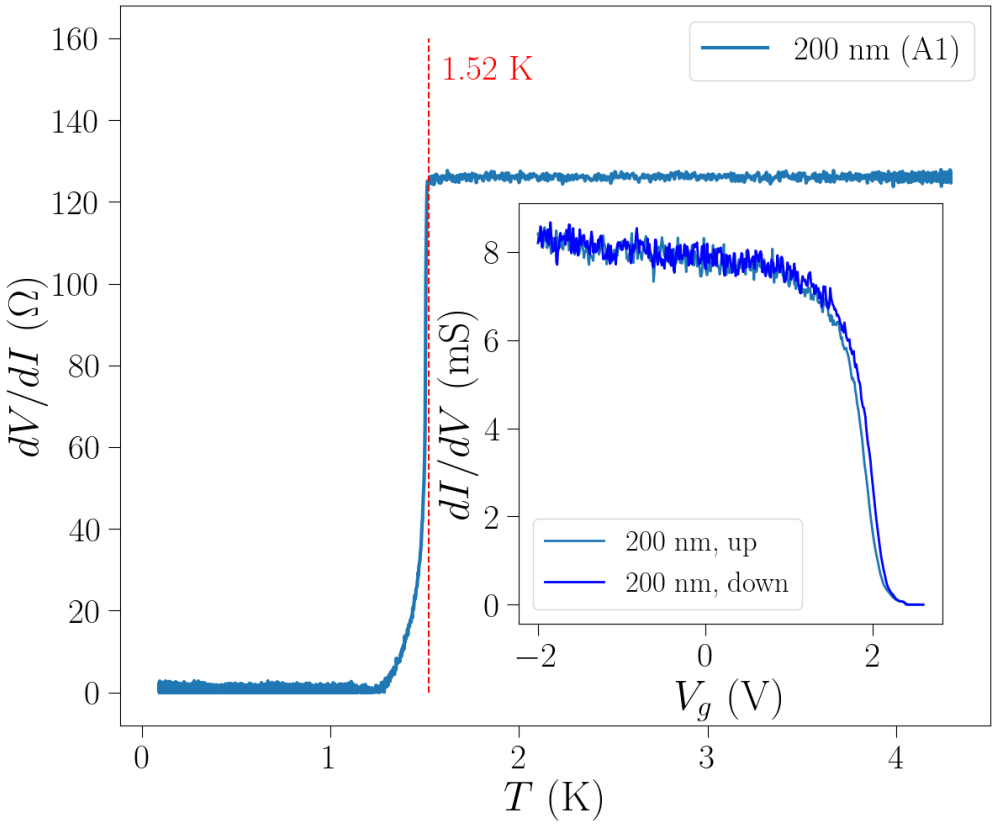

Figure 3.15 – Resistance of the device "A1" as a function of temperature at V_g = -2 V. From the curve, T_C has been estimated to be 1.52 K. The inset shows the pinch-off curve of the device at 4.2 K. There is a small shift in the threshold voltage depending on the direction of voltage ramping.

of the charge traps at the oxide interface. The main figure plots the resistance of the device at V_g = -2 V as a function of temperature. The resistance begins to drop below 1.52 K as the Al leads turn into superconductors. The Ge channel is then proximitized by the Al leads, which contributes to the further decrease in resistance at lower temperatures.

Further, Figure 3.16 shows the current-voltage characteristic (I-V curve) of this JoFET "A1" with a junction length of 200nm and a junction width of 4μm at the gate voltage of -2 V at different temperatures. At 1.55K, which is above T_C of aluminum, the I-V curve is linear, like in the case of a standard ohmic transistor. When the temperature is below T_C, the resistance drops due to the superconducting transition of aluminum leads. It is indicated by the decrease in slope in the violet curve. The light blue curve shows a further decrease in resistance when the temperature is much lower than T_C. There is a plateau in the zero-resistance state due to the Cooper pair's transport, as explained in the previous

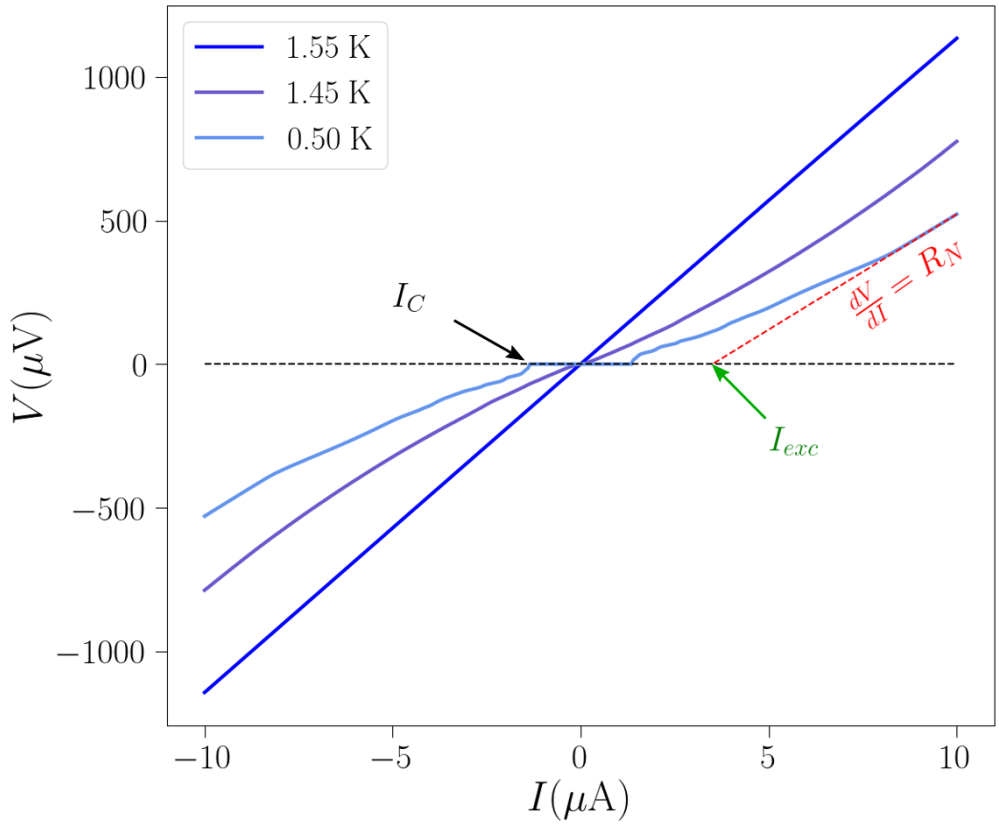

Figure 3.16 – Current-voltage characteristic of the JoFET "A1" with a junction length of 200 nm and a junction width of 4 µm at the gate voltage of -2 V and the temperature of 1.55 K (blue), 1.45 K (violet), and 0.50 K (light blue). The plateau in the light blue curve represents the zero-resistance state, which indicates the flow of the non-dissipative current. The zero-resistance state disappears in the violet curve due to the suppression of the proximity effect in germanium when the temperature is close to T_C of aluminum. When the temperature goes above T_C of aluminum, the aluminum leads change from superconducting to normal, which makes the resistance go up in the blue curve. The critical current (I_C) is defined by the current at the switching point of the zero-resistance state. The slope when $V > 2\Delta$ defines the normal state resistance (R_N). The excess current (I_{exc}) is the intercept between this slope and the horizontal axis.

paragraph. It can be seen from the light blue curve that there is a transition from the zero-resistance state to the normal state when the current passing through the junction is greater than a certain value. This is defined as the critical current (I_C) of the junction. The normal state resistance (R_N) is determined by the slope of the I-V curve at the large voltage drop across the junction ($V > 2\Delta$, where Δ is the superconducting gap). The interception between that slope and the

horizontal line $V = 0$ V is defined as excess current (I_{exc}), which is the result of the additional carrier transport due to Andreev reflection [16]. There are several non-linearity features observed in the light blue curve due to the transport of the carriers with energy below the superconducting gap. We will discuss this later on in this chapter.

3.4.2 Gate-tunability of the critical current

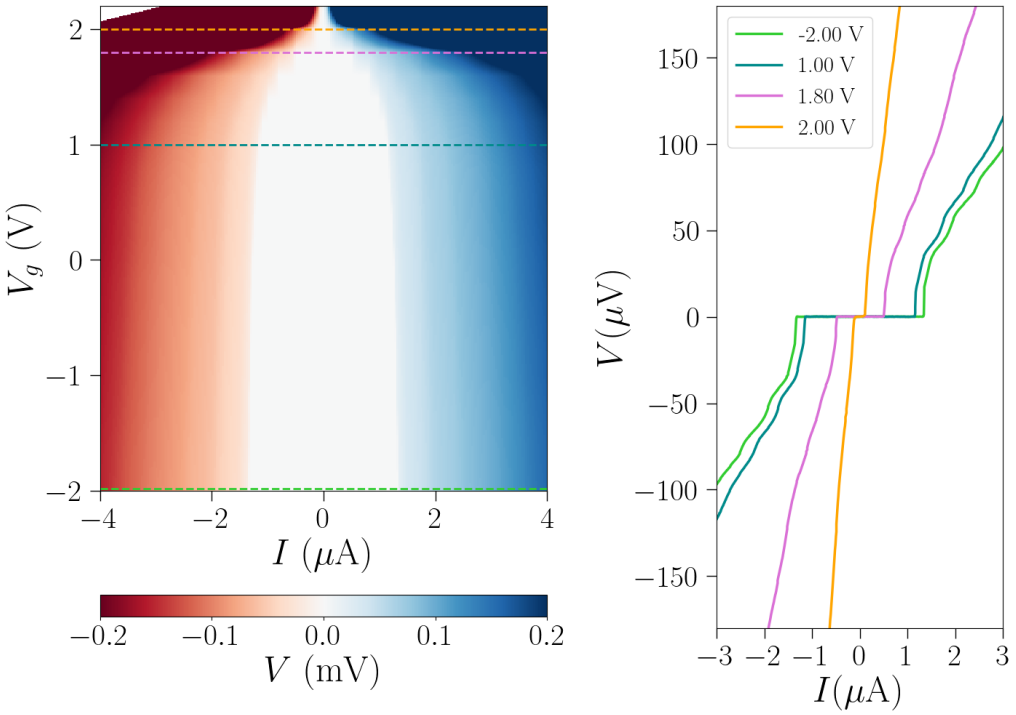

Figure 3.17 – (left) Voltage (V) measured across the JoFET "A1" as a function of the gate voltage (V_g) and the current (I). (right) Current-Voltage characteristic traces extracted from the colormap on the left. The width of the zero-resistance state in the trace changes with the gate voltage. This indicates the tunability of the critical current.

The value of the I_C can be tuned by applying the gate voltage (V_g) to modulate the carrier density in the junction. Figure 3.17 shows the measurement of the voltage drop across the junction of the device A1 with the different gate voltage values. It is observed that when the V_g becomes more negative, the plateau of the zero-resistance state becomes wider due to an increase in the hole carrier density in the germanium 2DHG.

According to the definitions of I_C, R_N, and I_{exc} provided earlier, Figures 3.18(a), (b), and (c) depict I_C, R_N, and I_{exc} extracted from the I-V curves of JoFET devices as functions of the gate voltage. From these extracted values, we

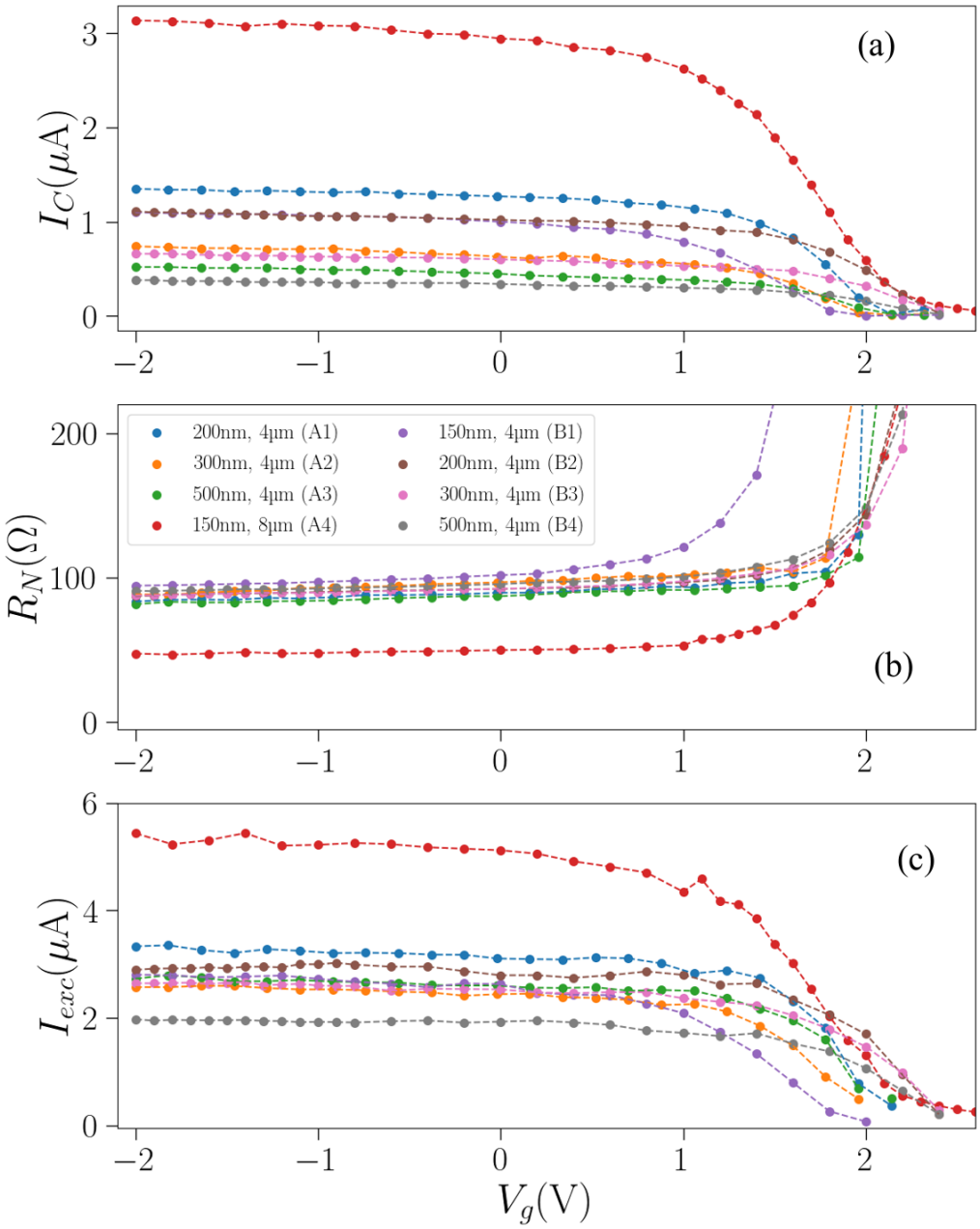

Figure 3.18 – Critical current (I_C) (a), normal state resistance (R_N) (b), and the excess current (I_{exc}) (c) as a function of the gate voltage (V_g). The data have been extracted from the I-V curves, similar to the one shown in Figure 3.17, of each device.

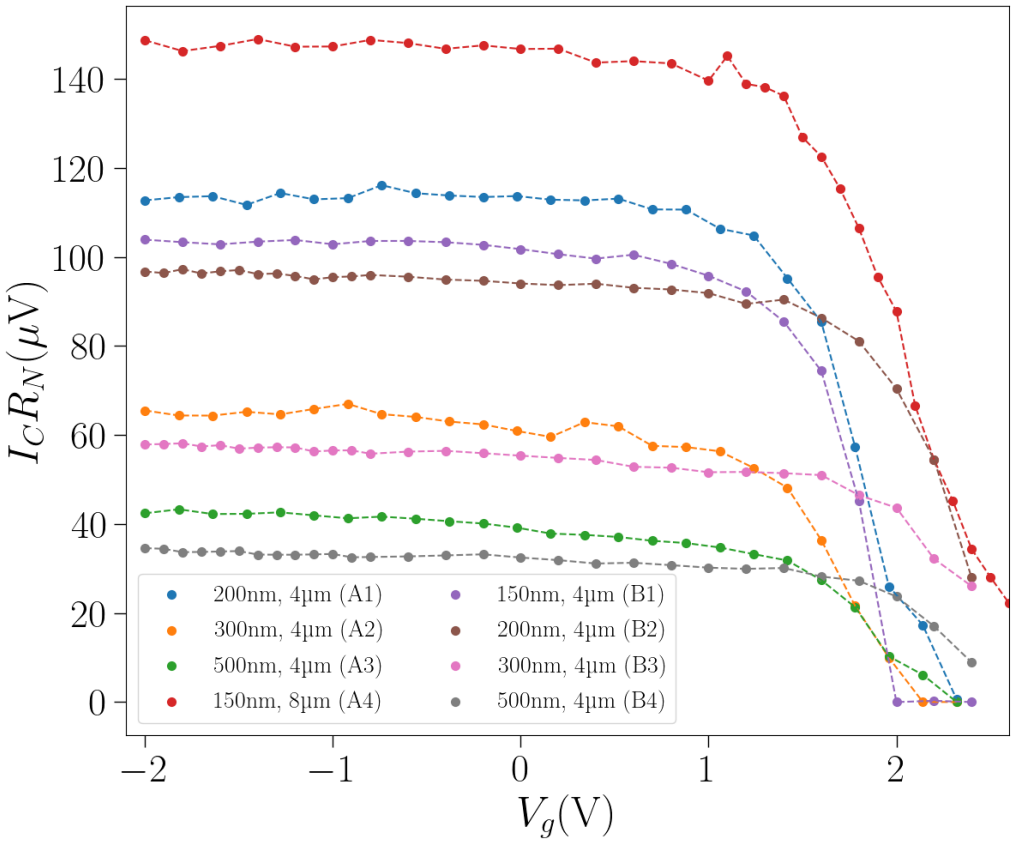

Figure 3.19 – The "$I_C R_N$" product calculated from the extracted value in Figure 3.18.

calculated the $I_C R_N$ products as functions of the gate voltage, as plotted in Figure 3.19. The $I_C R_N$ is also used as a "figure of merit" for the S-N-S junction, which can imply transparency and junction quality. In the case of the S-N-S junction, derived by the Kulik-Omel'yanchuk theories, the product has theoretical limits of $1.32\pi\Delta/2e$ and $2\pi\Delta/2e$ [80] in the diffusive (electronic mean free path, $l <$ normal coherence length, ξ) and clean ($l > \xi$) limits, respectively. The maximum $I_C R_N$ value reported in this work is found to be 149 µV (device A4, I_C = 3.13 µA, R_N = 47 Ω), which is approximately half of the value in the theoretical diffusive limit.

For comparison, Table 3.3 displays the $I_C R_N$ product values reported in the SiGe heterostructure platform. This work reports the highest $I_C R_N$ product for the Al-Ge-Al system in the SiGe heterostructure. This could be due to the very high transparency of the Al-Ge interfaces. We crudely estimated the Z-parameter using the Octavio-Blonder-Tinkham-Klapwijk (OBTK) formalism [17, 82], modified from BTK formalism. From the extracted value, the normalized excess current ($eI_{exc}R_N/\Delta$), where we used Δ = 212 µeV as estimated from the subgap features later in this chapter) at -2 V for the device "A4" is equal to 1.22, which corresponds

Table 3.3 – Table lists the values of the $I_C R_N$ product measured from the S-N-S junctions made in SiGe heterostructure.

Reference	**Device platform**	$I_C R_N (\mu V)$
N. W. Henrickx et al., 2019 [81]	Al-Ge-Al	17
F. Vigneau et al., 2019 [20]	Al-Ge-Al	8
K. Aggarwal et al., 2021 [65]	Al-Ge-Al	50
	Nb-Al-Ge-Al-Nb	360
A. Tosato et al., 2023 [66]	PtSiGe-Ge-PtSiGe	51
This work, 2023	Al-Ge-Al	149

to $Z \approx 0.3$, and a transparency coefficient $\tau = 1/(1+Z^2) = 0.92$. Additionally, we can estimate the mean transparency of the junction ($\langle\tau\rangle$) from the normal state resistance using the Landauer formula as $\frac{1}{R_N} = G_N = \frac{2e^2}{h} N \langle\tau\rangle$. In the accumulation regime, the data from the Hall measurement in Figure 2.2 gives the carrier density $n_{2D} \approx 7 \times 10^{11}$ cm^{-2}. We can calculate the Fermi wavelength $\left(\lambda_F = 2\pi/k_F = 2\pi/\sqrt{2\pi n_{2D}}\right)$ to be approximately 30 nm. Then, we expect to have $N = 2W/\lambda_F \approx 533$ conducting channels in this device. With the value of $R_N \approx 47\ \Omega$ at -2 V, we get $\langle\tau\rangle \approx 0.5$, which is relatively low and not in good agreement with the value of τ estimated from the normalized excess current using the OBTK formalism. Moreover, this is inconsistent with the observation of a high $I_C R_N$ value. Note that we made this estimation under the assumption that the carrier density in the JoFET is similar to that in the Hall bar geometry. Nevertheless, further study on the current-phase relation and the AC Josephson effect of the junctions is needed to conduct a more complete study on the junctions' transparency.

In Figure 3.20, we plotted the $I_C R_N$ product at V_g = -2 V as a function of $1/L^2$ and as a function of $1/L$. The red dashed line represents the linear fit of the data points, excluding "B1". We observed that the $I_C R_N$ product decreases as L increases. This suggests that our device could be in the long junction limit, where the Thouless energy (E_{Th}) is less than the superconducting gap (Δ). In this limit, $I_C R_N$ is limited by E_{Th}, as opposed to the short junction limit, where the $I_C R_N$ is governed by Δ [83]. However, as we can see from Figure 3.20, the result is not conclusive enough to be convinced whether the junction is in the ballistic limit, where $L <$ elastic mean free path (l_e) and $E_{Th} = \hbar v_F / L$ with v_F as the Fermi velocity [84], or the diffusive limit, where $L > l_e$ and $E_{Th} = \hbar D / L^2$ with D as the diffusive constant [85].

Utilizing the data from the Hall effect measurement in Figure 2.2, in the strong accumulation regime, the values of the carrier density in the 2DHG and the hole mobility are approximately 7×10^{11} cm^{-2} and 140×10^3 cm^2/Vs, respectively. When the gate voltage is brought close to the threshold, in the low carrier density limit, the carrier density has a value of 3×10^{11} cm^{-2}, and the hole mobility is close to 30×10^3 cm^2/Vs. From these values, we can estimate the upper and lower

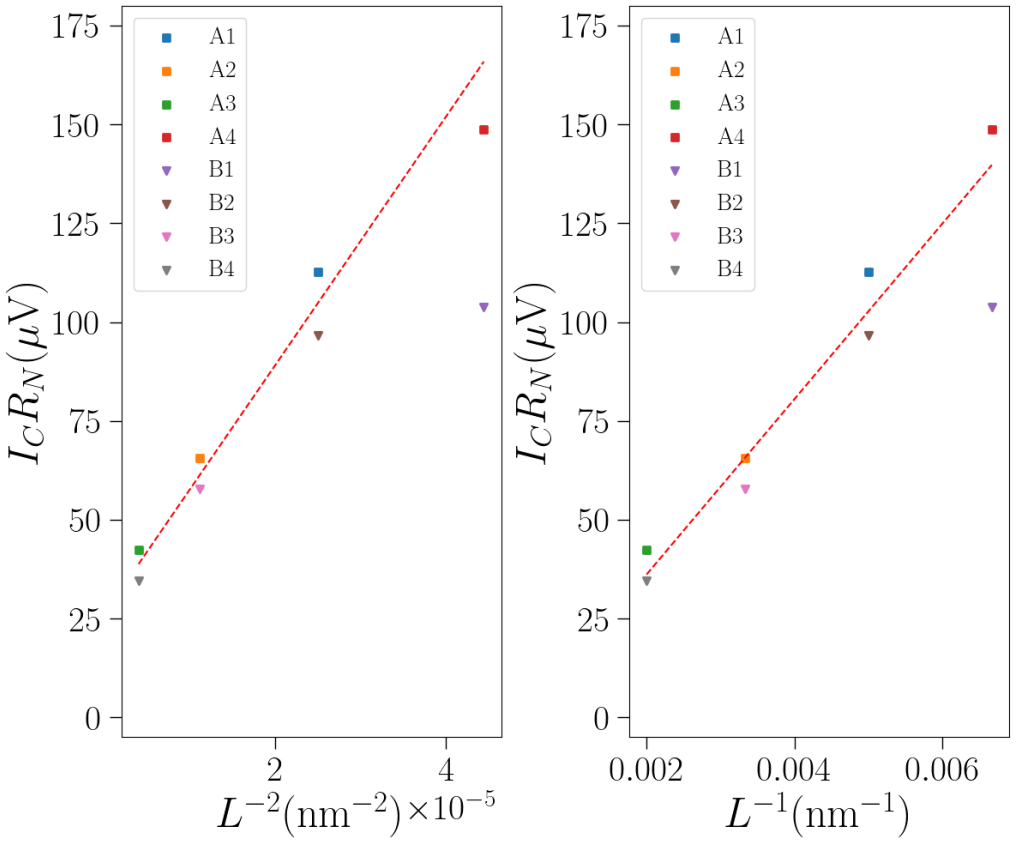

Figure 3.20 – $I_C R_N$ as a function of: (left) the inverse of the square of the junction length (L^{-2}), and (right) the inverse of the junction length. Both curves show the $I_C R_N$ decreasing when the junction length becomes longer.

values of the elastic mean free path $l_e = h\mu/e\lambda_F$ to be approximately $270 - 1500$ nm. This may suggest that our junction should be in the ballistic limit, as we have l_e larger than L in the high carrier density regime, at -2 V. However, we should keep in mind that this is based on the assumption that the electronic properties of the 2DHG in JoFET are indifferent to those in the Hall bar. In reality, the conducting channel of the JoFET is much shorter and closer to the etched surface and the aluminum contacts. These factors can introduce some disorder and scattering centers inside the conducting path, making our junction not in the true ballistic regime. Additionally, since the junction width is much larger than the contact separation, there could be carriers that travel across the junction with non-perpendicular angles, resulting in trajectories longer than the junction length "L". Thus, we believe that more data points at different junction lengths are necessary to affirm this conclusion.

In this section, the measurements were performed by setting the temperature to the base temperature of the dilution refigerator. Nevertheless, there could be

some heating effects that affect the actual temperature of the devices.

3.4.3 Temperature dependence of the critical current

The upper figure in Figure 3.21 displays the resistance (dV/dI) as a function of current (I) for device "B1" at various temperatures, with V_g set to -2 V. From each curve, we determined the critical current (I_C) by identifying the point at which the rate of change of resistance with respect to current ($(\Delta dV/dI)/\Delta I$) is maximized, as denoted by the green points in the figure.

To compare our results with theoretical predictions, we consider the temperature dependence of the critical current for a contact in the Josephson junction based on a two-dimensional gas system, as described by [41]:

$$I_C(\varphi) = \frac{\pi\Delta}{2eR_N} \frac{\sin(\varphi)}{\sqrt{1-\tau\sin^2(\frac{\varphi}{2})}} \times \tanh\left[\frac{\Delta}{2T}\sqrt{1-\tau\sin^2(\frac{\varphi}{2})}\right], \tag{3.8}$$

In this equation, I_C represents the current-phase relation (CPR) of the junction, Δ is the superconducting gap of the contact, R_N is the normal state resistance, φ is the phase difference across the junction, τ is the junction transparency, and T is the temperature.

The lower figure in Figure 3.21 depicts the temperature dependence of I_C for the six JoFET devices, which we extracted from the dV/dI versus I curves. The inset displays plots of $I_C(\varphi)$ as a function of temperature at different values of τ. On the y-axis, the values are normalized by the maximum critical current, denoted as $\tilde{I}_C$ (8.32 µA), for $R_N = 80\ \Omega$ and $\Delta = 212$ µV at $\tau = 1$ and $T \approx 0$. A significant discrepancy between $\tilde{I}_C$ and the measured I_C can be attributed to several factors, including the degradation of the temperature, the interface of the devices and/or the causes related to measurement setup. Nevertheless, the experimental results exhibit plateaus at low temperatures, indicating that our devices are not in the limit of $\tau \approx 1$.

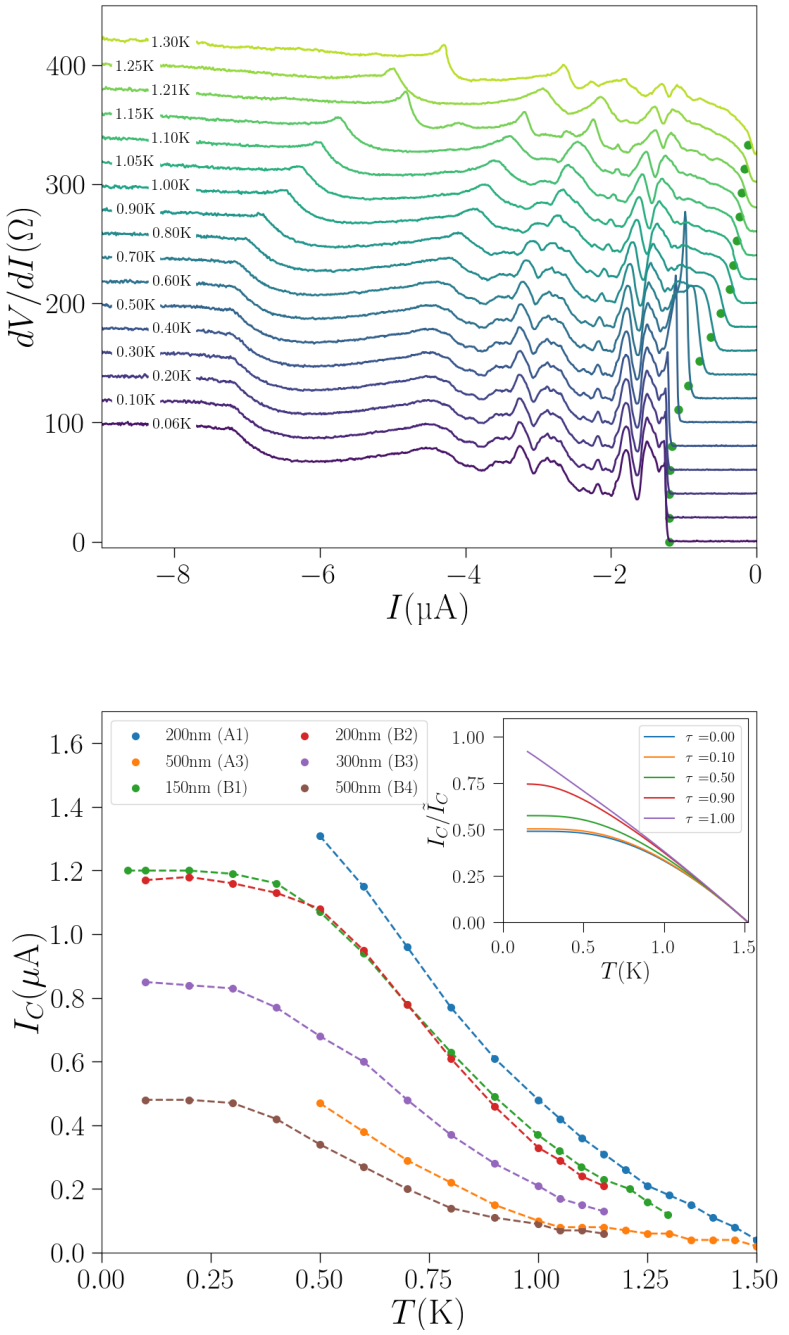

Figure 3.21 – (upper) The measured resistance (dV/dI) of the device "B1" as a function of the the voltage dropped (V) at different temperatures (T). Each curve is shifted by 20 Ω for the visibility. (lower) Critical current (I_C) as a function of temperature (T) extracted from the dV/dI versus I curves. The inset shows the plot of Equation 3.8 at various τ. We used $T_C = 1.52$ K, and $\Delta = 212$ μeV in this figure.

3.4.4 Fraunhofer diffraction

In the presence of the out-of-plane magnetic field, the phase of the superconductor in the JoFET is affected. Figure 3.22 shows the schematic diagram of the top-view of the JoFET in the out-of-plane magnetic field ($B_\perp$). The magnetic field causes the phase difference between points P_1 and P_2 to be related to the value of the flux enclosed in the loop, including the junction length (L) and the London penetration depth (λ), as shown by the equation: $\varphi(P_1) - \varphi(P_2) = 2\pi\Phi/\Phi_0$, where $\Phi = B_\perp(L+2\lambda)dz$. The Josephson relation of the critical current per surface area in the yz-plane can then be written as follows:

$$J_C(y,z,\varphi) = J_c(y,z)\sin(\varphi(z)), \tag{3.9}$$

where $J_C(y,z)$ is the critical current density of the junction without the effect of the magnetic field, and $\varphi(z) = \frac{2\pi}{\Phi_0}B_\perp(L+2\lambda)z + \varphi_0$.

Then, the critical current can be calculated by the integration of $\iint J_C(y,z,\varphi)dydz$. Under the assumption that the critical current density ($J_C(y,z)$) is homogeneous, the critical current under the effect of the magnetic field can be written as:

$$I_C^m = I_C \int_{-W/2}^{W/2} sin(kz+\varphi_0)\,dz = I_C \left| \frac{\sin\frac{\pi\Phi}{\Phi_0}}{\frac{\pi\Phi}{\Phi_0}} \right|, \tag{3.10}$$

where I_C^m is the magnetic field dependent critical current, I_C is the critical current without the magnetic field, W is the junction width, $k = \frac{2\pi}{\Phi_0}B_\perp(L+2\lambda)$, and $\Phi = B_\perp(L+2\lambda)W$ is the flux passing through the closed loop.

The equation is an analogy of the Fraunhofer diffraction pattern through a single-slit in optical physics, so it has also been called the Fraunhofer diffraction pattern in a Josephson junction. The derivation of the equation 3.10 is based on

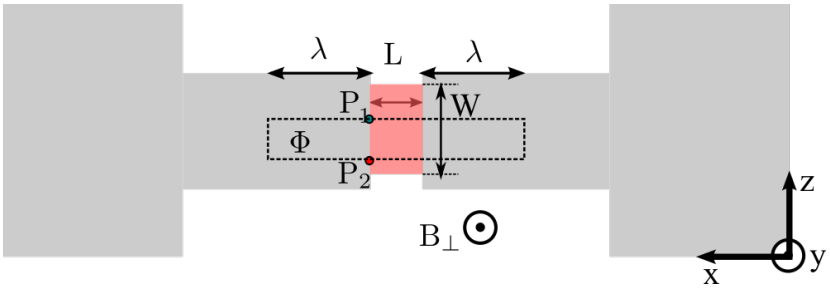

Figure 3.22 – Schematic diagram of the top-view of the JoFET in the out-of-plane magnetic field ($B_\perp$). The junction width is labeled by W and the junction length is labeled by L. The $B_\perp$ can penetrate into the superconducting leads upto a length scale of the London penetration depth (λ). The flux passing through the loop including the part of the L and the λ causes the phase difference between the point P_1 and the point P_2. The coordinate corresponds to the equations in the text is given in the bottom right of the figure.

the assumption that the $J_C(y, z)$ is uniform. This means that the critical current density is homogeneous if the Fraunhofer diffraction pattern follows the equation 3.10.

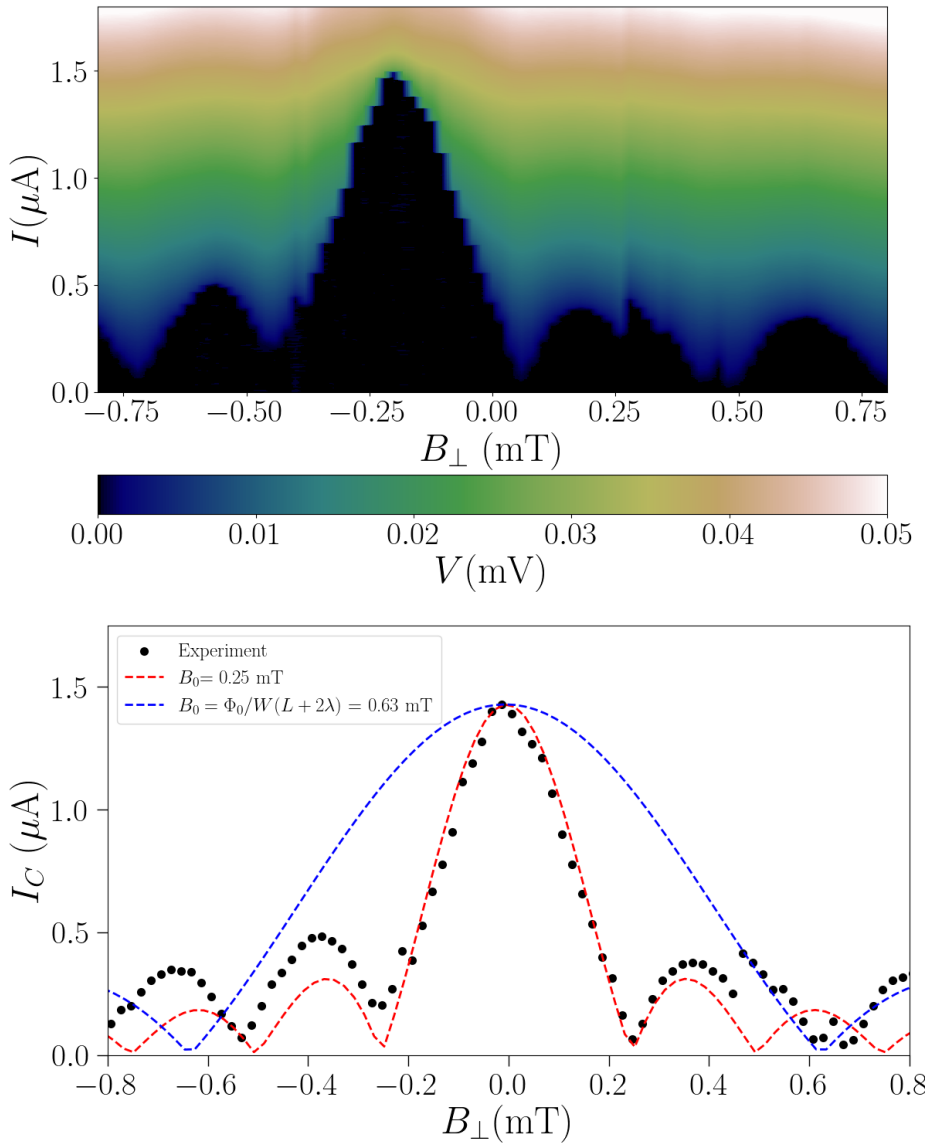

Figure 3.23 – (upper) Voltage drop (V) across the JoFET device "A1" as a function of the out-of-plane magnetic field ($B \perp$) and the current (I). (lower) Critical current extracted from the colormap above. The Fraunhofer fitting with the extracted critical current is shown by the red dashed line. The period of the Fraunhofer from the fitting is found to be 0.25 mT, in comparision with $\Phi_0/W(L+2\lambda) = 0.63$ mT calculated from the junction parameters.

Figure 3.23(upper) depicts the measurement of the voltage drop across the device "A1", which has a junction length of 200 nm and a junction width of 4 µm, in an out-of-plane magnetic field. In the lower plot, we have extracted the critical current values at all magnetic fields and fitted the critical current data using Equation 3.10. The fitting (red dashed curve) reveals a periodicity of 0.25 mT for the diffraction pattern, corresponding to an effective area value of approximately 8 µm², which is close to 2.5 $W \cdot (L + 2\lambda)$ when assuming $W = 4$ µm, as designed. This calculation suggests that $L + 2\lambda$ is equal to 2000 nm. This value exceeds the sum of the junction length and the penetration depth λ of the thin film of aluminum with a thickness of 50 nanometers ($\lambda = 310$ nm) [86]. The discrepancy could be attributed to the flux focusing effect on the junction, which increases the effective magnetic fields at the junction and expands the effective area of the closed loop. A similar phenomenon of finding the effective junction area to be much larger than the actual junction area has been previously reported in S-Sm-S Josephson junctions based on 2DEG or 2DHG [87, 88]. We also observed similar behaviors in our other devices ("A2" and "A3", see the raw data in the Appendix B). Additionally, we noticed that the critical current data can be fitted with the Fraunhofer equation, indicating that the critical current in the junction is distributed homogeneously. The blue dashed curve represents the plot of Equation 3.10 assuming the effective area is equal to $W \cdot (L + 2\lambda)$.

3.5 Subgap structure

3.5.1 Multiple Andreev Reflections (MARs)

As we mentioned earlier, there are several non-linearities observed in the light blue curve in Figure 3.16. The origin of these features is a process called multiple Andreev reflections (MARs). Figure 3.24 shows a schematic diagram of an S-N-S junction under an applied voltage bias. The leading transport process is governed by the single quasi-particles at the highest density of states just below the gap. When the voltage bias is larger than 2Δ (Figure 3.24(a)), the main process that happens is electron transport, which transports one electron. When the voltage bias is in the range between 2Δ and Δ (Figure 3.24(a)), the main process is the Andreev reflection, which transports two quasiparticles as a Cooper pair. When the voltage bias is between Δ and $\frac{2}{3}\Delta$, an electron from the state just below the gap can be reflected two times before being transferred to the right contact. The process transfers one Cooper pair and one electron, resulting in three quasiparticles in total. The number of MARs events is limited by the coherence time within the normal part and usually ranges from 2 to 5, and it is also commensurate with the value of the superconducting gap. Features of MAR can be seen in the I-V characteristics each time $neV = 2\Delta$ where n is an integer indicating the order of the MARs [89].

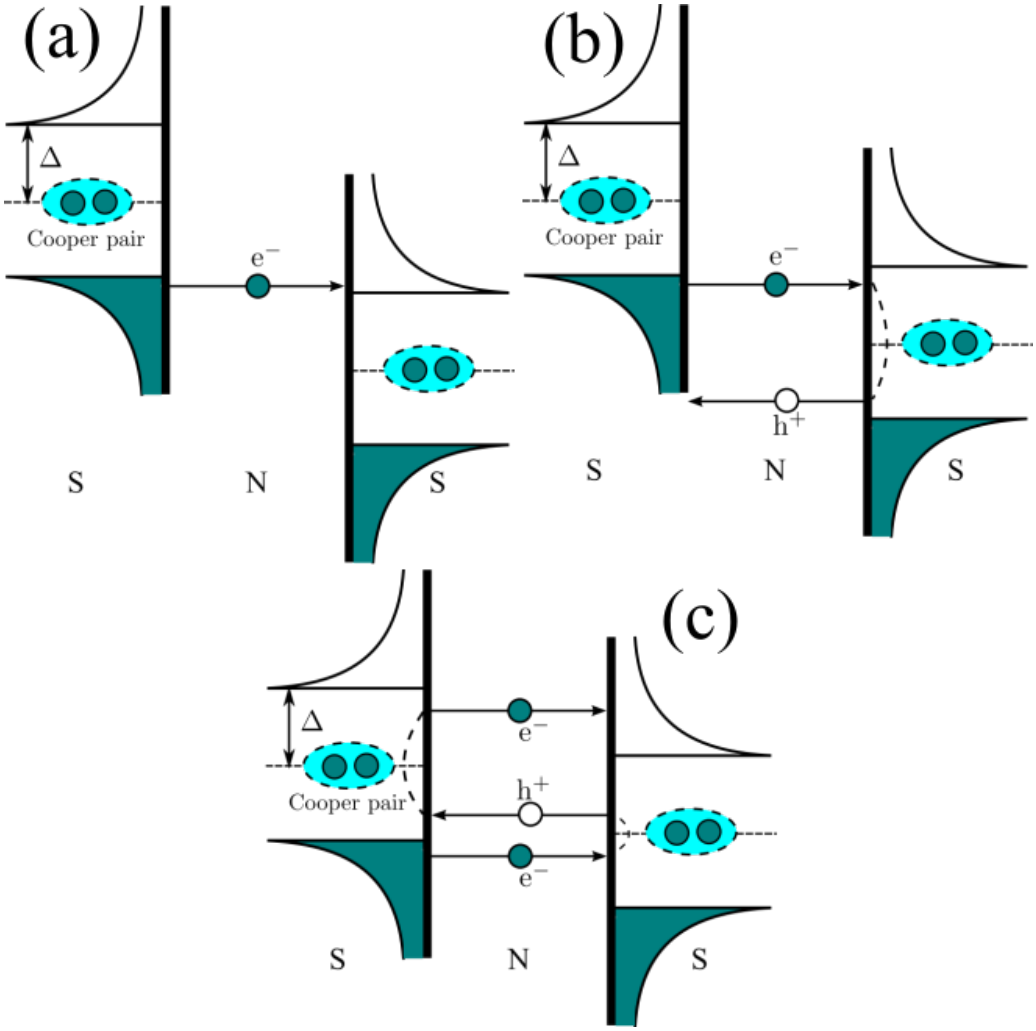

Figure 3.24 – Schematic of the energy band diagram of a superconductor-normal-superconductor (S-N-S) junction under different values of the applied voltage bias. The carriers just below the gap in the density of states are the ones that most contribute to the transport. **(a,** $V > 2\Delta$**)** The most commonly process is electron transport. This process transfers one quasiparticle. **(b,** $2\Delta > V > \Delta$**)** An electron is reflected as a hole at the N-S interface and transfers one Cooper pair. **(c,** $\Delta > V > \frac{2}{3}\Delta$**)** An electron is reflected as a hole and reflected as an electron again before traveling to the free state above the gap. This process transfers one quasiparticle and one Cooper pair.

3.5.2 MARs and superconducting gap

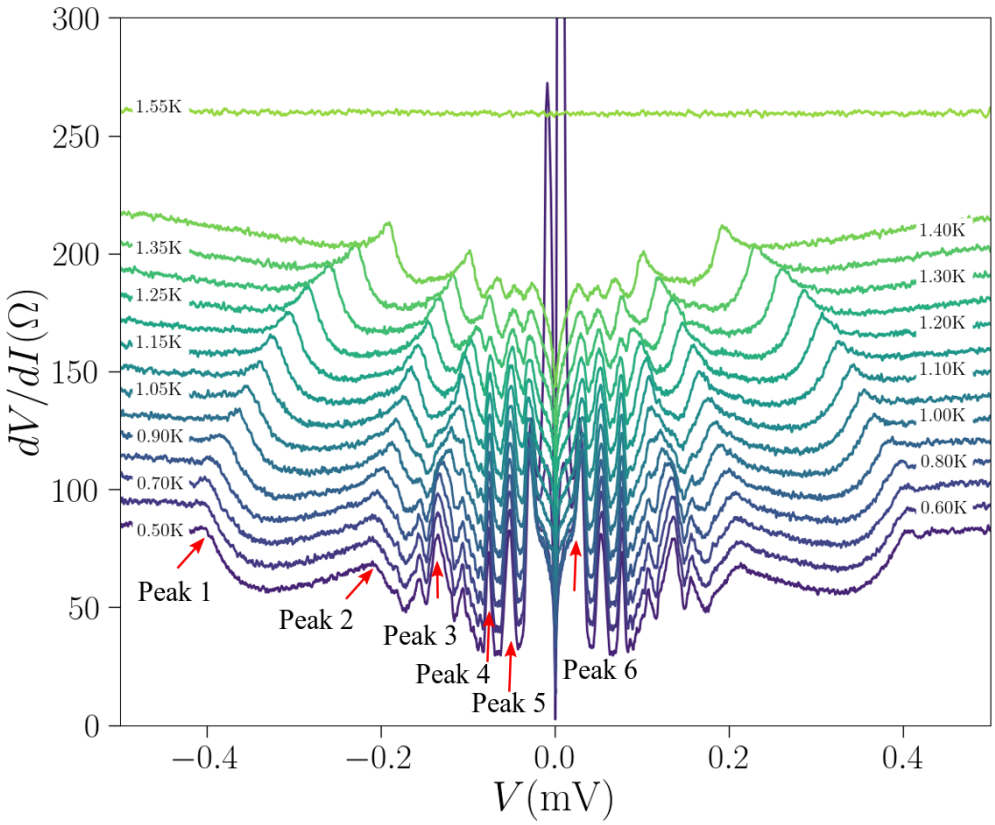

Figure 3.25 – The measured resistance (dV/dI) of the device "A1" as a function of the the voltage dropped (V) at different temperatures (T) Each curve is shifted by 10 Ω for the visibility. Here, V_g = -2 V.

Figure 3.25 shows the differential resistance (dV/dI) as a function of the voltage (V) across the device "A1" with a junction length of 200 nanometers and a junction width of 4 micrometers at different temperatures. At the lowest temperature (0.50 K), clear features are observed at approximately $V = \pm 0.4$ mV (Peak 1), ± 0.2 mV (Peak 2), and ± 0.13 mV (Peak 3). These features move towards lower voltage values as the temperature increases and disappear at T_C. These features are also called sub-gap anomalies, and they can be associated with the MAR of the first, second, and third orders, respectively. It is noticed that the resistance decreases when the order of MAR increases. It implies the high transparency of the junction, as the probability of the Andreev reflection is greater than the normal reflection. In addition to those peaks, we also observed additional peaks at $V = \pm 0.77$ mV (Peak 4), ± 0.53 mV (Peak 5), and ± 0.28 mV (Peak 6). These peaks (Peak 4, Peak 5, and Peak 6) are not moving when the temperature changes and disappear at a

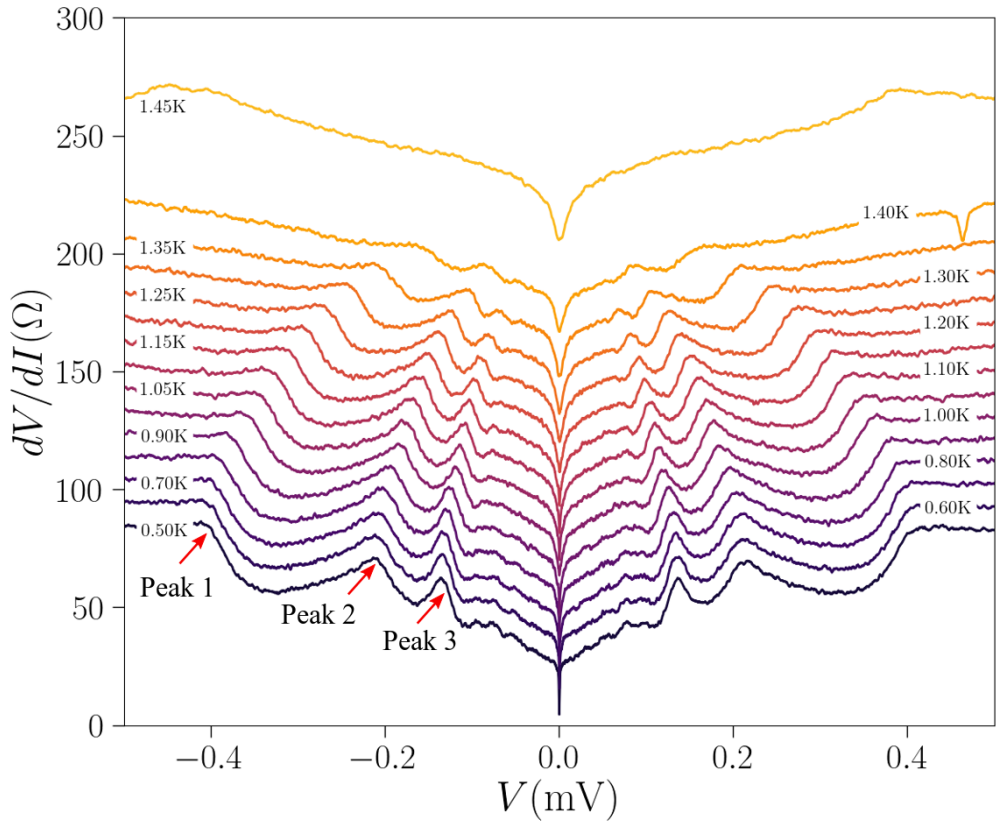

Figure 3.26 – The measured resistance (dV/dI) of the device "A1" as a function of the the voltage dropped (V) at different temperatures (T) Each curve is shifted by 10 Ω for the visibility. Here, V_g = -2 V, and $B_\perp$ = -2 mT.

small magnetic field (-2 mT), as demonstrated in Figure 3.26.

From Figures 3.25, and 3.26, we extract the positions of the features with respect to the voltage dropped as a function of the temperature. Figure 3.27(a) shows the plots of the extracted positions that correspond to the MAR up to the third order at the different temperatures. Since the first three peaks (Peak 1, Peak 2, and Peak 3) are expected to be the sub-gap features of the superconducting gap, we can estimate the superconducting gap of the aluminum leads using the linear regression method with the equation $V = 2\Delta/ne$. The extracted superconducting gap as a function of the temperature compared with the Bardeen-Cooper-Schrieffer theory of superconductivity (BCS theory) is plotted in Figure 3.27(b).From the theory, the predicted gap is given by [27]:

$$\frac{\Delta(T)}{\Delta_0} \approx 1.74(1 - \frac{T}{T_C})^{1/2}, \tag{3.11}$$

where $\Delta(T)$ is the superconducting gap at a certain temperature. T, Δ_0 is the

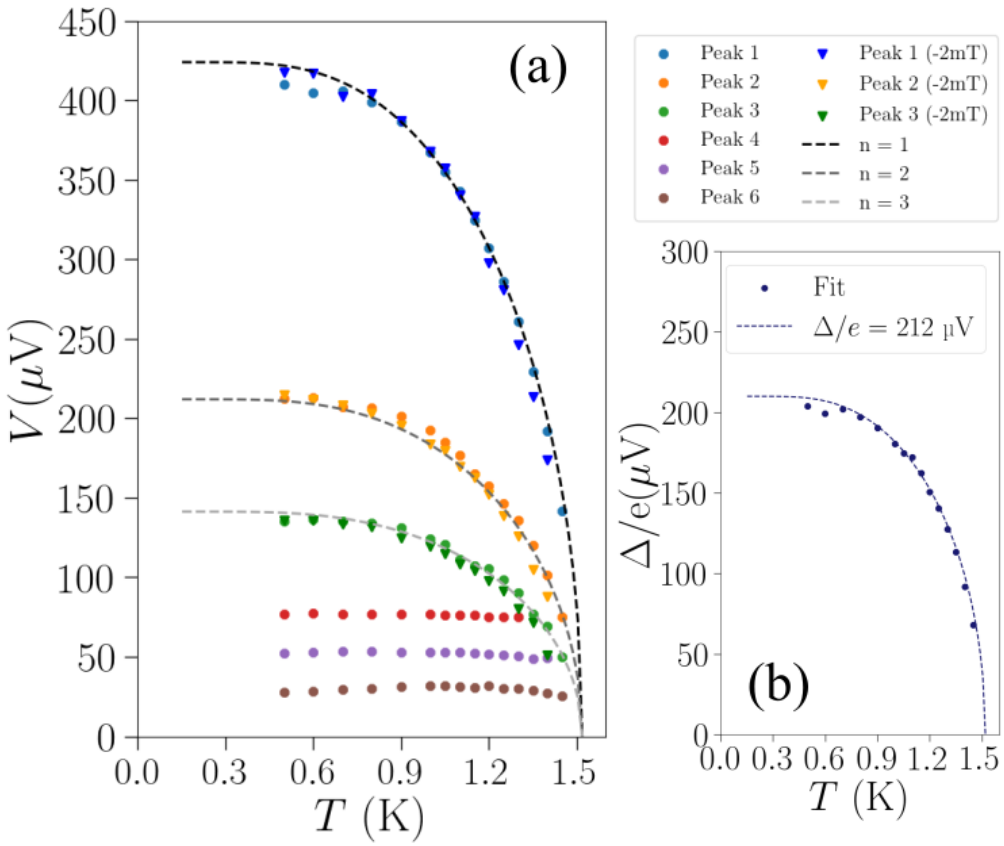

Figure 3.27 – (a) The measurement of the temperature dependence of the position in the voltage of the sub-gap features (Peak 1, Peak 2, Peak 3, Peak 4, Peak 5, and Peak 6) extracted from the curves in Figure 3.25, and Figure 3.26. (b) The derived superconducting gap (Δ) as a function of the temperature (T). The dashed lines in the figure represent the behavior of the superconducting gap according to Equation 3.11.

superconducting gap as the zero temperature, and T_C is the critical temperature.

From the data, Δ_0 is extracted to be 212 μeV. There is a small mismatch between the derived gap value and the value calculated from the equation $\Delta(T = 0) = 1.764 k_B T_C = 231$ μeV for the critical temperature of 1.52 K.

3.5.3 MARs: Dips or Peaks?

Figure 3.28 shows the resistance (dV/dI) as a function of the voltage drop (V) of the JoFETs with different junction lengths at V_g = -2 V, and at a temperature of 500 mK. The red dashed lines are plotted at the position in voltage where we expected the features related to MARs of the first and second orders. Qualitatively, we noticed that the shape of the features is significantly different for the device

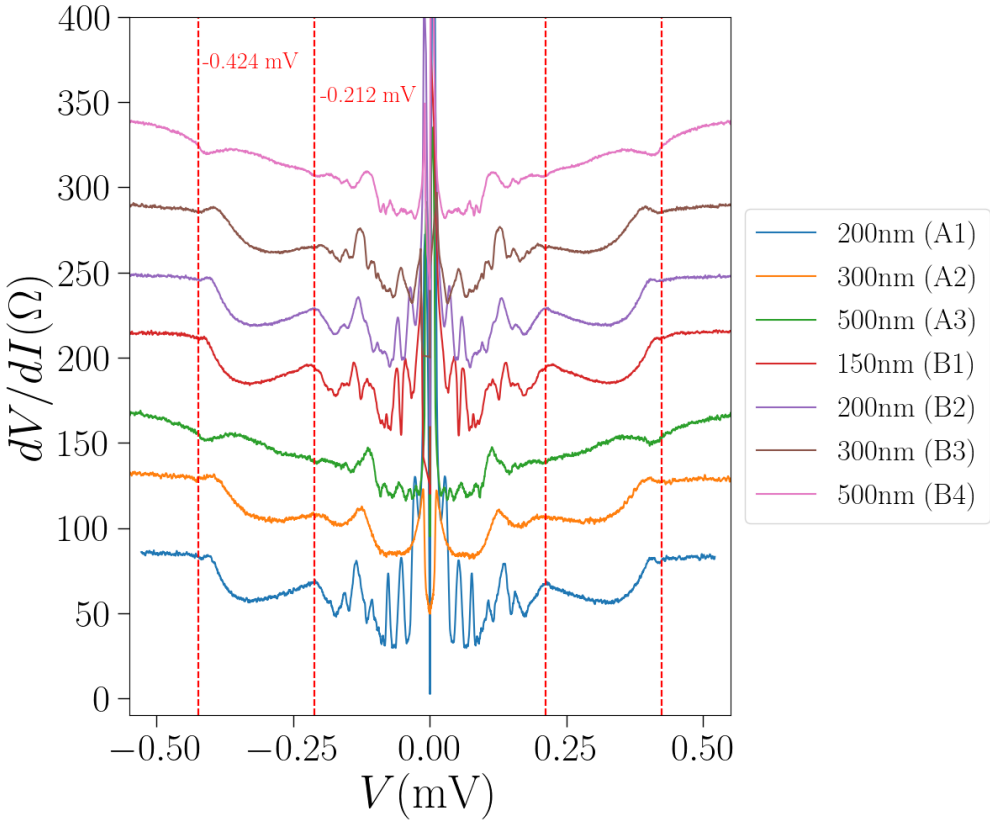

Figure 3.28 – Measured resistance (dV/dI) of several devices as a function of voltage dropped (V) at V_g = -2 V, and T = 500 mK. The red dashed lines mark the position in voltage where $V = 2\Delta/ne$ for n = 1, and 2.

with a junction length of 500 nm ("A3", and "B4") compared with the rest of the devices, as they appear to be dips instead of peaks.

Firstly, we attempt to describe the shape of the feature using a simple model where the current depends on the order of MARs and the transparency of the junction. The equation describing the current is given by [90]:

$$I(V) \approx (n+1)\tau^{n+1}V, \tag{3.12}$$

where n is the order of MARs, and τ is the transparency of the junction.

Figure 3.29 displays the I-V curves plotted from this equation at different values of τ. According to the model, when τ is low, the current from higher-order MARs decreases with n, resulting in the stair-case-shaped features, as shown by the green ($\tau = 0.4$) and red ($\tau = 0.3$) lines in Figure 3.29. Conversely, when τ is high, as demonstrated by the blue ($\tau = 0.9$) and orange ($\tau = 0.7$) lines, the rate of decrease is lower, and the current due to higher-order MARs still contributes significantly to the total current.

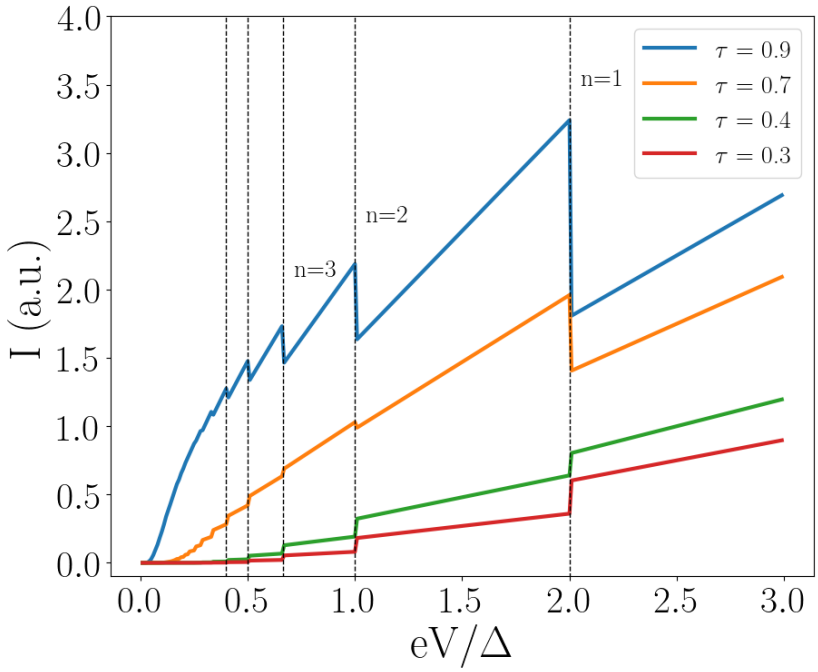

Figure 3.29 – Current (I) through the junction from the simple model (Equation 3.12).

From this simple model, we can observe that τ can affect the qualitative shape of the features in the I-V curves caused by MARs.

Further, we can use the extension of BTK formalism by Flensberg et al. [82] for the case of S-N-S junction with barriers "$H\delta(x)$" at each S-N interface (see Figure 3.30).

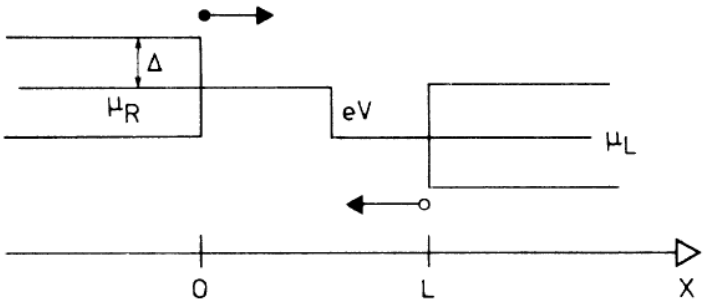

Figure 3.30 – Schematic diagram of the S-N-S junction in this model. The figure shows chemical potential of the leads (μ_R, and μ_L), superconducting gap (Δ), voltage bias between two leads (eV), and an eletron moving to the right and a hole moving to the left. The potential barriers "$H\delta(x)$" are located at $x = 0$, and L. The figure is reproduced from [82].

In this model, we categorize quasiparticles into two subpopulations: $f_{\rightarrow}(E,x)$ and $f_{\leftarrow}(E,x)$ for quasiparticles moving to the right and to the left, respectively. The axis along the junction is denoted as x, where the "N" region is in between $x = 0$ and $x = L$. Based on the model, we assume that quasiparticles moving to the right (left) at $x = 0$ ($x = L$) are the sum of Andreev-reflected, normally reflected, and transmitted electrons and holes at the terminal of the "N" region. Additionally, a quasiparticle gains energy of eV when it traverses the normal region under the applied bias.

From these assumptions, we can write three equations as follows [82]:

$$f_{\rightarrow}(E,0) = A(E)[1 - f_{\leftarrow}(-E,0)] + B(E)f_{\leftarrow}(E,0) + T(E)f_0(E), \tag{3.13}$$

$$f_{\leftarrow}(E,L) = A(E)[1 - f_{\rightarrow}(-E,L)] + B(E)f_{\rightarrow}(E,L) + T(E)f_0(E), \tag{3.14}$$

$$f_{\rightleftarrows}(E,L) = f_{\rightleftarrows}(E - eV, 0). \tag{3.15}$$

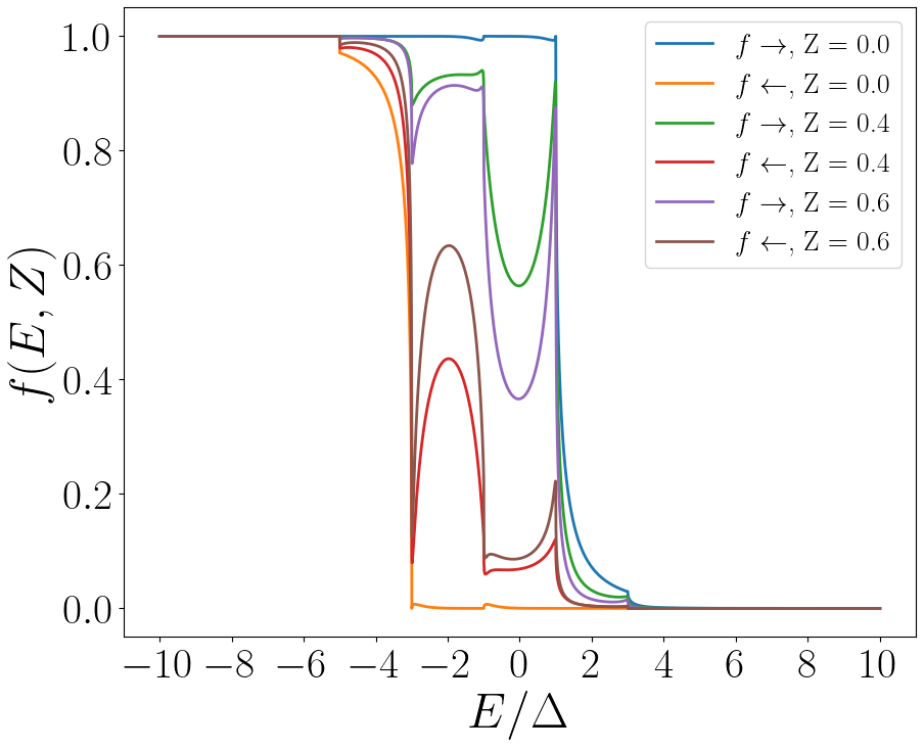

Figure 3.31 – Distribution functions $f_{\rightarrow}(E)$ and $f_{\leftarrow}(E)$ for $Z = 0$, 0.4, and 0.6. Here, we simulate the result at $T = 0.25T_C$, and $eV = 2\Delta$. The current (I) is proportional to the enclosed area between $f_{\rightarrow}(E)$ and $f_{\leftarrow}(E)$ in the graph.

Here, $A(E)$, $B(E)$, and $T(E)$ represent the probabilities of Andreev reflection, normal reflection, and transmission, respectively. Additionally, $f_0(E)$ denotes the Fermi distribution at a given temperature.

Since $A(E)$, $B(E)$, and $T(E)$ are even functions in energy space, the distribution of electrons with energy E moving to the right will resemble the distribution of holes with energy $-E$ moving to the left. This relationship can be expressed in the equation [82]:

$$f_{\rightarrow}(E,0) = 1 - f_{\leftarrow}(-E - eV, 0). \tag{3.16}$$

Then we can obtain the distribution function $f_{\rightarrow}(E)$ in a form of [82]:

$$f_{\rightarrow}(E) = A(E)f_{\rightarrow}(E - eV) + B(E)[1 - f_{\rightarrow}(-E - eV)] + T(E)f_0(E). \tag{3.17}$$

This equation exclusively involves electrons moving in the same direction, which we can solve self-consistently. Figure 3.31 presents the distribution function $f(E)$ at a bias of $eV = 2\Delta$ as a function of scaled energy (E/Δ) at various values of Z at a temperature of $T = 0.25T_C$.

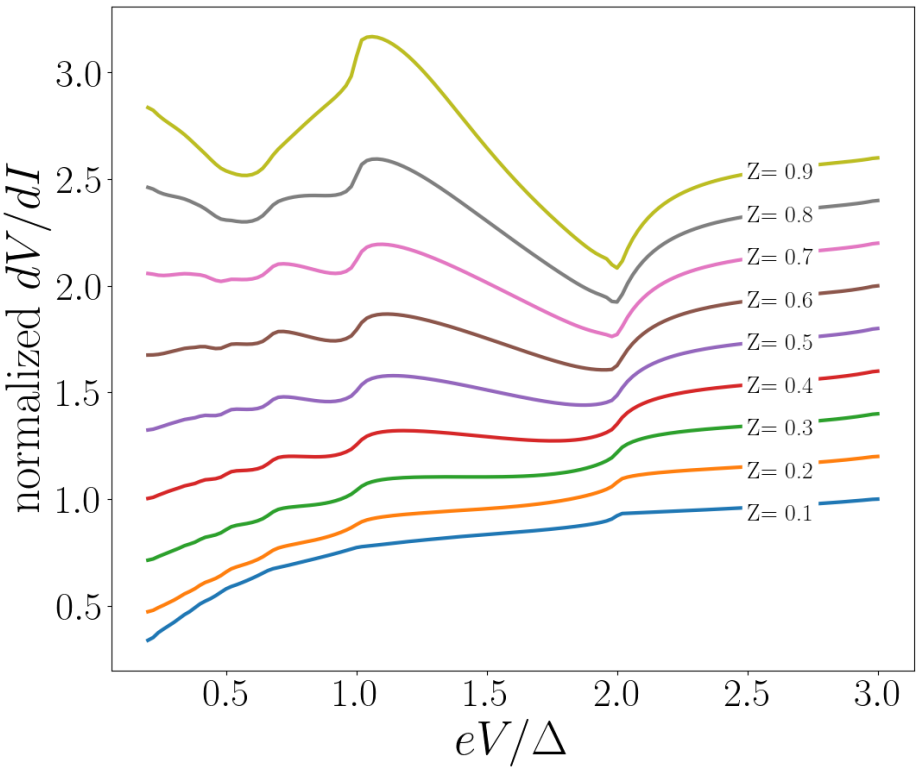

Figure 3.32 – Differential resistances (dV/dI) as a function of normalized voltage bias (eV/Δ) at $T = 0.25T_C$ for various value of Z.

Then, the current through the junction is governed by the sum of the number of particles flowing in each direction, as written in the equation [82]:

$$I = \frac{1}{eR_N} \int_{-\infty}^{\infty} [f_{\rightarrow}(E) - f_{\leftarrow}(E)]dE, \tag{3.18}$$

where I represents the current, and R_N is the normal state resistance of the junction. Consequently, we can compute I for different values of the voltage bias eV using the equation above.

Figure 3.32 illustrates the resistance (dV/dI) as a function of scaled voltage bias (eV/Δ) for various values of Z at $T = 0.25T_C$. From the figure, it becomes evident that the peak-like features at voltages where $2\Delta/eV = n$ in the low barrier case (e.g., $Z = 0.1$ in the blue curve) transition to dip-like features when Z is higher.

We employed two methods to estimate the parameter Z for use in the simulation and compared the results with experimental data. In the first method, we fitted the experimental data to the simulated data while excluding the experimental data below $2eV/3\Delta$ from the fit. This is for excluding some unidentified features in the experimental data that could not be related to MARs. For the second method, we extracted the normalized excess current ($eI_{exc}R_N/\Delta$) from the experiment and estimated the value of Z using the OBTK formalism.

Figure 3.33 (Figure 3.34) displays the resistance (dV/dI) of device "B2" ("B4") as a function of scaled voltage (eV/Δ) at V_g = -2V and $T = 400$ mK (approximately $0.26T_C$). In these figures, we have plotted the experimental results alongside the simulation results at $T = 0.25T_C$. The simulated results have been normalized by the R_N value extracted from the experimental data.

Qualitatively, the overall shape of the curve of the experimental results in the case of $L = 200$ nm seems to agree more with the simulation result compared with the case of $L = 500$ nm. This can be explained by the fact that we only considered the interface scattering in the OBTK formalism and neglected the scattering in the normal region. In the case of a shorter junction, there was less scattering inside the normal region. Additionally, the devices may comprise many conducting channels, while the OBTK formalism is first derived for the case of a single conducting channel. Using the OBTK formalism by assuming that we are looking at the average behavior of all the channels can be considered oversimplifying the system. To improve the accuracy of the simulation, we may have to use the multiple channel model that also considers the scattering inside the normal region [90, 91].

3.5.4 Magnetic field dependency

Figure 3.35 depicts the resistance (dV/dI) of the device labeled "A1" as a function of voltage drop (V) for various values of the perpendicular applied magnetic field ($B_{\perp}$) at $V_g = -2V$ and $T = 500$ mK. Below an applied magnetic field of 10 mT, the features associated with MARs up to the third order are clearly noticeable. However, the voltage positions of these features do not shift significantly

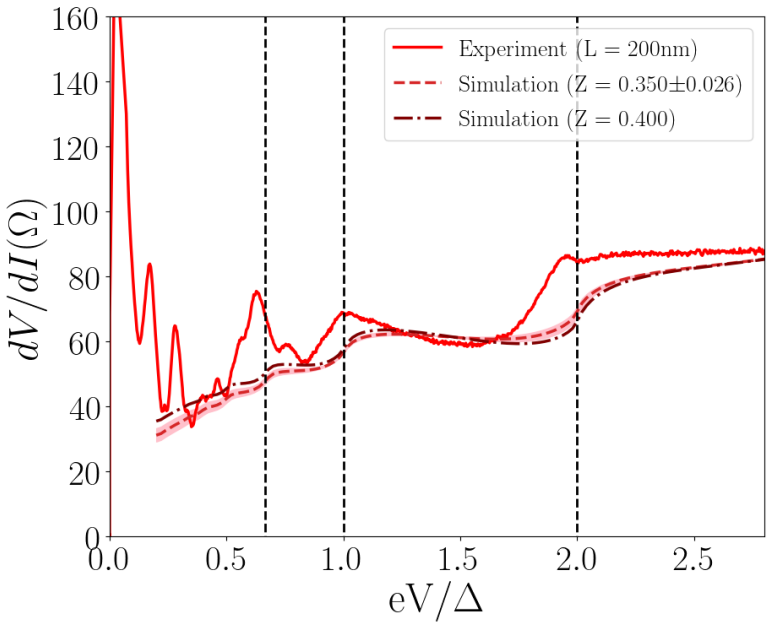

Figure 3.33 – The measured resistance (dV/dI) of the device "B2" as a function of normalized voltage (eV/Δ). The experimental data is plotted along with the simulation where Z are estimated from the curve fit ($Z = 0.350$), and from the excess current ($Z = 0.400$).

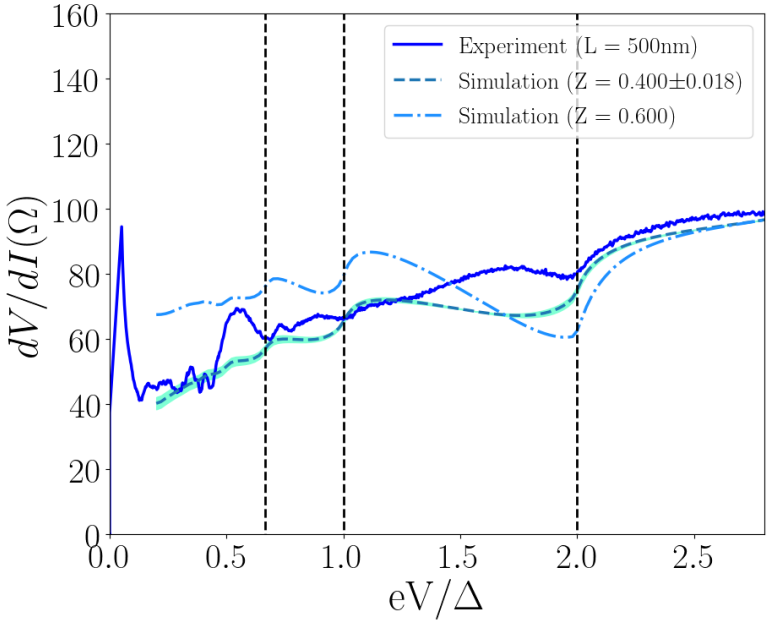

Figure 3.34 – The measured resistance (dV/dI) of the device "B4" as a function of normalized voltage (eV/Δ). The experimental data is plotted along with the simulation where Z are estimated from the curve fit ($Z = 0.400$), and from the excess current ($Z = 0.600$).

below 10 mT. We also observed Peak 4, Peak 5, and Peak 6, similar to those in Figure 3.25, which disappear at very low magnetic fields.

Above 10 mT, the features become much less pronounced, making it difficult to extract their positions in voltage. Nevertheless, we still observed some non-linearity features in the curve up to at least 40 mT. These non-linearity features could originate from the superconductivity of aluminum. This implies that the Al leads have a critical field above 40 mT, which is higher than the value reported for pure Al material [92]. This could be due to the fact that the Al leads are made of thin film granular Al. This is in good agreement with the observation that we found T_C to be higher than pure Al material as well.

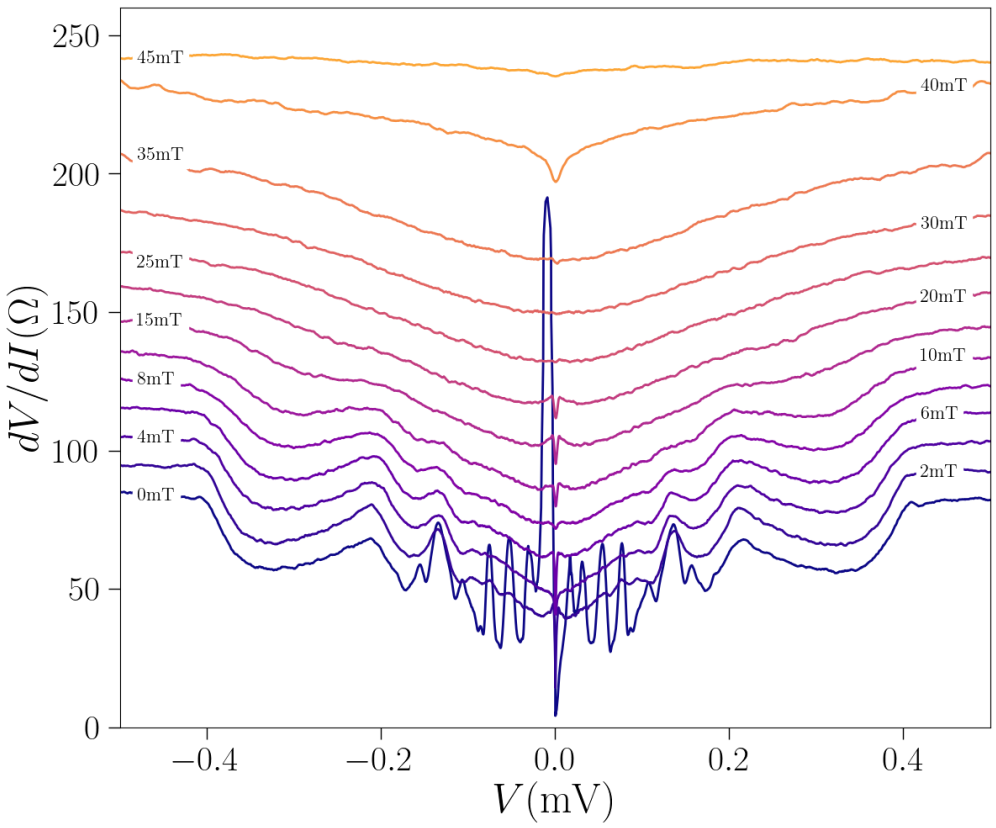

Figure 3.35 – The measured resistance (dV/dI) of the device "B1" as a function of the the voltage dropped (V) at applied magnetic field (B) Each curve is shifted by 10 Ω for the visibility. Here, V_g = -2 V, and T = 500 mK. The non-linearity features are observed for B below 40 mT.

3.5.5 Some ideas on the features that can not be associated to MARs

As we have seen earlier, we observed some strange peaks in the finite-voltage regime of the I-V curves those can not be related to MARs. We have several hypotheses about that.

Figure 3.36(upper) shows the resistance (dV/dI) as a function of current (I) and magnetic field ($B_\perp$) of the device "A1" at V_g = -2 V at a temperature of 500 mK. We recognized the Fraunhofer diffraction pattern and the strange peaks on the curve. We noticed that the strange peaks became less visible at the node of the Fruanhofer diffraction, so they may have an origin related to the supercurrent. In Figure 3.36(lower), we plot dV/dI as a function of normalized voltage (V/V_0) and $B_\perp$. The voltage dropped has been normalized by V_0 = 26.5 µV. We found that the strange peaks seemed to be equally spaced in voltage. From these two plots, we suspect that the strange peaks could be the Shapiro steps due to some radiofrequency signal that can pass inside the dilution refrigerator, despite several shielding layers. We could estimate the frequency of this signal to be $f = 2eV_0/h (\approx$ 13.5 GHz, in the super high frequency (SHF) band). Considering that the SHF band is commonly used in satellites telecommunications, this could be a possible explanation for the origin of these strange peaks.

Alternatively, the features could be originated from the interference of the particles at some length scale, as observed and explained qualitatively by G. Bastian et al. [93]. In their explanation, the particles are trapped in a cavity formed by two interfaces when the voltage drop condition is met. This could contribute to an increase in resistance. We also consider the possibility of Rowell-McMillan oscillations [94–96], where the particles are oscillating between two superconducting interfaces, causing the resonant features when $\Delta V = hv_{FN}/4ed_N$, where v_{FN} is the Fermi velocity in the normal region and d_N is the effective length that particles travel in the normal region. However, a systematic study may be needed to reach a solid conclusion on the origin of the strange peaks.

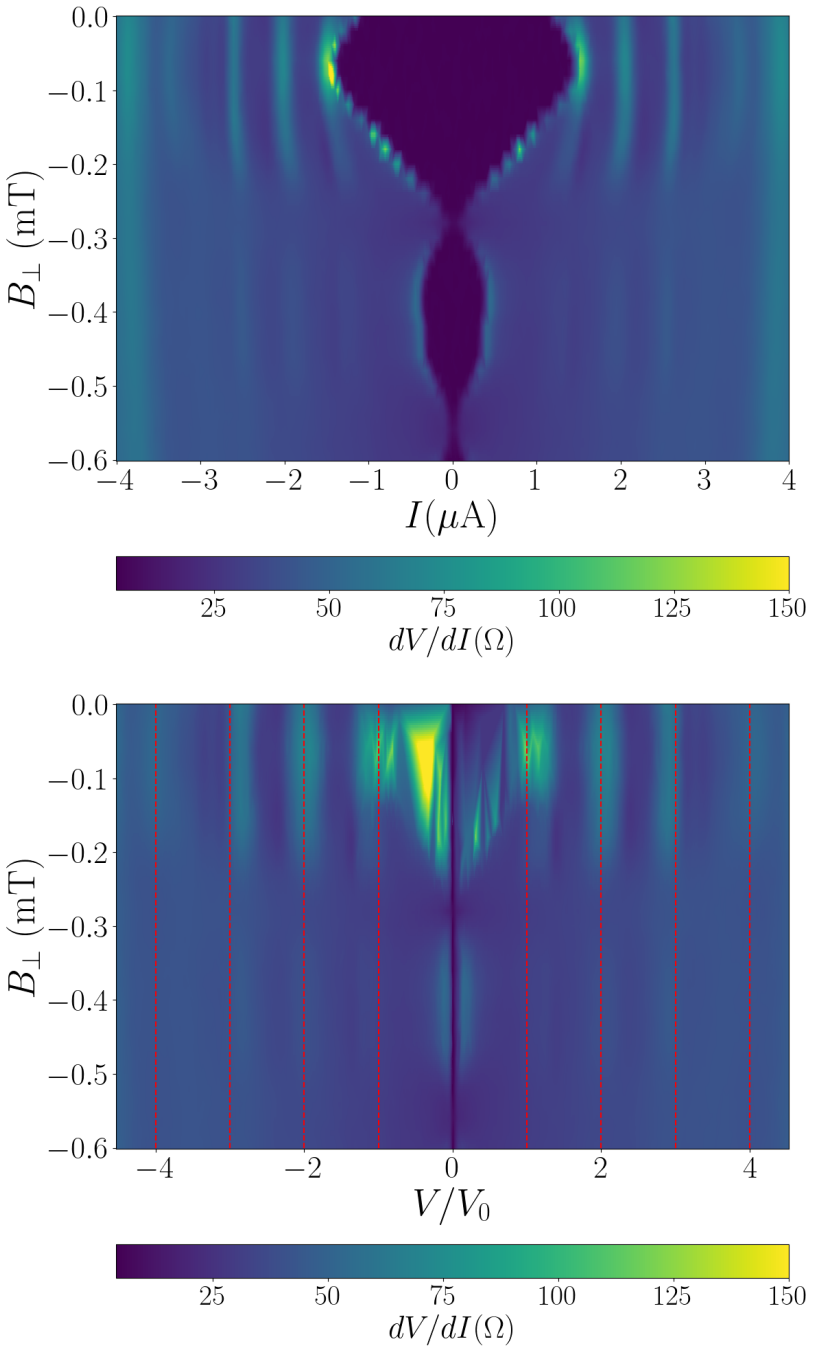

Figure 3.36 – (upper) The resistance (dV/dI) of device "A1" as a function of current (I) and out-of-plane magnetic field ($B_\perp$). There observed the strange peaks just outside the zero resistance state. (lower) dV/dI as a function of scaled voltage (V/V_0) and $B_\perp$. The red dashed lines show that the positions in voltage of the strange peaks are equally spaced. Here, V_g = -2 V, V_0 = 26.5 µV, and T = 500 mK.

CHAPTER 4

Superconducting resonators

A superconducting resonator is a device comprising capacitors and inductors. To make it become lossless, the elements are made of superconducting materials and operate at a temperature below the critical temperatures (T_C) of the materials. It has various applications in quantum information, such as performing qubit readout or mediating the interaction at a quantum level. In this chapter, we present our study on superconducting resonators as part of our goal to realize the gatemon on SiGe heterostructures. First, we review the basic model equations necessary to perfom simulations. The equations and simulation results are used to design the resonators. After that, we discuss the fabrication process of NbN superconducting resonators on the SiGe material platform and present their low temperature behavior. Lastly, we discuss the challenges and problems we encountered, as well as our perspective on gatemon integration.

4.1 Theory and simulation

4.1.1 Coplanar waveguide resonators: short introduction

In this thesis, we conducted a study on resonators employing coplanar waveguide (CPW) geometry, focusing on one of the simplest configurations: "conventional coplanar waveguide on a dielectric substrate of finite thickness." The CPW comprises a central strip of conductor with a width s, separated by semi-infinite ground planes at a distance w on both sides, as illustrated in Figure 4.1. This structure is deposited onto a dielectric material of thickness h, and a relative per-

mittivity ε_r. With this particular configuration, the capacitance per unit length, and the inductance per unit length can be expressed, using conformal mapping techniques assuming transverse electromagnetic (TEM) propagation along the central strip, by the equations [97, 98]:

$$C_l = C_{air} + C_r = 4\varepsilon_0 \frac{K(k_0)}{K(k_0')} + 2\varepsilon_0(\varepsilon_r - 1)\frac{K(k_1)}{K(k_1')}, \tag{4.1}$$

and

$$L_l = \frac{\mu_0}{4}\frac{K(k_0')}{K(k_0)}, \tag{4.2}$$

where the variables $k_0 = s/(s+2w)$, $k_0' = \sqrt{1-k_0^2}$, $k_1 = \sinh(\pi s/4h)/\sinh[\pi(s+2w)/4h]$, and $k_1' = \sqrt{1-k_1^2}$ are defined based on the CPW's geometry. The function $K(x)$ represents the complete elliptic integral of the first kind for a variable x.

Equation 4.1 can be rewritten as:

$$C_l = 4\varepsilon_0\varepsilon_{eff}\frac{K(k_0)}{K(k_0')}, \tag{4.3}$$

where the effective permittivity of the substrate, ε_{eff}, is given by:

$$\varepsilon_{eff} = 1 + \frac{\varepsilon_r - 1}{2}\frac{K(k_1)}{K(k_1')}\frac{K(k_0')}{K(k_0)}. \tag{4.4}$$

The characteristic impedance of the CPW is given by [97]:

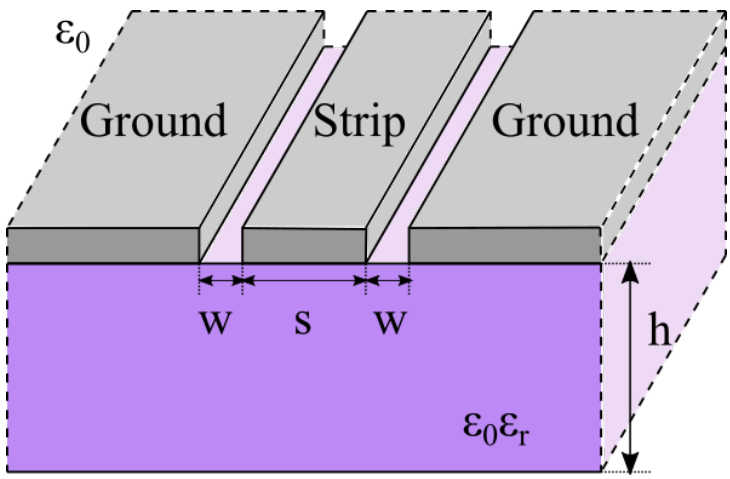

Figure 4.1 – The schematic illustrates a conventional coplanar waveguide (CPW) positioned on a dielectric substrate with finite thickness. The CPW consists of a central strip with a width of s, sided by semi-infinite ground planes separated by a gap of w on both sides.

$$Z_0 = \frac{1}{c\sqrt{\varepsilon_{eff}}C_{air}} = \frac{\sqrt{L_l}}{\sqrt{C_l}} \tag{4.5}$$

In this study, we aim to realize half-wavelength CPW resonators [99], where the voltage distribution across the resonators is maximized at both ends. This configuration is more practical for our application, as it allows the resonator to effectively mediate the signal between the transmission line and the qubit at both ends.

The resonance frequency of a half-wavelength CPW resonator is given by [100]:

$$f_0 = \frac{1}{2l\sqrt{L_l C_l}}, \tag{4.6}$$

where l is the total length of CPW.

We evaluate the performance of a resonator using a parameter called the quality factor (Q), defined as [101]:

$$Q = 2\pi f_0 \frac{energy\ stored}{power\ loss}. \tag{4.7}$$

In practice, the quality factor of a resonator on a chip comprises two components defined as:

$$\frac{1}{Q} = \frac{1}{Q_i} + \frac{1}{Q_c}, \tag{4.8}$$

where Q_i, and Q_c are referred to as the internal quality factor, and the coupling quality factor, respectively. Q_i corresponds to the dielectric loss of the substrate and the material, while Q_c corresponds to the dissipation of energy due to coupling with the environment, such as a qubit or a transmission line.

The quality factor is related to the photon loss rate (κ) of the resonator by the relation $\kappa/2\pi = f_0/Q$. In practice, our goal is to achieve a resonator with κ below 2 MHz for use in dispersive readout applications. Q, Q_i, Q_c and f_0 can be extracted from measurements of the transmission spectrum.

4.1.2 Simulation method

Before working on the fabrication process, we conducted simulations to anticipate the expected outcomes. The practical steps of our study in the simulation section are outlined as follows:

1. We implemented Equations 4.2, 4.3, 4.5 and 4.6 using simple Python codes to estimate the values of Z_r, L, C, and f_r for a resonator with specific geometry. Our goal here was to achieve f_r in the range of 4 to 8 GHz, and an impedance (Z_r) of 50 Ω to ensure impedance matching with other microwave elements.

2. A GDS design of a coplanar waveguide was created, utilizing the width and gap dimensions calculated in Step 1. Subsequently, we applied this design to the SONNET simulation software to validate the accuracy of our calculations. We expected that the simulation results would also yield $Z_r = 50\ \Omega$.

3. We generated a GDS design of a coplanar waveguide acting as a transmission line, positioned adjacent to a metal strip which serves as a component of a resonator coupling to the transmission line. Subsequently, we conducted simulations to analyze the mutual coupling capacitance (C_c) existing between these two elements. We further estimate Q_c using equation [100]:

$$Q_c = \frac{\pi}{4\pi^2 f_r^2 Z_r C_c^2 Z_0}, \tag{4.9}$$

where Q_c, f_r, C_c, Z_r, and Z_0 represent the coupling quality factor, the resonance frequency of the resonator, the simulated coupling capacitance, the characteristic impedance of the resonator, and the characteristic impedance of the transmission line, respectively.

We tuned Q_c by adjusting the spacing between the transmission line and the metal strip, or by adjusting the length of the coupling metal strip. Our target is to achieve a Q_c value of approximately 2000 to 3000, with f_r in the range of 4 to 8 GHz.

4. Finally, we created a full GDS design of a complete resonator coupled to a transmission line. Subsequently, we simulated this design using SONNET and compared the estimated values with the result obtained from the simulation.

Figure 4.2 shows a simulation result of a full resonator coupling to a transmission line. In the design depicted in Figure 4.2(a), the resonator is a CPW ($s = 13\ \mu$m, $w = 10\ \mu$m) with the length of 7900 μm, resulting in a calculated resonant frequency $f_{r,calculated} = 6.668$ GHz. The simulating layers consist of an infinitesimal thin lossless Al layer on 1 mm of $Si_{0.21}Ge_{0.79}$ ($\varepsilon_r = 15.2$, derived using a linear approximation from $\varepsilon_{Si} = 11.7$, and $\varepsilon_{Ge} = 16.1$ [78]) as shown in Figure 4.2(b). The simulation result in Figure 4.2(c) presents $f_{r,simulation} = 6.133$ GHz and $Q_c = 2021$, aligning with our expected range. The observed downshift in the resonant frequency could be due to the effect of the coupling capacitor, which is added up to the total capacitance and increases the denominator in Equation 4.6. Noted that, in the simulation, we treat the Al layer assuming it has no kinetic inductance.

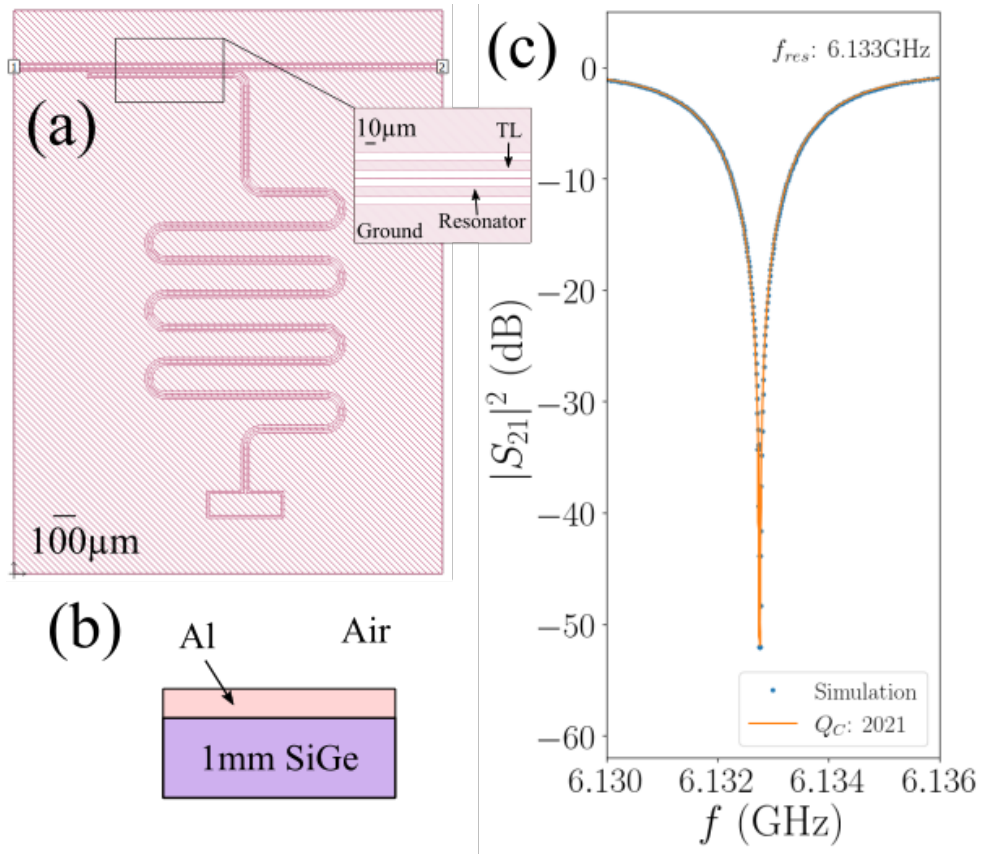

Figure 4.2 – (a) A design, consisting a superconducting resonator coupling to a transmission line, implemented in SONNET simulation software. (b) Schematic depicting the cross-section of the layer in (a). (c) Simulation result showing resonance at 6.133 GHz with a coupling quality factor (Q_c) of 2021.

4.2 Fabrication of NbN superconducting resonators

In this experiment, we realized NbN superconducting resonators on a SiGe heterostructure. We used thin film of NbN as the material for the resonators for two primary reasons. Firstly, NbN thin film exhibits a critical temperature (T_C) exceeding 8 K. Then, we can perform preliminary measurement at 4.2 K using enclosed vacuum chamber in liquid helium. This measurement tool is more accessible compared to the dilution refrigerator, and also yields faster feedback. Secondly, our aim is to investigate the integration of NbN material, high kinetic inductance material, onto the SiGe heterostructure. This step is a part of our plan to utilize NbN for making an on-chip LC filter in the future.

4.2.1 NbN thinfilm

The initial step in realizing the NbN resonators involves the preparation and characterization of NbN films. The thin films used in this experiment was grown, employing the sputter deposition technique, on a SiGe virtual substrate, which constitutes a layer (approximately 800 microns) of $Si_{0.21}Ge_{0.79}$ on a Si substrate. The virtual substrate was cleaved into small pieces (approximately 2 $\times$ 2 cm^2 each), and cleaned using acetone and isopropanol. Subsequently, the samples were introduced into a deposition chamber at 180°C under vacuum. The samples underwent a thermalization process within the chamber for a duration of fourteen hours before launching the deposition process. The growth recipe used in this thesis has been adapt from the recipe previously used in our group [100, 102].

The deposition has been done with reactive sputtering of a 3-inch-diameter Nb target in an atmosphere of Ar and N_2. The deposition configuration was set to confocal mode.

We characterized NbN films by measuring square resistances ($R_\square$) and critical temperatures (T_C) using the Physical Properties Measurement System (PPMS). The measurement was performed by F. Gustavo. Figure 4.3 shows $R_\square$ as a function of temperature for two NbN samples. The first sample, labelled as Sample 1, is a square piece of sample with approximately 1 cm in size on each side. The voltage probes were connected with wire bonds. The two probes are separated by a distance of about the size of the sample. The second sample, labelled as Sample 2, is an NbN strip. The strip was fabricated by ICP etching using O_2 and SF_6 on a patterned photoresist. The strip width is 100 μm and the voltage probes of the strip are separated by a distance of 4000 μm. This gives a distance of 40 squares. We initially deposited 20 nm of NbN on both samples.

Both samples exhibit low resistances at room temperature. This is due to the thermally excited carriers in the SiGe material. In both curves, the figure demonstrates sharp increases in the resistances at temperatures around 180 K, which indicates the freeze-out of these thermally excited carriers. The gradual increase in resistance when the temperature decreases could be due to weak localization or the effect of disorder. The trends have been observed and reported in NbN [103]

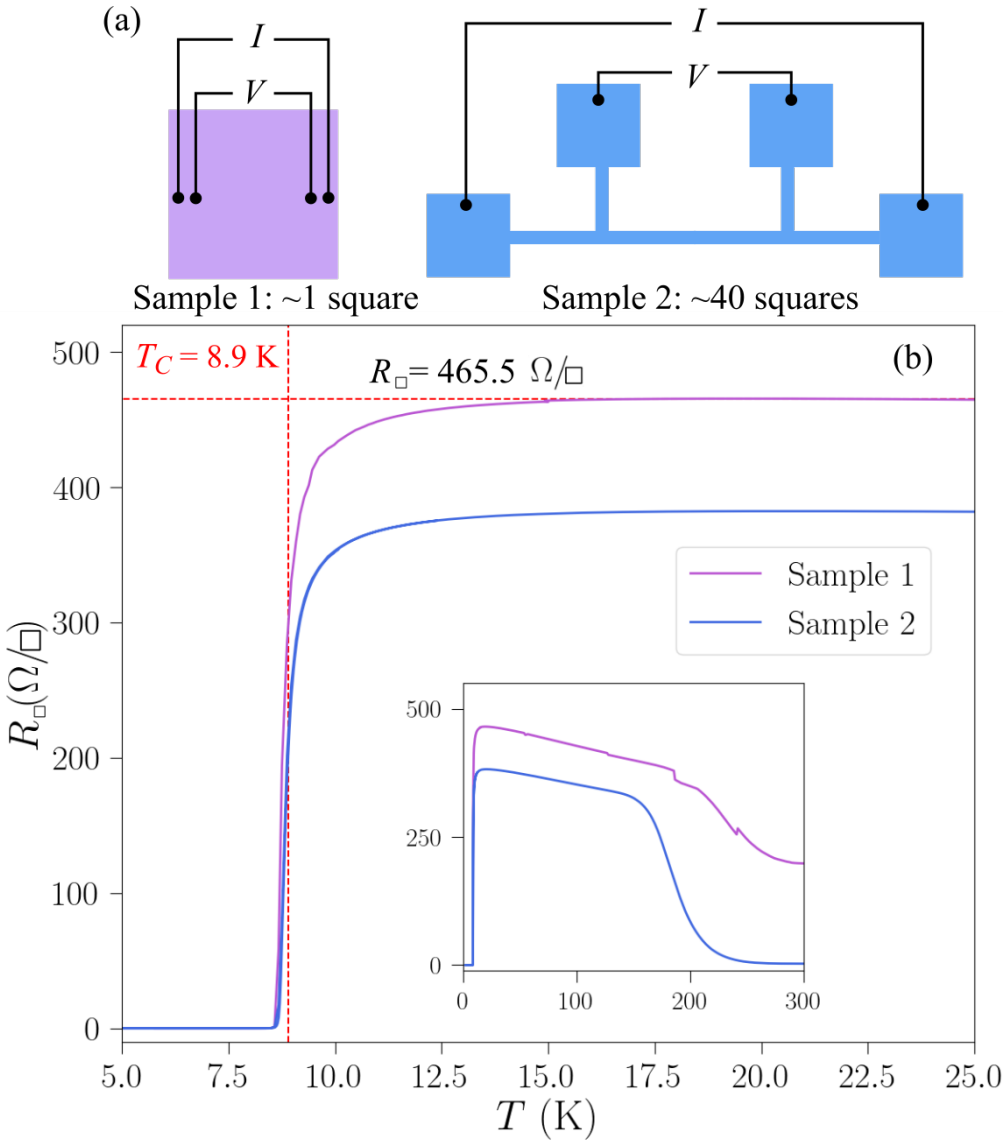

Figure 4.3 – (a) Schematic depicting the measurement setup for two samples. Sample 1 comprises a square piece of NbN on SiGe, while Sample 2 consists of an NbN strip containing approximately 40 squares, measured in a 4-point configuration. (b) Plot displaying the square resistances as a function of temperature for Sample 1 and Sample 2. Both samples exhibit a critical temperature of 8.9 K.

and granular Al [104]. The $R_\square$ before the superconducting transitions for Sample 1, and Sample 2 are measured to be 465.5 Ω/□, and 382.3 Ω/□, respectively. NbN films in both samples have T_C of 8.9 K. We calculated the kinetic inductance ($L_{k,\square}$) using the equation [105]:

$$L_{k,\square} = \frac{\hbar R_\square}{\pi \Delta} = \frac{\hbar R_\square}{1.764 \pi k_B T_C}, \tag{4.10}$$

which yields $L_{k,\square}$ equal to 71 pH/$\square$ for Sample 1 and 58 pH/$\square$ for Sample 2. The difference could be explained by the "poor" evalulation of $R_\square$ of Sample 1. However, the designs of the resonators in this chapter have been made while assuming $L_{k,\square}$ to be 71 pH/$\square$ because Sample 2 has been measured at the later stage.

4.2.2 Design and process flow

To fabricate resonators, we made the design using the information from the simulation and the NbN characterization. Here, we also took into account L_k of NbN in the inductance part to rewrite Equation 4.6:

$$f_0 = \frac{1}{2l\sqrt{(L_{k,l} + L_{g,l})C_l}}, \tag{4.11}$$

where $L_{k,l}$, and $L_{g,l}$ are the kinetic inductance per unit length, and the geometrical inductance per unit length, respectively. The former parameter is defined by $L_{k,l} = L_{k,\square}/s$, and the latter parameter can be calculated using Equation 4.2.

Figure 4.4(a) and (b) show the process flows and an example of the design of a transmission line and resonators. In general, we made lithography patterns for a sample size of 2 × 1 cm^2 of $Si_{0.21}Ge_{0.79}$ virtual substrate. After we cleaved the sample from the 200-mm wafer, we cleaned it with acetone and isopropanol. Then we deposited 20 nm of NbN film using the method mentioned in the previous section. Following that, we applied AZ1512 photoresist to the sample. It was exposed by the laser lithography technique and was developed by AZ developers. We etched the NbN using the ICP etching technique with O_2 and SF_6. After that, we made a pattern for the bonding pad layer using the same lithography technique. We deposited 300 nm of Al as a bonding pad layer to prevent chip cracking. We will discuss about this bonding pad layer later.

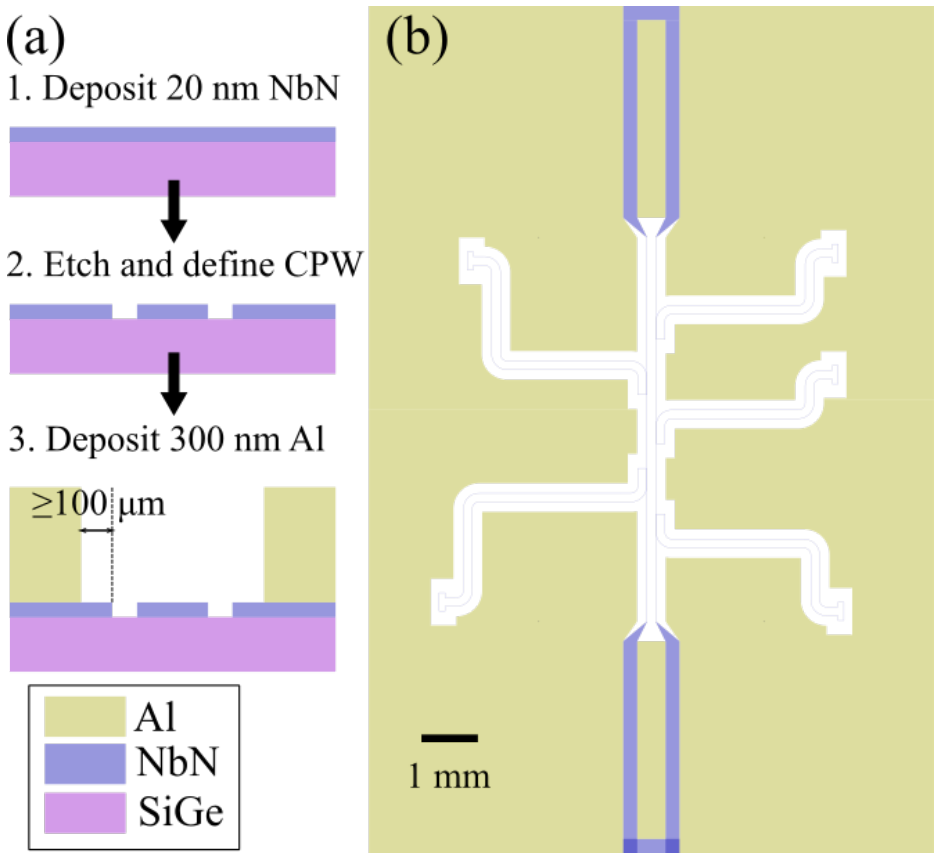

Figure 4.4 – Schematic illustrating the fabrication process of NbN resonators. (a) The process flow comprises the following steps: (1) Deposition of a 20 nm NbN layer. (2) ICP etching to define the coplanar waveguide (CPW). (3) Deposition of a 300 nm Al layer for bonding pads. (b) A graphical design system (GDS) layout corresponding to the process flow depicted in (a).

4.2.3 Device preparation

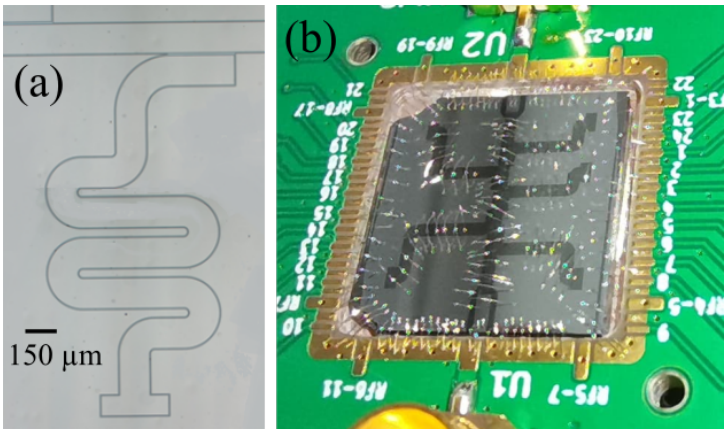

Figure 4.5 – (a) Optical image of an NbN resonator on a SiGe virtual substrate fabricated using this process flow. (b) Photo of a sample with bondings on a PCB. This is an example of a sample ready to be measured.

4

Figure 4.5(a) is an optical microscope image showing an example of a fabricated NbN resonator. To be prepared for measurements, we usually cut the sample into the size of 1 × 1 cm^2, and glued the sample to a PCB with the silver paint. Following that, we made several bondings to connect the ground plane of the CPW to the ground of the PCB as well as to connect the ground plane across the sample. In the measurement, we send the signal through microwave connectors on the PCB. We made the bonding between the transmission line and the PCB bond pads connecting to the microwave connectors. Figure 4.5(b) is an image of the sample on the PCB with bondings. The size of the golden frame on the PCB is around 1.1 × 1.1 cm^2. Noted that, Figure 4.5(a) and (b) were taken from different samples.

4.3 Characterization of NbN resonators on SiGe virtual substrates

We performed the resonator characterization of the sample in Figure 4.5(b) at a temperature of 10 mK in a dilution refrigerator setup. The output signal is generated by a vector network analyzer (VNA) CM M5180 through an attenuation of -70 dB to one end of the transmission line. The signal from another end of the transmission line is first amplified by a +39 dB amplifier (LNF-LNC4_8C) at 4 K before entering back into the input of the VNA. We put the DC blocks at both terminals of the refrigerator.

4.3.1 Basic characterization

To perform the basic characterization of the resonator, first we measured the transmission (S_{21}) as a function of frequency (f). Figure 4.6 shows the magnitude of S_{21} as a function of f at VNA output powers from -30 to 10 dBm. We observed five clear dips at every values of VNA power. These dips correspond to the resonances of the resonators. The inset in the figure shows a zoom-in of the resonance response of a resonator. There is a clear shift of the resonant frequency towards lower frequencies at high power. The resonant shift effect can be due to the nonlinearities in the NbN thin films [106].

Then, we normalized the measured S_{21}. Figure 4.7(a) shows an example of normalized magnitude ($|S_{21}|$) and normalized phase ($\angle S_{21}$) of the transmission specturm. We used the normalized data to extract the resonator parameters,

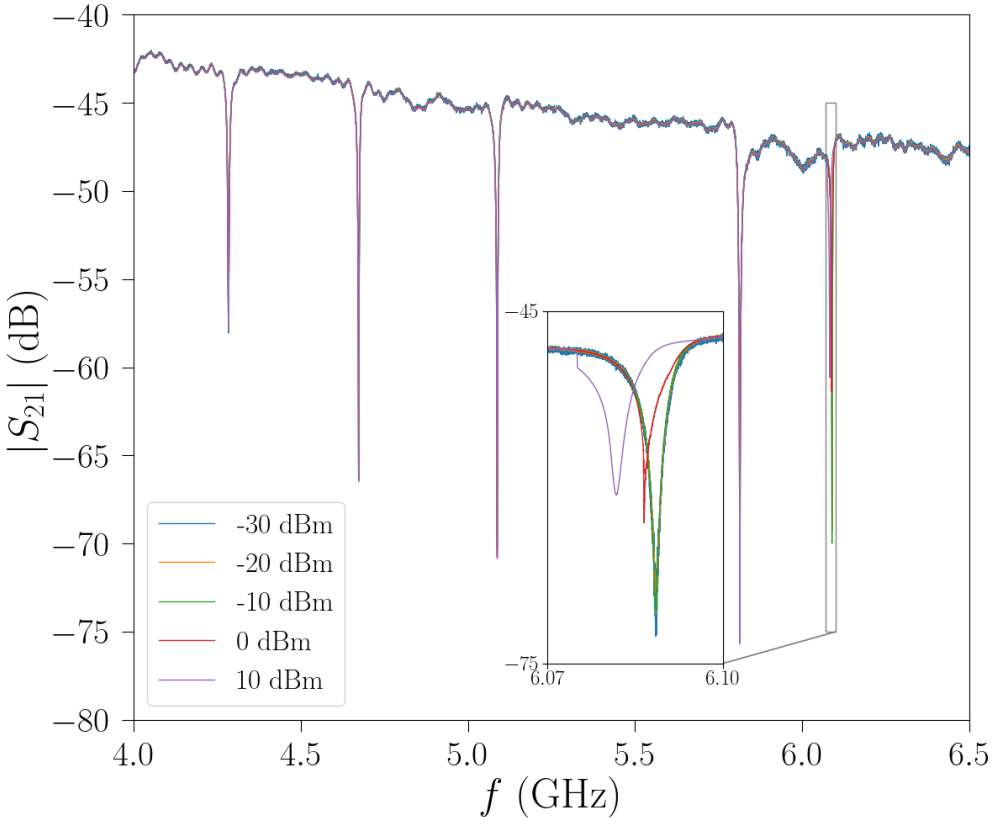

Figure 4.6 – The magnitude of the transmission ($|S_{21}|$) of the sample depicted in Figure 4.5(b) is shown as a function of frequency (f) at various VNA power levels. Five resonances corresponding to resonators positioned at 4.28, 4.67, 5.09, 5.81, and 6.09 GHz are observed. The inset illustrates the frequency shift of the 6.09 GHz resonator with changing VNA power. The measurement temperature is set at 10 mK.

including f_0, Q_i, and Q_c. We normalized the transmission data by setting the transmission background to 0 dB, and removing the phase shift and the electronic delay due to the experimental setup. The normalized transmission can be described by the equation [107]:

$$\tilde{S}_{21}^{-1} = 1 + \frac{Q_i}{Q_c} e^{i\phi} \frac{1}{1 + i2Q_i\delta x}, \tag{4.12}$$

with $\delta x = (f - f_0)/f_0$, and $\tilde{S}_{21}$, Q_i, Q_c, and ϕ are normalized transmission data, the internal quality factor, the coupling quality factor, and the impedance mismatch, respectively.

Figure 4.7(b) represents $\tilde{S}_{21}^{-1}$ in the complex plane. The experimental data is represented by dots, and the circle fit is illustrated by the red line. Within the complex plane, the data at $\tilde{S}_{21}^{-1} = 1$ represents the data far away from the resonance. Further, from Equation 4.12, we can see that $\tilde{S}_{21}^{-1} = 1 + e^{i\phi}Q_i/Q_c$ at resonance $f = f_0$. Thus the diameter (D) is determined by $D = Q_i/Q_c$,

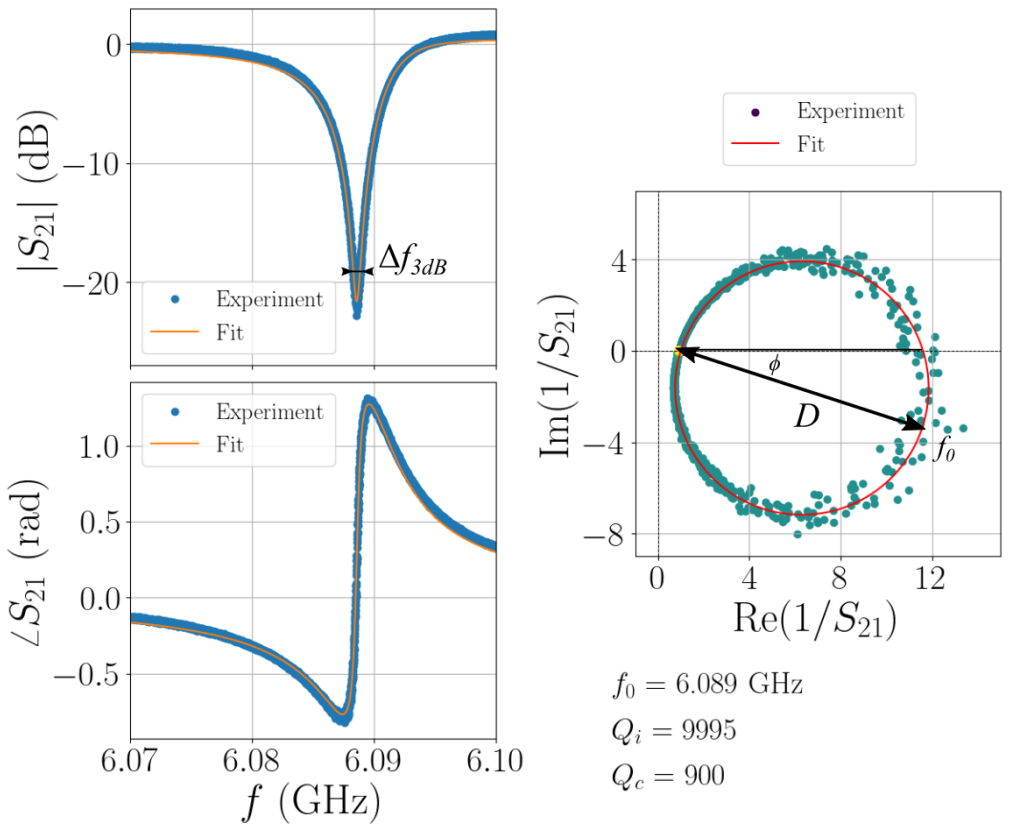

Figure 4.7 – Normalized transmission data of a resonator at a VNA power of -30 dBm. (a) The plot illustrates the magnitude ($|S_{21}|$) and phase ($\angle S_{21}$) as functions of frequency (f). (b) The data from (a) is represented in a parametric plot format.

and ϕ is the rotation of the center of the circle from the real axis. Additionally, $Q = f_0/\Delta f_{3dB}$ is used to determine the quality factor. The Δf_{3dB} is defined by the frequency difference between two frequency points at the full width at half maximum (FWHM) of $|\tilde{S}_{21}|$.

Table 4.1 presents the extracted resonator parameters at a VNA power of -20 dBm, obtained using the mentioned fitting method in the complex plane. Additionally, a comparison is drawn between the extracted resonant frequencies ($f_{0,meas}$) and the designed frequencies (f_{design}), calculated using the equation provided in Section 4.1. It is observed that $f_{0,meas}$ is downshifted by approximately 500 MHz compared to f_{design} for all resonators. This discrepancy could potentially be attributed to the influence of coupling capacitors, which augment the total capacitance of the resonators, and the misevaluation of the kinetic inductance. From the design, we estimated Q_c value of 2000; however, it remains unclear why the extracted values fall significantly lower than the estimated value, by more than half. We suspect that employing laser lithography, which features a beam resolution of approximately 2 μm, to define the few microns separation between the resonators and the transmission line could impact the actual separation distance, thus influencing the C_c and Q_c.

Table 4.1 – Table lists the values of the lengths of the resonators (l_{res}), the designed resonant frequencies (f_{design}), the measured resonant frequencies (f_{meas}), the internal quality factors (Q_i), and the coupling quality factor (Q_c) of the resonators in Figure 4.5(b).

l_{res} **(mm)**	f_{design} **(GHz)**	$f_{0,meas}$ **(GHz)**	Q_i	Q_c
4.1	6.57	6.09	10011 ± 29	868 ± 2
4.4	6.13	5.81	8296 ± 12	372 ± 1
4.7	5.73	5.09	6800 ± 7	419 ± 1
5.2	5.18	4.67	5446 ± 12	470 ± 1
5.7	4.73	4.28	1943 ± 2	472 ± 1

4.3.2 Power dependance

We studied the power dependency of Q_i and Q_c up to a single photon regime, which is a regime of qubit operation. The number of photons within the resonator for this configuration is defined by the equation [102]:

$$\langle n_{ph} \rangle = \frac{Q_c}{2\pi f_0} \left(\frac{Q_i}{Q_i + Q_c} \right)^2 \frac{P_{in}}{h f_0}, \tag{4.13}$$

where $\langle n_{ph} \rangle$ and P_{in} are the photon number and the input power, respectively. From the equation, we can see that $\langle n_{ph} \rangle$ can be controlled by adjusting the VNA power.

Figure 4.8 shows the behavior of Q_i and Q_c as a function of $\langle n_{ph} \rangle$ for five resonators in Figure 4.5(b). Each resonator is identified by its corresponding resonant frequency, as indicated in Table 4.1. The parameters are derived using the circle fit method at different VNA power. The calculation of photon numbers

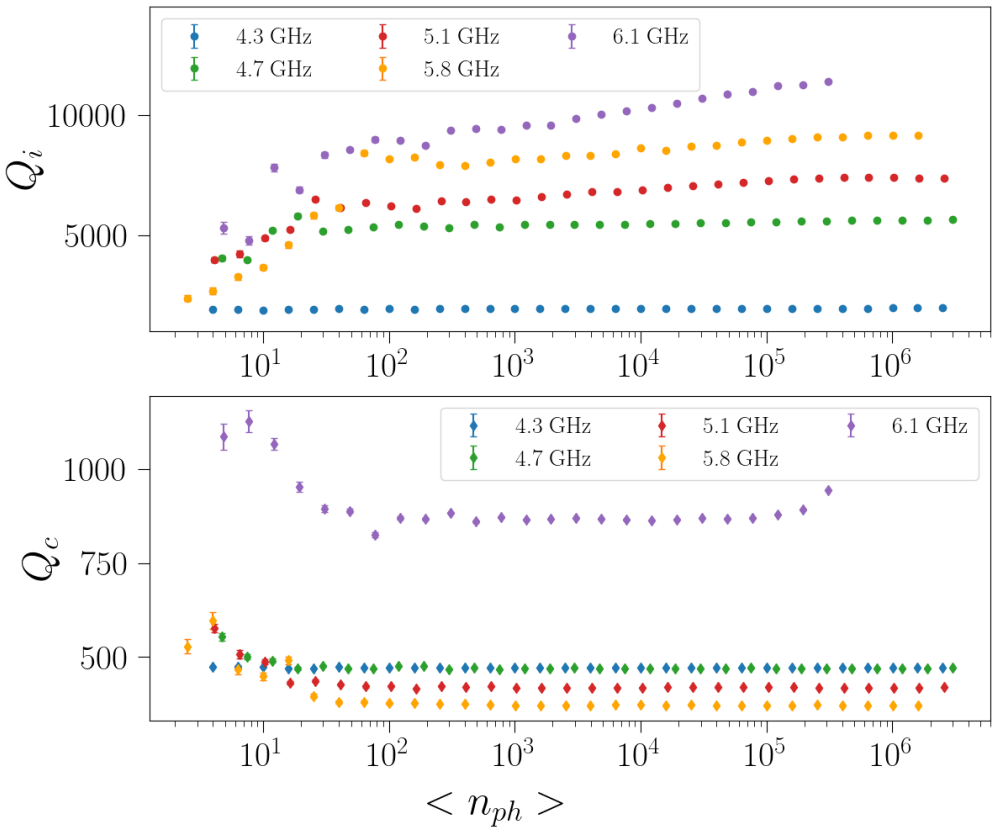

Figure 4.8 – Internal quality factor (Q_i) and coupling quality factor (Q_c) of the resonators shown in Figure 4.5(b) plotted as a function of the average photon number ($\langle n_{ph} \rangle$)

takes into account a -70 dB attenuation in P_{in}.

The figure shows a gradual increase in Q_i as photon numbers increase. However, the observed degree of increment is notably smaller compared to what have been reported in the literature [102, 107]. This phenomenon could potentially be attributed to the presence of numerous surface two-level-states (TLS) [108], which may contribute to the loss in the resonators. This suspicion is partly linked to the fact that our substrate is SiGe, which could potentially exhibit higher microwave loss compared to standard materials like sapphire or silica, commonly used in planar resonators.

We expect Q_c to be independent of the applied power since it solely depends on the coupling capacitance governed by the design. The results demonstrate that this statement holds true for high photon numbers. However, the variability observed at lower photon numbers may be attributed to fluctuations in the fitting process, as transmission signals tend to exhibit more noise at lower VNA powers.

4.4 Challenges on realizing resonators on SiGe heterostructures and gatemon integration

In this section, we discuss the challenges we encountered in fabrication and measurement.

4.4.1 Bonding and chip cracking

One of the challenges we encountered in the fabrication of planar resonators on SiGe heterostructures was chip cracking caused by bonding process. Initially, during the first fabrication trial, we observed an increase in $|S_{21}|$ with f. This behavior is indicative of a CPW capacitively coupled to the bonding pads. In other words, this suggests that the transmission line may potentially be cut. We observed similar result on another repetition trial. Later, we did an investigation on this issue. Figures 4.9(a) and (b) show optical images in dark field of NbN resonators on SiGe heterostructures. In these images, several straight lines are visibly passing through the transmission line and some resonators. SEM images, shown in Figures 4.9(c) and (d), provide a closer view of the areas indicated by the red arrows in Figures 4.9(a) and (b), respectively. The SEM images confirm that these straight lines are indeed the cracks on the chip, and they seem to propagate along crystal planes. This cracking process could be attributed to a combination of strain accumulating in the SiGe heterostructure on the Si substrate, and the bonding force.

To test this hypothesis, we fabricated two samples with the same design: one on a Si substrate, and another on a SiGe virtual substrate. We observed the crack only in the SiGe sample after several times of bonding. Additionally, we conducted a bonding test on a SiGe virtual substrate by preparing several samples and depositing different combinations of layers, including: 1) 20 nm NbN, 2) 20 nm Al, 3) 20 nm NbN on 10 nm Al_2O_3, 4) 20 nm Al on 10 nm Al_2O_3, 5) 10 nm Al_2O_3 on 20 nm NbN, 6) 50 nm Al, 7) 100 nm Al, and 8) 200 nm Al. Upon bonding these samples, we observed similar straight line cracks on every sample except sample number 8. Figure 4.9(e) and (f), taken from sample number 8, indicate the presence of a crack originating from the bonding process. However, this crack stopped before propagating into the SiGe layer. To mitigate this issue, we incorporated a 300 nm Al layer into the design as a bonding layer.

4.4.2 Effect of wire bondings on across the transmission lines and the resonators

Figure 4.10 illustrates the transmission spectra of two samples measured at 10 mK. Each sample comprises a transmission line and five resonators, with the CPW layer composed of 20 nm NbN on SiGe virtual substrates. The first sample features a 300 nm Al layer at the edge for bonding to the PCB's ground. In contrast, the second sample incorporates a 300 nm Al layer spanning the entire chip, enabling

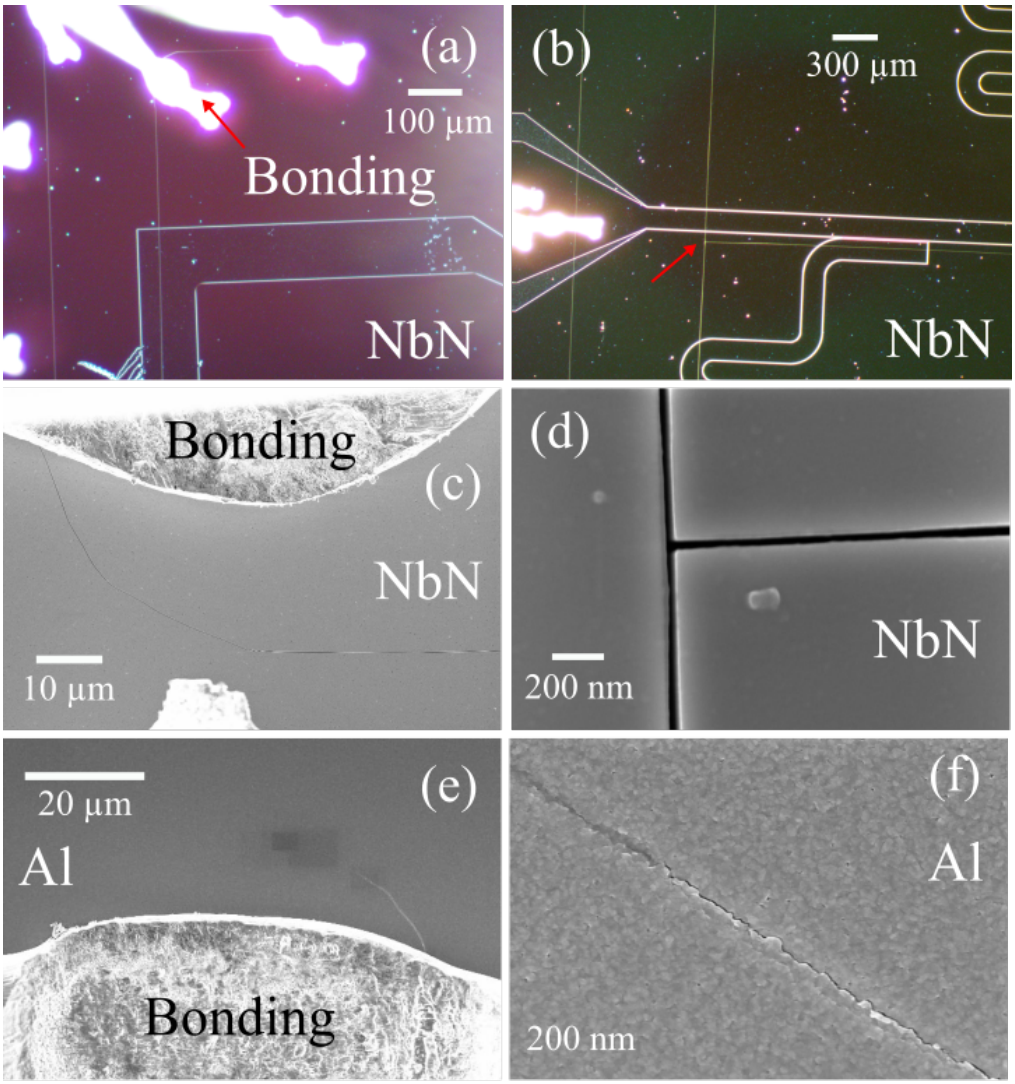

Figure 4.9 – Images explaining the chip cracking due to the bonding. (a) Dark field optical image near the bonding point. (b) Optical image depicting the crack propagation along the chip. (c) SEM image of the region indicated by the red arrow in (a). (d) SEM image focused on the region indicated by the red arrow in (b). (e) SEM image illustrating the initiation of the crack on the 200 nm Al layer. (f) SEM image demonstrating the fading of the crack on Al layer.

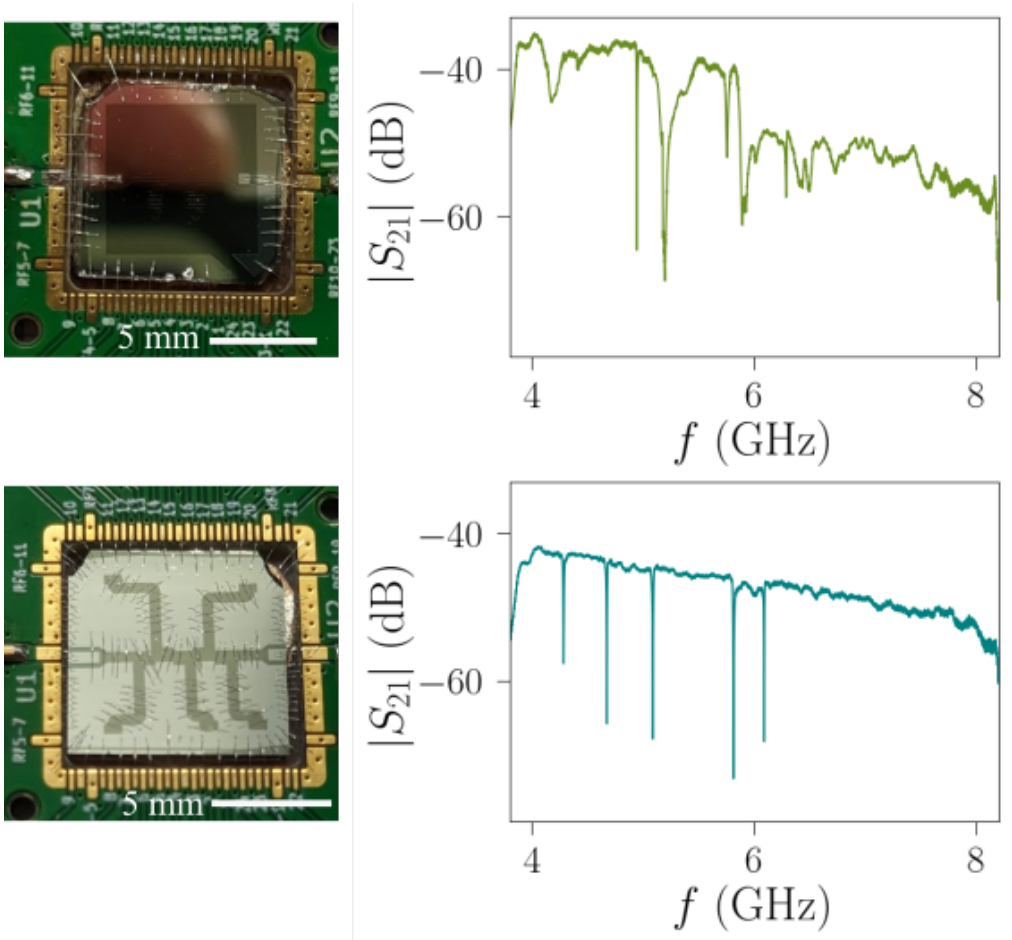

Figure 4.10 – Photos of two samples and their transmission magnitude ($|S_{21}|$) as a function of frequency (f) are presented. In both samples, the ground planes are connected to the PCB ground through wire bondings. The second sample (lower image) features additional wire bondings across the resonators and the transmission line.

bonding not only to the PCB's ground but also across the resonators and the transmission line. The measurement results clearly reveal that the resonances are more pronounced in the second sample. This can be explained by considering disrupted sections of the NbN, caused by the presence of resonators, as inductors. The wire bondings play a role in connecting these NbN sections across the chip and to the ground, contributing to improved resonance visibility.

4.4.3 Prospective on gatemon integration

In our gatemon design, we intend to implement resonators on either SiGe or Al_2O_3 surfaces. To validate the feasibility of this approach, we fabricated NbN

resonators on three different surfaces: Si substrate, SiGe virtual substrate, and 10 nm Al_2O_3 over SiGe virtual substrate. The transmission magnitude ($|S_{21}|$) as a function of frequency (f) for these samples is illustrated in Figure 4.11, with measurements conducted at a temperature of 4.2 K. The result shows visible resonances across all the samples. This assures that the fabrication process for these resonators is likely applicable to our gatemon design.

The result presented in Section 4.3 demonstrates that we can achieve Q_i values exceeding 2000 in multiple resonators. This suggests that the overall quality factor will not be primarily limited by Q_i, which is largely influenced by the material and substrate properties. As a result, we can pragmatically anticipate Q to be in the range of 2000 to 3000 by adjusting the design to modify the coupling capacitance and Q_c. However, it is important to keep in mind that fabricating gatemon may feature more fabrication steps, which can potentially reduce Q_i by introducing contaminants and parasitic surface states to the samples [108].

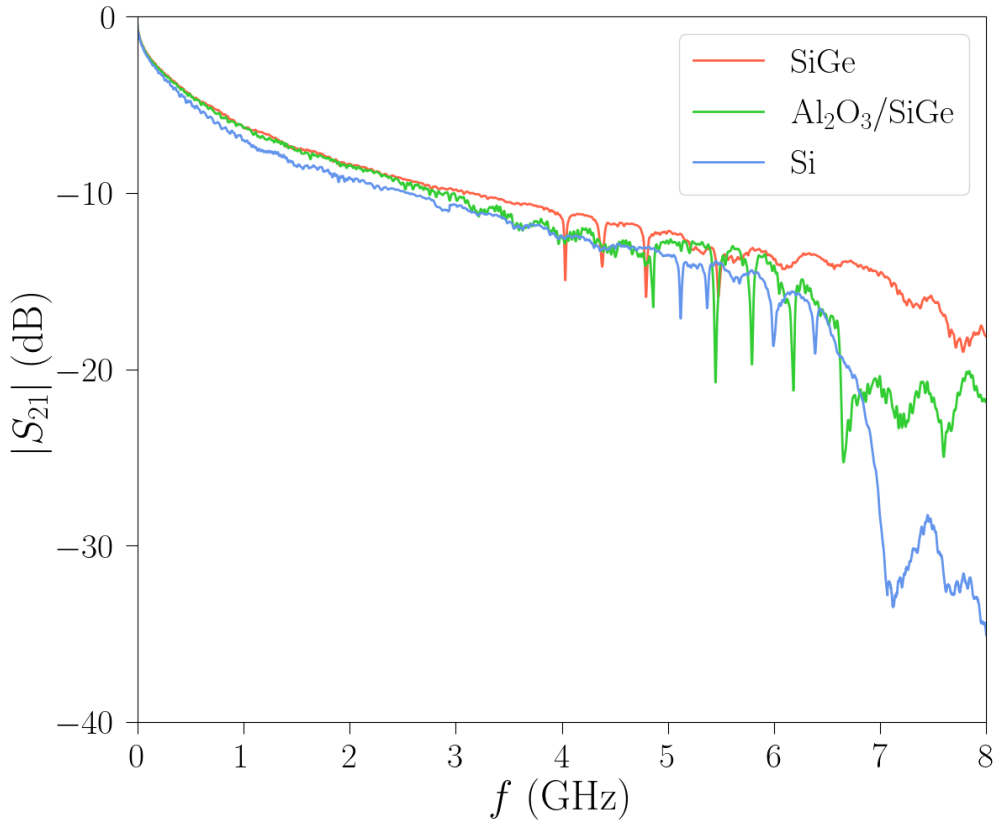

Figure 4.11 – Magnitude of the transmission spectrum ($|S_{21}|$) as a function of the frequency (f) of three samples measured at 4.2 K. The design for all the samples features a transmission line with five resonators. The three samples are fabricated on three different substrates: Si, SiGe, and 10 nm Al_2O_3 over SiGe.

CHAPTER 5

Gatemon

In the previous chapters, we demonstrated high-transparency Al-Ge-Al Josephson junctions and NbN superconducting resonators on SiGe material. Now, it is time to combine them to create the most exciting device in this thesis. This chapter presents the story of a gate-tunable transmon (gatemon) device. We begin by designing the device based on the information we obtained from measurements and simulations. Next, we demonstrate the coupling between the resonator and the qubit. Lastly, we present the gate-tunability of the qubit's resonance frequency and discuss the prospects for future experiments.

5.1 Device: design and points of consideration

5.1.1 Overview of the design and the process flow

Overall, the design has been made to fit on a 2 cm $\times$ 1 cm^2 piece of SiGe sample. The process flow has been slightly modified from the fabrication recipe presented in Chapter 2. The main fabrication steps are listed below:

1. Preparing the sample: cleaving, cleaning the surface, and defining alignment markers.
2. Mesa etching over patterned negative resist MAN2403 using CF_4 and Ar as etchants.
3. Etching over patterned negative resist MAN2403 and depositing Al for ohmic contacts, qubit capacitors, and Al resonators.

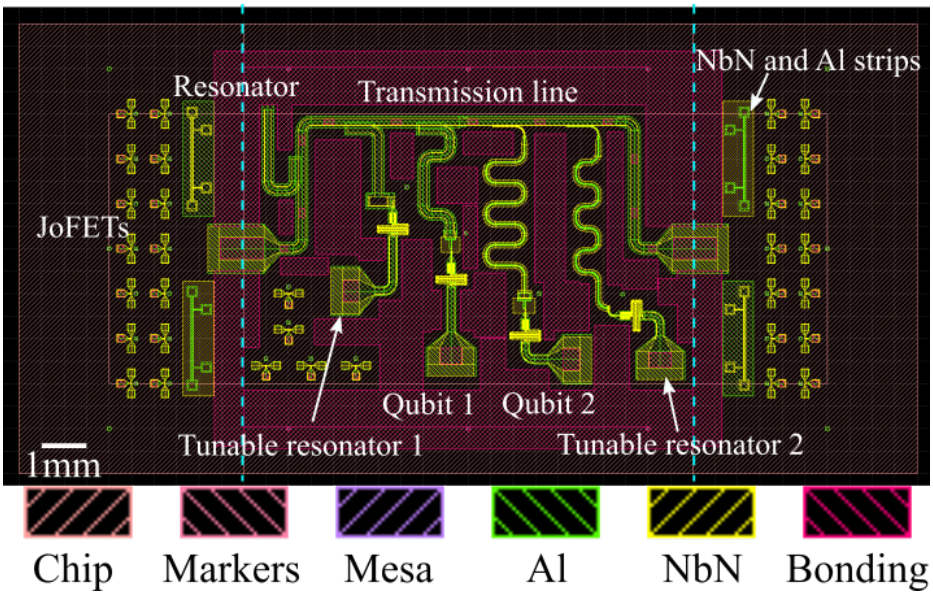

Figure 5.1 – GDS design of the sample is shown in the figure. The design includes an NbN transmission line coupled to the NbN resonator, Tunable resonator 1, Tunable resonator 2, Qubit 1, and Qubit 2. Additionally, there are several JoFETs, NbN strips, and Al strips on the sides to perform DC characterization tests. The color patterns in the design represent different lithography layers, as indicated in the figure.

4. Depositing Al_2O_3 at 280°C as an insulating layer.
5. Depositing 20 nm of NbN and etching over patterned ZEP520A to define gates and NbN resonators.
6. Depositing 300 nm of Al on the ground plane area to create bonding pads.

One of the changes implemented in the design is the use of NbN as the gate layer, replacing Ti/Au. This modification was made due to NbN's higher kinetic inductance compared to Ti/Au and Al. The intention is to take advantage of NbN's properties to design on-chip filters on the gate line, which could decrease the microwave leakage and consequently improve the qubit lifetime.

Additionally, an extra layer of 300 nm of Al was added as bonding pads. This adjustment was based on the study on the fabrication and measurement of the resonator discussed in Chapter 4. The study shows that connecting the ground plane throughout the chip with multiple bonding points enhances the resolvability of the resonator signals during transmission measurements (see Figure 4.10). However, it was also observed that bonding and thermal cycling can result in visible cracks on the chip, as explained in Subsection 4.4.1. To overcome this issue, an extra layer of Al was introduced to prevent chip cracking.

Furthermore, we would like to note that for the ohmic lift-off process, we

utilized NMP (N-Methyl-2-pyrrolidone) solvent at 80°C instead of AR300-76 or acetone as this allows us to work with higher lift-off temperature.

The design is divided into three parts, as depicted in Figure 5.1. The chip was subsequently cleaved into these three parts for separate measurements. The left and right sections consist of multiple JoFETs, as well as NbN and Al strips. As we modified the process flow, these devices were included to verify the superconducting properties of NbN and Al, and to test the junction properties.

The middle section of the chip contains an NbN transmission line. There are five devices positioned adjacent to the transmission line, as shown in Figure 5.1. These five devices are described as follows:

1. Resonator: A quarter-wavelength NbN resonator with a calculated resonance frequency of 4.6 GHz.
2. Tunable resonator 1: An NbN resonator capacitively connected to an Al-Ge-Al junction. The resonance frequency is designed to be between 5.8 and 11.6 GHz.
3. Tunable resonator 2: An Al resonator connected to an Al-Ge-Al junction to the ground plane. The resonance frequency is designed to be between 3.75 and 7.5 GHz.
4. Qubit 1: An NbN resonator capacitively coupled to an Al-Ge-Al gatemon. The resonator is designed to have a calculated resonance frequency of 6.95 GHz.
5. Qubit 2: An Al resonator capacitively coupled to an Al-Ge-Al gatemon. The resonator is designed to have a calculated resonance frequency of 6.19 GHz.

The fixed-frequency NbN resonator serves as a reference resonator for comparison with previous NbN resonator experiments. The tunable resonators are designed to operate in two regimes: the quarter wavelength resonator regime (when the junction is fully closed), and the half wavelength resonator regime (when the junction is fully opened). The junctions connected to the tunable resonators are expected to have a maximum critical current (I_C) of up to 2 μA, which corresponds to a Josephson inductance ($L_J = \frac{\Phi_0}{2\pi I_C \cos\varphi}$) [28] approximately 0.05 times the total inductances (geometrical and kinetic) of the resonators, allowing a tunability up to a few GHz of frequency.

Unfortunately, we observed significant leakage of DC current from the gate lines connected to Tunable resonator 1 and Qubit 1. Furthermore, in the preliminary measurement, we did not observe any gate effect on Tunable resonator 2. Due to time constraints, we were unable to conduct further investigations on this particular device. Therefore, we will focus on providing detailed explanations of Qubit 2 which we observed a significant gate effect on the resonator response.

As we performed the SEM measurement on the junctions of each device in several fabrication steps, we attribute the observed leakage to the modification of oxide properties caused by the electron beam. This conclusion is based on our observation that when we measured JoFETs on the side, we noticed current leakage

specifically from the junctions that were exposed to the electron beam for a longer period of time during SEM imaging. It is worth noting that in some cases, the exposed junctions did not exhibit leakage, but we observed a shift in the threshold voltage towards zero or negative values. In contrast, for the unexposed junctions, we always measured positive threshold voltages with no significant current leakage within a gate voltage range of ± 2 V.

5.1.2 Device description: Qubit 2

Figure 5.2 shows (a) the drawing design and the fabricated device of Qubit 2, and (b) a schematic of circuit representation of Qubit 2. The device consists of an Al resonator with coplanar waveguide geometry (length = 8.504 mm, central width = 13 μm, gap = 10 μm, Al thickness = 50 nm), a gatemon qubit based on an Al-Ge-Al junction, and an on-chip low-pass filter. The resonant frequency of the resonator is calculated to be 6.19 GHz, using the equations and method described in Section 4.2.

The photon loss rate (κ) of a resonator depends on the coupling quality factor (Q_c) and the internal quality factor (Q_i). Q_i is influenced by substrate loss, material loss, and surface quality. On the other hand, Q_c is determined by the capacitances of the transmission line, the resonator, and their mutual capacitance. Initially, we designed this resonator to couple capacitively to the NbN transmission line with a targeted Q_c of around 2000 and κ of 3 MHz. However, we observed that the measured Q_c values in our resonator experiments were approximately half of the designed values. To address this mismatch, we tried to qualitatively compensate for the mismatch by reducing the separation between the resonator and the transmission line from 2 to 1 μm.

Additionally, the resonator features a metal pad capacitively connected to the gatemon qubit. We simulated the capacitances of this metal pad, the qubit capacitance (C_{qb}) neglecting the junction capacitance, and the mutual capacitance between the resonator and the qubit ($C_{\boldsymbol{g}}$). From the simulated values of the design, we expect the coupling strength ($g/2\pi$) to be approximately 100 MHz.

Gatemon qubit

As explained in a precedent chapter, gatemon is a variation of the transmon qubit, and its Hamiltonian can be expressed as:

$$H = E_C \hat{n} -^2 -E_J \cos(\hat{\varphi}), \tag{5.1}$$

Here, E_C represents the charging energy determined by the qubit's capacitance, and $\hat{n}$ represents the number of the Cooper pair. E_J corresponds to the Josephson energy provided by the qubit's Josephson junction, while $\hat{\varphi}$ is the phase across the junction. To minimize the effects of charge noise, the transmon is typically designed such that $E_J \gg E_C$, placing it in the "transmon regime". In the case of

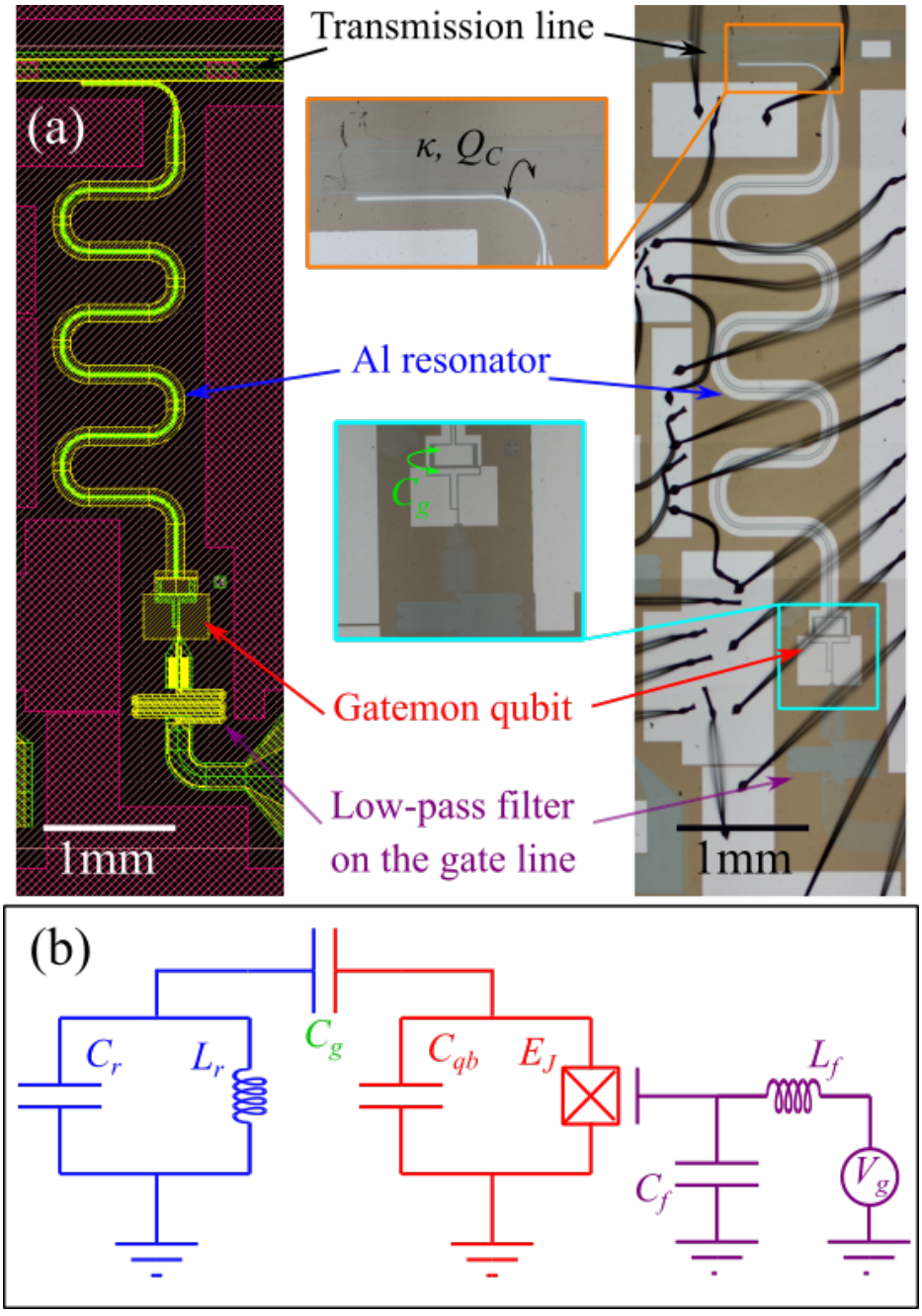

Figure 5.2 – **(a)** GDS design and optical images of the Qubit 2 device are shown. The device consists of an Al resonator, a gatemon qubit, and a low-pass filter on the gateline. **(b)** The schematic represents the circuit diagram of the device described in **(a)**.

gatemon, unlike the split transmon, E_J is tuned by manipulating I_C through the gate voltage.

From the equation, it is clear that we need to design two components: a capacitor and a Josephson junction connected in parallel. One design constraint we must consider is the frequency band of the amplifier used in the setup. Our measurement setup is equipped with an amplifier operating in the range of 4 to 8 GHz, so our goal is to design a qubit that can be tuned within that range. Another important consideration is the qubit's anharmonicity (α). In the case of the transmon, which relies on a tunneling S-I-S junction, the anharmonicity is equal to E_C [12]. However, in the case of an S-N-S junction, typically with higher transparency, the anharmonicity is defined by [36]:

$$\alpha = -E_C \left(1 - \frac{3\sum T_i^2}{4\sum T_i}\right), \tag{5.2}$$

which can decrease to $E_C/4$ for a highly transparent junction. If the designed value of E_C is too low and comparable to the linewidth of the first excited state transition (f_{01}), it becomes more challenging to selectively drive only the f_{01} transition as the energy levels start to overlap with adjacent states. On the other hand, if the qubit has a large E_C, we would need to design a Josephson junction with a lower E_J value, as the qubit frequency f_{01} is determined by the product of E_J and E_C through the equation $f_{01} = \sqrt{8E_J E_C}$. This poses an experimental challenge in fabricating and controlling a Josephson junction with a stable, small I_C step size. We designed the qubit while taking into account the discussions and considerations mentioned earlier.

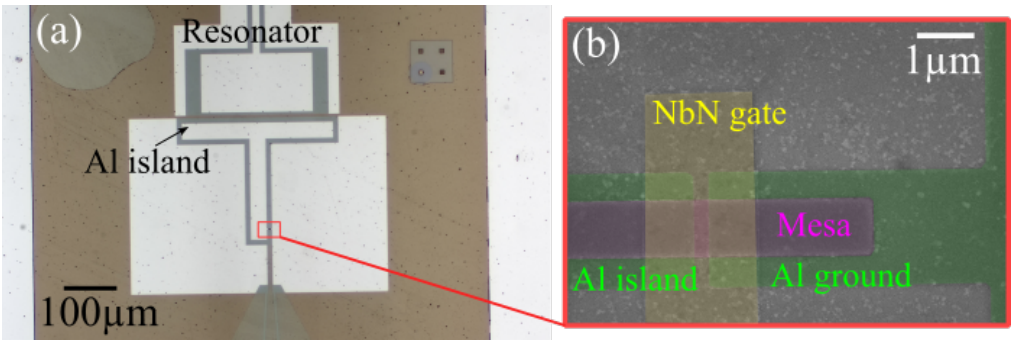

Figure 5.3 – **(a)** Optical image of the gatemon qubit consists of an Al island and an Al-Ge-Al junction with NbN top gate. The island is coupling capacitively to the resonator through the metal pad visible in the image. **(b)** False-colored SEM image of the junction.

Figure 5.3 shows optical and false colored SEM images of the gatemon part, which consists of a T-shaped Al island and an Al-Ge-Al junction with the NbN top gate. The Al island is designed to have $C_{qb} = 0.115$ pF, corresponding to a charging energy of ($E_C = \frac{e^2}{2C_{qb}}$) of 168 MHz. The junction has been designed to

have a contact separation of 250 nm and a junction width of 1 μm. Based on previous measurements on JoFETs, we expect this junction to have I_C around 100 nA, resulting in a maximum Josephson energy of $E_J = \frac{\Phi_0 I_C}{2\pi} = 48$GHz, and a qubit frequency up to 8 GHz. By tuning E_J, the qubit should enter the transmon regime ($E_J \approx 70E_C$) at f_{qb} above 4 GHz.

Low-pass filter on the gate line

In addition to the resonator and the gatemon, we incorporated a low-pass filter on the gateline to mitigate microwave leakage. The filter design, inspired from [100, 109], includes a finger capacitor and an inductance provided by a meander of NbN strip, which contributes to the kinetic inductance. The capacitance value was estimated through simulation (SONNET) to be 0.17 pF. The meander consists of 1732 squares of NbN. From the measurement of the NbN thin film growth on SiGe heterostructure with the same growth condition, we estimated a square kinetic inductance of $L_{k,\square} = \hbar R_\square / 1.764\pi k_B T_C = 72$ pH/$\square$. Then, the total expected kinetic inductance of the strip is 123 nH. The cutoff frequency (f_c) of this filter is given by:

$$f_c = \frac{1}{2\pi\sqrt{LC}}. \tag{5.3}$$

The given parameters yield f_c of 1.1 GHz, which is far below maximum estimated qubit frequency.

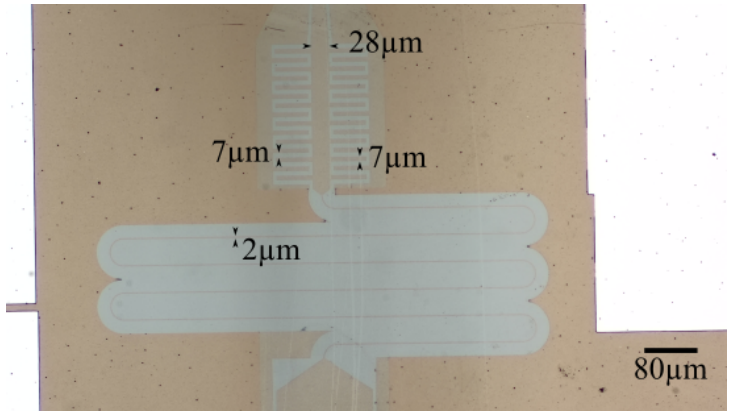

Figure 5.4 – Optical image of the low-pass LC filter. The filter includes a finger capacitor, which contributes to the capacitance, and an NbN meander, which contributes to the kinetic inductance. The geometry of the filter results in a calculated cutoff frequency of 1.1 GHz.

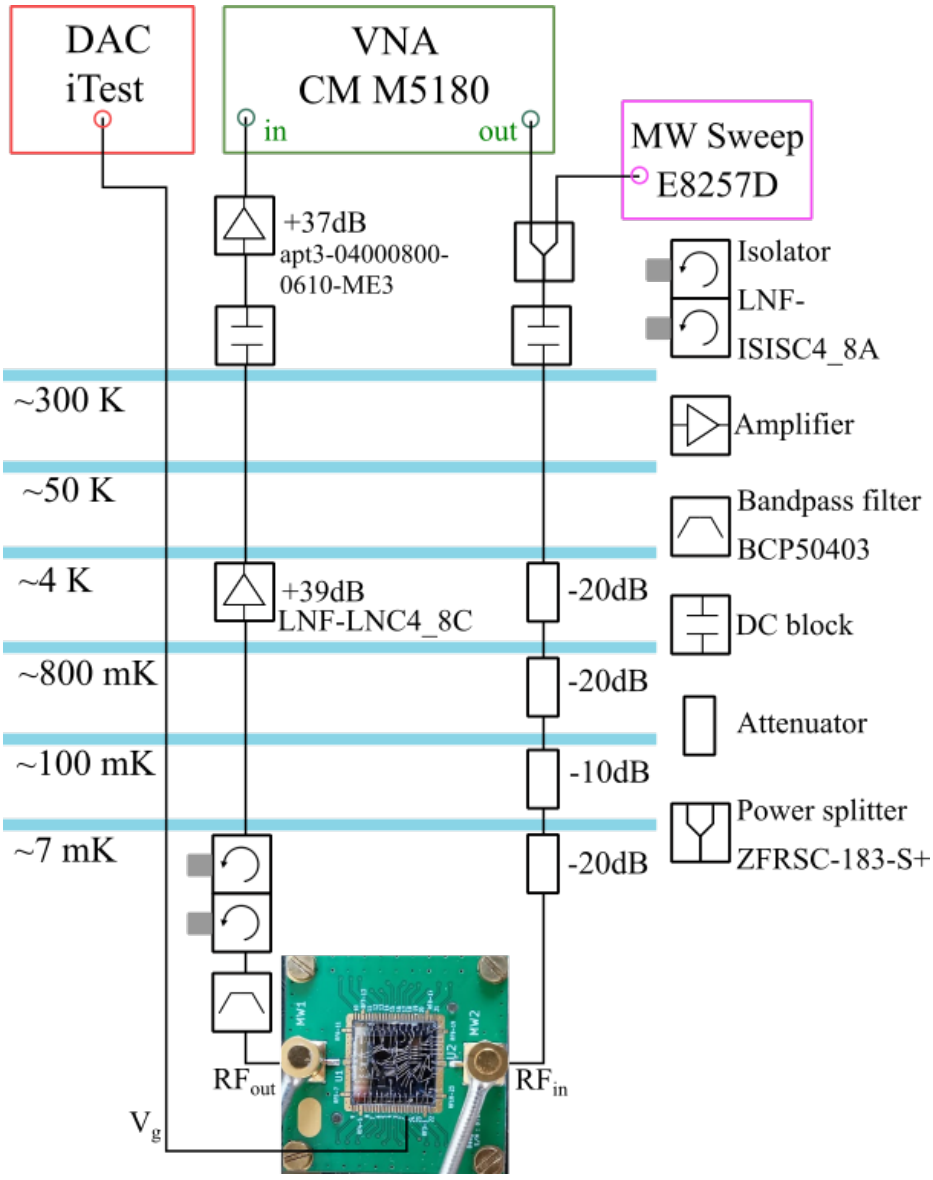

Figure 5.5 – Schematic of the measurement setup for gatemon characterization. The input RF signal is generated by a vector network analyzer (VNA) and passes through several attenuators at different temperatures. The output signal is filtered and amplified before being analyzed by the VNA. The gate voltage is controlled by a digital-to-analog converter (DAC).

5.2 Resonator characterization

The sample was measured in a BLUFORS dilution refrigerator system with a base temperature of 7 mK. Figure 5.5 illustrates the measurement scheme used for performing the experiments.

To prepare for the measurement, the sample was bonded to a daughterboard PCB that had two radiofrequency (RF) connectors. Multiple bonds were made between the sample's ground plane and the PCB's ground, as well as across the resonators and the transmission line. An optical image in the figure shows the bonded sample on the PCB. The daughterboard was connected to a loom with 24 DC connectors via a motherboard. The RF connectors on the PCB were connected to the RF lines inside the refrigerator.

We perform the transmission measurement with this setup. First, a microwave signal generated by a vector network analyzer (VNA, Copper Mountain M5180) was sent through an RF line connected to RF_{in} on the sample. The RF line was equipped with multiple attenuators at different stages of the refrigerator, resulting in a total attenuation of -70 dB. This attenuation was intended to reduce thermal radiation from the environment reaching the sample. Subsequently, the signal at RF_{out} passed through a 4-8 GHz bandpass filter and an isolator (LNF-ISISC4_ 8A). The signal was first amplified by a low-noise amplifier (LNF-LNC4_ 8C) using a high electron mobility transistor (HEMT) mounted at the 4K stage. It was then further amplified by a room temperature amplifier (apt3-04000800-0610-ME3) before reaching the VNA. DC block components were added at both terminals at the entrance of the refrigerator.

For gate voltage control (V_g), a dedicated DC line was connected to a digital-to-analog converter (DAC, iTest).

Noted that, all the DC lines are equipped with various DC and RF filters, and the unused DC lines are connected to the ground during the measurement. All the unused RF lines are covered with ground caps to prevent incoming radiation. Additionally, during the measurement of the resonator characterization experiment, the RF_{in} line was also connected to a microwave source (Agilent E8257D) with a power splitter (ZFRSC-183-S+). However, this microwave source was turned off during the measurement.

5.2.1 Gate effect on S_{21}

Figure 5.6 shows magnitude of the transmission coefficient ($|S_{21}|$) within the frequency range of 4 to 8 GHz at $V_g = 0$ and -2 V for the gate connected to Qubit 2. We observed a gate response in the transmission at around 5.67 GHz, close to the designed value of 6.19 GHz, as shown in the inset. This frequency shift of a few hundred MHz downshift aligns with our observations in previous resonator experiments. Outside this frequency range, we did not observe any considerable response on transmission with respect to V_g. Additionally, we did not observe any effect of the gate of other devices (Tunable Resonator 1, Tunable Resonator 2,

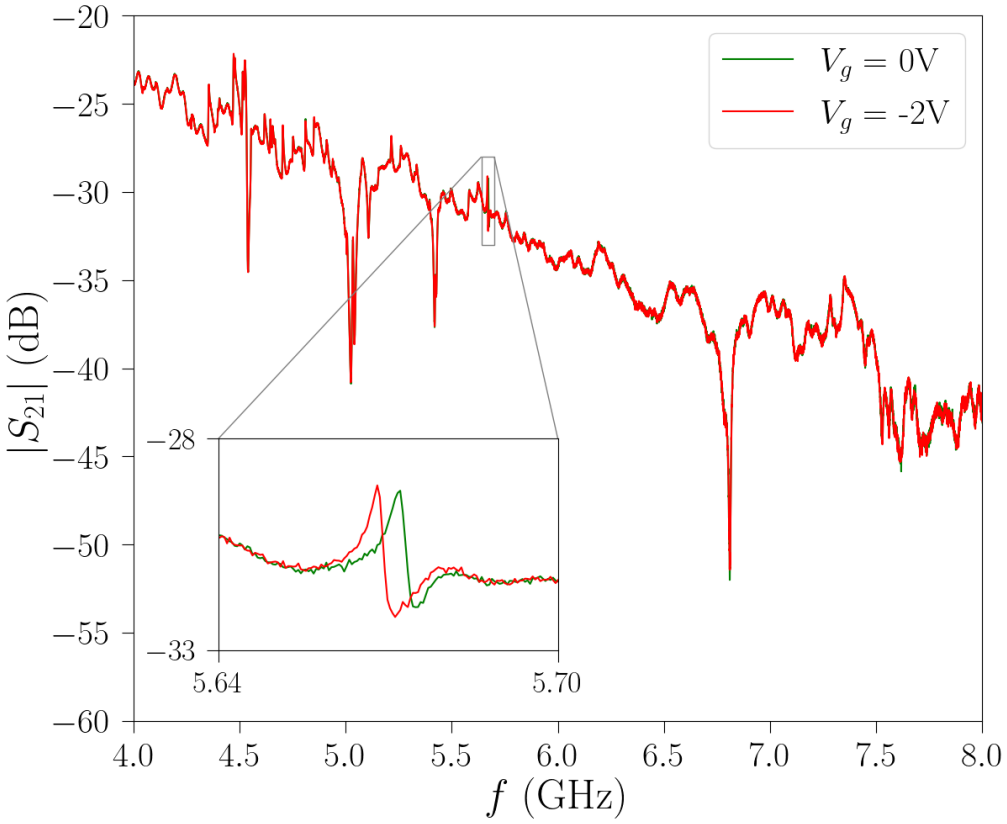

Figure 5.6 – Magnitude of the transmission coefficient $|S_{21}|$ in the frequency range between 4 and 8 GHz at gate voltages of 0 V and -2 V. The inset shows a zoomed-in view of the transmission data specifically for the resonator of Qubit 2.

Qubit 1) on S_{21}. This observation helped us identify the resonator that we were studying.

Additionally, we noticed that the resonance signal does not exhibit a symmetric dip. We attribute this asymmetry to a mismatch between the input and output impedances of the transmission line, as it is loaded with various components along its length [110].

5.2.2 Quality factor in the low power regime

We are interested in the quality factor of the resonator in the low-power regime, as this is typically the power range in which we perform qubit experiments. To characterize the resonator in this regime, we conducted a transmission measurement and performed a circle fit to extract the resonance frequency (f_r), Q_i, and Q_c. The results of the measurement and the fit are demonstrated in Figure 5.7, obtained at $V_g = 0$ V and with a VNA output power (P_{VNA}) of -40 dBm. The

extracted values from the fit are as follows: $f_r = 5.673$ GHz, $Q_c = 11044 \pm 135$, $Q_i = 3404 \pm 58$, and $Q = 2602 \pm 35$. Comparing these values with the resonators presented in Chapter 4, we observed a reduction in Q_i. One possible reason of this reduction is due to surface impurities introduced during the fabrication process, as, in this sample, the resonators and the transmission line were fabricated on the etched SiGe surface. On the other hand, we noticed an increase in Q_c, which we attribute to the fact that we reduced the gap between the resonator and the transmission line in the design from the optimal simulated value, as we mentioned in the previous section. Nonetheless, the obtained values of Q and f_r yield κ of 2.18 ± 0.03 MHz, which we expect to provide a resolvable dispersive shift.

Then, we can estimate an average photon number (n_{ph}) in the resonator using the equation [102]:

$$\langle n_{ph} \rangle = \frac{Q_c}{2\pi f_0} \left(\frac{Q_i}{Q_i + Q_c} \right)^2 \frac{P_{in}}{h f_0}. \tag{5.4}$$

To estimate the input power (P_{in}) at the resonator, we considered the attenua-

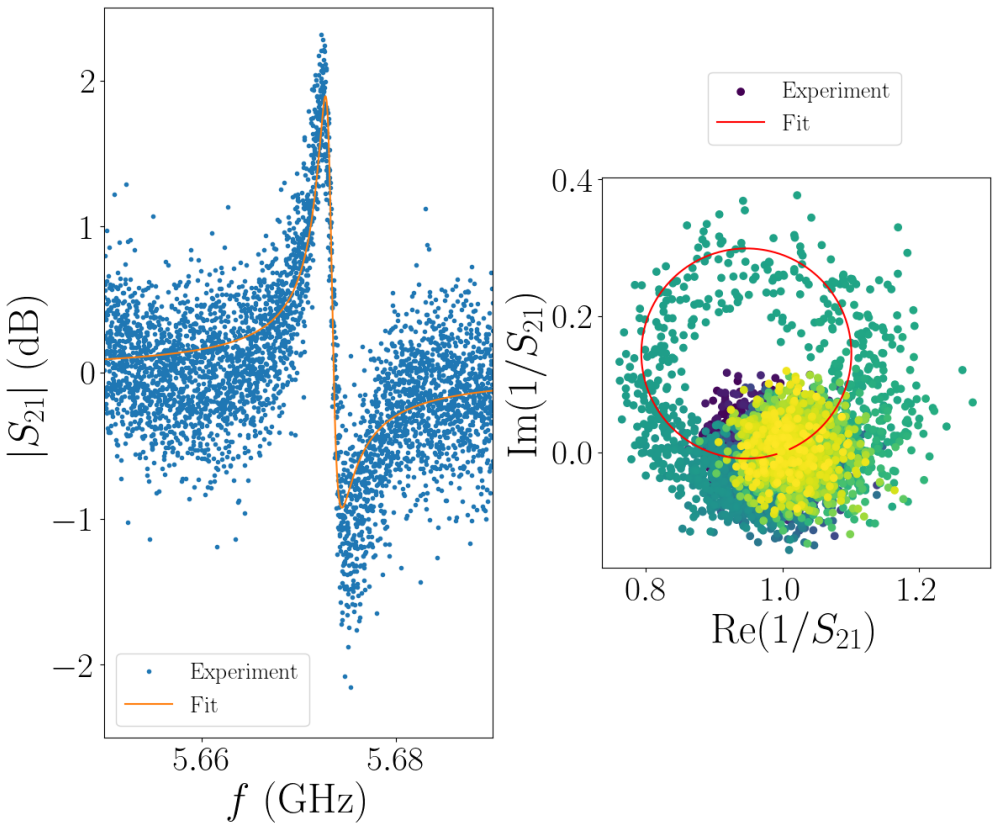

Figure 5.7 – Transmission spectrum of the resonator and the circle fit obtained at P_{VNA} = -40 dBm and an estimated P_{in} below -126 dBm, both at $V_g = 0$ V.

tion of each component. According to the datasheet, the power splitter provides a -6 dB attenuation. The measured attenuation in the RF lines was approximately -10 dB at 5 GHz. By taking P_{VNA} to be -40 dBm, we can make a rough estimation of P_{in} at the resonator to be around -40 dBm - 70 dB - 6 dB - 10 dB = -126. This corresponds to an estimated photon number of approximately 1.15 ± 0.03. It is important to note that we have not accounted for the attenuation of the NbN transmission line, which is difficult to determine precisely. However, it is expected to contribute to a further decrease in the number of photons.

5.3 Qubit-resonator coupling

In this section, we study the resonator response with the gate voltage, which demonstrates the coupling between the qubit and the resonator. Before conducting experiment in this section, we warmed up the sample and relaunched the cooldown again with an intention to re-initialize the threshold voltage.

5.3.1 Energy level diagram of the qubit-resonator interaction

The qubit-resonator interaction can be modeled using the generalized Jaynes-Cummings Hamiltonian [111]:

$$H = \hbar\omega_r a^\dagger a + \sum_j \hbar\omega_j \left|j\right\rangle \left\langle j\right| + \sum_j \hbar g_j \big(a \left|j+1\right\rangle \left\langle j\right| + \text{h.c.}\big). \tag{5.5}$$

In this equation, the first term describes the energy of the resonator, where a and $a^\dagger$ are the annihilation and creation operators of the resonator, respectively, and $\omega_r/2\pi$ represents the resonance frequency. The second term accounts for the qubit energies, with $\hbar\omega_j$ representing the eigenenergies of the qubit in the states $|j\rangle$, where $j = 0, 1, \ldots$. The interaction between the qubit and the resonator is represented by the third term. Here, $g_j = g_0\sqrt{j+1}$ represents the coupling strength between the resonator and the j^{th} qubit state. The term $a\left|j+1\right\rangle\left\langle j\right|$ describes the transition of the qubit state due to the coupling to the resonator while the term *h.c.* represents its hermitian conjugate for the reverse process.

Figure 5.8 represents the schematic of the energy level diagram of the qubit-resonator interaction modeled with Jaynes-Cummings Hamiltonian (the figure has been taken from [111]) when $\hbar\omega_a$, the transition energy between the qubit ground state and the first excited state, equal to $\hbar\omega_r$. In the presence of the coupling, the qubit energy states hybridize with the resonator states. As a result, the qubit and the resonator form a new quantum system where the excited state splits by $2\hbar g_0$. This split is called "vaccum Rabi splitting". For higher qubit's energy levels, the splits equal to $2\hbar g_j = 2\hbar g_0\sqrt{j+1}$. In an experiment, we can observe a phenomenon known as "avoided crossing" or "anticrossing" due to this effect. It occurs when the frequency of the qubit is tuned close to the frequency of the resonator. The two energy levels come close but do not cross; instead, they repel each other due to their interaction.

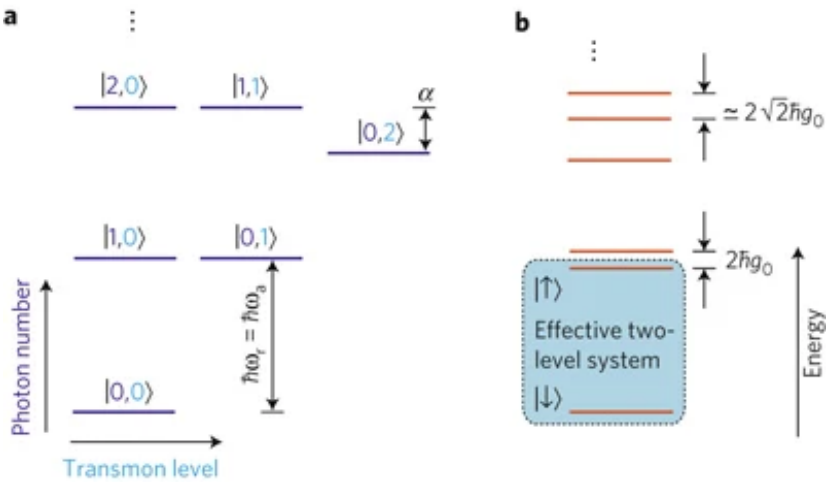

Figure 5.8 – **(a)** The energy level diagram shows a resonator with a transition energy $\hbar\omega_r$ and a qubit with the eigenenergy of its first excited state $\hbar\omega_a$, in the absence of coupling. **(b)** When coupling is introduced, vacuum Rabi splitting occurs at each excited state, resulting in the formation of two energy levels with a separation of $2\hbar g_j\sqrt{j+1}$. Figure taken from [111].

5.3.2 Anticrossing at different P_{in}

Figure 5.9 illustrates the transmission measurement as a function of voltage at different P_{VNA} (where the actual input power at the device is expected to be attenuated by -86 dB or more). At $P_{VNA} = -40$ dBm, which is estimated to be close to the single photon regime, we observed the presence of a repelling of two resonant traces, indicating an anticrossing, in conjunction with non-monotonic trends in the resonant frequency. The non-monotonic variation of the critical current with the gate voltage is consistently observed in gate-tunable S-N-S junctions [13, 15], further confirming the validity of this observation as the gatemon-resonator coupling.

As we increase the power, the anticrossing gradually fades out. We attribute this behavior to two primary factors: first, the broadening of energy levels due to the high number of photons in the resonator, and second, the reduction in the splitting of higher-order vacuum Rabi levels [111]. When the broadening exceeds the level separation, the energy levels effectively merge and become continuous, and the anticrossing disappears as show in Figure 5.9, when $P_{VNA} = 0$ dBm. Nevertheless, it is difficult to extract g directly from our experiment as we do not observe any vertical line-cut where the upper and lower branches of the anticrossing are both clearly present. Additionally, the hysteresis behavior and the threshold shifting (see the following subsection) make it more challenging to fit the data and make an estimation of g.

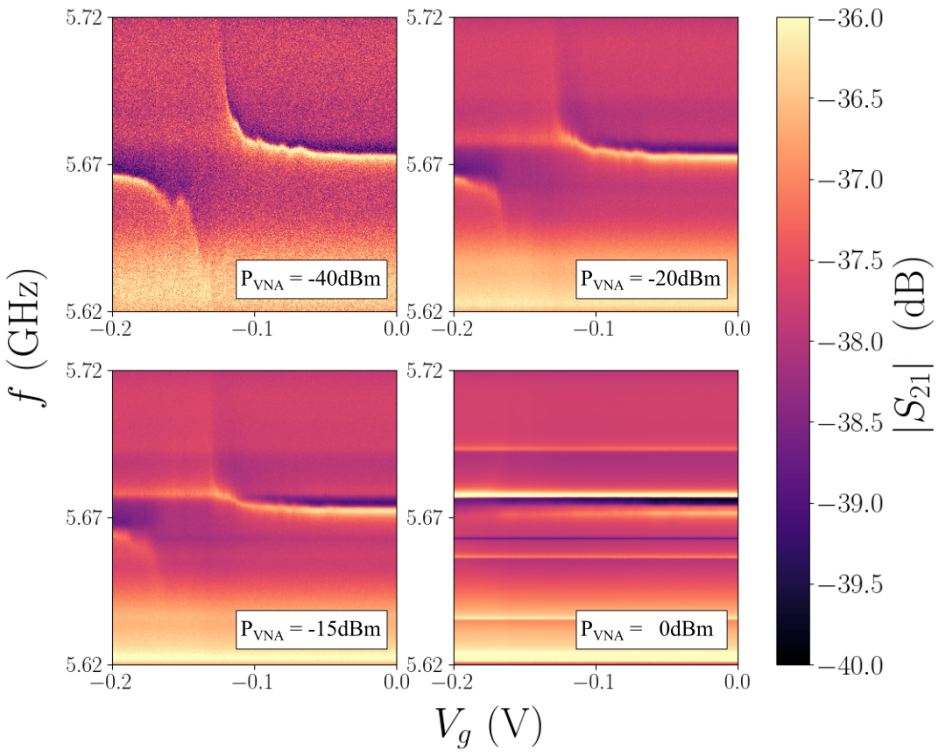

Figure 5.9 – Magnitude of $|S_{21}|$ plotted as a function of frequency and gate voltage at different P_{VNA} values. The anticrossing branch is most visible at the lowest input power ($P_{VNA} = -40$ dBm). As the power increases, the visibility of the anticrossing feature diminishes, and it eventually disappears when $P_{VNA} = 0$ dBm.

5.3.3 Anticrossing and hysteresis behavior

Further, we observed hysteresis behavior in our junction. Figure 5.10 illustrates the transmission measurement as a function of frequency and gate voltage at $P_{VNA} = -30$ dBm. In the upper panel, the gate voltage is swept from 0 to -0.2 V, while in the lower panel, the sweep direction is reversed. We observe a pronounced shift in the anticrossing feature, indicating a significant threshold shift. This behavior can be attributed to the presence of charge traps on the oxide surface of the sample, which lead to different responses during charge accumulation and depletion processes. We have consistently found that the position of the anticrossing feature is reproducible when the sweep is performed in the same direction and within the same voltage range. Moreover, we have observed that the threshold voltage shifts towards more negative values as the scan range is expanded in the negative direction. The threshold resets to the initial value when we warm up and relauanch the cooldown. It is important to note that we took several SEM images

of this gatemon, which likely contributes to the observed negative threshold voltage and threshold shifting phenomenon. Although it may not be a good move for achieving a stable gatemon, we performed the SEM imaging to verify the result of the lift-off process of the junction. If not indicated, all the results presented in this chapter were obtained with voltage ramping in the negative direction starting from zero.

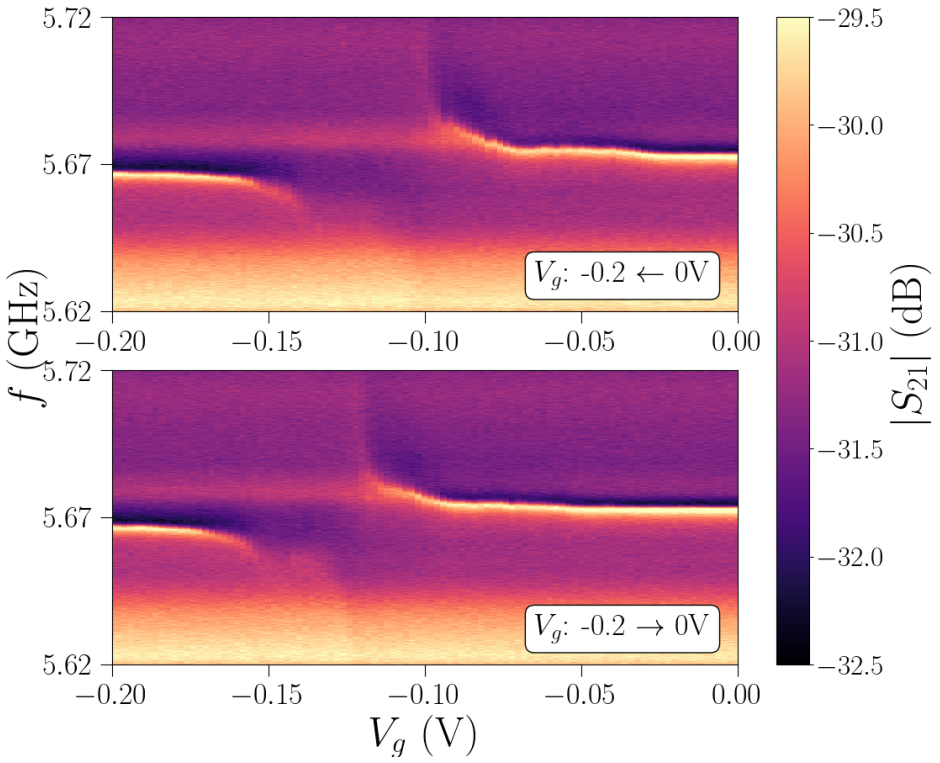

Figure 5.10 – Magnitude of $|S_{21}|$ plotted as a function of frequency and gate voltage at $P_{VNA} = -30$ dBm. The measurement exhibits a noticeable shift in the anticrossing feature when the direction of voltage ramping is reversed.

5.4 Gatemon measurement in the frequency domain

In this section, we perfromed a preliminary measurement of the gatemon in the frequency domain to extract the qubit frequency and the linewidth.

5.4.1 Two-tone spectroscopy: setup and result

We employed the two-tone spectroscopy technique to characterize the qubit. This method involves a probe tone and a drive tone. In this technique, we use a low-power signal as the probe tone to investigate the behavior of the qubit via a mediated resonator. Following that, we introduce a high-power signal with a swept frequency as the drive tone to induce the qubit's state transition. By carefully selecting the frequency of the probe tone and the drive tone, we can acquire a spectroscopic representation of the qubit's energy levels.

Figure 5.11 depicts the measurement setup employed for two-tone spectroscopy. From our experiences, we have encountered charge relaxation in devices that exhibit a negative threshold voltage and significant hysteresis behavior. This relaxation process can lead to instability in the induced carriers within the junction, resulting in fluctuations in both I_C and the qubit frequency (f_{qb}). In this setup, we utilized lock-in measurement modulation on the gate line to counteract possible instability in the gate voltage. The first tone (the probe tone) was generated by a microwave source (Signal Core, SC5521A). The signal was split into two paths. One path served as the local oscillator frequency ($\omega_{LO}/2\pi$) for a passive double-balanced mixer (MM1-0320L). The other path was connected to a digital attenuator (LDA-5018V). Subsequently, another power splitter was incorporated before the signal entered the cryogenic system. Prior to entering the refrigerator, we measured the input power (P_{meas}) using a power spectrum analyzer. The signal then underwent a series of attenuators before reaching the sample. On the gate line, an AC signal with an intermediate frequency ($\omega_{IF}/2\pi$), significantly lower than the filter cutoff frequency, was added to the DC voltage using a 1:1 transformer (SP 921a). The combined DC voltage and AC signal were transmitted to the sample via the gate line. The RF output signal subsequently passed through a bandpass filter, an isolator, and multiple amplifiers before reaching the mixer. The downconversion output of the mixer, at a frequency of $\omega_{IF}/2\pi$, was connected to the lock-in as a measured transmission response (V_{if}). For the qubit excitation, another microwave source (Agilent E8257D) served as the second tone (the drive tone). The drive frequency was applied through the transmission line of the sample. When the drive tone is in resonance with the qubit frequency, it causes a shift in the resonant frequency of the resonator, as observed by a change in the magnitude of the transmission response. Since the qubit frequency depends on E_J through $f_{qb} \propto E_J = \frac{\Phi_0 I_C(V_g)}{2\pi}$, we can extract the qubit frequency as a function of the gate voltage (V_g) applied by DAC iTest. The internal clocks of all instruments were synchronized.

Figure 5.12 shows the transmission response (V_{if}) as a function of the gate

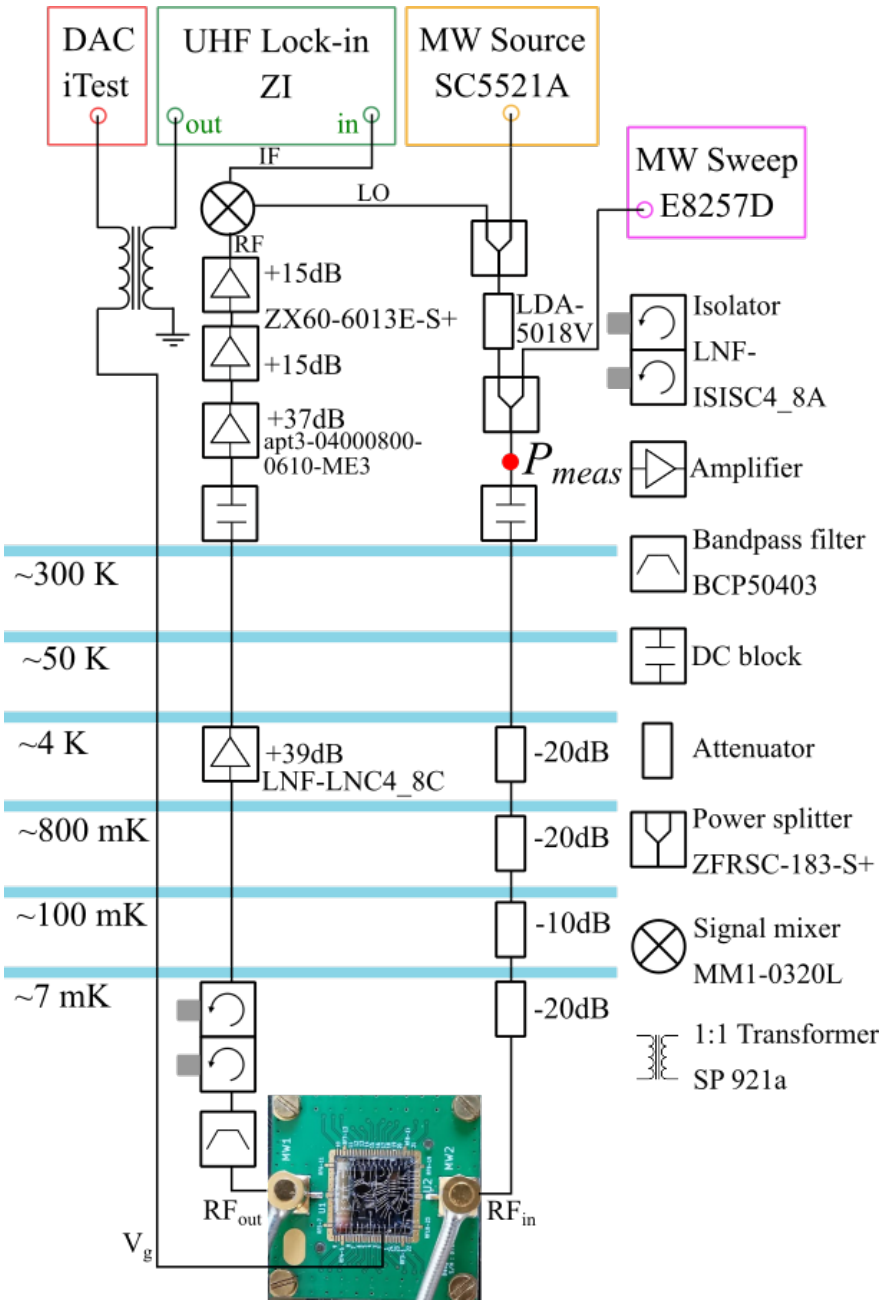

Figure 5.11 – Schematic of the measurement setup for two-tone spectroscopy. The probe tone is generated using SC5521A microwave source, and is attenuated by LDA5018V along with several fixed attenuators. The measurement is modulated through the gate (V_g) using UHF Lock-in. The modulated output signal is filtered and amplified before being mixed using MM1-0320L. The mixed signal with the modulated frequency $\omega_{IF}/2\pi$ is sent back to UHF. The drive tone, applied through the NbN transmission line, is provided by E8257D microwave source.

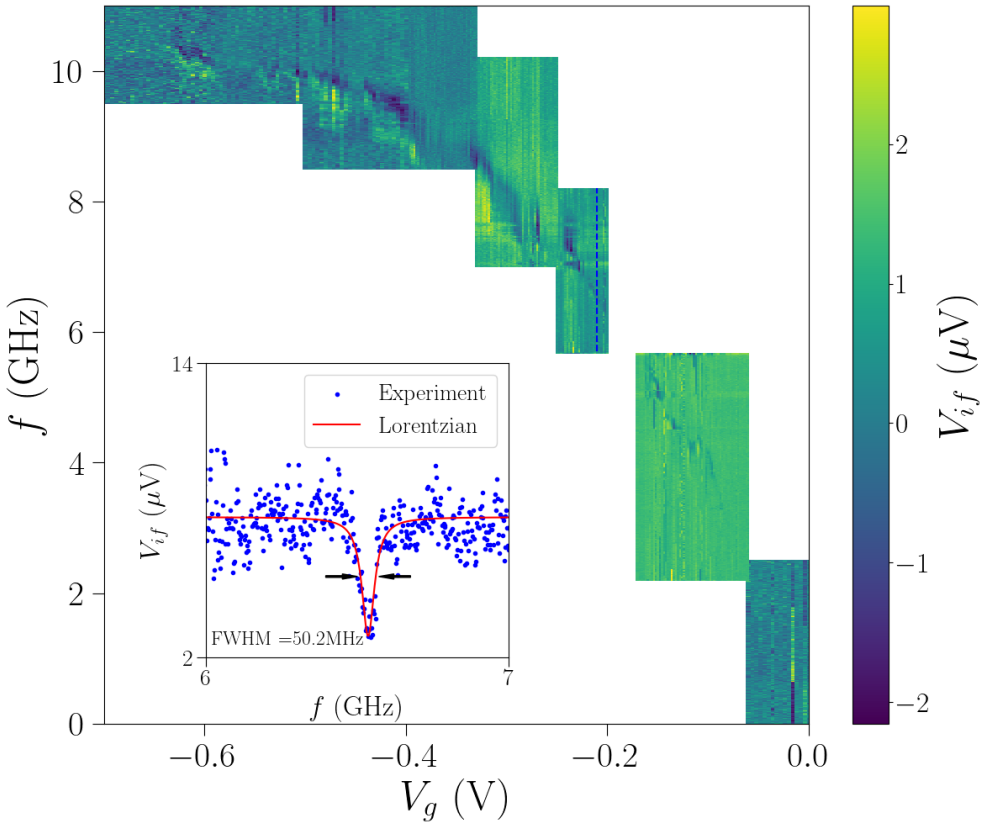

Figure 5.12 – Transmission response (V_{if}) plotted as a function of the qubit drive frequency (f) and gate voltage (V_g). The probe frequency is adjusted to follow the shifted resonance frequency of the resonator, which is extracted from the anticrossing measurement. The dark blue dip observed in the color plot corresponds to the frequency modulation of the gatemon by the gate voltage. The inset shows a linecut taken along the blue line at $V_g = -0.21$ V, and a Lorentzian fit is applied to determine the full width at half maximum (FWHM), which is measured to be 50.2 ± 5.3 MHz.

voltage (V_g) and the frequency of the drive tone (f). Here, P_{meas} was measured to be -46.3 dBm before entering the cryogenic system. The ω_{LO} is set to follow the resonance frequency of the resonator at the different gate voltages, extracted from the anticrossing measurement at P_{VNA} = -40 dBm. We modulated the gate voltage with an AC voltage of 2 mV at 113 Hz. The figure demonstrates a line trace in the color plot. We interpret the trace as representing the qubit frequency since it shows an increasing trend with the gate voltage, and saturates at around 10 GHz, corresponding to I_C = 125 nA, in good agreement with the expected value for the junction with this geometry. This color plot is obtained at the drive power of -10 dBm.

5.4.2 Qubit frequency as a function of gate voltage

Following that, we extracted the qubit frequency and the full width at half maximum (FWHM) using a Lorentzian fit, as demonstrated in the inset of Figure 5.12. Figure 5.13 presents the results for the qubit frequency and FWHM as a function of the gate voltage. We compare the shape of the curve for f^2, which is theoretically proportional to the critical current of the junction of the gatemon, with I_C measured in a JoFET with the same junction geometry on the same chip. The measured I_C exhibits a maximum value of 100 nA, comparable to the estimated value of 125 nA for the gatemon. However, the result in the inset shows several disagreements. Firstly, the JoFET exhibits a threshold voltage (V_{th}) of 1.6 V, while the gatemon has a threshold voltage of approximately zero. Secondly, the slopes near the threshold in both curves differ. We attribute these differences to the exposure of the gatemon to the electron beam during SEM imaging, as mentioned earlier, which could have modified the oxide properties of the devices. To obtain conclusive results, further measurements on more devices would be necessary.

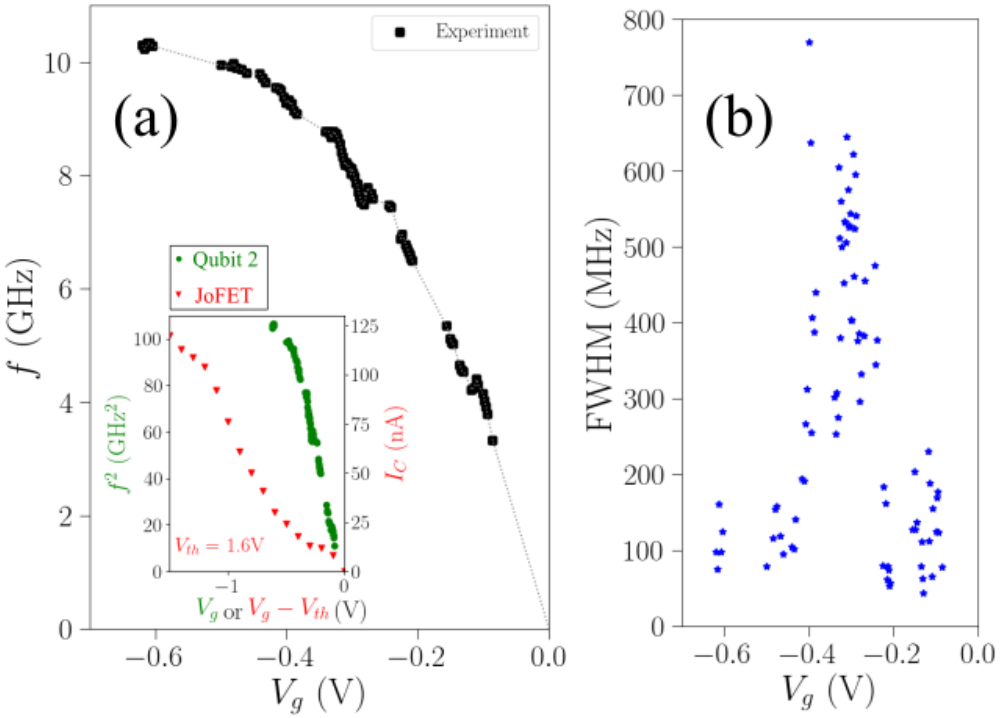

Figure 5.13 – **(a)** The qubit frequency, and **(b)** the full width at half maximum (FWHM) extracted from Figure 5.12 using the Lorentzian fit. The inset in **(a)** shows a qualitative comparison of the shape of the curves between $f^2 \propto E_J \propto I_C$ of this gatemon and I_C of a JoFET on the side that has the same junction geometry. The horizontal axis has been subtracted by 1.6 V in the case of I_C measured in the JoFET.

In Figure 5.13(b), the FWHM is shown, reaching its lowest value of 50.2 ± 5.3 MHz at V_g = -0.21. The FWHM increases and reaches its highest value of 769.5 ± 41.5 MHz at a gate voltage of -0.40 V. We believe this increase is due to the gradual shift of the threshold voltage as we move towards more negative voltages. This causes greater instability in the gate voltage, resulting in a higher FWHM. The trend of the FWHM decreasing as the applied gate voltage moves further away from the threshold, towards the close-to-saturation regime, can be attributed to the lower rate of change of I_C with respect to the gate voltage in the saturation region. As the change of I_C is lower, it has a lesser impact on the instability in f_{qb}. Having the FWHM in the same order of magnitude as E_C could be the reasone that we do not observe the second excited state of the qubit when we increased the drive power.

Obtaining a lowest FWHM of 50.2 MHz and a resonator's photon loss rate of 2.18 MHz suggests that the linewidth may not be broadened due to the quality factor of the resonator, but rather by the internal loss of the qubit itself. We believe this is most likely due to the surface quality, as the fabrication process involves several steps, and the threshold shifting. Based on the FWHM value, in the lowest case, we can expect a coherence time in the order of nanoseconds. However, we did not perform measurements in the time domain as we lack instruments with high enough time resolution, for example around a few points per nanosecond.

5.5 Conclusion and perspectives

While it is still debatable whether we should call this device "a gatemon" or "an S-N-S junction connected to a capacitor, capacitively coupling to a resonator", I have learned a lot from exploring the possibility of making a qubit out of this material platform. First, the results show that the resonator fabricated with this process flow on this heterostructure yields a quality factor of 2602, which should be high enough to perform the dispersive readout for the dispersive shift over 2 MHz. Second, we illustrate the qubit-resonator coupling as shown by the anticrossing feature. Third, we demonstrate the tunability of the resonance frequency of the device as a function of the gate voltage, which is the main feature of the so-called gatemon. Our device yields the narrowest FWHM of 50.2 MHz. It implies a coherence time in the order of nanoseconds, far from the state-of-the-art top-down fabrication-based InAs gatemon with ∼2 μs of coherence time [15]. After all, we think it is a promising preliminary study with a lot of room to improve, and I would like to discuss a few possibilities here.

The first point I want to make is about the fabrication. I think incorporating both NbN and Al on the transmission line and the resonators could add some complexity to the device. For example, relying on L_k of NbN can lead to a variation in each fabrication run due to the film properties and, over time, due to the thin film degradation or oxidation. This could be simplified by using only one material for both resonators and the transmission line, which I may pick Al here.

Secondly, we should keep in mind that doing the SEM imaging can cause oxide modification or oxide damaging [112], leading to gate instability in the devices. It would be beneficial if we investigated a bit about the statistics of the yield of the junction lift-off with this process flow to reduce the necessity of SEM imaging. Additionally, in the case that SEM imaging is necessary, we should do it only on a JoFET device further away from a qubit.

Lastly, from Figure 5.12, we notice several horizontal lines that could be attributed to other resonances on the transmission line. In the future, we could incorporate the qubit drive line in the design, [4] as an example architecture, which is dedicated only for driving the qubit, to have a cleaner signal.

CHAPTER 6

Toward the cos 2φ qubit

Apart from quantum error correction which implies a very large number of physical qubits [113], implementing protected qubits is another approach to achieving fault-tolerant quantum computing [114]. The cos 2φ qubit is a variation of the protected qubit, which, as its name implies, relies on the cos 2φ periodic potential well in the inductance part of the Hamiltonian. This potential well is associated with two Cooper pairs co-transport. One way to realize that is by combining superconducting elements, superinductances, with Josephson tunneling junctions, S-I-S junctions, to induce the two Cooper pairs transfer, one in each S-I-S branch [115]. Alternatively, it has been demonstrated experimentally on high-transparency S-N-S juncions in parallel [116]. The latter is based on the fact that a high-transparency S-N-S junction can have higher harmonics in the current-phase relation, which corresponds to multiple Cooper pairs co-transport.

In this chapter, we first discuss the basic concept of the cos 2φ qubits based on S-Sm-S junctions. Then, we present preliminary results to verify the existence of cos 2φ element in our junctions using two approaches. In the first approach, we review the theory of Superconducting Quantum Interference Devices (SQUID). Then, we extract the CPR of the junctions and show that they comprise higher harmonic terms. In another approach, we demonstrate half-integer Shapiro steps in irradiated junctions.

6.1 Basic concept of the $\cos 2\varphi$ qubits based on hybrid superconductor-semiconductor Josephson junctions

In terms of implementation, the $\cos 2\varphi$ element can be realized by two S-Sm-S junctions connected in parallel, forming a superconducting loop. By shunting the $\cos 2\varphi$ element to a capacitor, the circuit diagram of the $\cos 2\varphi$ qubit is shown in Figure 6.1(a).

Adapted from the transmon Hamiltonian, the Hamiltonian of the qubit in Figure 6.1(a) takes the form [116]:

$$\hat{H} = 4E_C\hat{n}^2 + \mathcal{U}_{J,1}(\hat{\varphi}_1) + \mathcal{U}_{J,2}(\hat{\varphi}_2), \tag{6.1}$$

where E_C is the charging energy, $\hat{n}$ is the number operator, $\hat{\varphi}$ is the phase operator, and $\mathcal{U}_{J,i}$ is the potential energy of the i^{th} junction, respectively.

When a magnetic field is applied to the superconducting loop, a magnetic flux of Φ is trapped inside the loop. Due to the flux quantization, the sum of the phase differences between both junctions and the phase difference due to the magnetic flux trapped has to satisfy the condition of the periodicity of the wave function. In other words, the sum must be the product of an integer multiplied by 2π. This can be written as [27]:

$$\varphi_1 - \varphi_2 + \frac{2\pi\Phi}{\Phi_0} = 2n\pi, \tag{6.2}$$

where, Φ is the flux passing through the superconducting loop, and $\Phi_0 = h/(2e)$ is the magnetic flux quantum.

Using Equation 6.2, we can rewrite the Hamiltonian to be:

$$\hat{H} = 4E_C\hat{n}^2 + \mathcal{U}_{J,1}(\hat{\varphi}) + \mathcal{U}_{J,2}(\hat{\varphi} + 2\pi\Phi/\Phi_0). \tag{6.3}$$

Then, we recall the potential energy of a single S-Sm-S junction, introduced in Chapter 1, as [40, 41]:

$$\mathcal{U}_J(\hat{\varphi}) = -\Delta\sum_i \sqrt{1 - T_i\sin^2(\hat{\varphi}/2)}, \tag{6.4}$$

where Δ is the superconducting gap and T_i is the transparency of the transport channel i.

In the case of a high-transparency S-Sm-S junction, we expect the higher harmonic terms, which can be expressed in terms of components of the Fourier cosine series as:

$$\mathcal{U}_J(\hat{\varphi}) = \sum_k A_k\cos(k\hat{\varphi}), \tag{6.5}$$

where A_k is the Fourier coefficient of the k^{th} harmonic.

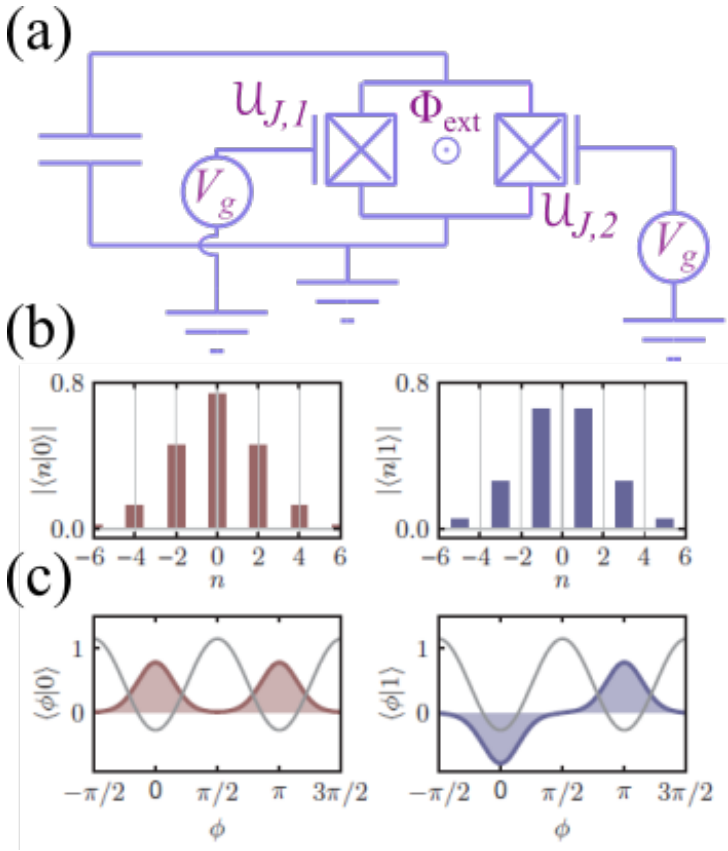

Figure 6.1 – (a) Circuit diagram of the $\cos 2\varphi$ qubit. Note that the junctions in the diagram are S-Sm-S Josephson junctions. (b) Wave functions of the first two eigenstates ($|0\rangle$ and $|1\rangle$) in the charge space. (c) Wave functions of the first two eigenstates ($|0\rangle$ and $|1\rangle$) in the phase space. The subfigures (b) and (c) are reproduced from [117].

Assuming that the two junctions are identical, the qubit can be tuned to the sweet spot where the external magnetic flux $\Phi = \Phi_0/2$. At the sweet spot, the expression of the potential energy term can be rewritten in the form of the Fourier cosine series as:

$$\begin{aligned}\mathcal{U}_{J,1}(\hat{\varphi}) + \mathcal{U}_{J,2}(\hat{\varphi} + 2\pi\Phi/\Phi_0) &= \sum_{k\in 2\mathbb{Z}+1} [A_k \cos(k\hat{\varphi}) + A_k \cos(k\hat{\varphi} + \pi)] \\ &\quad + \sum_{k\in 2\mathbb{Z}} [A_k \cos(k\hat{\varphi}) + A_k \cos(k\hat{\varphi} + 2\pi)] \\ &= \sum_{k\in 2\mathbb{Z}} 2A_k \cos(k\hat{\varphi}), \end{aligned} \tag{6.6}$$

which comprises only the even harmonic terms.

If we neglect the harmonic terms with an order higher than four, corresponding to four and higher numbers of Cooper pairs cotunneling events, the Hamiltonian can be reduced to the form:

$$\hat{H} = 4E_C\hat{n}^2 - \sum_{k\in 2\mathbb{Z}} 2A_k \cos(k\hat{\varphi}) \approx 4E_C\hat{n}^2 - E'_J \cos(2\hat{\varphi}), \tag{6.7}$$

as the Hamiltonian of the $\cos 2\varphi$ qubit, where $E'_J = 2A_2$ is the effective Josephson energy.

The plots of the wave functions of the first two eigenstates ($|0\rangle$ and $|1\rangle$) in the charge space, and the phase space of the Hamiltonian in Equation 6.7 are shown in Figure 6.1(b), and (c), respectively [117]. In the charge space, $|0\rangle$ is the superposition of the even Cooper pair parity states, while $|1\rangle$ is the superposition of the odd Cooper pair parity states. In the phase space, $|0\rangle$ and $|1\rangle$ are the symmetric and antisymmetric wave functions localized in the 0 and π wells, respectively. The protection in the bit-flip arises from the fact that the $|0\rangle$ and $|1\rangle$ contain only the states with even and odd numbers of Cooper pairs, respectively. Thus, the transition of the qubit state due to the noise that does not induce single Cooper pair tunneling is suppressed greatly. Further, like in the case of transmon, the $\cos 2\varphi$ qubit is protected from dephasing when it is engineered to have the effective Josephson energy much larger than the charging energy ($E'_J \gg E_C$).

As a reminder, the concept of the qubit we discussed in this section can only be realized from the hybrid S-Sm-S junctions with higher harmonic terms. This led to our motivation for the experiments in this chapter to quest for higher harmonic terms in our devices.

6.2 Superconducting QUantum Interference Device

6.2.1 Quantum Interference Device

A DC SQUID is a device with two Josephson junctions connected in parallel in a superconducting loop. To begin with, in the case of the two junctions connected in parallel, the total critical current flowing through the SQUID can be described by the equation:

$$I_{SQUID} = I_{C_1} f_1(\varphi_1) + I_{C_2} f_2(\varphi_2), \tag{6.8}$$

where I_{SQUID} is the sum of the total critical current passing through both junctions, I_{C_i} is the maximum critical currents passing through the junction i, $f_i(\varphi)$ is the current-phase relation (CPR) of the junction i, and φ_i is the phase difference between the superconductors across the junction i.

Equation 6.8 can be rewritten using Equation 6.2 to be:

$$I_{SQUID} = I_{C_1} f_1(\varphi_1) + I_{C_2} f_2(\frac{2\pi\Phi}{\Phi_0} + \varphi_1). \tag{6.9}$$

6.2.2 Symmetric SQUID

In the case of the symmetric SQUID where $I_{C_1} = I_{C_2}$, and if we assume the sinusoidal CPR on both junctions, the total critical current passing through both junctions can be written as in the equation:

$$I_{SQUID} = I_{C_1}(\sin\varphi_1 + \sin\varphi_2). \tag{6.10}$$

Using the flux quantization relation, we obtain:

$$I_{SQUID} = 2I_{C_1}\cos(\frac{\pi\Phi}{\Phi_0})\sin(\varphi_1 + \frac{\pi\Phi}{\Phi_0}). \tag{6.11}$$

The maximum of the total critical current can be found by calculating the derivative of the equation 6.11 with respect to the φ_1. It yields the following condition:

$$\sin(\varphi_1 + \frac{\pi\Phi}{\Phi_0}) = \pm 1, \tag{6.12}$$

for the maxima.

Substituting this condition in the equation 6.11 gives maxima of the total critical current at:

$$I_{SQUID} = 2I_{C_1}|\cos(\frac{\pi\Phi}{\Phi_0})|, \tag{6.13}$$

which is the modulation of the critical current by the magnetic flux passing through the junction. On the other hand, the change in the critical current can be used to precisely detect the small magnetic field as well.

6.2.3 Asymmetric SQUID and CPR

The case of the asymmetric SQUID is when the critical current of one junction in a SQUID loop is significantly greater than the critical current of the other junction ($I_{C_1} \gg I_{C_2}$). For simplicity, we assume that CPR of the first junction is sinusoidal, as in a conventional tunneling junction. Then, the maxima of total critical current $I_{SQUID,max}$ will always happen near the maximum of f_1, where $\varphi_1 = \pi/2$. Applied to Equation 6.9, the critical current passing through the asymmetric SQUID can be written as follows:

$$I_{SQUID} = I_{C_1}\sin(\pi/2) + I_{C_2}f(\frac{2\pi\Phi}{\Phi_0} + \frac{\pi}{2}). \tag{6.14}$$

The equation means that we can extract CPR of the second junction from an experiment by measuring I_{SQUID} as a function of Φ and offsetting by I_{C_1}. Experimentally, the CPR of a Josephson junction as a function of the flux can be measured with an asymmetric SQUID with $I_{C_1} > 10I_{C_2}$ [65, 118–121].

6.3 SQUID based on SiGe heterostructure

In this section, we study SQUID devices in a SiGe heterostructure. The SQUIDs have been fabricated on the SiGe heterostructure presented in Chapter 2 (22 nm $Si_{0.21}Ge_{0.79}$/16 nm Ge-QW/$Si_{0.21}Ge_{0.79}$) using similar process flows. The Josephson junctions were established by depositing Al on the Ge quantum well to form Al-Ge-Al as S-N-S junctions.

Figure 6.2 presents images of SQUID devices from two fabrication batches. The second batch (Figure 6.2(d)) has been designed to have the SQUID loop area much larger than the first batch (Figure 6.2(c)). Figures 6.2(a) and (b) show SEM images of the SQUID devices from the first batch. The SQUID in 6.2(a) was designed to be "geometrically symmetric." Both of the junctions have junction widths (W_1 and W_2) of 2 µm and junction lengths (L_1 and L_2) of 200 nm. To be precisely defined, the junction widths, shown as W_1 and W_2 in the figure, refer to

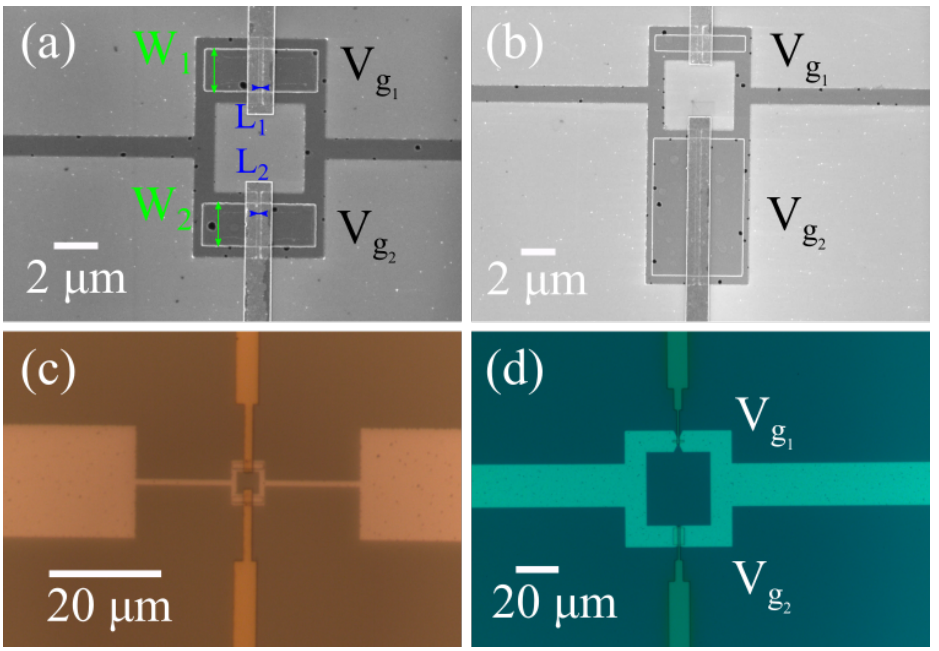

Figure 6.2 – Microscope images of the SQUID devices from two fabrication batches. In each subfigure, W_1 and W_2 corresponds to the mesa widths of the upper and the lower junction, respectively. The junction lengths, defined by seperation between Al contacts, of the upper and the lower junctions are labeled by L_1 and L_2. (a) SEM image of a symmetric SQUID from the first batch (L_1 = 200 nm, L_2 = 200 nm, W_1 = 2 µm, W_2 = 2 µm, SQUID loop area (S) = 4 × 4 µm^2). (b) SEM image of an asymmetric SQUID from the first batch (L_1 = 300 nm, L_2 = 300 nm, W_1 = 1 µm, W_2 = 8 µm, S = 4 × 4 µm^2). (c) Optical image of a SQUID from the first batch. (d) Optical image of an asymmetric SQUID from the second batch (L_1 = 300 nm, L_2 = 300 nm, W_1 = 1 µm, W_2 = 8 µm, S = 30 × 34.5 µm^2).

the widths of the mesas. L_1 and L_2 are defined by the gaps between Al contacts in the junctions. In contrast, the SQUID in Figure 6.2(b) is a "geometrically asymmetric" SQUID as it has two junctions with junction widths of 1 µm and 8 µm, respectively. The junction lengths are 300 nm for both junctions. The SQUID in (a) have a loop area of 7×5 µm^2 measured from the middle of the Al loop. The device in (b) have a loop area of 9.5×5 µm^2 measured from the middle of the Al loop. Figure 6.2(c) depicts an optical image of a SQUID from the first batch showing a loop area (S) of 7×5 µm^2, compared to that of 44.5×40 µm^2, as well measured from the middle of the Al loop, in Figure 6.2(d). The SQUID in Figure 6.2(d) has junction lengths of 300 nm for both junctions and junction widths of 1 µm and 8 µm, respectively. Despite the fact that we referred to the devices as "symmetric SQUID" or "asymmetric SQUID," their critical currents and consequently their asymmetricities can be tuned by the gate voltages (V_{g_1} and V_{g_2}, as shown in the figure).

Here, we will present the results from preliminary measurements of the devices in Figures 6.2(a) and (b). Then, we will discuss the issues and improvements. These lead us to the perspective on the device in Figure 6.2(d).

6.3.1 Device (a): $L_1 = 200$ nm, $L_2 = 200$ nm, $W_1 = 2$ µm, $W_2 = 2$ µm, $S = 7 \times 5$ µm^2

In this subsection, we will discuss the result of the measurement of the device shown in Figure 6.2(a), the symmetric SQUID.

I_C and R_N of the junctions

First, we performed DC measurements to extract the critical currents (I_C) and the normal state resistances (R_N) of the junctions. To do so, we set the gate voltage on the first junction (V_{g_1}) to 4 V, assuming it is effectively closed. Then, we measured the current-voltage (I-V) characteristic of the device at different values of the gate voltage on the other junction (V_{g_2}). We extracted the critical current (I_{C_2}) and the normal state resistance (R_{N_2}) of the second junction from the I-V curves. Afterward, we repeated the same measurement while setting V_{g_2} to 4 V and sweeping V_{g_1} to extract the critical current (I_{C_1}) and the normal state resistance (R_{N_1}) of the first junction.

Figure 6.3 shows I_C and R_N of Junction 1 (blue) as a function of V_{g_1}, and Junction 2 (green) as a function of V_{g_2}. Despite designing these two junctions to be similar, they exhibit a slight difference in I_C. This discrepancy could be attributed to variations in the transparency of each junction. The junctions exhibit an $I_C R_N$ product of 65 µV, which is relatively high compared to the values that have been reported in SiGe-based JoFETs.

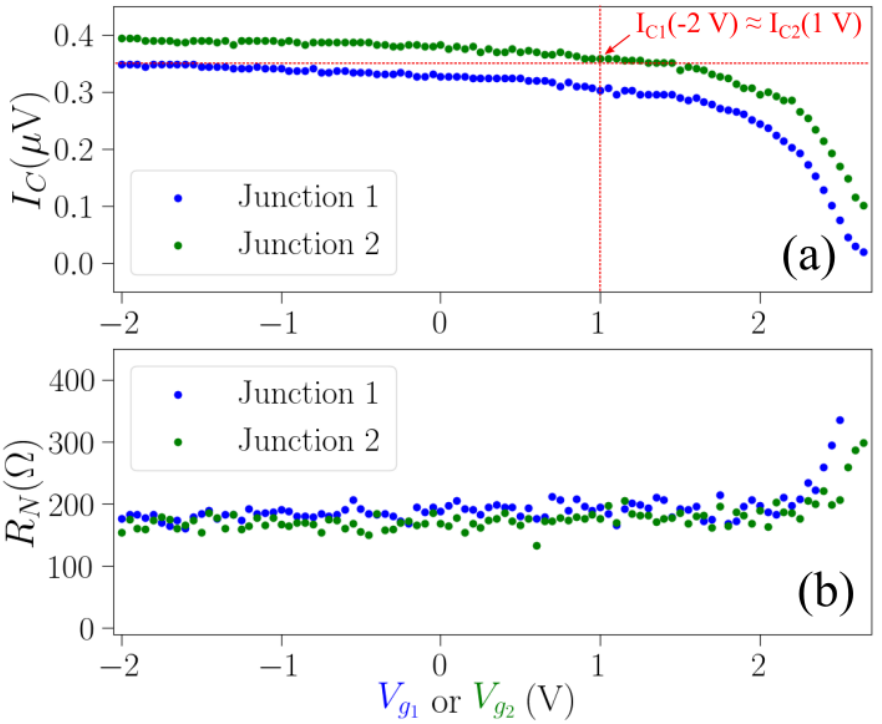

Figure 6.3 – (a) The critical currents (I_C) of both junctions in the device shown in Figure 6.2(a) plotted as a function of gate voltage. (b) The normal state resistances (R_N) of both junctions in the device depicted in Figure 6.2(a) plotted as a function of gate voltage. The blue (green) curve is extracted from measurements with the gate voltage in Junction 2 (1) set at 4 V.

6

SQUID measurement

Following that, we conducted SQUID measurements on the device. We set V_{g_1} to -2.0 V and then recorded the I-V characteristics of the device as a function of a sweeping perpendicular magnetic field ($B_\perp$) with respect to the SQUID loop, at different V_{g_2} values. Figure 6.4 shows the results of the measurement at V_{g_2} values of -2.0, 1.0, 2.5, and 2.9 V, respectively.

Based on the information from Figure 6.3, we anticipated that I_{C_1} would be equal to I_{C_2} at around V_{g_2} of 1.0 V. In this regime, as shown in the upper right panel, we observed an interference pattern resembling that of a symmetric SQUID. In the lower left panel, as V_{g_2} was increased and I_{C_2} decreased, the SQUID transitioned to an asymmetric regime. From the 2D plot in the bottom left panel, the interference pattern appeared slightly skewed. The lower right panel presents the highly skewed interference pattern due to a further increase in gate voltage V_{g_2} to 2.9 V, creating an asymmetric condition for the CPR measurement.

From the I-V characteristic at V_{g_2} = 1.0 V, we extracted I_C as the critical current flowing through the SQUID (I_{SQUID}). Figure 6.5 illustrates I_{SQUID} as a function of $B_\perp$ at V_{g_1} = -2.0 V and V_{g_2} = 1.0 V. The red dashed line in the plot represents the curve fit of the data using Equation 6.11. The interference pattern closely aligns with the equation's plot, and we calculated the oscillation period to be 67 µT, corresponding to a SQUID loop area of 29 µm^2. This value is close to the theoretical value of 59 µT, calculating from the designed area (35 µm^2).

Additionally, we observed that the maximum I_{SQUID} is slightly greater than I_{C_1} at -2.0 V in Figure 6.3. We suspect that the magnetic field offset due to the residual magnetic field in the dilution refrigerator is slightly overcompensated, and it could potentially decrease the measured value of I_C shown in Figure 6.3.

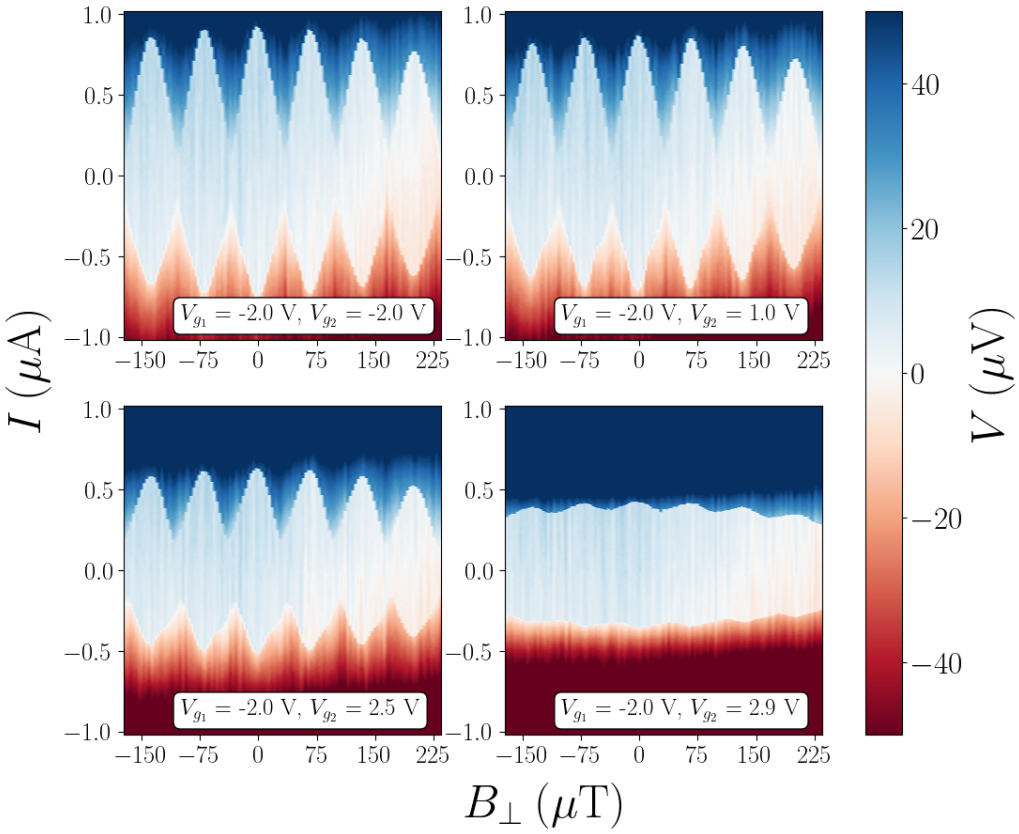

Figure 6.4 – The voltage drop (V) across the SQUID device depicted as a function of the out-of-plane magnetic field ($B \perp$) and the current (I) at the gate voltage of the first junction set at -2.0 V. The gate voltage applied to the second junction is varied as follows: (upper left) -2.0 V, (upper right) 1.0 V, (lower left) 2.5 V, and (lower right) 2.9 V. The skewness of the interference pattern is observable in the two lower panels of the figure.

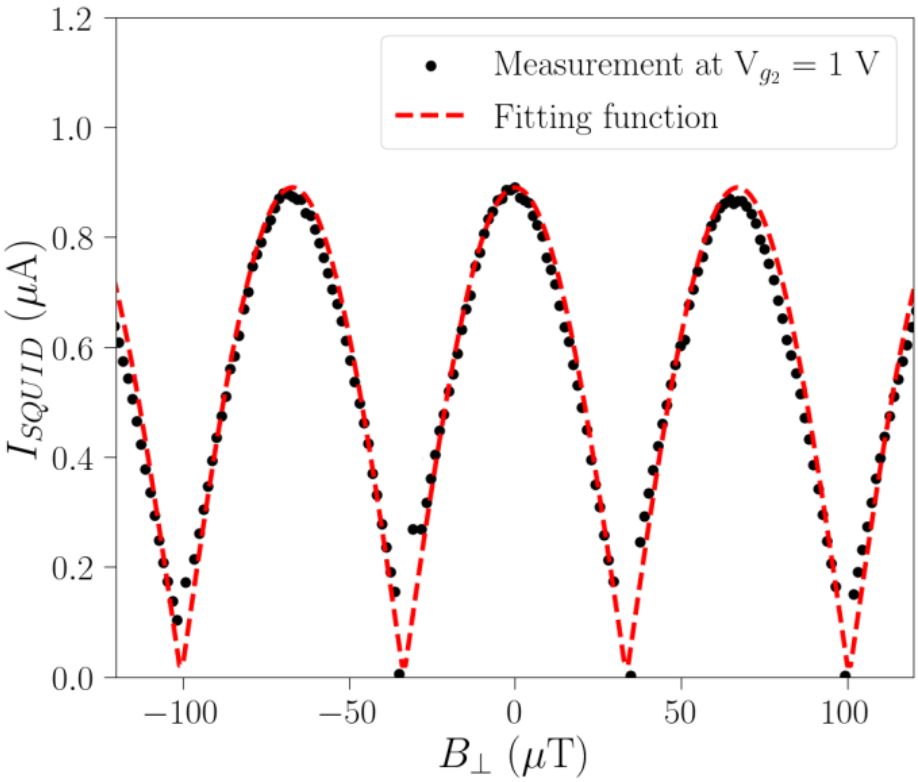

Figure 6.5 – The measured SQUID current (I_{SQUID}) is presented as a function of the perpendicular magnetic field ($B_\perp$), extracted from the I-V characteristics of the SQUID shown in Figure 6.2(a), under the symmetric regime (V_{g_1} = -2.0 V and V_{g_2} = 1.0 V). The red dashed line represents the curve fit of the symmetric SQUID equation. The fitting yields a period of 67 μT for the SQUID oscillations.

6

CPR measurement

In Figure 6.6, the extracted I_{SQUID} curves are shown for V_{g_1} = -2.0 V and V_{g_2} ranging from 2.8 to 3.1 V. The gate voltage range of V_{g_2} from 2.9 to 3.1 V corresponds to a regime where the ratio of I_{C_1}/I_{C_2} is larger than 10 (see Figure 6.8(b)). To obtain a rough estimate of the junction's transparency (τ), the critical current profile of the junction was fitted using the CPR corresponding to a short S-N-S junction, as described by Golubov et al. [41]:

$$I_s(\varphi) = \frac{\pi\Delta}{2eR_N} \frac{\sin(\varphi)}{\sqrt{1-\tau\sin^2(\frac{\varphi}{2})}} \times \tanh\left[\frac{\Delta}{2T}\sqrt{1-\tau\sin^2(\frac{\varphi}{2})}\right], \tag{6.15}$$

where, I_s is the CPR of the junction, Δ is a superconducting gap of the contact, R_N is the normal state resistance, φ is the phase difference across the junction, τ is the junction transparency, and T is the temperature.

Here, the phase difference across the junction depends on the magnetic flux (Φ) within the SQUID loop. We neglected the temperature dependence, and fitted the measured SQUID current:

$$I_{SQUID} = I_{C_1} + I_{C_2} f\left(\frac{2\pi\Phi}{\Phi_0} + \frac{\pi}{2}\right), \tag{6.16}$$

with the skewed sine function:

$$f(x) \propto \frac{\sin(x)}{\sqrt{1 - \tau \sin^2\left(\frac{x}{2}\right)}}, \tag{6.17}$$

to extract the values of τ, I_{C_1}, and I_{C_2}.

The extracted τ and the critical current ratio (I_{C_1}/I_{C_2}) are plotted in Figure 6.7. The results show a transparency of around 0.48 at -2.8 V. This value appears to decrease as the gate voltage increases. The estimated transparency values are lower than expected for the high value of the $I_C R_N$ product. This discrepancy

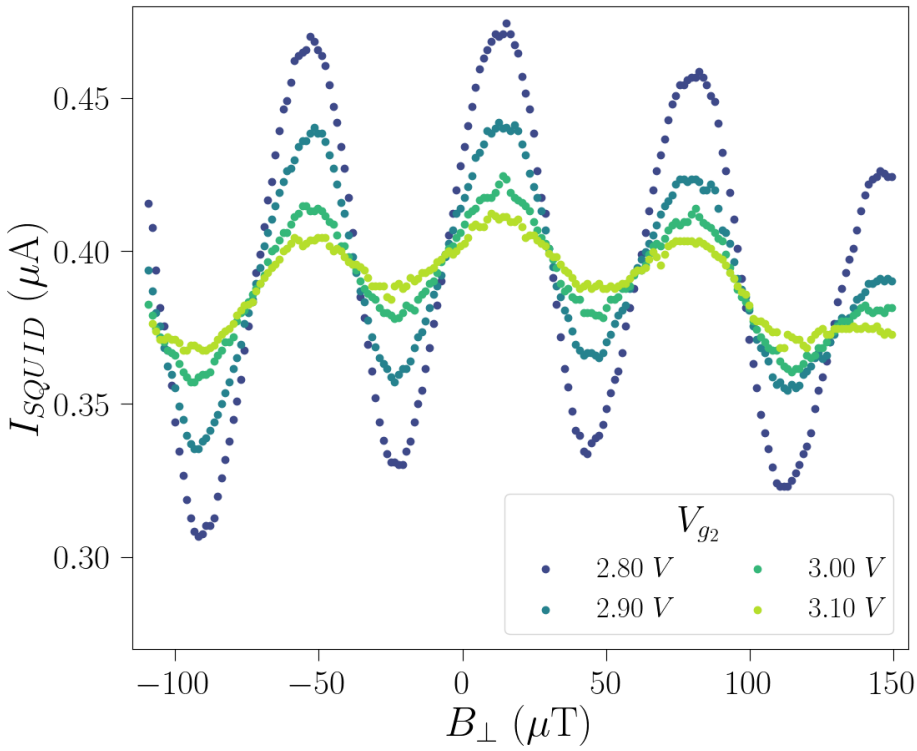

Figure 6.6 – The measured SQUID current (I_{SQUID}) is plotted as a function of the perpendicular magnetic field ($B_\perp$), extracted from the I-V characteristics of the SQUID shown in Figure 6.2(a) at V_{g_1} = -2.0 V and V_{g_2} ranging from 2.8 to 3.1 V.

may be attributed to the measurement being conducted when the gate voltage was close to depletion, affecting the carrier density in the transport channel.

Additionally, the result in Figure 6.7(a) shows large fitting uncertainties. This can be understood by considering the nature of the skewed sine function. Figure 6.8 illustrates I_C as a function of Φ/Φ_0 at V_{g_1} = -2.0 V and V_{g_2} = 2.90 V. The fit of the data to the skewed sine function, indicated by the red line, is not significantly distinguishable from the fit to the regular sine function, indicated by the green line. The inset in the figure presents the skewed sine function at various τ values. It demonstrates that the skewness is not very noticeable when τ is far from unity.

In conclusion, to fulfill the condition of $I_{C_1} > 10\ I_{C_2}$ in this symmetric SQUID, we set V_{g_2} above 2.9 V, near the threshold voltage. This may reduce the transparency of the junction. When the transparency is too low, it results in substantial fitting uncertainties.

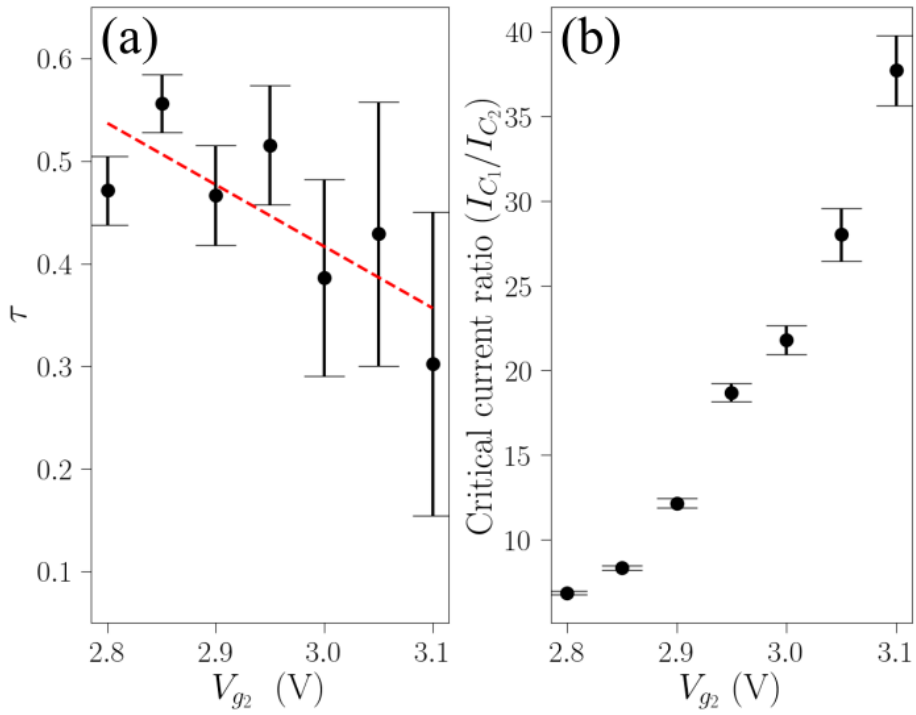

Figure 6.7 – (a) Transparency (τ) of the junction as a function of the gate voltage (V_{g_2}). The uncertainty of the fit is indicated by the error bars in the figure. The transparency exhibits a decreasing trend with increasing gate voltage. (b) Critical current ratio (I_{C_1}/I_{C_2}) as a function of V_{g_2}.

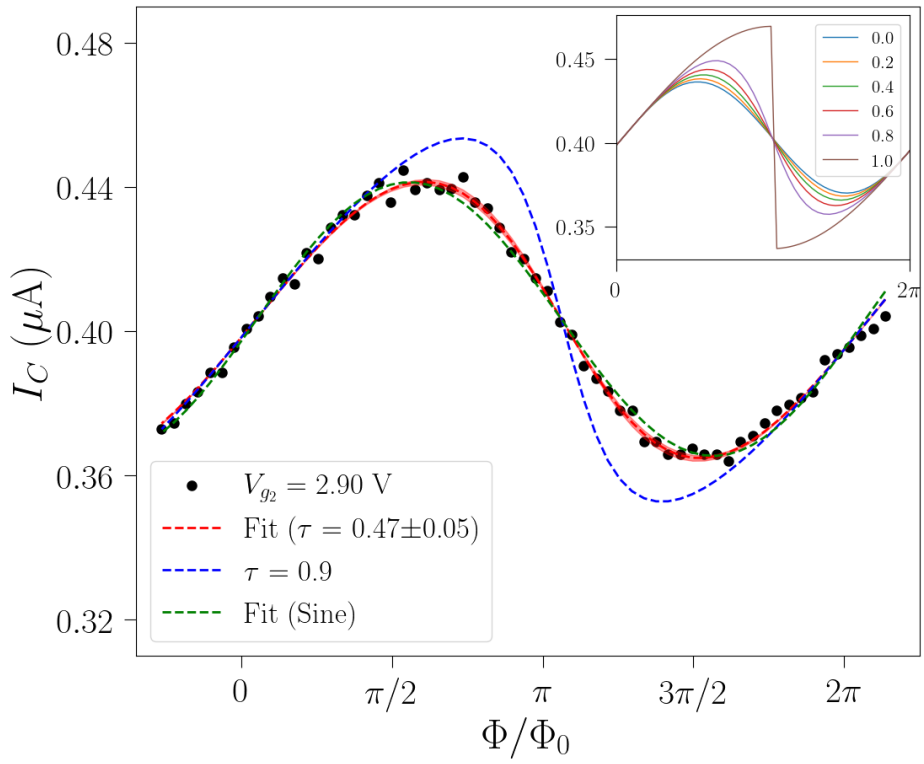

Figure 6.8 – The critical current curve (I_C) as a function of normalized magnetic flux (Φ/Φ_0) extracted from the I-V characteristic of the SQUID in Figure 6.2(a) when V_{g_1} = -2.0 V, and V_{g_2} = 2.9 V. The red dashed line shows the fit of the data with the current-phase relation (CPR) of the short junction model. The green dashed line shows the fit of the data with a sine wave. The blue dashed line shows the plot of the CPR in the case of transparency (τ) = 0.9. The inset shows the CPR at different τ.

6.3.2 Device (b): L_1 = 300 nm, L_2 = 300 nm, W_1 = 1 µm, W_2 = 8 µm, S = 9.5 × 5 µm^2

Here, we present the results of the measurement on the asymmetric SQUID depicted in Figure 6.2(b). The advantage of this asymmetric SQUID is that we can now satisfy the condition of $I_{C_1} > 10\ I_{C_2}$ without needing to bring the junction close to depletion. The experiments in this subsection were conducted by A. Leblanc, a doctoral student in the group.

Figure 6.9 illustrates the extracted I_C as a function of $B_\perp$, with the gate voltage in the small junction (V_{g_1}) set to (solid purple) -2 and (dashed dark blue) 4 V. The gate voltage in the large junction (V_{g_2}) was maintained at -2 V. When V_{g_1} = 4 V, as indicated by the blue dashed line labeled as I_2, the small junction is effectively closed, resulting in an interference pattern resembling the Fraunhofer pattern of the large junction. The diffraction period is approximately 105 µT, corresponding

to a junction area of 19.6 µm^2. Assuming an 8 µm junction width, the actual length is calculated to be 2.45 µm, considerably larger than the designed value of 300 nm.

The purple solid line, labeled as I_1, exhibits an interference pattern resembling a distorted Fraunhofer pattern of the large junction. We interpret this as a combination of the CPR of the small junction and the Fraunhofer diffraction of the large junction. The inset shows the subtraction $(I_1 - I_2)$ and the fitting of $I_1 - I_2$ using Equation 6.17. The data fits the skewed sine function with τ of 0.7 and a CRP periodicity of 52 µT. However, the data seems to align well with the skewed sine function at a lower value of τ, as demonstrated by the green dashed line for $\tau = 0.1$, for instance.

We consider several causes of inaccuracy. First, the period of the SQUID oscillation is comparable to the period of the Fraunhofer diffraction of the large junction, and the CPR has been affected by the reduction of I_C caused by the Fraunhofer effect. Similar to what we have observed in our JoFETs, the measured

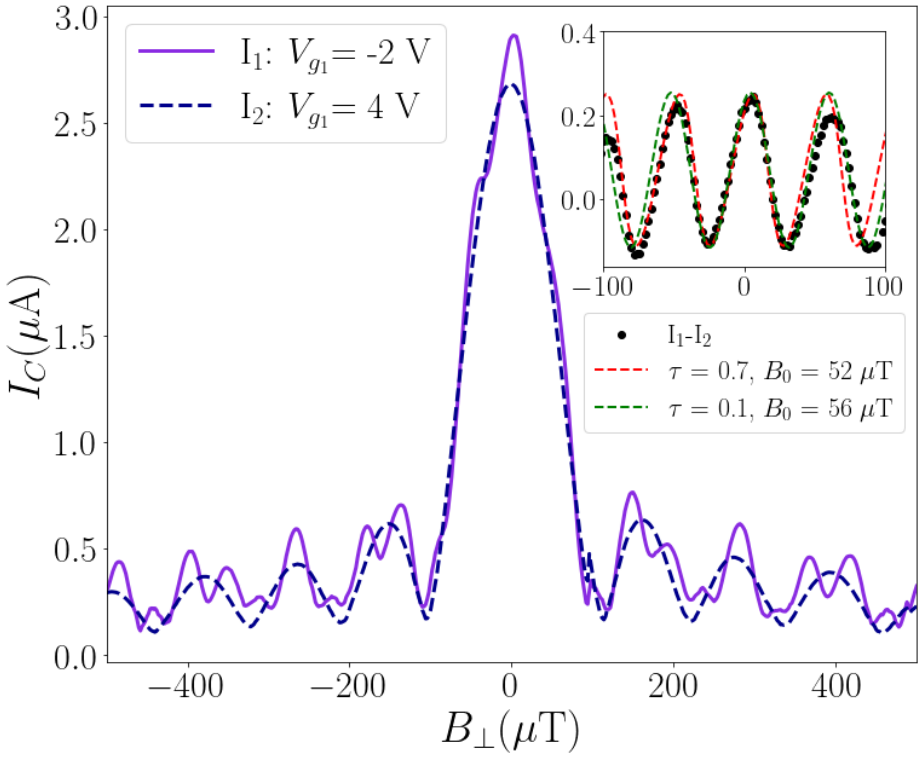

Figure 6.9 – The measured critical current (I_C) as a function of the perpendicular magnetic field ($B_\perp$) extracted from the I-V characteristics of the SQUID in Figure 6.2(b) at V_{g_2} = -2.0 V and V_{g_1} equals to: (I_1, solid purple) -2 V, and (I_2, dashed dark blue) 4 V. The inset shows the fitting of $I_1 - I_2$ with the CPR of the short junction model.

period of the Fraunhofer diffraction pattern for the large junction is much smaller than theoretical value for this junction geometry. This could be attributed to flux focusing and penetration depth, which make the effective junction area much larger than the designed values. Another source of inaccuracy could be the lacking of the statistic of the data, as critical current measurement is a stochastic process.

6.4 Shapiro steps: the effect of microwaves on Josephson current

Shapiro steps, first reported in 1963 by S. Shapiro [122], are step-like features in the current-voltage (I-V) characteristic of a Josephson junction irradiated with photons. In this section, we will review the related theory and discuss why studying Shapiro steps is related to the $\cos 2\varphi$ qubit.

6.4.1 Josephson equations and AC Josephson effect

First, we introduce two well-known Josephson equations.

For simplicity, we consider a Josephson junction with purely sinusoidal current-phase relation. Then, the critical current of a junction at a function of phase is given by [27]:

$$I_s = I_C \sin(\varphi), \tag{6.18}$$

Here, I_s represents the supercurrent across the junction, I_C is the critical current, which is the maximum supercurrent the junction can sustain, and φ is the superconducting phase difference across the junction.

The second equation, which describes the evolution of the phase of a voltage-biased junction over time, can be written as [27]:

$$\frac{\mathrm{d}\varphi}{\mathrm{d}t} = \frac{2e}{\hbar} V, \tag{6.19}$$

In this equation, V denotes the voltage drop across the junction.

Combining these two Josephson equations, when a specific voltage V is applied across the junction, the supercurrent through the junction can be expressed as:

$$I_s = I_C \sin\left(\varphi_0 + \frac{2e}{\hbar} V t\right), \tag{6.20}$$

In this equation, φ_0 represents the initial phase difference across the junction.

This implies that the supercurrent flowing through the junction will become an alternating current with an oscillation frequency proportional to the voltage across the junction. It is also referred to as the "AC Josephson effect."

6.4.2 Inverse AC Josephson effect and Shapiro steps

On the contrary, if we consider the scenario where a Josephson junction is exposed to microwave radiation with a frequency ω_{RF}. The voltage across the junction can be expressed as:

$$V = V_0 + V_{RF}\cos(\omega_{RF}t), \tag{6.21}$$

Here, V represents the voltage across the junction, V_0 is the DC voltage applied to the junction, and V_{RF} is the magnitude of the radiated voltage.

Consequently, the phase difference across the junction becomes:

$$\varphi = \varphi_0 + \frac{2e}{\hbar}V_0 t + \frac{2e}{\hbar}\frac{V_{RF}}{\omega_{RF}}\sin(\omega_{RF}t). \tag{6.22}$$

By substituting this into Equation 6.18, we obtain the supercurrent:

$$I_s = I_C\sin(\varphi) = I_C\,\mathfrak{Im}\left[\exp\left(i(\varphi_0 + \frac{2e}{\hbar}V_0 t + \frac{2e}{\hbar}\frac{V_{RF}}{\omega_{RF}}\sin(\omega_{RF}t))\right)\right] \tag{6.23}$$

Here, we define $z = (2eV_{RF})/(\hbar\omega_{RF})$, and $\alpha = \omega_{RF}t$, then substitute these into Equation 6.23 to get:

$$I_s = I_C\,\mathfrak{Im}\left[\exp\left(i(\varphi_0 + \frac{2e}{\hbar}V_0 t)\right)\cdot\exp(iz\sin(\alpha))\right]. \tag{6.24}$$

The term $\exp(iz\sin(\alpha))$ can be expressed in the form of Bessel functions as:

$$\exp(iz\sin(\alpha)) = \sum_{k=-\infty}^{\infty}(-1)^k J_k(z)\exp(-ik\alpha), \tag{6.25}$$

where $k \in \mathbb{Z}$.

Substituting this back into Equation 6.23 yields:

$$I_s = I_C\,\mathfrak{Im}\left[\exp\left(i(\varphi_0 + \frac{2e}{\hbar}V_0 t)\right)\cdot\sum_{k=-\infty}^{\infty}(-1)^k J_k(z)\exp(-ik\alpha)\right] \tag{6.26}$$

$$I_s = I_C\sum_{k=-\infty}^{\infty}\mathfrak{Im}\left[(-1)^k J_k(z)\exp\left(i(\varphi_0 + \frac{2e}{\hbar}V_0 t - k\alpha)\right)\right] \tag{6.27}$$

$$I_s = I_C\sum_{k=-\infty}^{\infty}(-1)^k J_k(z)\sin\left(\varphi_0 + \frac{2e}{\hbar}V_0 t - k\alpha\right). \tag{6.28}$$

Equation 6.28 is referred to as the "inverse AC Josephson effect [123]." This equation indicates that the DC component of the supercurrent will be zero unless the condition:

$$\frac{2e}{\hbar}V_0 t = k\alpha \tag{6.29}$$

$$V_0 = \frac{k\hbar\omega_{RF}}{2e}, k \in \mathbb{Z}, \tag{6.30}$$

is satisfied.

Thus, the supercurrent has a DC part given by:

$$I_s = I_C(-1)^k J_k(\frac{2eV_{RF}}{\hbar\omega_{RF}})\sin(\varphi_0). \tag{6.31}$$

In practice, we can measure the DC current $I = I_N + I_s$, where $I_N = V_0/R_N$ is the normal current. In the I-V characteristic, this results in current plateaus with widths of $J_k(2eV_{RF}/\hbar\omega_{RF})$ when the DC voltages are equal to $V_0 = k\hbar\omega_{RF}/2e$. These step-like plateau features are known as "Shapiro steps,", as shown in Figure 6.10. The figure illustrates the I-V characteristics of a Josephson junction under 72 GHz radiation at different power levels. From the figure, it can be observed that the voltage steps of $\hbar\omega_{RF}/2e$ (labeled in blue) remain the same across all the curves since they are determined by the radiation frequency. Conversely, the plateaus (labeled in red and purple) vary with radiation powers, which are related to V_{RF}.

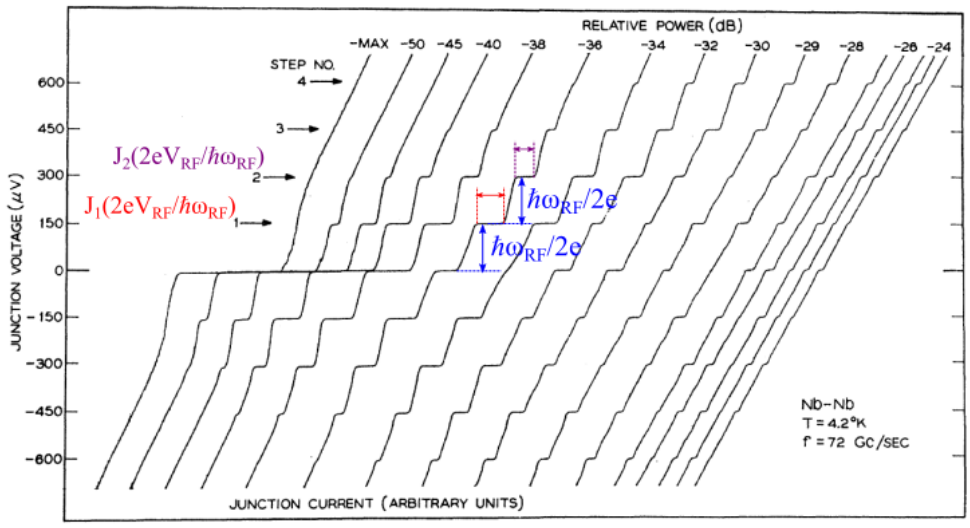

Figure 6.10 – I-V characteristics of a Nb-Nb point-contact Josephson junction under the exposure of microwave radiation at 72 GHz at various microwave powers. The figure is reproduced from [124].

6.5 On the hunt for (Half-integer?) Shapiro steps

From the first Josephson equation, if we assume that a junction also possesses a second harmonic term, Equation 6.18 can be redefined as:

$$I_s = I_{C,1}\sin(\varphi) + I_{C,2}\sin(2\varphi), \tag{6.32}$$

Here, $I_{C,1}$ and $I_{C,2}$ represent the magnitudes of critical currents associated with the transport of one Cooper pair and two Cooper pairs, respectively.

Substituting Equation 6.22 into Equation 6.32 yields:

$$\begin{aligned} I_s =& I_{C,1}\,\mathfrak{Im}\left[\exp\left(i(\varphi_0 + \frac{2e}{\hbar}V_0 t + \frac{2e}{\hbar}\frac{V_{RF}}{\omega_{RF}}\sin(\omega_{RF}t))\right)\right] + \\ & I_{C,2}\,\mathfrak{Im}\left[\exp\left(2i(\varphi_0 + \frac{2e}{\hbar}V_0 t + \frac{2e}{\hbar}\frac{V_{RF}}{\omega_{RF}}\sin(\omega_{RF}t))\right)\right] \end{aligned} \tag{6.33}$$

$$\begin{aligned} I_s =& I_{C,1}\,\mathfrak{Im}\left[\exp\left(i(\varphi_0 + \frac{2e}{\hbar}V_0 t)\right)\cdot\exp(iz\sin(\alpha))\right] + \\ & I_{C,2}\,\mathfrak{Im}\left[\exp\left(2i(\varphi_0 + \frac{2e}{\hbar}V_0 t)\right)\cdot\exp(2iz\sin(\alpha))\right]. \end{aligned} \tag{6.34}$$

By using the same trick, we obtain:

$$\begin{aligned} I_s =& I_{C,1}\sum_{k=-\infty}^{\infty}(-1)^k J_k(\frac{2eV_{RF}}{\hbar\omega_{RF}})\sin\left(\varphi_0 + (\frac{2e}{\hbar}V_0 - k\omega_{RF})t\right) + \\ & I_{C,2}\sum_{k=-\infty}^{\infty}(-1)^k J_k(\frac{4eV_{RF}}{\hbar\omega_{RF}})\sin\left(2\varphi_0 + (2\cdot\frac{2e}{\hbar}V_0 - k\omega_{RF})t\right). \end{aligned} \tag{6.35}$$

From the equation, additional to the Shapiro steps occurring when $V_0 = k\hbar\omega_{RF}/2e$, we also expect to see "half-integer Shapiro steps," which, as implied by the name, are step-like features occurring at $V_0 = (k/2)\hbar\omega_{RF}/2e$. These half-integer Shapiro steps can serve as indicators for the presence of the second harmonic term mentioned in Equation 6.32.

In this context, we conducted preliminary measurements on a SQUID device from the same chip as the one shown in Figure 6.2(a). The two junctions in the measured device have junction widths of 1 µm and 5 µm, respectively, with both junction lengths being 200 nm. In the experiment, microwave radiation is generated by a microwave generator, and the signal passes through a -60 dB attenuator before reaching a microwave connector on the PCB. This microwave connector is linked to the Al contacts of the SQUID using wire bonding techniques.

Figure 6.11(a) shows I-V characteristics at different microwave frequencies. The gate voltage on the 1 µm junction (V_{g_1}) was set to 2.2 V, and the gate voltage on the 5 µm junction (V_{g_2}) was set to 4 V. The microwave power at the generator

was set to -3 dBm. From the figure, several features are observed at approximately 6, 8, 10, and 12 µV for radiation frequencies of 3, 4, 5, and 6 GHz, respectively. The expected voltage positions, indicated by the red arrows, for these features and calculated using Equation 6.30 are 6.21, 8.28, 10.35, and 12.42 µV, respectively. This suggests that the observed features could be Shapiro steps. Noted that, a variation in plateau widths with frequency can be attributed to the chip's different microwave losses at varying microwave frequencies, affecting the effective V_{RF} absorbed by the junction. Figure 6.11(b) shows I-V characteristics at different microwave powers, at the frequency of 3 GHz. The gate voltage configuration was

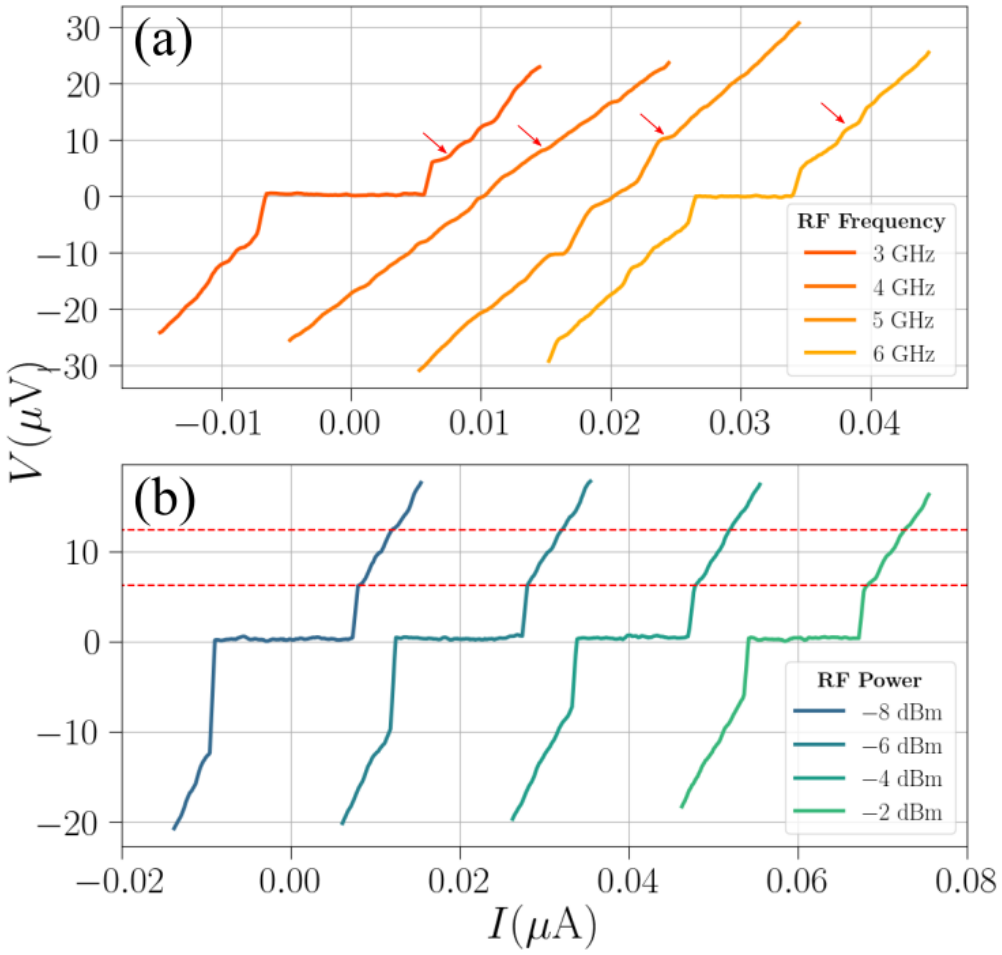

Figure 6.11 – (a) I-V characteristics of an asymmetric SQUID ($L_1 = 200$ nm, $L_2 = 200$ nm, $W_1 = 1$ µm, $W_2 = 5$ µm, $S = 4 \times 4$ µm^2, $V_{g_1} = 2.2$ V, $V_{g_2} = 4$ V) based on SiGe heterostructure as a function of radiated microwave frequencies. The applied microwave power at the generator is set to be -3 dBm. (b) I-V characteristics of the same SQUID as a function of applied microwave powers. The microwave frequency is fixed at 3 GHz.

the same as that in measurements shown in Figure 6.11(a). The red dashed lines are drawn at 6.21 and 12.42 µV, representing the expected positions of the first and second integer Shapiro steps, respectively. In addition to the features aligned with the red dashed lines, there are noticeable features between them. While not conclusive, these features could potentially correspond to the integer and half-integer Shapiro steps, respectively. Additionally, changes in the widths of the zero resistance states were also observed at different powers, indicating that microwave radiation has an effect on the junction.

In conclusion, we investigated the effect of microwave radiation on the I-V characteristics of the junction in the SQUID device. We observed features that can be interpreted as integer and half-integer Shapiro steps. However, due to time constraints, we did not perform further experiment to validate the results.

6.6 Perspective of the experiment

As we have encountered challenges in accurately estimating τ from the CPR measurements conducted on the devices shown in Figure 6.2(a) and (b), we worked on designing and fabricating a new batch of SQUID devices. The device in Figure 6.2(d) has been designed by taking into account the previously mentioned issues. The SQUID loop has an area of 1035 µm^2, large enough to have several SQUID oscillations per one Fraunhofer period. Here, we would like to present the results from some measurements carried out by A. Leblanc, a doctoral student in the group, who is credited for the data and the analysis in this section.

6.6.1 Device (d): $L_1 = 300$ nm, $L_2 = 300$ nm, $W_1 = 1$ µm, $W_2 = 8$ µm, $S = 44.5 \times 40$ µm^2

The inset in Figure 6.12 shows measured critical current (I_C) as a function of applied magnetic field (B) at the center of the middle Fraunhofer peak when the gate voltages in both junctions are set to -2 V. In this experiment, utilizing a threshold detector instrument synchronized with a sawtooth signal generator enables the acquisition of the large numbers of raw data points in a much shorter period of time. We think that the residual magnetic field from the magnetic components within the setup might lead to a slight deviation of the Fraunhofer diffraction center from zero. The main figure shows the amplitude of the fast Fourier transform (FFT) of the raw data depicted in the inset, plotted as a function of Φ_0/Φ. The transformed data shows that the CPR can be effectively described using multiple harmonics within the Fourier series. This statement is supported by the presence of peaks at $\Phi_0/\Phi = 1$ and 2.

6.6.2 Half-integer Shapiro steps on irradiated junction

Figure 6.13(a) displays the DC current (I_{DC}) as a function of the differential resistance (R_{diff}) of the device in Figure 6.2(d), as a function of microwave power.

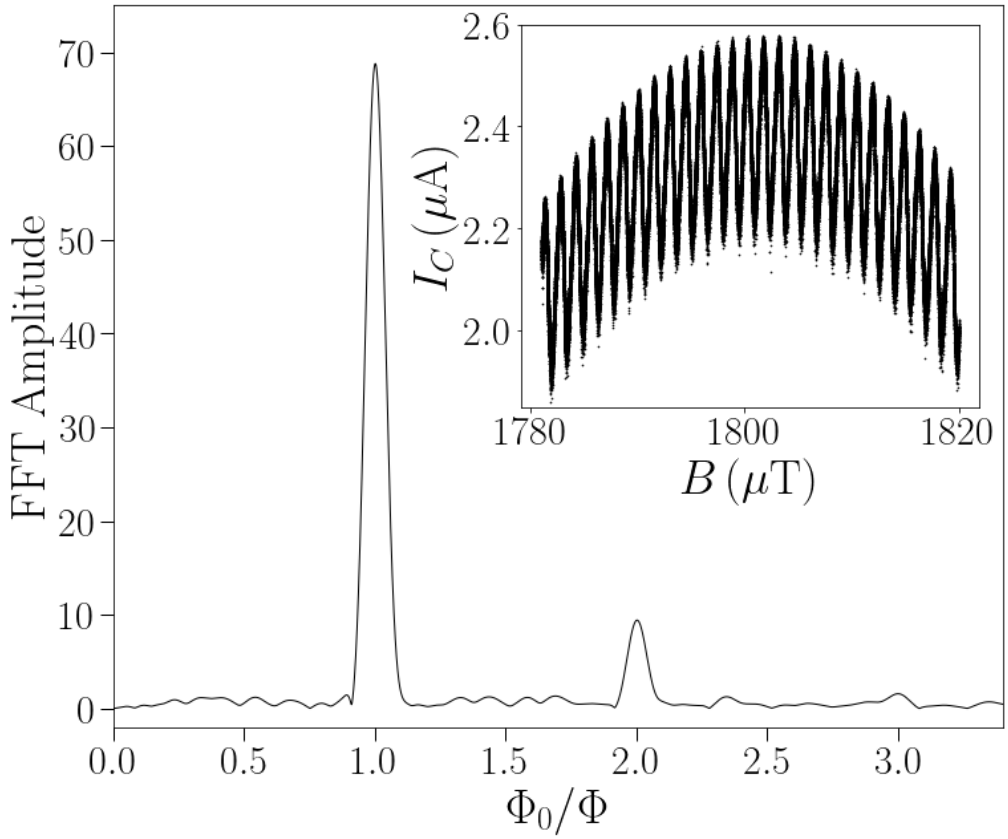

Figure 6.12 – (inset) The critical current (I_C) as a function of the applied magnetic field (B) of the device in Figure 6.2(d). (main figure) Amplitude of the fast fourier transform as a function of the number of harmonics (Φ_0/Φ) processed from the raw data in the inset [A. Leblanc, a doctoral student in the lab].

This measurement is conducted with a microwave frequency set at 3.05 GHz. The gate voltage in the smaller junction is set at -2 V, while the gate voltage in the larger junction is maintained at 2 V. The figure reveals distinct plateaus, indicated by black areas in the color map. The widths of the plateau change in response to varying microwave powers. We interpret these distinct features as Shapiro steps. From the same device, Figure 6.13(b) shows the DC voltage (V_{DC}), plotted on a normalized voltage axis, as a function of R_{diff} against varying microwave power. On the normalized V_{DC} axis, it demonstrates that the positions of these features in located in voltage at both integer and half-integer of the voltage steps.

Additionally, Figure 6.13(c) demonstrates the I-V characteristic along with R_{diff} as a function of I_{DC} at the microwave power of -65 dBm. The curve of R_{diff} versus I_{DC} shows cleary the features at the half-integer of normalized V_{DC}. This assures that the observed features are indeed integer and half-integer Shapiro steps.

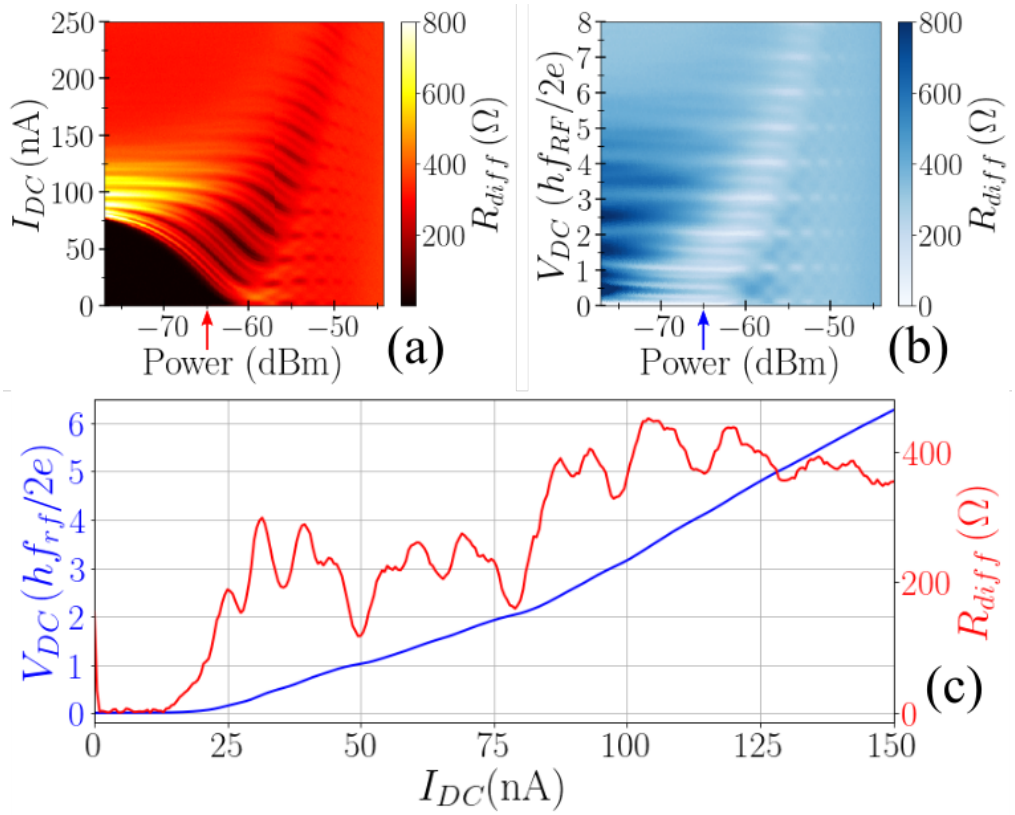

Figure 6.13 – (a) The DC current (I_{DC}) as a function of differential resistance (R_{diff}) and microwave powers of the device in Figure 6.2(d) at V_{g_1} = -2 V, and V_{g_2} = 2 V. (b) The normalized DC voltage (V_DC in a unit of $hf_{RF}/2e$) as a function of R_{diff} and microwave powers from the same device. (c) (blue) I-V characteristic, and (red) R_{diff} versus I_{DC} at the microwave power of -65 dBm. [A. Leblanc, a doctoral student in the lab].

Conclusion

Superconducting qubits based on the principle of circuit quantum electrodynamics (cQED) is arguably one of the most advanced quantum computing platforms so far, as the knowledge on qubit fabrication, qubit manipulation, and qubit readout has been well-established and can be highly engineered. Gate-tuanble transmon, or gatemon, in short, is a variant of transmon, where the Josephson junction is made of superconductor-semiconductor-superconductor (S-Sm-S) materials. In the S-Sm-S junction, the Josephson energy of the junction can be tuned by the gate voltage, allowing the tuning of the qubit energy, which is a crucial requirement for the logic gate operations. Among many semiconductor materials, germanium (Ge) is the one that catches our interest due to its compatibility with CMOS technology, high hole mobility, and low metal-Ge Schottky barrier [22]. These bring us to our interest in studying hybrid superconductor-semiconductor devices based on Ge for quantum information applications. We aim to fabricate the devices with a top-down approach on SiGe heterostructures.

To begin with, we first study gate-tunable S-Sm-S junctions in Josephson field effect transistors (JoFETs), as they are one of the simplest hybrid devices. We develop the fabrication recipe for Al-Ge-Al JoFETs with high transparency and high yields. The good Al-Ge interface of the junction relies on well-controlled dry etching combined with in-situ Ar etching.

There is an in-depth study of the properties of Ge-based JoFETs as a function of gate voltage, temperature, and magnetic field in the early stages of the thesis. Below the superconducting transition of the Al contacts, the devices exhibit a strong superconducting proximity effect due to the very high transparency at the S-Sm interfaces. The $I_C R_N$ products extracted from the measurements exhibit a value up to 149 µV for the shortest junction length (150 nanometers). The normalized excess current ($I_{exc} R_N/\Delta$) gives a transparency of $\tau \approx 0.92$ [82]. Sub-

gap anomaly features indicating multiple Andreev reflections (MARs) are observed up to the third order.

Following that, NbN superconducting resonators, fabricated on SiGe substrates, are studied by transmission measurement. We perform the measurement to collect the transmission amplitude and phase of the transmission line coupled to the resonators. From this data, we can extract the resonant frequency (f_r), internal quality factor (Q_i), and coupling quality factor (Q_c) of the resonators. We found that these parameters extracted from the measurement are in good agreement with the simulation and calculation.

In the later stage, combining our understanding on JoFETs and resonators, we design and fabricate gatemons (gate-tunable transmons) by integrating the Al-Ge-Al junctions in the superconducting circuits, comprising capacitors and S-Sm-S based Josephson junctions, and coupling them to the resonators. We perform qubit measurements on a gatemon. The qubit exhibits anticrossing, the signature of the resonator-qubit interaction. We perform two-tone spectroscopy measurements to extract the resonant frequency of the gatemon as a function of gate. The resonant frequency of the qubit is gate-tunable with the highest measurable frequency of 10 GHz, which is in good agreement with the value of the critical current of the junction with the same geometry. The qubit shows the narrowest linewidth of 50.2 MHz. From the linewidth, we estimate crudely that the coherence time could be in the order of a few nanoseconds, far below that of the state-of-the-art of 30 µs [50]. We think that the qubit suffers from threshold shifting and gate instability due to the charge trap on the oxide interface.

In another part of the story, we study several SQUIDs, fabricated with the same process recipe as JoFETs. We perform the measurement of the critical current as a function of the applied magnetic field and found that the current-phase relationship of the junctions is non-sinusoidal. Additionally, we observe integer and half-integer Shapiro steps in irradiated junctions. These indicate the existence of the $\cos 2\varphi$ element, the requirement for the protected qubit, in the junction transport.

In terms of perspectives, we think that the project poses the potential to be pursued further in several directions, thanks to the reliable fabrication recipe for Al-Ge-Al junctions we developed during this thesis.

On one hand, there are many things we can study to better understand the physics of the junctions with JoFET geometry. We can gain more information about whether the transport is ballistic or diffusive by getting more statistics of the junction parameters (I_C and R_N) with various lengths. The study of junction transport in the non-zero resistance regime also raises an interesting question about the mysterious features that cannot be associated with MARs, which we can perform a systematic study on.

In terms of technology development, the qubit that we fabricated in this thesis is still in the very early stages. There is a lot more to be optimized and improved, as we mentioned at the end of Chapter 5. Additionally, it could also be interesting to implement the junctions on other kinds of S-Sm-S based quantum information

devices, such as the parametric amplifier [125] as an example.

Lastly, benefiting from the high transparency, we can pursue the realization of the protected $\cos 2\varphi$ qubit based on Ge. The first step could be to study the suppression of the $\cos \varphi$ term, which can be performed by the Josephson diode effect experiment [126].

As a closure, we present several hybrid S-Sm devices with many further possibilities to consider. For this, I give the best wishes to the next student who takes it on the next journey.

Appendices

APPENDIX A

Fabrication recipes

In this appendix, I have listed the fabrication recipes for all the devices presented in this thesis, along with the machines used for each fabrication step.

A.1 Machines

- Electron beam lithography: JEOL-6300FS (100kV, I = 1 or 5 nA)
- Laser lithography: HEIDELBERG INSTRUMENTS µPG-101
- Optical lithography: MJB4
- ICP for SiGe etching: SI-500-324 SENTECH
  - Chamber cleaning: Cleaning wafer (unpolished Si), 15 sccm O_2 + 50 sccm SF_6 + 10 sccm Ar, ICP Power 600 W, RF Power 30 W, Pressure 1.05 Pa, 20°C, for 5 minutes → 140 sccm Ar, ICP Power 0 W, RF Power 0 W, Pressure 5 Pa, 20°C, for 1 minute
  - Chamber conditioning: Conditioning wafer (unpolished Si), 10 sccm CF_4 + 40 sccm Ar, ICP Power 200 W, RF Power 25 W, Pressure 1.3 Pa, 20°C, 5 minutes
  - Etching: Carrier wafer (sample glued on unpolished Si by CGR7016), 10 sccm CF_4 + 40 sccm Ar, ICP Power 200 W, RF Power 25 W, Pressure 1.3 Pa, 20°C, for the duration of the etching time
  - Chamber cleaning: Cleaning wafer (unpolished Si), 15 sccm O_2 + 50 sccm SF_6 + 10 sccm Ar, ICP Power 600 W, RF Power 30 W, Pressure 1.05 Pa, 20°C, for 5 minutes → 140 sccm Ar, ICP Power 0 W, RF Power 0 W, Pressure 5 Pa, 20°C, for 1 minute

ICP for NbN etching: Plasmalab100 OXFORD

- Chamber preparation: Cleaning wafer (unpolished Si), 50 sccm O_2, ICP Power 1500 W, RF Power 100 W, Pressure 10 mTorr, 20°C, for 10 minutes → 5 sccm O_2 + 10 sccm SF_6, ICP Power 0 W, RF Power 0 W, Pressure 5 mTorr, 20°C, for 2 s → 5 sccm O_2 + 10 sccm SF_6, ICP Power 0 W, RF Power 50 W, Pressure 5 mTorr, 20°C, for 8 minutes
- Etching: Carrier wafer (sample glued on unpolished Si by CGR7016), 5 sccm O_2 + 10 sccm SF_6, ICP Power 0 W, RF Power 0 W, Pressure 5 mTorr, 20°C, for 2 minutes → 5 sccm O_2 + 10 sccm SF_6, ICP Power 0 W, RF Power 50 W, Pressure 5 mTorr, 20°C, for the duration of the etching time
- Chamber cleaning: Cleaning wafer (unpolished Si), 50 sccm O_2, ICP Power 1500 W, RF Power 100 W, Pressure 10 mTorr, 20°C, for 10 minutes

- Oxygen plasma etching for resist removal: PICO MW PCCE 7 DIENER (300 W)
- Evaporator for Al, Cr, Ti, and Au deposition: MEB550 PLASSYS
- Sputtering maching for NbN deposition: MP600S PLASSYS
- Atomic layer deposition machine for aluminum oxide: FIJI-200 ULTRATECH
- Chip cleaning: Unless otherwise mentioned, chip cleaning means 5 minutes in acetone with ultrasound, followed by 5 minutes in IPA with ultrasound, and blowing with N_2 until dry

A.2 JoFETs and SQUIDs

Chip preparation

- Cleaving: Diamond pen/ Diamond scribber followed by chip cleaning

A

Markers

- Resist spinning: PMMA 4%, 4000 rpm for 60 s (2000 rpm/s) → bake at 180°C for 5 min
- E-beam exposure: 1100 µC/cm^2
- Resist developing: 30 s MIBK:IPA 1:3 → 30 s IPA
- Marker deposition: No etch, 5 nm Ti, 75 nm Au
- Lift-off: Acetone → followed by chip cleaning

Mesa etching

- Resist spinning: VM652, 4000 rpm for 60 s (2000 rpm/s) → MAN2403, 4000 rpm for 30 s (2000 rpm/s) → bake at 90°C for 90 s
- E-beam exposure: 420 µC/cm^2
- Resist developing: 45 s MF26 → 15 s MF21A: DI water 1:9
- Mesa etching: SiGe etching 25 s
- Cleaning: chip cleaning → 3 min O_2 plasma → chip cleaning

Ohmic contacts

- Resist spinning: ZEP520A, 4000 rpm for 60 s (2000 rpm/s) → bake at 180°C for 5 min
- E-beam exposure: 480 µC/cm^2
- Resist developing: 60 s MIBK:IPA 1:1 → 20 s MIBK:IPA 89:11
- SiGe top layer etching: SiGe etching 11 s
- Ohmic contact deposition: in-situ Ar etch, 300 V, 36 s → 50 nm Al
- Lift-off: AR300-76 → rinse with DI water for 5 min → chip cleaning → 6 min O_2 plasma → chip cleaning

Insulating layer deposition

- ALD machine: 10 min in-situ O_2 plasma → 108 cycle Al_2O_3 plasma-assisted for 10 nm, 280°C

Gate deposition

- Resist spinning (double layers): PMMA 4%, 4000 rpm for 60 s (2000 rpm/s) → bake at 180°C for 5 min → repeat from the beginning
- E-beam exposure: 1100 µC/cm^2
- Resist developing: 30 s MIBK:IPA 1:3 → 30 s IPA
- Marker deposition: No etch, 10 nm Ti, 130 nm Au
- Lift-off: Acetone → followed by chip cleaning

A.3 NbN resonators

Chip preparation

- Cleaving: Diamond pen/ Diamond scribber followed by chip cleaning

NbN deposition

- ALD machine (for some sample mentioned NbN on Al_2O_3): 10 min in-situ O_2 plasma → 108 cycle Al_2O_3 plasma-assisted for 10 nm, 280°C
- NbN sputtering deposition: 180°C thermalization for 14 hours → $I = 2$ A, $V = 314$ V on Nb target, 35 sccm Ar 40% N_2 0.1 mbar, 22 s sputtering time for 20 nm

Resonator patterning

- Resist spinning: AZ1512, 4000 rpm for 60 s (2000 rpm/s) → bake at 100°C for 90 s → laser lithography manual focus
- Resist developing: 30 s AZ developer: DI water 1:1 → DI water rinsing
- Resonators and markers patterning: NbN etching 2 min
- Cleaning: chip cleaning

Bonding pad layer

- Resist spinning: AZ1512, 4000 rpm for 60 s (2000 rpm/s) → bake at 100°C for 90 s → laser lithography manual focus
- Resist developing: 30 s AZ developer: DI water 1:1 → DI water rinsing
- Bonding pad deposition: in-situ Ar etch, 300 V, 36 s → 300 nm Al
- Lift-off: Acetone → followed by chip cleaning

A.4 Gatemon

Chip preparation

- Cleaving: Diamond pen/ Diamond scribber followed by chip cleaning

A

Markers

- Resist spinning: PMMA 4%, 4000 rpm for 60 s (2000 rpm/s) → bake at 180°C for 5 min
- E-beam exposure: 1100 µC/cm^2
- Resist developing: 30 s MIBK:IPA 1:3 → 30 s IPA
- Marker deposition: No etch, 10 nm Ti, 80 nm Au
- Lift-off: Acetone → followed by chip cleaning

Mesa etching

- Resist spinning: VM652 4000 rpm for 60 s (2000 rpm/s) → MAN2403, 4000 rpm for 30 s (2000 rpm/s) → bake at 90°C for 90 s
- E-beam exposure: 420 µC/cm^2
- Resist developing: 45 s MF26 → 15 s MF21A: DI water 1:9
- Mesa etching: SiGe etching 25 s
- Cleaning: chip cleaning → 3 min O_2 plasma → chip cleaning

Ohmic contacts

- Resist spinning: VM652, 4000 rpm for 60 s (2000 rpm/s) → MAN2403, 4000 rpm for 30 s (2000 rpm/s) → bake at 90°C for 90 s
- E-beam exposure: 420 µC/cm^2
- Resist developing: 45 s MF26 → 15 s MF21A: DI water 1:9
- SiGe top layer etching: SiGe etching 11 s
- Ohmic contact deposition: Ar etch, 300 V, 36 s → 50 nm Al
- Lift-off: NMP at 80°C → chip cleaning → 6 min O_2 plasma → chip cleaning

Insulating layer deposition

- ALD machine: 10 min in-situ O_2 plasma → 108 cycle Al_2O_3 plasma-assisted for 10 nm, 280°C

NbN deposition

- NbN sputtering deposition: 180°C thermalization for 14 hours → I =2 A, V= 314 V on Nb target, 35 sccm Ar 40% N_2 0.1 mbar, 22 s sputtering time for 20 nm

Gate layer

- Resist spinning: ZEP520A, 4000 rpm for 60 s (2000 rpm/s) → bake at 180°C for 5 min
- E-beam exposure: 480 µC/cm^2
- Resist developing: 60 s MIBK:IPA 1:1 → 20 s MIBK:IPA 89:11
- Resonators and gates patterning: NbN etching 80 s
- Resist removal: 4 min Deep UV flushing → 60 s MIBK:IPA 1:1 → 20 s MIBK:IPA 89:11 → chip cleaning

Bonding pad layer

- Resist spinning: AZ1512, 4000 rpm for 60 s (2000 rpm/s) → bake at 100°C for 90 s → laser lithography manual focus
- Resist developing: 30 s AZ developer: DI water 1:1 → DI water rinsing
- Bonding pad deposition: in-situ Ar etch, 300 V, 36s → 300 nm Al
- Lift-off: Acetone → followed by chip cleaning

APPENDIX B

Supplemental data on transport in JoFETs

In this appendix, we present the supplemental data on transport in JoFETs as a function of gate voltage, temperature, and magnetic field. The device labels (A1, A2, A3, A4, B1, B2, B3, and B4) refer to those in Table 3.2.

The current-voltage ($I-V$) characteristics at different gate voltages (V) have been collected at the base temperature without an applied magnetic field. We use the data from these $I-V$ characteristics to produce Figures 3.18, 3.19, and 3.20.

The curves of the differential resistance (dV/dI) as a function of the current (I) at different temperatures (T) have been collected at the gate voltage (V_g) of -2 V without an applied magnetic field. The data from these curves has been used to produce Figure 3.21. Note that each curve has been shifted by 20 Ω for visibility.

The current-voltage ($I-V$) characteristics as a function of the magnetic field ($B_\perp$) have been collected at the base temperature, with the gate voltage (V_g) set to -2 V. The data supports the statement in Section 3.4.4 as we observe the discrepancy between the measured and calculated periods of the Fraunhofer diffraction pattern in the devices A1, A2, and A3.

B.1 Current-voltage characteristics at different gate voltages

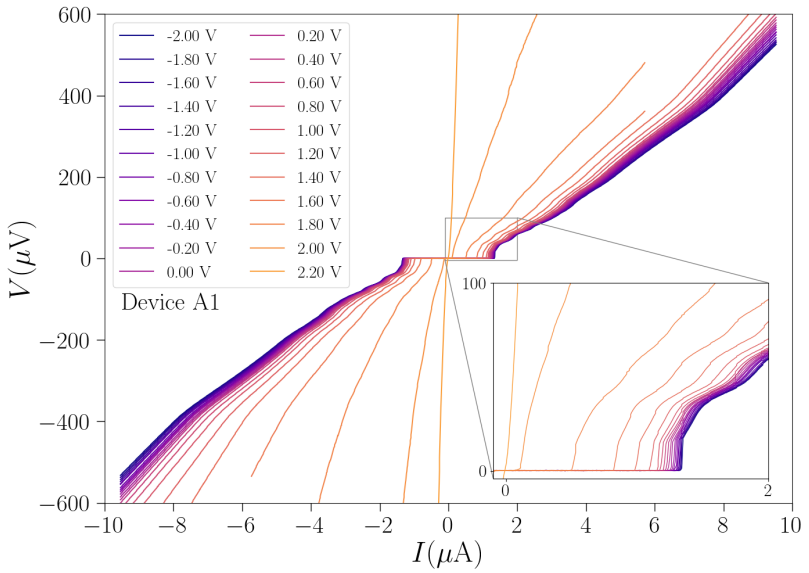

Figure B.1 – Current-voltage ($I - V$) characteristic of the device A1 at different gate voltages (V_g).

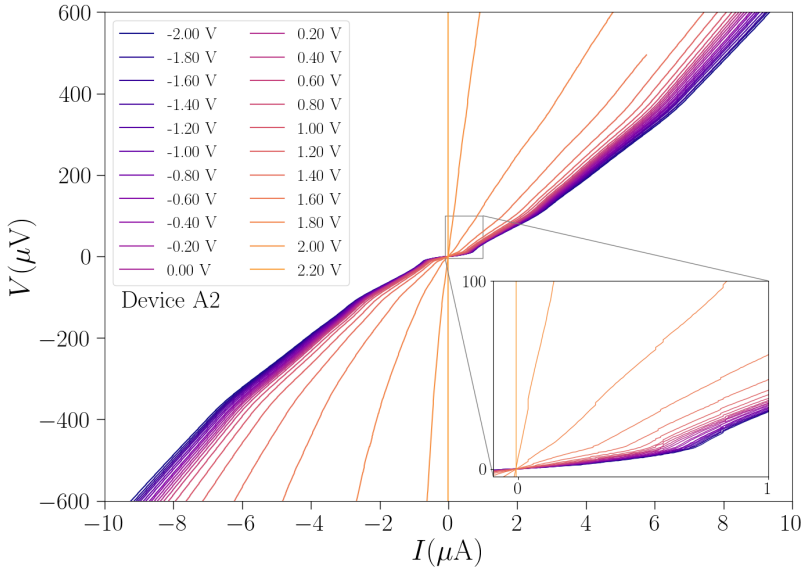

Figure B.2 – Current-voltage ($I - V$) characteristic of the device A2 at different gate voltages (V_g).

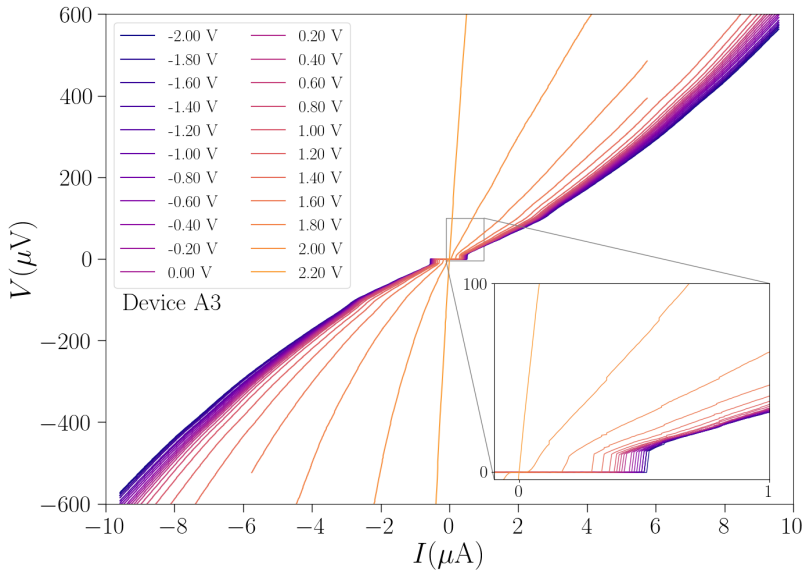

Figure B.3 – Current-voltage ($I - V$) characteristic of the device A3 at different gate voltages (V_g).

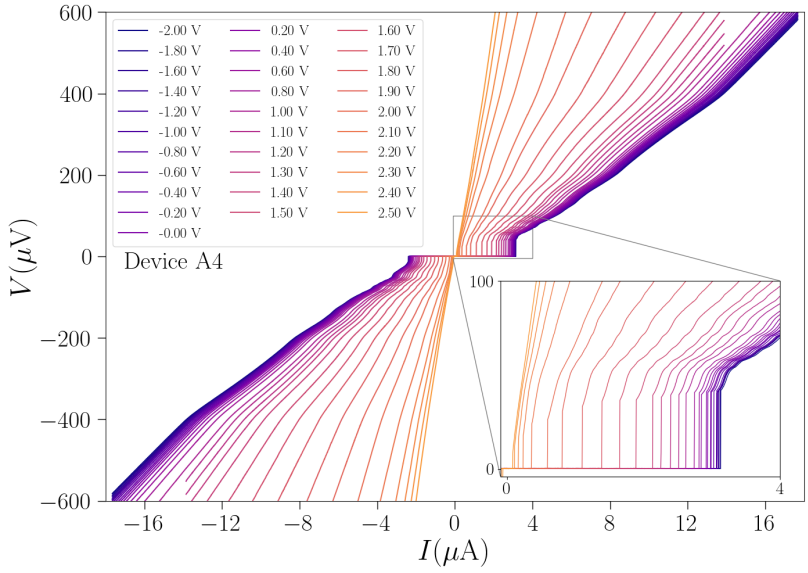

Figure B.4 – Current-voltage ($I - V$) characteristic of the device A4 at different gate voltages (V_g).

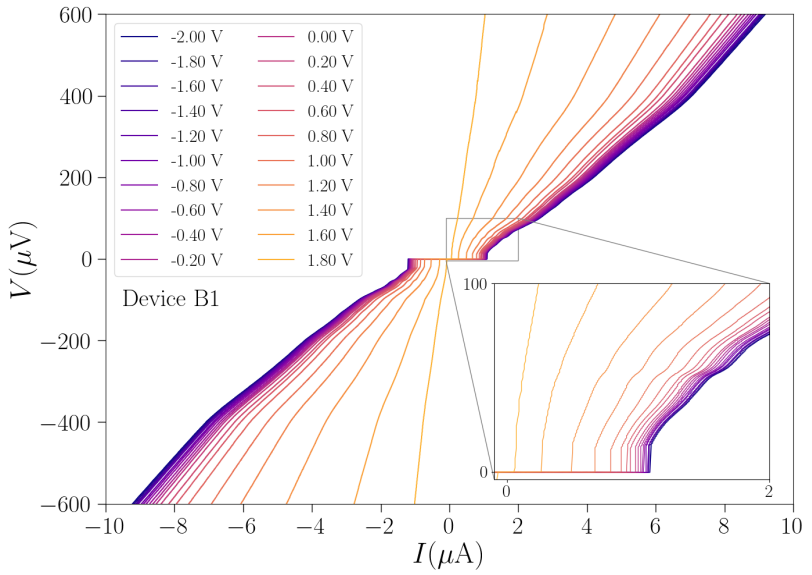

Figure B.5 – Current-voltage ($I - V$) characteristic of the device B1 at different gate voltages (V_g).

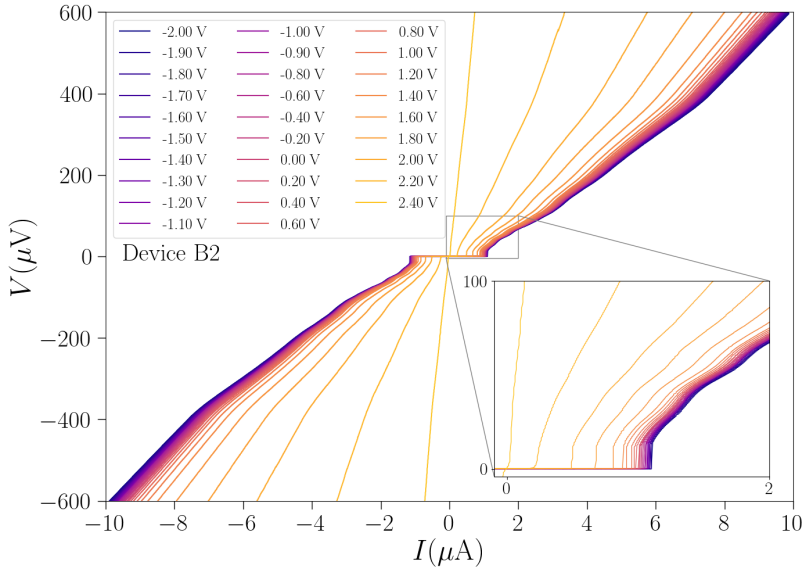

Figure B.6 – Current-voltage ($I - V$) characteristic of the device B2 at different gate voltages (V_g).

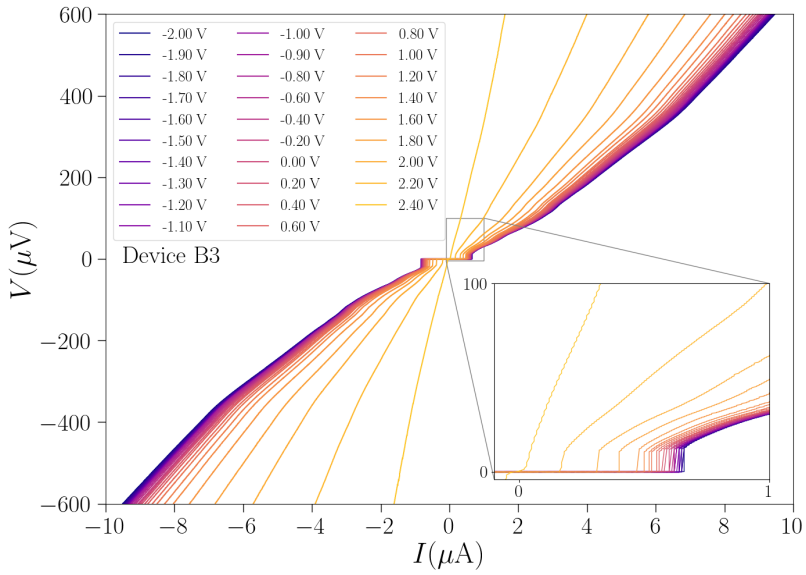

Figure B.7 – Current-voltage ($I - V$) characteristic of the device B3 at different gate voltages (V_g).

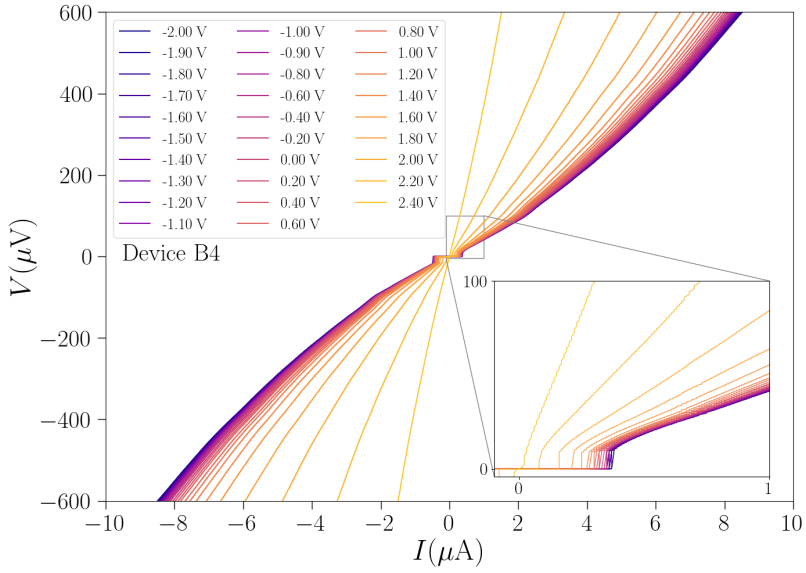

Figure B.8 – Current-voltage ($I - V$) characteristic of the device B4 at different gate voltages (V_g).

B.2 Differential resistance curves as a function of current at different temperatures

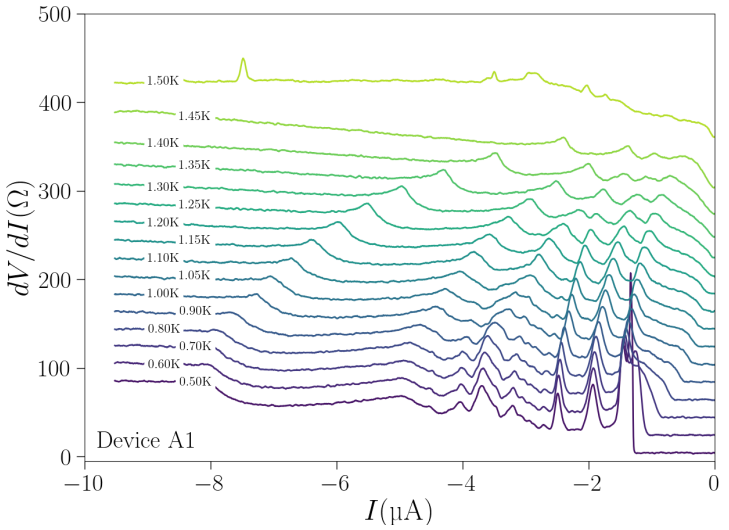

Figure B.9 – Differential resistance (dV/dI) of the device A1 as a function of the current (I) at different temperatures (T) at V_g= -2 V.

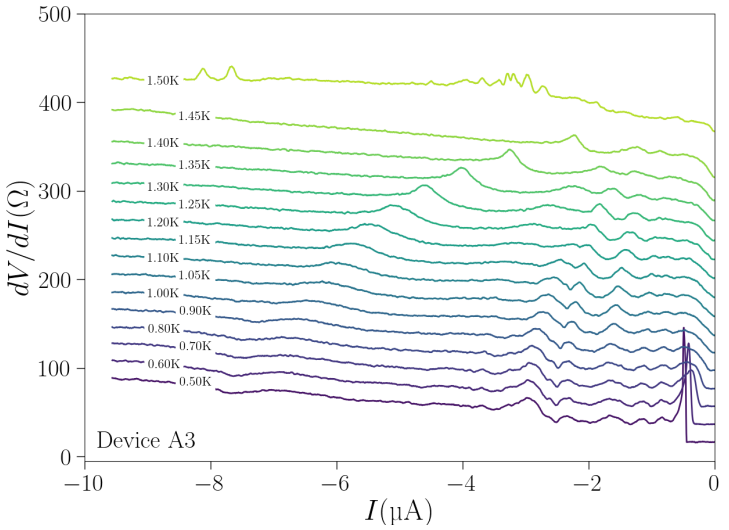

Figure B.10 – Differential resistance (dV/dI) of the device A3 as a function of the current (I) at different temperatures (T) at V_g= -2 V.

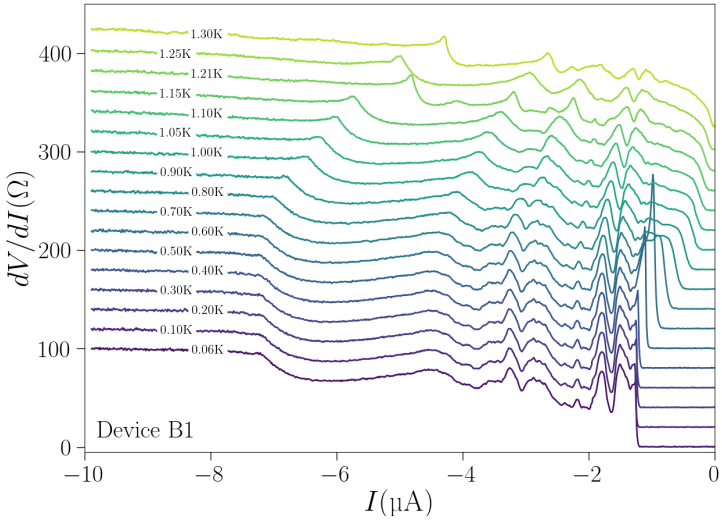

Figure B.11 – Differential resistance (dV/dI) of the device B1 as a function of the current (I) at different temperatures (T) at V_g= -2 V.

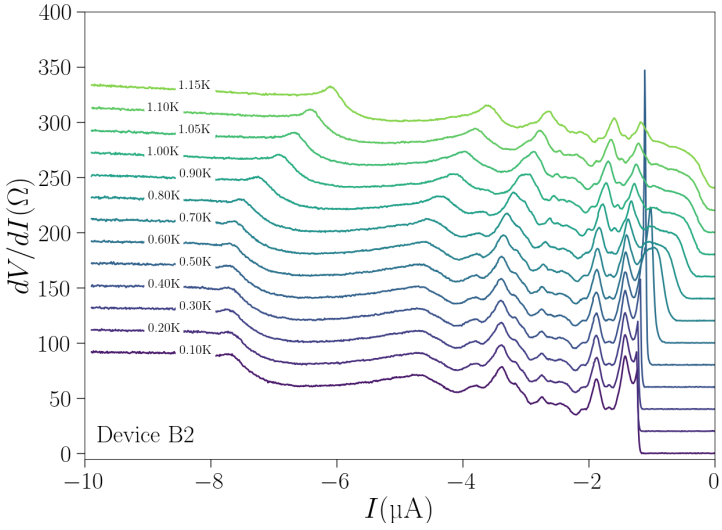

Figure B.12 – Differential resistance (dV/dI) of the device B2 as a function of the current (I) at different temperatures (T) at V_g= -2 V.

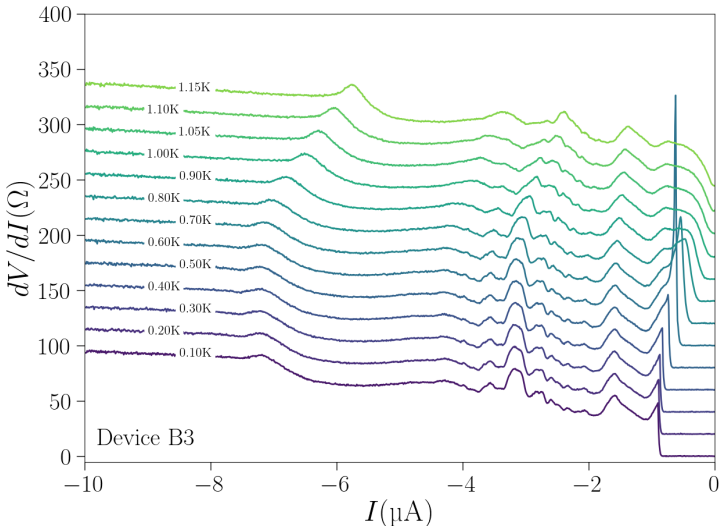

Figure B.13 – Differential resistance (dV/dI) of the device B3 as a function of the current (I) at different temperatures (T) at V_g= -2 V.

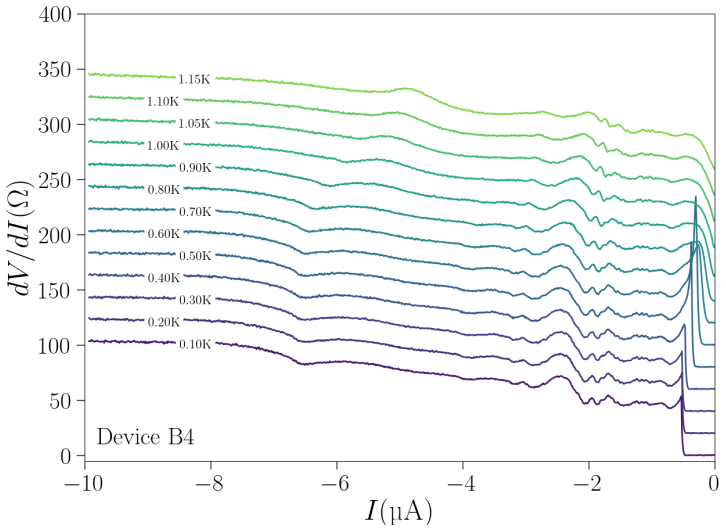

Figure B.14 – Differential resistance (dV/dI) of the device B4 as a function of the current (I) at different temperatures (T) at V_g= -2 V.

B.3 Current-voltage characteristics as a function of magnetic field

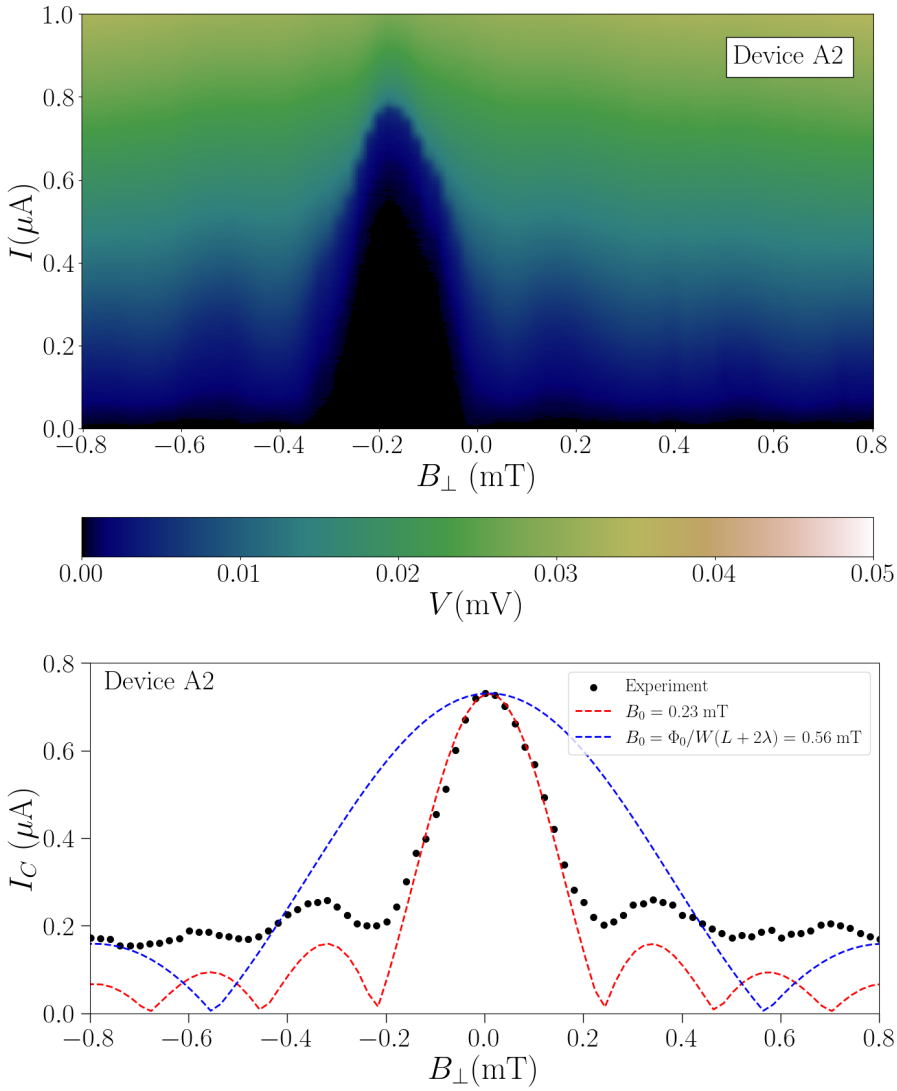

Figure B.15 – (upper) Voltage drop (V) across the device A2 as a function of the current (I) and the out-of-plane magnetic field ($B_\perp$). (lower) Critical current extracted from the colormap above. The Fraunhofer fitting with the extracted critical current is shown by the red dashed line. The period of the Fraunhofer from the fitting is found to be 0.23 mT, in comparison with $\Phi_0/W(L+2\lambda) = 0.56$ mT calculated from the junction parameters (blue dashed line).

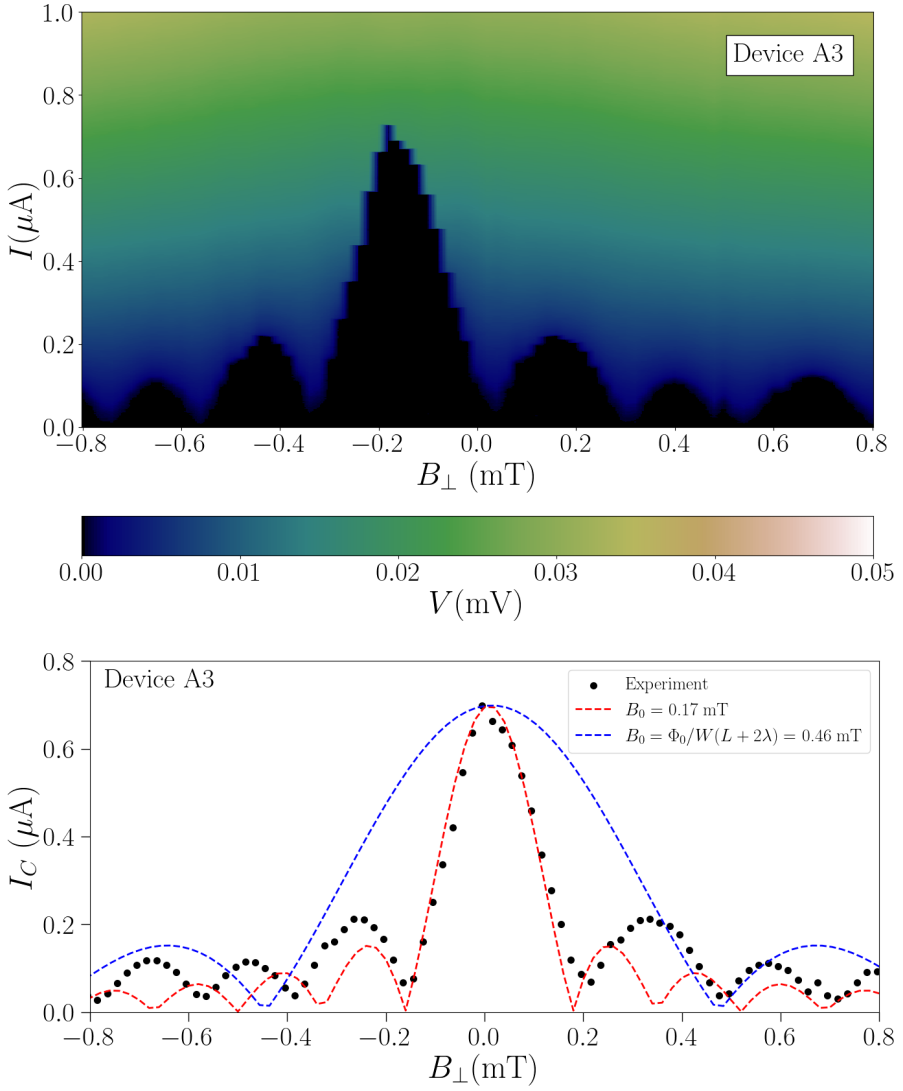

Figure B.16 – (upper) Voltage drop (V) across the device A3 as a function of the current (I) and the out-of-plane magnetic field ($B_\perp$). (lower) Critical current extracted from the colormap above. The Fraunhofer fitting with the extracted critical current is shown by the red dashed line. The period of the Fraunhofer from the fitting is found to be 0.17 mT, in comparison with $\Phi_0/W(L+2\lambda) = 0.46$ mT calculated from the junction parameters (blue dashed line).

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