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PRELIMINARY RESEARCH AND DEVELOPMENT OF BPM ELECTRONICS UPGRADE FOR THE RCS RING IN CSNS II*

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Abstract

The first phase of the China Spallation Neutron Source (CSNS) project aims to accelerate negative hydrogen ions to 80 MeV using a linear accelerator. Subsequently, these negative hydrogen ions are converted into protons after stripping, and then injected into a rapid cycling proton synchrotron. The proton beam is further accelerated to an energy of 1.6 GeV and guided through a beam transport line to a tungsten target, where spallation reactions generate neutrons. With the initiation of the Phase II project of the China Spallation Neutron Source (CSNS II), the target power is anticipated to increase significantly to 500 kW in the future. Upgrading the existing 32 sets of BPM electronics on the Rapid Cycling Synchrotron (RCS) ring is essential to accommodate the enhanced beam power and fulfill the new requirements of the beam measurement. This paper focuses on the novel design and validation of the BPM electronics, as well as the execution of tests during beam operation.

INTRODUCTION

The primary objective of the China Spallation Neutron Source (CSNS) project's first phase is to accelerate negative hydrogen ions to 80 MeV using a linear accelerator [1]. Subsequently, these negative hydrogen ions are converted into protons through stripping and then injected into a rapid cycling proton synchrotron [2]. The proton beam is further accelerated to 1.6 GeV and guided through a beam transport line to a tungsten target, where spallation reactions produce neutrons. With the initiation of the Phase II project of the China Spallation Neutron Source (CSNS II), the target power is anticipated to increase significantly to 500 kW in the future. Upgrading the existing 32 sets of BPM electronics on the Rapid Cycling Synchrotron (RCS) ring is necessary to accommodate the increased beam power and meet the new requirements of the beam tuning personnel.

ELECTRONICS SYSTEM DESIGN

System Architecture

In the Rapid Cycling Synchrotron (RCS) of the China Spallation Neutron Source (CSNS), there are four quadrants, each equipped with 8 BPM detectors. The dual-bunch revolution frequency ranges from 1 MHz to 2.44 MHz, with the bunch length compressed from 500 ns to 100 ns. Each bunch completes approximately 20,000 turns within an acceleration cycle of 20 ms. The signal dynamic range of the BPM is 10^4. The electronics system is divided into two parts. The Front-End Controller (FEC) readout boards handle digitizing the front-end signals, conducting real-time beam position calculations, and buffering raw ADC data and position data. The System-On-Chip

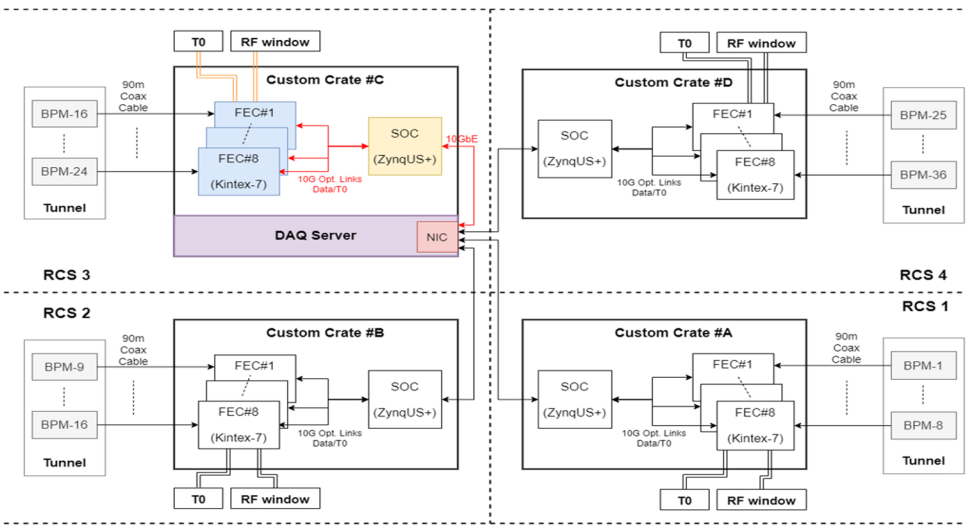

Figure 1: RCS-BPM system architecture diagram.

(SOC) data aggregation boards manage reading data from 8 FECs, with a front-end data bandwidth of 80 Gbps. They

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package the data, distribute it to the server, and configure the FECs. Each local station in a quadrant consists of 8 FEC boards and 1 SOC board. Illustrated in Figure 1 is the RCS-BPM system architecture diagram. This paper primarily focuses on the design and debugging of the front-end readout card (FEC).

Electronic Circuit Design

Through analysis of the 20 ms ADC RAW signal spectrum obtained from the BPM during the RCS injection to extraction process, as depicted in Figure 2, it was determined that designing the analog filter at 25 MHz effectively covers the main signals of interest. Table 1 compares several different parameters related to BPM electronics.

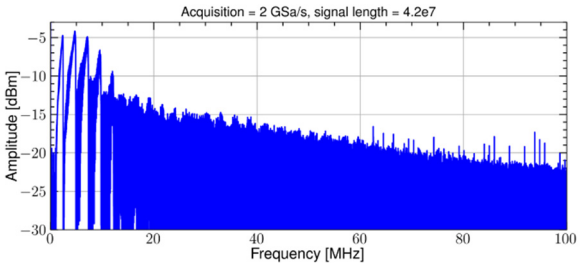

Figure 2: Frequency response diagram of 20 ms BPM electrode signal.

The front-end electronics employ transformer-coupled isolation to attenuate ground noise and utilize a 4-stage passive resistor divider for signal attenuation. The attenuation ratio is adjusted via analog switch switching, offering attenuation levels of 1, 0.25, 0.1, and 0.025. Subsequently, the signal undergoes amplification using a programmable amplifier.

Table 1: Comparison of Different BPM Electronics Parameters

Facility	Sampling rate MHz	Granularity bit	LPF MHz
Libera Hadron	250	16	55
HIAF	250	16	20/300
J-PARC	40	14	5
CSNS	250	14	25

Utilizing the Kintex7-325T FPGA platform, each node features 8 channels of digitizing ADCs with a sampling rate of 250 MHz and 14-bit resolution. The analog front-end provides 4 adjustable dynamic range settings and incorporates a 4 GB DDR3 memory. Output is transmitted through a 10 Gigabit optical interface, supporting a maximum throughput of up to 4 GB (connected to the data aggregation card). This system performs signal conditioning, ADC digitization, RAW ADC data buffering via DDR3 memory, real-time position calculations, and data transmission through network or optical interface. The hardware architecture is illustrated in Figure 3.

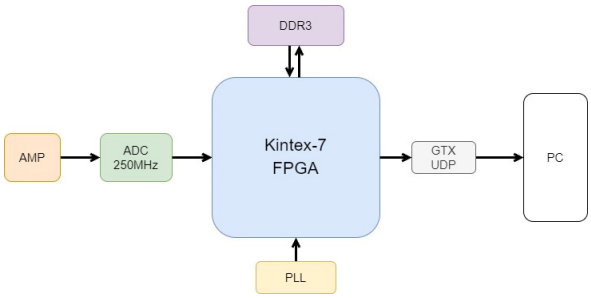

Figure 3: Diagram of BPM electronics.

FPGA Program Design

In the FPGA program design, various interface designs are implemented, including SPI interface design and configuration for programmable amplifiers, ADCs, PLLs, etc. Additionally, there is ADC data interface design for converting DDR LVDS to parallel data, DDR3 interface design based on the MIG core, and UDP network interface design. The framework of the FPGA program is illustrated in Figure 4.

During the debugging process of the program, physical location constraints are applied to registers, and IDELAYE2 primitives are utilized to adjust the delay of the input clock, enabling precise fine-tuning. This approach effectively addresses issues arising from mismatches between high-speed data and clock signals due to variations in path delays.

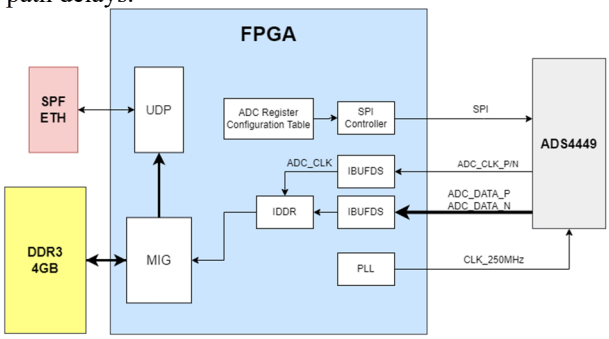

Figure 4: Diagram of the FPGA program framework.

The implementation of a DDR3 data buffering interface is crucial for ensuring the stable operation of DDR3 internal memory with a data bandwidth of 512 bits at 200 MHz, surpassing the data bandwidth of the ADC, which is 16 bits × 4 channels at 250 MHz. This configuration facilitates the electronic storage of 20 ms BPM RAW signals, as depicted in the block diagram presented in Figure 5.

Figure 5: Diagram of ADC's data to MIG.

In the process of single-board debugging, communication with the host computer is established using the UDP protocol through the SFP port. The host computer utilizes

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Python software to read the data transmitted by the FPGA and configure FPGA registers to facilitate communication between the host computer and FPGA. This setup achieves a data transfer bandwidth of approximately 800 Mbps, as illustrated in Figure 6.

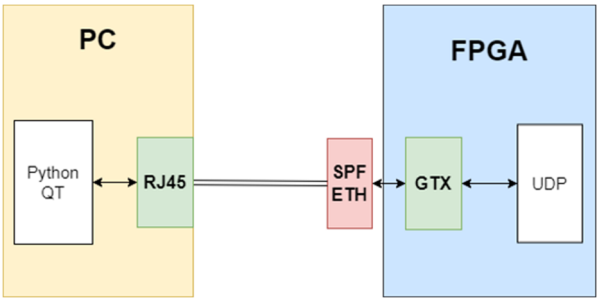

Figure 6: Diagram of UDP data transmission interface.

Position Signal Processing

The process of position signal processing includes correcting the ADC data, integrating the waveform within a defined window, and determining the position through the difference-over-sum method [3]. Equations (1) and (2) are employed for correcting the ADC channels, while Equations (3) and (4) are utilized for computing the difference and sum. Window integration of the difference and sum values from time (e) to (s) is performed using Equations (5) and (6). Finally, Equation (7) calculates the position signal by evaluating the ratio of the difference to the sum.

$$A' = K * A + b \quad (1)$$

$$C' = K * C + b \quad (2)$$

$$\Delta = A' - C' \quad (3)$$

$$\Delta = A' + C' \quad (4)$$

$$V_\Delta = \int_{W_s}^{W_e} \Delta \quad (5)$$

$$V_\Sigma = \int_{W_s}^{W_e} \Sigma \quad (6)$$

$$X = \frac{V_\Delta}{V_\Sigma} \quad (7)$$

TESTING AND EXPERIMENTATION

System Testing

The zero-input noise of the electronics was evaluated by short-circuiting the input and connecting a detector to measure the noise level in the absence of beam current. The zero-input noise of the electronics with the detector, in the absence of beam current, was found to be below 3 mV.

To assess the linearity and Integral Non-Linearity (INL) at various settings, a signal generator such as the KEYSIGHT 33500B was utilized to input a sine wave. The linearity and INL at different settings of the electronics are depicted in Figure 7. The results demonstrate excellent linearity across different settings. Furthermore, when subjected to a 2 MHz sine wave input, the Effective Number of Bits (ENOB) was determined to exceed 9.5, indicating high performance.

Beam-On Experiment

During the operational phase of the accelerator, experiments were performed utilizing the RF BPM in RCS. The electronics were employed to capture and store the 20 ms BPM signals for subsequent offline analysis. Furthermore, Libera electronics were utilized to store both the 20 ms data and Turn-By-Turn (TBT) data from the RF BPM for comparative analysis with the CSNS electronics. The data processing was conducted using Python, with the application of two thresholds to define the bunch window. Position calculations were executed on the ADC data obtained from both the self-developed electronics and the Libera electronics. Figure 8 illustrates the processed results of the 20 ms ADC data acquired by the self-developed electronics, while Figure 9 displays the processed outcomes of the 20 ms ADC data collected by the Libera electronics.

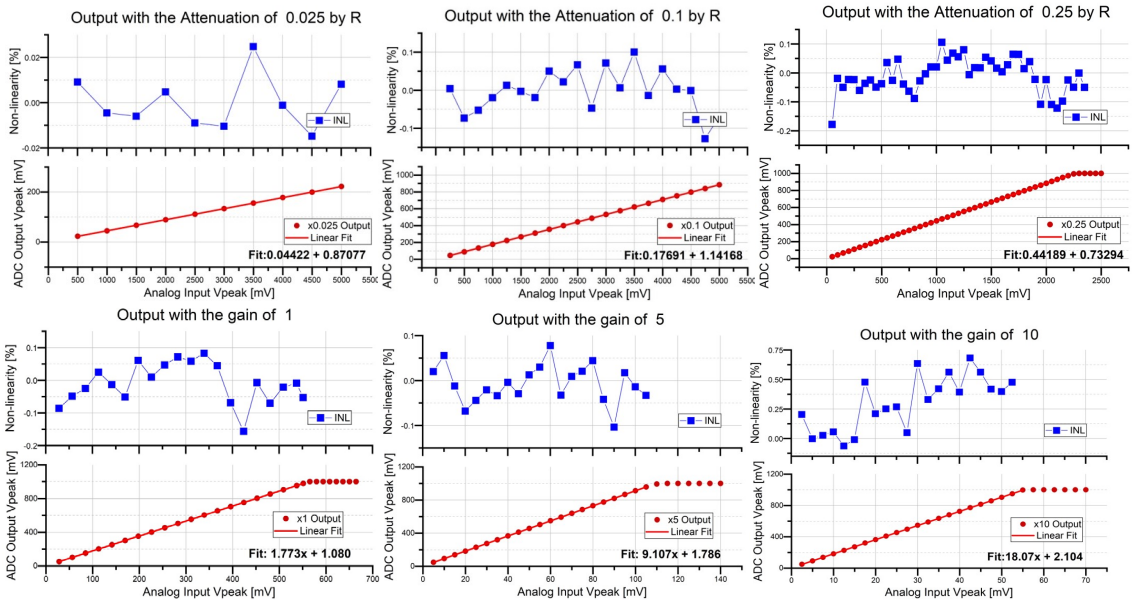

Figure 7: The figure showing the linearity and INL (Integral Non-Linearity) at different settings.

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Additionally, Figure 10 showcases the Turn-By-Turn (TBT) data obtained from the Libera electronics.

A comparative analysis of Figures 8 to 10 reveals that the results obtained through the offline dual-threshold algorithm applied to the Libera ADC RAW data align closely with the Libera TBT results. The bunch window determined by the offline dual-threshold algorithm proves to be effective, with the outcomes from the FEC electronics exhibiting a similar trend to those derived from the Libera ADC RAW data.

Moreover, an experiment was conducted utilizing an FPGA-based position algorithm to enable real-time calculation of position information and provision of Turn-By-Turn (TBT) data. This experiment was conducted on the TUNE BPM of the RCS, as depicted in Figure 11.

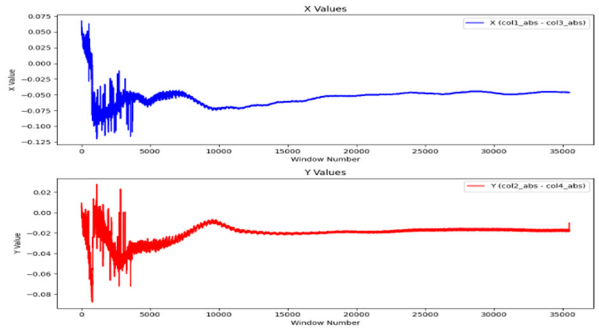

Figure 8: CSNS electronics ADC_RAW data was processed using a dual-threshold window algorithm.

CONCLUSIONS

To address the updated specifications for the RCS BPM system at CSNS II, a comprehensive redesign of the electronics architecture was undertaken, accompanied by the development of new hardware components. Extensive FPGA programming and testing were executed to attain a sampling rate of 250 MHz, facilitate storage of 20 ms ADC data, enable precise position signal calculations, and offer Turn-By-Turn (TBT) data functionality. Subsequent beam experiments were performed, yielding results that were in line with those obtained using the Libera electronics. The forthcoming phase will focus on refining the electronics board design and conducting additional comprehensive testing procedures.

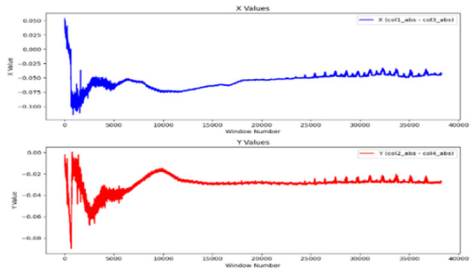

Figure 9: Libera electronics ADC_RAW data was processed using a dual-threshold window algorithm.

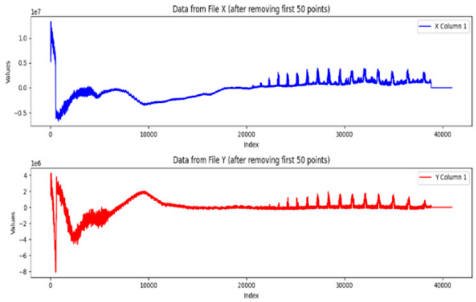

Figure 10: Libera electronics TBT Data with RF BPM.

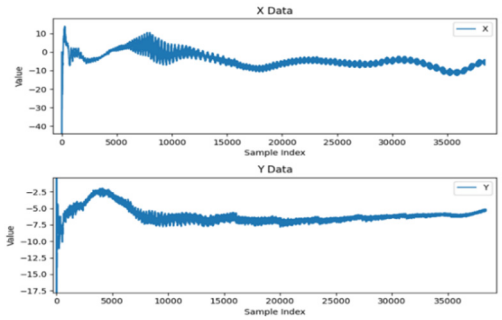

Figure 11: CSNS electronics TBT Data with TUNE BPM.

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