**LHCb Collaboration**

LHCb-MUON 2003-009
January 2003

# The CARIOCA Front End Chip for the LHCb muon chambers

**D. Moraes**[1], **W. Bonivento**[2], **N. Pelloux**[2], **W. Riegler**[2]

[1]LAPE-IF/UFRJ, CP 68528 Cidade Univ., BR-21945970 Rio de Janeiro, Brazil

[2]European Laboratory for Particle Physics (CERN), CH-1211 Genève 23, Switzerland

**Abstract**

The CARIOCA chip is an 8 channel Amplifier Shaper Discriminator chip for the LHCb muon system wire chambers, developed in IBM 0.25 $\mu$m CMOS technology. This note describes the specifications, overall functionality and building blocks of the chip.

# 1 Introduction

CARIOCA (**C**ERN **A**nd **RIO** **C**urrent-mode **A**mplifier) is an octal amplifier-shaper-discriminator circuit, with baseline restoration, dedicated to the Multi Wire Proportional Chambers (MWPC) of the LHCb Muon system [1]. It is developed in 0.25 $\mu$m CMOS technology, that operates at 2.5 volts. The CARIOCA amplifier is developed in the current-mode approach, that is attractive for fast circuits. The chip has to amplify, shape and discriminate the current signal induced on the wire chamber electrodes.

For the development of the chip, the circuit was divided into various sub-circuits, allowing the realization and test of the individual prototypes. In this paper we describe the circuit topology and design, together with some simulations. More details and results obtained with several prototypes are described in [2]- [6].

# 2 Overview and Specifications

The task of the wire chambers of the LHCb Muon System is to measure the arrival time of muons to better than 3 ns r.m.s. The chamber signal is characterized by a fast rising edge and a long $1/(t + 1.5\,\text{ns})$ tail, going over into a DC current lasting for about 20 $\mu$s . This signal has to be shaped to a unipolar narrow pulse in order to cope with the high rates expected in the experiment.

A detector gas gain of $10^5$ together with an amplifier peaking time of 10 to 15 ns is found to be the optimum working point for this detector. This results in an average pulse height of about 60 fC of charge, when referred to a delta input signal. To obtain a narrow pulse, a tail cancellation circuit has to be implemented which should correctly work for at least 99 % of chamber signals (up to 250 fC input charge), which sets the specification for the gain and linear range of the chip. In order to allow the desired threshold of 10 fC, the equivalent noise charge (ENC) at the input should not exceed 2 fC up to the largest detector capacitance of 250 pF. In addition, the amplifier input impedance should be less than 50 $\Omega$ to keep crosstalk low.

High rates of up to 800 kHz per channel in some detector regions require fast pulse shaping and baseline restoration circuits to compensate for baseline shifts and fluctuations. A total accumulated dose of 1 MRad during the life of the experiment requires radiation tolerant chip technology.

# 3 Topology and Architecture

The CARIOCA integrated circuit is developed in two versions: one for cathode readout (positive input polarity version) and another for anode readout (negative input polarity version). Each chip is composed of eight identical channels and a bias network, that provides the bias voltages and currents to the channels. The block diagram of a single CARIOCA channel is shown in Figure 1.

The input of the CARIOCA circuit is pseudo-differential, consisting of two identical current-mode amplifiers. One amplifier is connected to the chamber pad through a trace on the printed circuit board (PCB). The other, dummy amplifier, has a floating input and it is used to provide DC balance to the shaper and common mode rejection to pickup, crosstalk and noise on the power supply lines. Following the amplifier there is a shaper circuit and a differential amplifier which provide further gain together with signal and amplifier tail cancellation. The

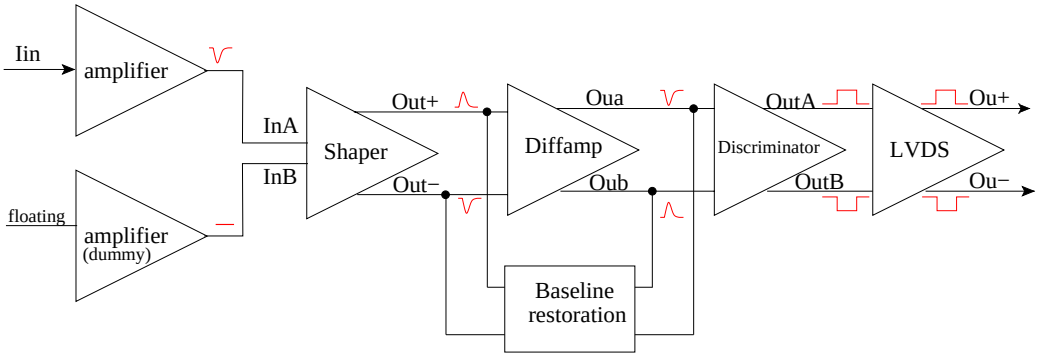


Figure 1: CARIOCA channel block diagram.

differential amplifier output is fed to the discriminator. The discriminator output is sent to the LVDS driver that provides the chip output signal.

A baseline restoration circuit, realized as a nonlinear feedback loop around the second differential amplifier, limits baseline fluctuations [7].

# 4 Current-mode Amplifier

The CARIOCA amplifier input stage is a cascode structure with a large input transistor, followed by a voltage to current converter and a current mirror. The input transistor ($N1$) is a $n$-channel with a length of 0.7 $\mu$m and width 1600 $\mu$m, giving to an input capacitance of 6 pF. This transistor operates in moderate inversion and has 42 mA/V transconductance (gm) at a drain current of about 3.2 mA. The folded transistor ($N2$) is chosen to have an open loop gain of about 30. The compensation capacitor ($C_{feed}$) of 406 fF is used to split the first two poles of the circuit and improve the stability. The designs of positive and negative polarity amplifiers, shown in Figure 2, are very similar and they have the same working principle. The main difference is the output stage current mirror ($N5/N6$). Since we want to have both amplifiers with the same output polarity, the current of the negative input polarity amplifier is inverted by an additional current mirror ($N7/N8$).

Current sources are realised with high impedance cascode transistors. A global bias circuit provides the required bias voltages for the circuit, setting the correct DC voltage level.

Figure 3 shows the simulated output voltage waveforms on the node between the amplifier and the shaper. The positive amplifier has a gain of 3.0 mV/fC while the negative one has a gain of 2.7 mV/fC at an input capacitance of 60 pF. Considering the MWPC pad capacitance range (50 pF to 250 pF) the sensitivity decays from 3.2 mV/fC (2.8 mV/fC) to 2.1 mV/fC (1.6 mV/fC) and the peaking time increases from 7 ns (7 ns) to 14 ns (15 ns) for the positive (negative) input polarity amplifier.

The CARIOCA amplifier has a bandwidth of 22 MHz and 15 MHz for the positive and negative polarity amplifiers, respectively. Both amplifiers show a small signal gain around 30 dB. The input impedance is smaller than 50 $\Omega$ for both amplifiers as shown in Figure 4.

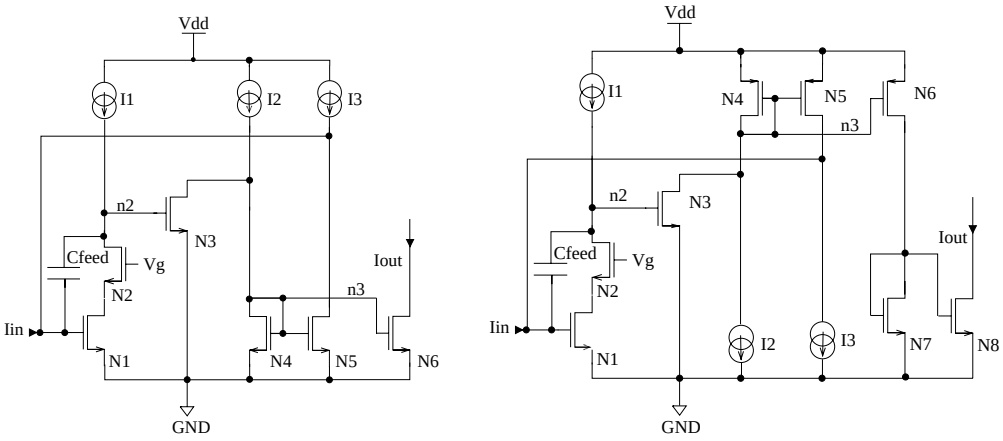


Figure 2: Simplified schematic of the CARIOCA amplifier for positive (a) and negative (b) input polarity.

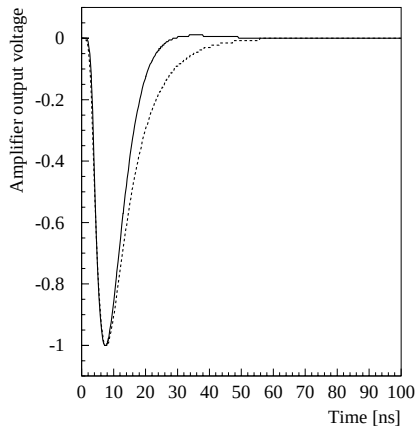


Figure 3: Normalized output voltage of the positive (full line) and negative (dashed line) input polarity amplifiers for a delta input charge of 60 fC at 60 pF input capacitance.

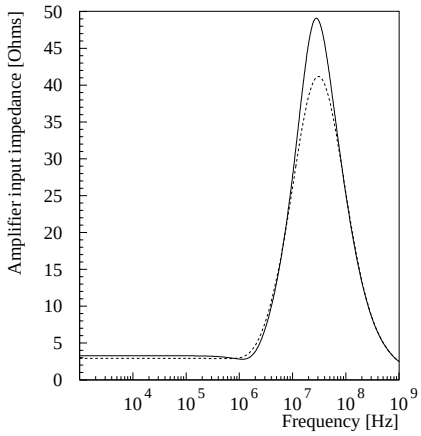


Figure 4: Input impedance of the positive (full line) negative (dashed line) input polarity amplifiers.

## 4.1 Open Loop Analysis

One important issue of this circuit is to investigate the stability of the amplifier with its feedback. The stability study is done by breaking the circuit feedback and analysing the dependence of the poles and phase margin on circuit parameters.

CARIOCA is a transimpedance amplifier and for small signal analysis it can be modeled as a three pole system. The dominant pole is located on the input node. Due to Miller effect, the shunt resistance at this node ($R_{in}$) is dominated by the transconductance of $N5$ ($gm_5$) and can be written as:

$$R_{in} = \frac{1}{A * gm_5} \, , \tag{1}$$

where $A$ is the amplifier open loop gain. The shunt capacitance on the input node ($C_{in}$) is determined by the detector capacitance in parallel with the compensation capacitor ($C_{feed}$), as seen at the input (Miller effect) and the gate capacitance of $N1$, which is negligible. This shunt capacitance can is given by

$$C_{in} = C_{det} + C_{feed}(1 + gm_1 * Rl_2) \, , \tag{2}$$

where $Rl_2$ is the resistance load of the first stage, and it is dominated by the Miller effect, even when the detector capacitance ($C_{det}$) varies from 50 pF up to 220 pF, which makes the amplifier less sensitive to $C_{det}$ spread.

The dominant pole is located at about 10 Hz and 0.1 Hz for the negative and the positive version, respectively. The non dominant pole is on node $N2$, where the shunt resistance is equal to the resistive load of the first stage ($Rl_2$). The shunt capacitance on this node is the compensation capacitance in parallel to the gate capacitance of $N3$. The corresponding pole frequency is at about 10 MHz for both polarities. The third pole is situated at node $N3$. This pole is rejected to a high frequency of about few GHz because it has small shunt resistance and capacitance.

In order to calculate the open loop gain and to study the phase margin, we use the Cadence schematic. The schematic does not take into account wire capacitances present in the circuit

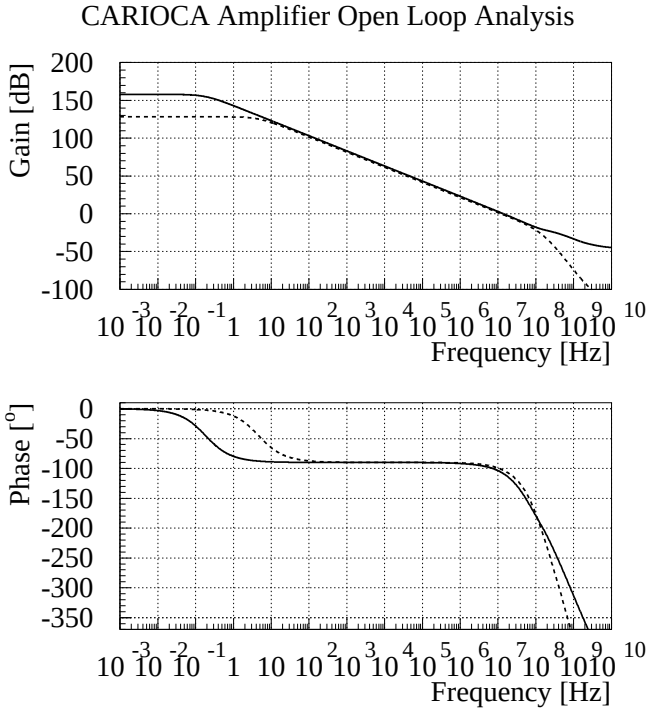


Figure 5: Positive (full line) and negative (dashed line) input polarity amplifiers open loop response gain (a) and phase (b) Bode plots.

layout, which can be neglected compared to the transistor capacitance. Figure 5 shows the Bode diagram for the positive and and negative input polarity amplifiers. Both amplifiers version have a good phase margin that decayes from 79 ° (72 °) to 59 ° (50 °) for the negative (positive) input polarity version, for a detector capacitance from 50 pF to 220 pF.

# 5 Shaper

The CARIOCA shaper is a one stage pole/zero filter with 2 poles and 2 zeros. The input stage is a current-to-voltage converter shown in Figure 6. The output current from the amplifiers ($I_{amp}$ and $I_{dummy}$) are converted into voltage ($V_{inA}$ and $V_{inB}$) by a 5 k$\Omega$ resistor and these voltages are sent to the shaper inputs. A simplified schematic of the shaper circuit is shown in Figure 7. It consists of a differential amplifier in a folded cascode configuration with common-mode feedback. The DC output voltage is set by the common-mode voltage ($V_{CM}$) via 5 k$\Omega$ resistors. The common-mode voltage is chosen to be 1.27 V to explore the maximum dynamic range of the signals.

The tail cancellation is performed by a double pole-zero compensation network [8, 9] composed by $R_1$, $R_2$, $R_3$, $C_1$ and $C_2$. The pole/zero network transfer function is given by:

$$H(s) = \frac{s + 1/\tau_1}{s + 1/\tau_2} \cdot \frac{s + 1/\tau_3}{s + 1/\tau_4} \tag{3}$$

where $\tau_1$=9 ns, $\tau_2$=2.6 ns, $\tau_3$=80 ns and $\tau_4$=40 ns.

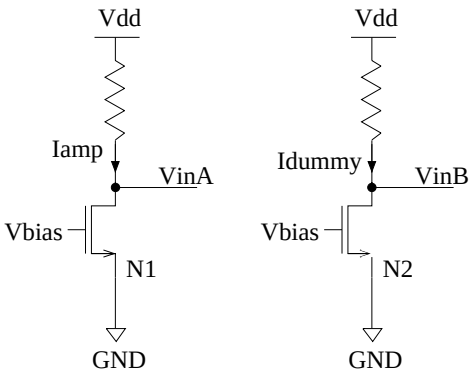


Figure 6: Current to voltage converter at the input of the shaper circuit. $I_{amp}$ and $I_{dummy}$ are the currents that come from the amplifiers and $V_{inA}$ and $V_{inB}$ are the voltages sensed by the shaper input transistors $N3$ and $N4$, respectively.

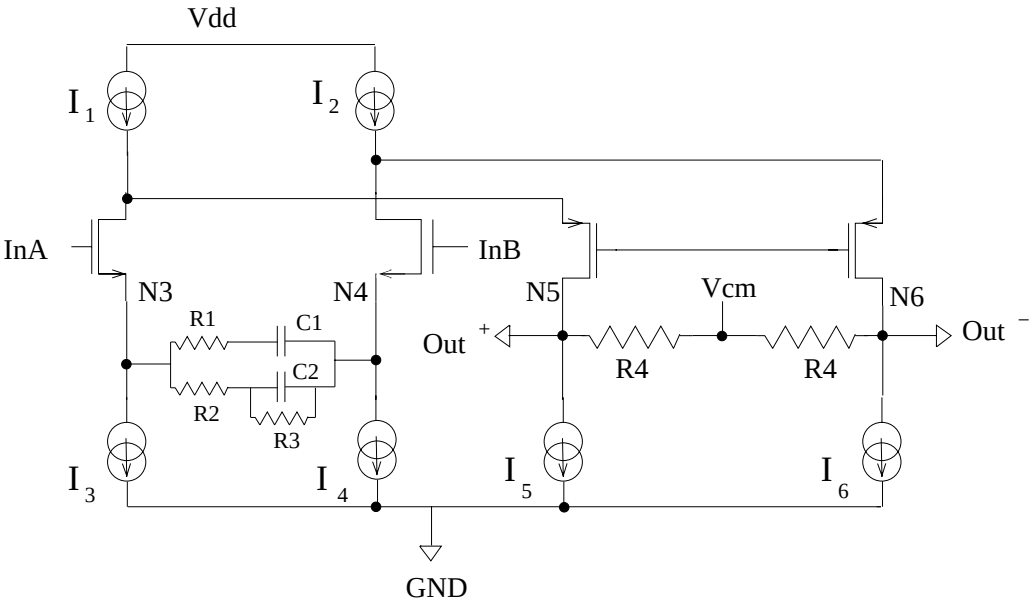


Figure 7: Simplified schematic of the shaper circuit.

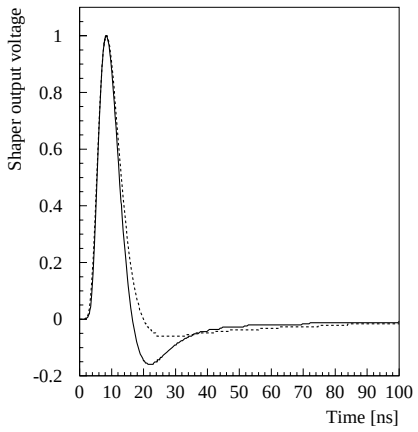


Figure 8: Normalised positive (full line) and negative (dashed line) amplifier and shaper differential output voltage, for a delta input charge of 60 fC and 60 pF input capacitance.

Figure 8 shows the shaper output for positive and negative input polarity amplifiers with delta input charge of 60 fC. The shaper gain is about 4.0 mV/fC and 3.6 mV/fC for the positive and negative polarity amplifiers, respectively.

The shaper circuit is designed with a speed such that the amplifier peaking time is not significantly degraded. The contribution to the peaking time is about 1 ns. Therefore the dominant high frequency pole is located at about 140 MHz. The shaper voltage gain peaks at about -37 dB in the range of 6 to 23 MHz.

# 6 Differential Amplifier

The differential amplifier follows the basic design shown in Figure 9 [10]. It serves as gain and shaping amplifier. The gain is set by the load impedance $Z$ and the source impedance $Y$. The source impedance is a combination of resistors and capacitances, making a pole/zero structure to cancel the time constant of the amplifier output. Since the positive and negative input polarity amplifiers have a different tail, two different pole/zero structures are chosen, i. e., the value of $Y$ differs from positive to negative input polarity version.

The DC output voltage of the differential amplifier is established by common mode feedback. The output nodes are connected to the gates of $N_5/N_6$ and $N_9/N_{10}$, that operate in their linear region as resistors, with 100 mV across $N_5/N_6$ and 62 mV across $N_9/N_{10}$. Common mode gain is achieved by modulating the field effect transistor (FET) resistances via common mode output voltage. Common mode feedback drives the common mode output voltage to the reference voltage $Vcm$. This reference voltage is common to the differential amplifier and the baseline restoration circuit and is set to 1.5 V. The bias current ($I_{bias}$) is set by a bias network. The drain currents of the input pair $N_1/N_2$ is set by the mirrors $N_{14}$ and $N_{17}$ and it is a factor four higher than the bias current.

The differential amplifier transfer function can be written as:

$$H(s) = \frac{s + 1/\tau_1}{s + 1/\tau_2} \, , \tag{4}$$

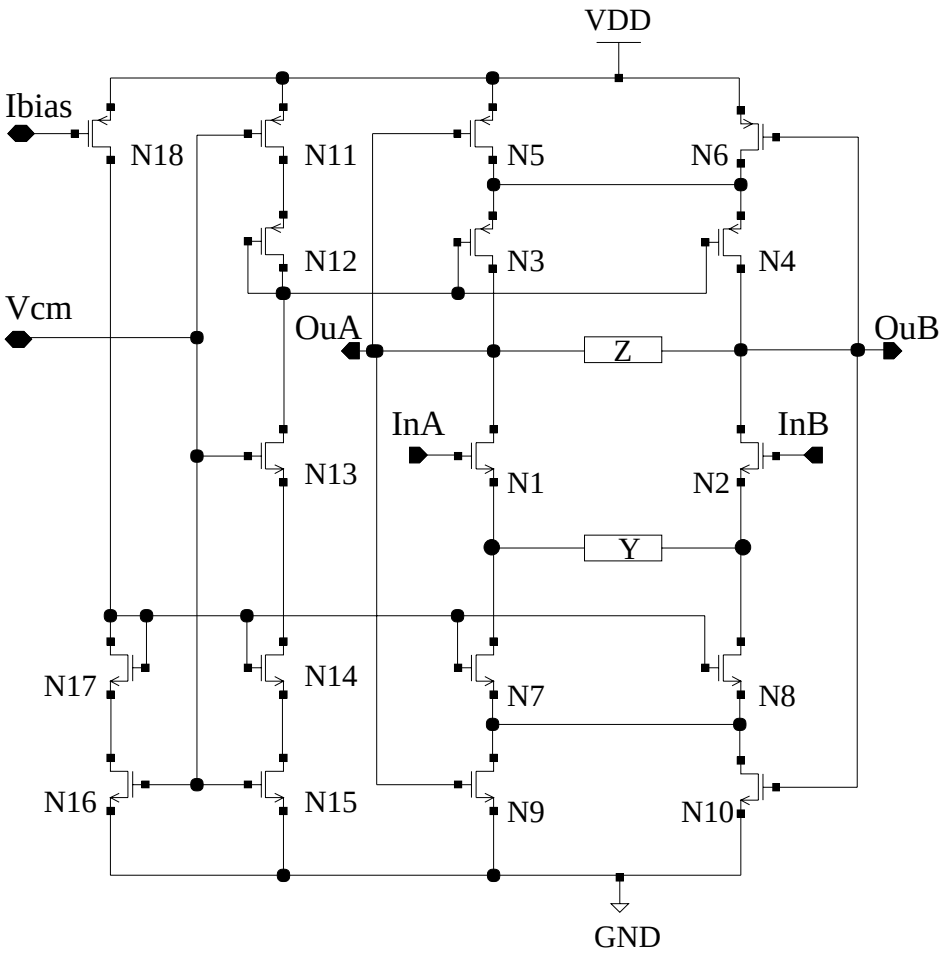


Figure 9: Differential amplifier schematic.

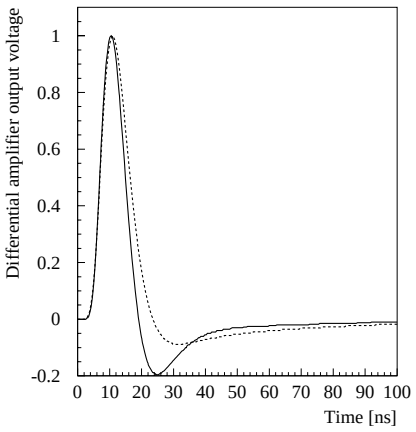


Figure 10: Positive (full line) and negative (dashed line) polarity amplifiers, shaper and differential amplifier normalised output voltage, considering a delta input charge of 60 fC and 60 pF input capacitance.

where $\tau_1$=6.3 ns (10 ns) and $\tau_2$=3.2 ns (3.9 ns) for the positive (negative) input polarity amplifiers.

Figure 10 shows the differential amplifier output at 60 pF input capacitance for positive and negative input polarity with a delta input charge 60 fC. The differential amplifier shows a linear voltage gain of 1.6 (6.3 mV/fC) and 2.0 (7.4 mV/fC) for the positive and negative input polarity, respectively, over the expected signal range.

The equivalent frequency spectrum of differential amplifier shows a gain of approximately -32 dB (-28 dB) for the positive (negative) input polarity amplifier, in the range of 6 to 24 MHz with a -3 dB bandwidth of about 145 MHz.

# 7 Baseline Restoration Circuit

An active baseline restoration (BLR) is implemented in the CARIOCA chip. This circuit, shown in Figure 11, consists of three amplifiers with the same structure of the one in Figure 9. The only difference is that the bias current mirror has a gain 1, which makes the input pair drain current equal to the bias current. The standing current in the first and third amplifiers ($BLR1$ and $BLR3$) is set by a polysilicon resistor $R$ referred to the power supply, and not by $I_{bias}$. This current it is not fixed on the second amplifier ($BLR2$) because it has influence on the circuit time constant, as described below.

The BLR1 stage samples the differential amplifier output voltage and feeds the BLR2 stage with the current $I_1 = gm_1 V_{out}$. The BLR2 stage integrates the current giving the output voltage $V_2 = 1/sCI_1$. The BLR3 stage produces the output current $I_3 = gm_3 V_2$ which results in the voltage $\Delta V = RI_3$ where $R$ is the resistor on the shaper output. Using all these relations and assuming the gain $A$ of the differential amplifier, the voltages $V_{in}$ and $V_{out}$ are related by

$$V_{out} = V_{in} - \Delta V \qquad \rightarrow \qquad V_{out} = \frac{A}{1 + \frac{1}{s\tau}} V_{in} \qquad \tau = \frac{C}{ARgm_1 gm_3} \tag{5}$$

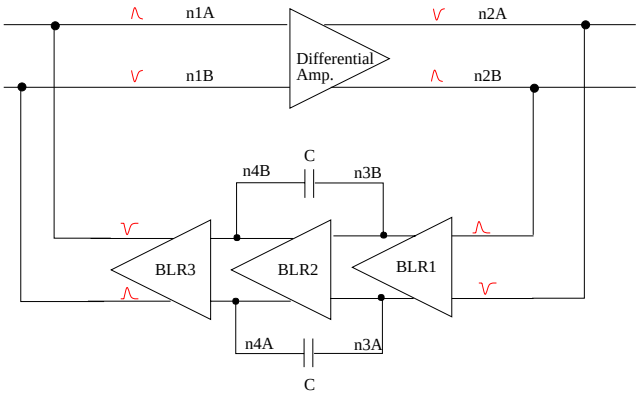


Figure 11: Schematic of the baseline restoration circuit.

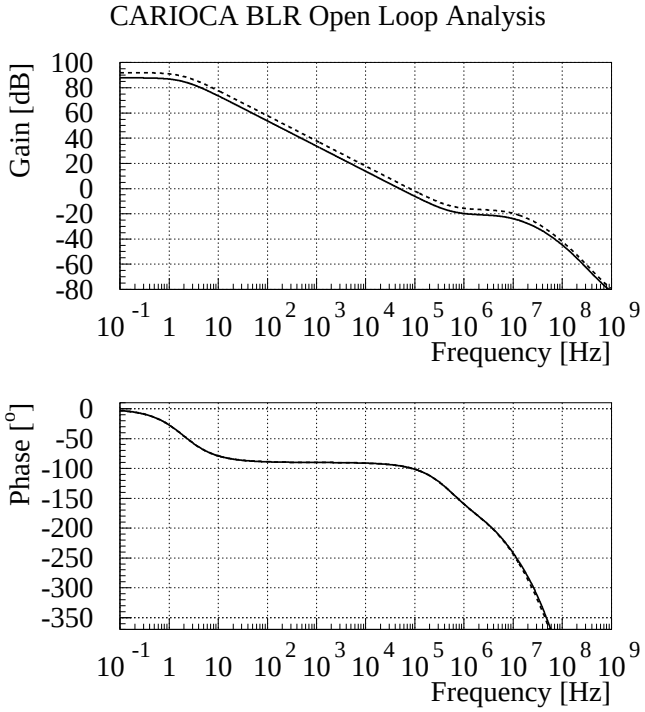


Figure 12: Baseline restoration open loop response - gain (a) and phase (b) Bode plots- for positive (full line) and negative (dashed line) input polarity amplifiers.

This transfer function is equal to a simple $RC$ differentiating element and if all the stages would be linear in the entire signal range the BLR would just differentiate the signal resulting in a bipolar signal shape. The essential feature of the BLR is that the first stage is nonlinear i.e. the signal is clipped at a design value of 50 mV. Therefore only small signals enter the feedback which provides the desired baseline restoration.

## 7.1 Open Loop Analysis

The Base Line Restoration block is introducing a feedback loop in the circuit. As for the amplifier, one should verify if the BLR loop is not introducing any instability in the channel. We first locate the poles position, then the phase margin, obtained by plotting the Bode Diagram of the open loop gain, gives us a clear idea of the system stability. The BLR loop consists of 3 blocks, as shown in Figure 11. All three blocks use the same structure with almost the same transistors size and same bias. For each node the shunt resistance is thus in the same range of magnitude. The shunt capacitances seen at each node will determine the pole positions.

Due to Miller effect, the shunt capacitance on node $n3A$ and $n3B$ is dominated by the feedback capacitance of the BLR2. The pole corresponding these nodes is shifted to low frequency and becomes the dominant pole. The corresponding frequency is around 2 Hz. The non dominant pole is on node $n4A$ and $n4B$ at about 500 KHz.

The other poles, corresponding to nodes $n1A$, $n1B$, $n2A$ and $n2B$ have almost the same frequency which is about few MHz. For the negative version, the phase margin is 81° while for the positive version, the phase margin is 84°, as shown in Figure 12.

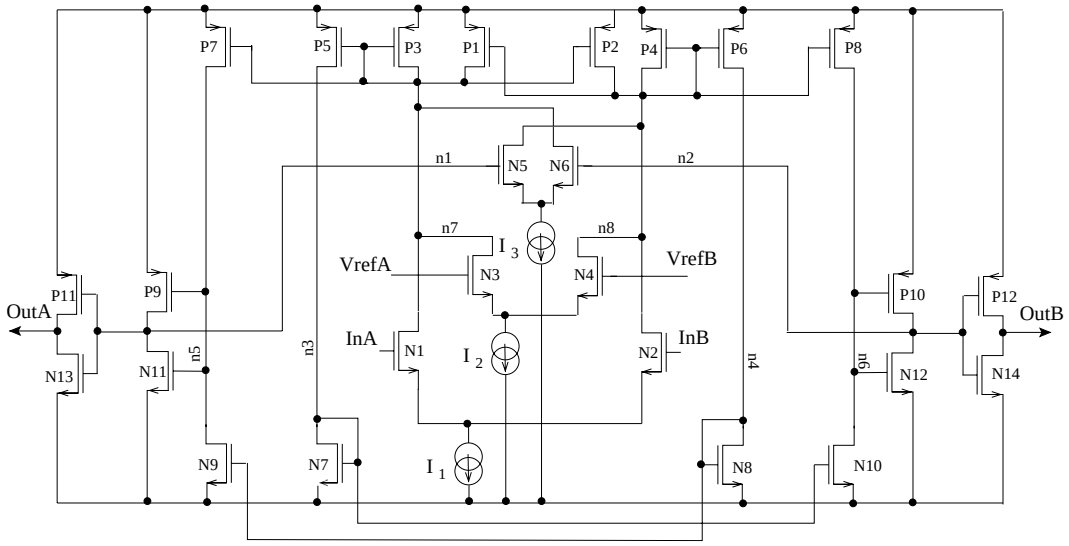


Figure 13: Discriminator circuit schematic.

# 8 Discriminator

The discriminator, whose design is based on an existing circuit [10], is a high-gain differential amplifier with symmetric current-mirror loads. Figure 13 shows the schematic. The threshold voltage is set in a differential way on the nodes $VrefA$ and $VrefB$ and these voltages unbalance the current through the main differential pair. The amount of hysteresis is programmable by means of a current source ($I_3$), which shifts the effective discriminator threshold. The bias currents $I_1$, $I_2$ and $I_3$ are supplied from an external input through current mirrors.

Figure 14 shows the discriminator output voltage for the positive and the negative input polarity circuits with 60 fC input charge and 60 pF input capacitance, considering a threshold of 10 fC. The discriminator gain peaks at -84 dB in the range from 7 to 13 MHz.

# 9 LVDS Driver Properties

The LVDS driver provides an LVDS-like low-level logic output, with nominal swing of 160 mV centred at 1.2 V with 100 $\Omega$ termination resistor, corresponding to the reduced range link described in [11]. This cell consists of a single to differential converter, a main LVDS driver stage and a bias network, shown in Figure 15.

# 10 Input Test Pulse

Each channel is provided with an internal pulse injector. For the negative version, the pulse injector consists of a single inverter stage as input followed by a 50 fF serial capacitor. While for the positive version, two inverters in serie are followed by a 50 fF serial capacitance, as shown in Figure 16.

A voltage step from 0 to 2.5 Volts, called INPUT_TEST, fires the inverter stage. The output swing magnitude of the inverter stage is controled by the DC voltage TEST_LEVEL. The input

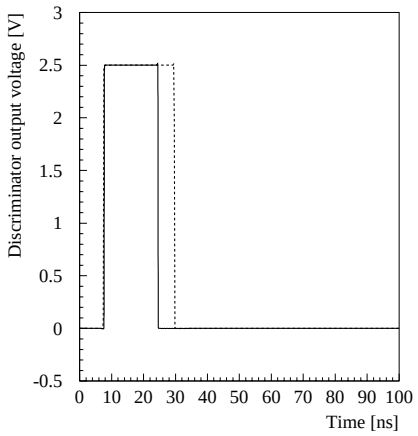


Figure 14: Positive (full line) and negative (dashed line) polarity amplifiers, shaper, differential amplifier and discriminator output voltage for a delta input of 60 fC, 60 pF input capacitance and 10 fC threshold.

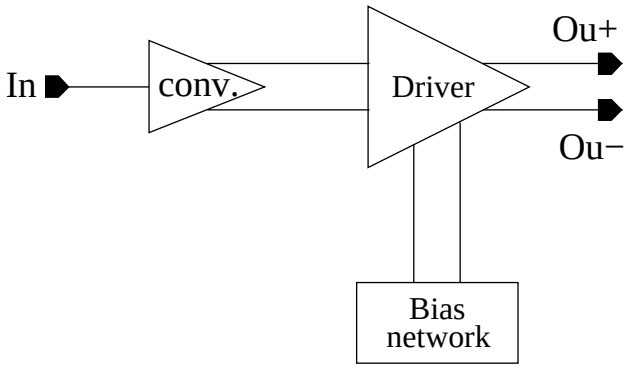


Figure 15: Block diagram of the LVDS driver.

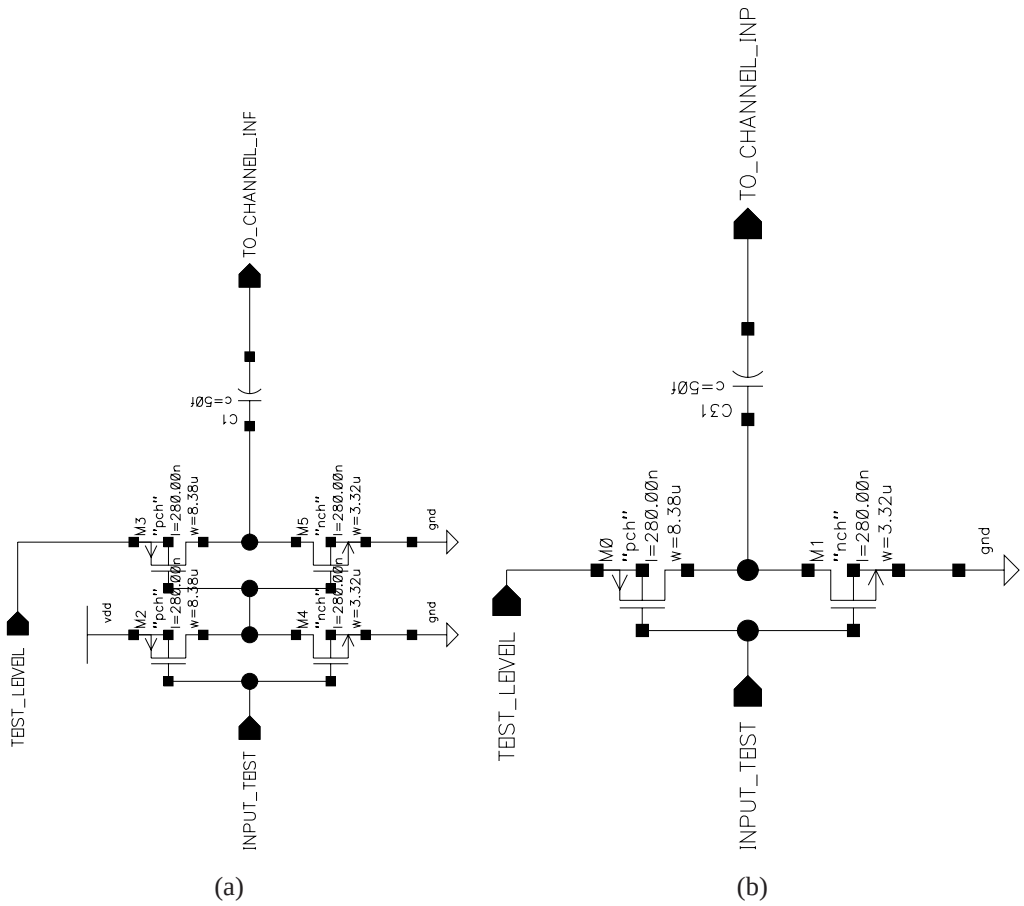


Figure 16: Input test pulse block diagram.

charge is given by:

$$Q_{in} = C_{inj} * V_{TEST\_LEVEL} \, . \tag{6}$$

The pulse injector can inject a charge from 50 fC to 125 fC. This minimum charge is defined by the DC voltage TEST_LEVEL, that cannot be smaller than 1 V, otherwise the inverter does not work properly.

# 11 Input/Output Pad Protection

The analog I/O pads use a dedicated electrostatic discharge (esd) protection circuit (Figure 17) to protect against discharges due to handling of the chip. To protect the CARIOCA chip from high voltage discharges in the chamber, and external protection circuit is required.

# 12 Acknowledgements

We acknowledge in particular the support of CNPq, FUJB, FAPERJ and the European Commission (contract CT1*-CT94-0118).

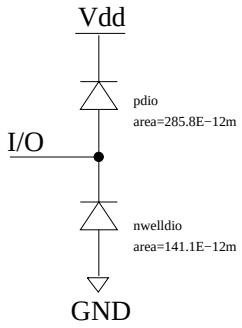


Figure 17: Analog input/output pad protection schematic.

# References

[1] LHCb Collaboration, LHCb Muon System: Technical Design Report, CERN-LHCC-2001-010, LHCb-TDR-4 (2001).

[2] D. Moraes, Spontaneous R parity violation measurement at DELPHI and CARIOCA : a new front-end electronic for the LHCb muon detector / Moreas, D. , 11 Apr 2002 . - 230 p . - CERN-THESIS-2002-021

[3] D. Moraes, W. Bonivento, P. Jarron, W. Riegler, F. dos Santos, Development of the CARIOCA front-end chip for the LHCb muon detector, NIM A 491(2002)233-243.

[4] D. Moraes, W. Bonivento, P. Jarron, W. Riegler, F. dos Santos, "Status of the CARIOCA Project", in *Proceedings of the VII Workshop on Electronics for LHC Experiments* (Stockholm, Sweden, 2001) CERN 2001-005, CERN/LHCC/2001-034.

[5] D. Moraes, F. Anghinolfi, P. Deval, P. Jarron, W. Riegler, A. Rivetti, B. Schmidt, 2001 IEEE International Conference on Circuits and Systems, Volume I, 360-363.

[6] D. Moraes, F. Anghinolfi, P. Deval, P. Jarron, W. Riegler, A. Rivetti, B. Schmidt, "CARIOCA - A Fast Binary Front-End Implemented in 0.25um CMOS using a Novel Current-Mode Technique for the LHCb Muon detector", in *Proceedings of the VI Workshop on Electronics for LHC Experiments* (Cracow, Poland, 2000) CERN-2000-010, CERN/LHCC/2000-041.

[7] John Oliver, private communication, Harvard University High Energy Physics Lab.

[8] R.A.Boie *et al.*, Signal shaping and tail cancellation for gas proportional detectors at high counting rates, NIM A 192 (1982) 365.

[9] M. Newcomer *et al.*, Progress in development of the ASDBLR ASIC for the ATLAS TRT, in *Proceedings of the V Workshop on Electronics for LHC Experiments* (Colorado, USA, 1999) CERN/LHCC/99-33.

[10] C. Posch *et al.*, CMOS front-end for the MDT sub-detector in the ATLAS Muon Spectrometer, development and performance, in *Proceedings of the VII Workshop on Electronics for LHC Experiments* (Stockholm, Sweden, 2001) CERN 2001-005, CERN/LHCC/2001-034.

[11] Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI), IEEE P1596.3-1995, IEEE Standard Document (1995).