

## ARTICLE

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# Solid-state qubits integrated with superconducting through-silicon vias

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As superconducting qubit circuits become more complex, addressing a large array of qubits becomes a challenging engineering problem. Dense arrays of qubits benefit from, and may require, access via the third dimension to alleviate interconnect crowding. Through-silicon vias (TSVs) represent a promising approach to three-dimensional (3D) integration in superconducting qubit arrays—provided they are compact enough to support densely-packed qubit systems without compromising qubit performance or low-loss signal and control routing. In this work, we demonstrate the integration of superconducting, high-aspect ratio TSVs—10 μm wide by 20 μm long by 200 μm deep—with superconducting qubits. We utilize TSVs for baseband control and high-fidelity microwave readout of qubits using a two-chip, bump-bonded architecture. We also validate the fabrication of qubits directly upon the surface of a TSV-integrated chip. These key 3D-integration milestones pave the way for the control and readout of high-density superconducting qubit arrays using superconducting TSVs.

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## INTRODUCTION

Superconducting qubits are lithographically defined electrical circuits comprising Josephson junctions, inductors, capacitors, and interconnects that are engineered to behave as well-isolated quantum-mechanical two-level systems<sup>1–3</sup>. Superconducting qubits use materials such as aluminum (Al), titanium nitride (TiN), and niobium (Nb) and substrates such as silicon (Si) and sapphire (Al<sub>2</sub>O<sub>3</sub>) that are compatible with—and strongly leverage—CMOS manufacturing toolsets and approaches<sup>4</sup>. Their lithographic scalability, compatibility with microwave control, and operability at the nanosecond timescale have all converged to place superconducting qubits at the forefront of nascent quantum processor development. Current state-of-the-art superconducting circuits feature single-qubit gate fidelities exceeding 99.9% and two-qubit gate fidelities exceeding 99%<sup>5</sup>.

To date, most multi-qubit demonstrations on superconducting qubit processors have been performed in a planar architecture: qubits and interconnects have been co-fabricated on a single-chip surface, with control and readout wiring brought in laterally from the edges of the chip<sup>6–8</sup>. While this approach can potentially support tens of qubits, interconnect crowding precludes lateral interconnection as circuits become larger.

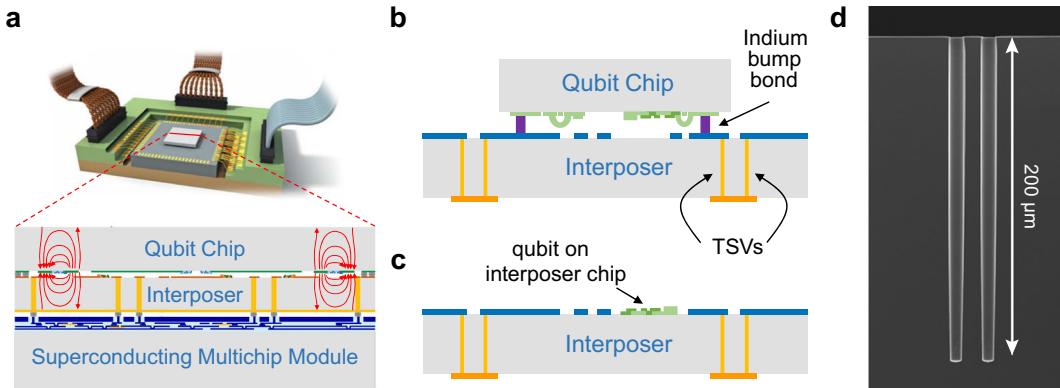
Addressing the interior elements of a large two-dimensional (2D) array requires moving out of a planar geometry to route wires past the outer elements of the array. In the short- and medium-term, accessing the interior of a qubit array can be achieved with a single extra metallization layer (i.e., air bridges and standard flip-chip bonding) or by a single layer of vertical I/O (i.e., pin-chips, pogo pins, and similar technologies)<sup>9–16</sup>. However, larger and more complex quantum system architectures may need to utilize multiple levels of qubits and complex signal routing, which necessitates the development of multilayer control and routing capabilities. In addition, as processor size increases, through-substrate ground connections will need to be introduced to eliminate parasitic chip modes, in the same spirit as via walls in

large interposer boards for classical electronics. All of these considerations point to a need for more sophisticated and capable 3D-integration approaches for superconducting qubits.

Three-dimensional (3D) integration as developed for conventional computing and imaging applications conceptually offers a solution for signal routing. However, many preexisting 3D-integration techniques involve processes and materials that are incompatible with high-coherence superconducting qubits. Many through-silicon via (TSV) interposer, multilayer stacking, and semiconductor technologies use deposited interlayer dielectrics (ILDs) to isolate signals in multilayer wiring<sup>17,18</sup>. However, industry-standard ILD materials, such as silicon dioxide (SiO<sub>2</sub>) and silicon nitride (Si<sub>3</sub>N<sub>4</sub>), decrease qubit lifetimes due to the interaction of the qubit electric field with the many defects present in such lossy, amorphous dielectrics<sup>19</sup>. In addition, common conductors used for metallization, such as copper, are not superconducting. Electric currents traveling in such normal metals cause heating and excite quasiparticles that degrade qubit performance<sup>20</sup>. Monolithic approaches using superconducting Nb circuitry with multiple wiring layers for dense signal routing can provide adequate connectivity, and even a pathway to integrated superconducting control electronics<sup>21</sup>, yet these are also associated with low qubit coherence due to, for example, lossy integrated dielectric films<sup>22–25</sup>.

To mitigate the incompatibility of both monolithic and standard 3D-integration techniques with high-coherence qubits, we have developed a “3-stack” chip concept that enables vertical signal delivery to a 2D array of qubits while maintaining qubit coherence<sup>12,13</sup>. The 3-stack (Fig. 1a) consists of three chips, fabricated independently according to best practices for each particular functionality, that are bump-bonded together using thermocompression bonding of indium pillars. The top chip—the qubit chip—contains high-coherence superconducting qubits fabricated on a silicon wafer. The bottom chip—a superconducting multi-chip module (SMCM)—has multiple planarized

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**Fig. 1 3D-integration scheme for readout and control of qubit arrays.** **a** Schematic rendering of the “3-stack”: a qubit chip (top) is connected to a wiring and signal processing circuitry chip (bottom) through an interposer chip (middle). Superconducting through-silicon vias (TSVs) provide electrical connection between the qubit and routing chips. Panel adapted from ref. <sup>12</sup>. **b** “2-stack” in which qubits are biased and measured through TSVs on the interposer chip. **c** Qubits fabricated directly on the surface of the interposer chip. **d** SEM cross-section of an etched TSV before wafer thinning, demonstrating the high aspect ratio etch processes leveraged in this work.

superconducting layers connected by vias and uses processes that have been advanced by digital superconducting electronics<sup>21</sup>. The SMCM chip may be used for both passive signal routing and active elements for qubit control and measurement such as single-flux-quantum circuits<sup>26</sup> or traveling-wave parametric amplifiers<sup>27</sup>.

The middle chip—known as the interposer chip—is the key innovation in this work. It contains TSVs lined with superconducting titanium nitride that connect the qubit and SMCM chips without resistive loss and without requiring close proximity between the qubits and the routing chip. When paired with indium bump bonds, this enables a low-resistance electrical path between the three chips<sup>10,12</sup>. The TSV-integrated interposer makes it possible to leverage the multilayer signal routing in the SMCM while maintaining isolation of qubits from lossy dielectrics. In particular, the silicon that comprises the interposer chip both provides physical distance to prevent overlap between the qubit electrical field and that of the dielectrics in the SMCM, and spreads the qubit electromagnetic field over a large mode volume to reduce sensitivity to loss modes. The interposer chip therefore alleviates a scaling bottleneck for the superconducting qubit platform.

In this paper, we present the integration of high aspect ratio superconducting TSVs with superconducting qubits. Our fabrication toolset enables compact TSVs—with a footprint of  $10\text{ }\mu\text{m} \times 20\text{ }\mu\text{m}$  passing through a  $200\text{ }\mu\text{m}$  chip—which allow for close packing of the TSVs and supports integration of TSVs directly into qubit readout and control circuitry. We demonstrate these capabilities in a “2-stack” that comprises the qubit chip and the TSV-integrated interposer chip. The chips are mechanically and electrically integrated using indium bump-bonding<sup>12</sup>, as shown in Fig. 1b and described in the “Methods”. A TSV pitch of 1 TSV per  $100\text{ }\mu\text{m}$  enables up to 10,000 TSV interconnects on a  $10\text{ mm} \times 10\text{ mm}$  chip, ensuring consistent ground connection across the chip; tighter pitches are also used in readout and control circuitry (Fig. 1d). We show that our process is compatible with high-performance qubits by demonstrating  $10\text{--}20\text{ }\mu\text{s}$   $T_1$  relaxation times both for qubits separately fabricated on a qubit chip and bump-bonded to the interposer in the 2-stack, and for qubits that are fabricated directly on the surface of the interposer chip (Fig. 1c). This work represents an important step toward realizing high-density 3D integration of arrays of qubits.

## RESULTS

We benchmark the integration of superconducting TSVs with superconducting qubits using capacitively-shunted flux qubits (CSFQs)<sup>28,29</sup>. The CSFQs used in this work are designed for

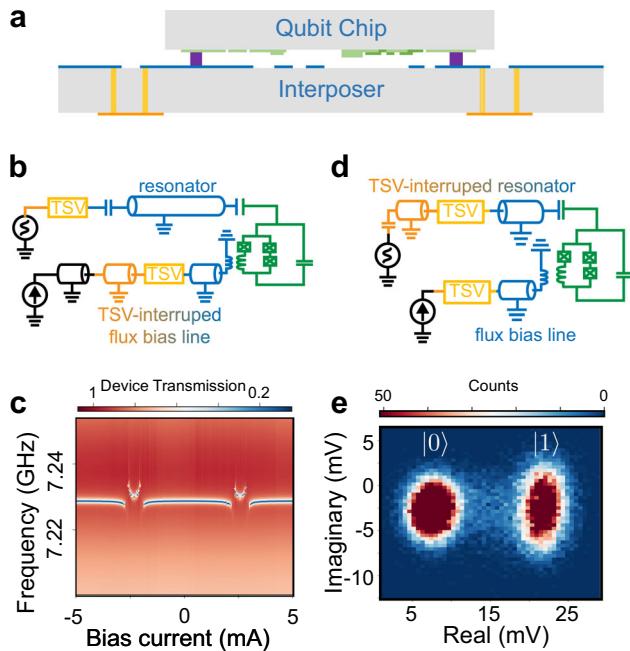
quantum annealing applications requiring tunable magnetic fields, large qubit-to-qubit coupling, and high connectivity<sup>30</sup>. Planar equivalents of these devices exhibit relaxation times of  $T_1 = 10\text{--}20\text{ }\mu\text{s}$ <sup>12</sup>, much longer than those demonstrated in commercial monolithic quantum annealing systems<sup>25</sup>. Control of annealing qubits requires several mA of baseband ( $<100\text{ MHz}$ ) current in order to tune the qubit Hamiltonian. More generally, qubit excitation and readout requires the ability to send high-fidelity microwave signals in the 3–10 GHz range. Here, we demonstrate such baseband and microwave control of CSFQs using TSV-integrated bias and readout elements.

### Qubit control and readout through interposer chip

Our first set of devices demonstrate the active control of a qubit using off-chip lines that pass from one side of the interposer to the other via a  $50\text{ }\Omega$  TSV transition (Fig. 2). Specifically, 2-stack devices with TSVs in flux bias lines, used for baseband qubit frequency control, and in coplanar waveguide (CPW) resonators, used for microwave qubit readout, were designed and fabricated. Devices testing baseband and microwave control functionality were separately fabricated and measured; the mean qubit lifetime across all such devices was  $T_1 = 10\text{ }\mu\text{s}$ .

In Fig. 2b, c, we demonstrate baseband control of the CSFQ frequency using a TSV-integrated flux bias line inductively coupled from the interposer chip to the qubit chip. A direct current is introduced to the bottom side of the interposer chip through a CPW input line. The current passes through a  $50\text{ }\Omega$  baseband transition—comprising a set of TSVs, surrounding TSV ground shields, and top- and bottom-side metallizations—that is designed to ensure good signal integrity across baseband frequencies. This current continues through a second CPW section on the top side of the interposer chip, and then couples inductively to a CSFQ located on the qubit chip with a mutual inductance of  $M = 0.4\text{ pH}$ . This suffices to tune the CSFQ’s first transition frequency over a full flux quantum by applying  $\sim 5\text{ mA}$  to the bias line, as evidenced by the periodicity of the avoided crossing between the qubit and the resonator (Fig. 2c). This is well within the bounds of the typical TSV critical current, which exceeds 10 mA. We see no heating of the dilution refrigerator during the persistent application of this current, which is consistent with all aspects of the circuit remaining superconducting. Thus, we demonstrate that the interposer and TSV-integrated baseband transition support CSFQ frequency tuning through several flux quanta.

We next use a TSV-integrated resonator as a test of the ability of the TSVs to carry microwave signals (Fig. 2d, e). Splitting a resonator or other microwave component across the two



**Fig. 2 2-stack devices used to demonstrate control and readout circuitry incorporating TSVs.** **a** Schematic showing color coding. Green: qubit chip; blue: top of interposer chip; yellow: TSVs; orange: bottom of interposer chip; black: room temperature electronics. Circuit schematics show the surface placement of qubits, resonators, and bias lines, including TSV transitions in the flux bias line (**b**) and readout resonator (**d**). The device was probed from the top surface through an additional TSV transition. **c** Spectroscopy of a readout resonator taken while biasing a qubit using a flux bias line incorporating a TSV transition. Four avoided crossings between the qubit and the resonator are observed, indicating that the qubit has tuned through more than a full flux quantum. **e** Single-shot readout using a readout resonator incorporating a microwave-optimized TSV transition. The data represent sequential preparation of the qubit in the  $|0\rangle$  and  $|1\rangle$  states, respectively as labeled. The readout partially excites the  $|1\rangle$  state into  $|2\rangle$  due to the relatively high photon number used for readout<sup>40</sup>. This leads to the slight skew in the distribution corresponding to  $|1\rangle$ , but does not impact the fidelity of the measurement because the  $|0\rangle$  state is unaffected.

interposer planes enables novel designs and a more compact per-qubit footprint. In addition, from a technological perspective this test is particularly sensitive, because any signal distortions in the microwave range would impact our ability to read the qubit state with high fidelity. We pattern the first half of a  $\lambda/4$  CPW resonator onto the bottom of the interposer (Fig. 2d) and pass to the top of the chip using a  $50\Omega$  TSV transition, this time optimized to maintain signal integrity at microwave frequencies (see ref. <sup>9</sup> for more details). The second half of the resonator is patterned on the top of the interposer, where it capacitively couples to the CSFQ on the qubit chip. Figure 2e shows single-shot readout statistics for the CSFQ prepared in its ground (left) and excited (right) states, using a measurement integration time of  $2.5\mu\text{s}$ . These data correspond to a separation infidelity of  $\epsilon_S = 2.1 \times 10^{-5}$  (defined as the integrated overlap of the Gaussian distributions to which these data were fit). Thus, we demonstrate that TSV transitions can support microwave signals sufficient to perform high-fidelity qubit readout.

#### Qubit thermalization in multi-chip architectures

Strong thermalization in any multitier qubit stack is critical to ensure that qubits maintain the tens-of-mK temperatures required to avoid spurious excitations. As shown schematically in Fig. 3a,

the qubit chip thermalizes through its superconducting (and therefore poorly thermally conducting) indium bump bonds to the interposer chip. The interposer chip is itself separated from the copper package—which provides the cold thermal bath—by a silicon support ring that mimics the SMCM chip and by superconducting aluminum wirebonds. None of these are canonically good thermal conduction paths, so we must verify that qubits are able to sufficiently thermalize in the 2- and 3-stack architectures.

The ability to do high-fidelity single-shot readout using TSV connections enables us to probe qubit thermalization in the 2-stack architecture. This can be tested with the same device used in Fig. 2d, e. In Fig. 3b, we show a histogram of 21,000 single-shot measurements of a qubit that has been passively prepared in its thermal steady state. A DC current of  $2.3\text{ mA}$  was applied during the duration of this experiment; no heating of the dilution refrigerator was observed. We measure an excited state probability  $P_e = 3.3\%$ , corresponding to an effective qubit temperature of  $T_Q = 52.5\text{ mK}$  at the qubit transition frequency  $3.718\text{ GHz}$ . This compares favorably to single-qubit-chip thermalization temperatures of  $35\text{--}40\text{ mK}$ <sup>31</sup>. Well-established techniques exist for initializing a pure quantum state at these temperatures<sup>32–34</sup>; we therefore confirm that qubit performance in the 2-stack is on par with that in single-chip architectures.

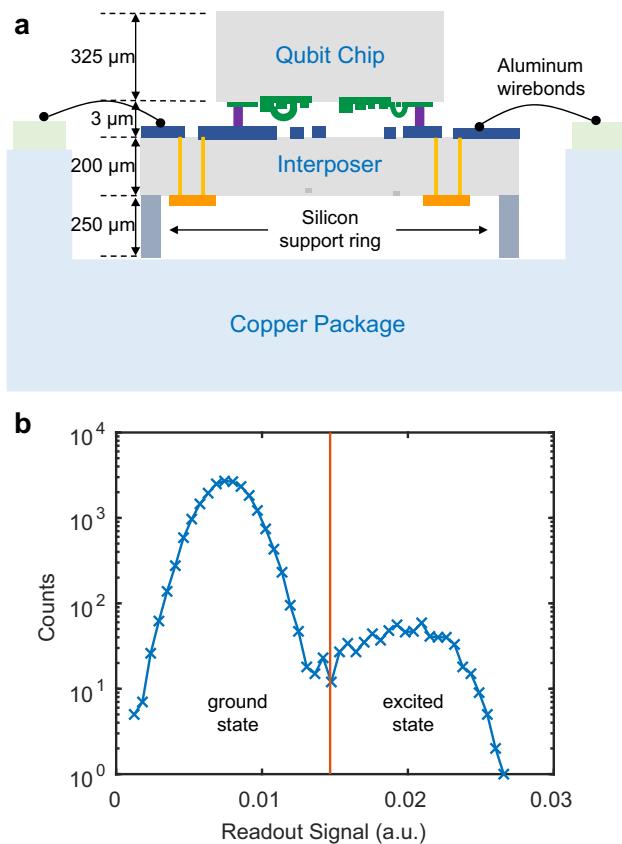
#### Integration of qubits on TSV interposer surfaces

To take full advantage of the additional surface that the top of the interposer chip provides, the interposer top should ideally be compatible with active Josephson junction elements including tunable couplers and qubits. This is a highly nontrivial engineering challenge: the interposer chip top sees substantial mechanical and chemical processing far beyond that used for a standard qubit chip (see “Methods”). Deposition and patterning processes all must be optimized for compatibility with these additional processing steps, imposing significant constraints. Overcoming these challenges and adding coherent active elements and qubits on the interposer, however, pays dividends in opening up new architectural possibilities for denser qubit packing and novel qubit coupling schemes<sup>30</sup>.

In Fig. 4, we demonstrate the fabrication of coherent CSFQs directly on the surface of the interposer chip. Figure 4a–c show scanning electron microscope images of the top side of the interposer, including TSVs, control and readout circuitry, and Josephson junctions. Despite the process integration challenges required to create the TSVs, we measure relaxation times ( $T_1$ ) for qubits fabricated on the interposer surface averaging  $12.5\mu\text{s}$  across four co-fabricated qubits (Fig. 4e). These coherence times are consistent with similar annealing qubits fabricated on silicon surfaces that have not undergone TSV processing steps<sup>12</sup>. Such qubits are sufficient for off-chip coupling elements for gate-model quantum computing and are on par with devices being developed for high-coherence annealing<sup>12,35</sup>. This validates an important new capability for the 2-stack and 3-stack architectures<sup>30,36</sup>.

#### DISCUSSION

In this work, we have demonstrated integration of superconducting TSVs into superconducting qubit readout and control circuitry, enabled by the small footprint and high aspect ratio of our superconducting TSVs. The TSVs provide densely-packed ground connections across the interposer and enable active readout and control modalities to cross through the interposer without degrading signal performance and with the potential for reduced crosstalk. The TSVs occupy a footprint that is orders of magnitude smaller than that of current-generation superconducting qubits, enabling the use of TSV-integrated control and readout elements without impacting the effective footprint of each qubit. We have



**Fig. 3 Qubit thermalization through interposer chip.** **a** Schematic showing the path from the qubit chip to the thermal bath (i.e., the copper package). The qubit chip thermalizes via superconducting indium (purple), aluminum (green), and titanium nitride (blue, orange) metallization layers and wirebonds, as well as through bulk silicon. **b** Histogram of 21,000 single-shot measurements of a sample CSFQ that has been passively prepared in its thermal state. We extract an excited state probability of  $P_e = 3.3\%$ , which corresponds to an effective qubit temperature of  $T_q = 52.5$  mK for a qubit with transition frequency  $\omega_q/2\pi = 3.718$  GHz.

designed and demonstrated compact,  $50\ \Omega$  TSV transitions that support both baseband and microwave signals, showing that we can route high-fidelity control and readout signals through the third dimension in a multi-chip stackup. We show that qubits thermalize effectively in our multi-chip stackup, despite the additional thermal resistance introduced by the integration of multiple chips. These capabilities confirm and demonstrate the utility of our TSV design and fabrication in enabling the readout and control of 3D-integrated qubit arrays.

The utilization of TSV-integrated interposers demonstrated here advances the state of the art in superconducting TSVs for quantum computing applications in several important ways. TSVs with sloped-wall geometries have been previously demonstrated to suppress substrate modes on qubit chips<sup>37</sup>; however, these TSVs are the same size as typical superconducting qubits ( $\sim 100\text{--}300\ \mu\text{m}$  per side) and if incorporated into both readout and control circuitry would significantly increase the per-qubit footprint. High-aspect ratio TSVs have been used to connect to large area kilopixel transition-edge sensor bolometer arrays<sup>38</sup>; however, these TSVs lacked critical currents sufficient to enable flux control of qubit frequencies, and they required the use of atomic layer deposition instead of the chemical vapor deposition (CVD) used here. The TSVs integrated into the interposer chip in this work combine the aspect ratio and the critical current necessary for full qubit readout and control.

Complex quantum system architectures may benefit from multiple levels of qubits and several routing layers. Our ability to fabricate coherent CSFQs directly on the surface of interposer chips supports a variety of 3D-integrated qubit architectures. One can use the top side of the interposer chip to introduce a second qubit plane and increase the qubit density beyond what is achievable in a single-tier architecture. For applications in which different Josephson junction critical current densities are required for different circuit components, those components can be fabricated on separate chips, thereby minimizing additional processing on each chip and increasing design flexibility. Active elements, such as tunable couplers, can be fabricated on the surface of the interposer chip in order to enable novel schemes with stronger, more compact coupling<sup>30</sup>. These 2-stack demonstrations passing high-fidelity baseband and microwave signals through compact TSVs are critical enabling capabilities for connecting superconducting multilayer routing to high-coherence qubits. Future work will demonstrate the full 3-stack integration of qubits, interposer, and multilayer signal routing.

## METHODS

### TSV-integrated interposer fabrication

The fabrication of the TSV-integrated interposer follows a via-first process on an industry-standard 200 mm wafer fabrication line. The TSVs are etched into 725  $\mu\text{m}$  thick high-resistivity silicon wafers. A Bosch etch process consisting of rapidly alternating cycles of silicon etching and sidewall polymerization is used to etch high-aspect-ratio TSVs with smooth sidewalls (low scalloping). We etch blind TSVs  $>200\ \mu\text{m}$  deep with a sidewall slope  $>89^\circ$ . A thin film of TiN is deposited using an optimized CVD process to provide superconducting film coverage along the sidewalls of the TSVs and over the wafer surface; this becomes the bottom of the wafer, as shown in orange in Figs. 1–4. This metal is subtractively patterned using thick resist and plasma etching.

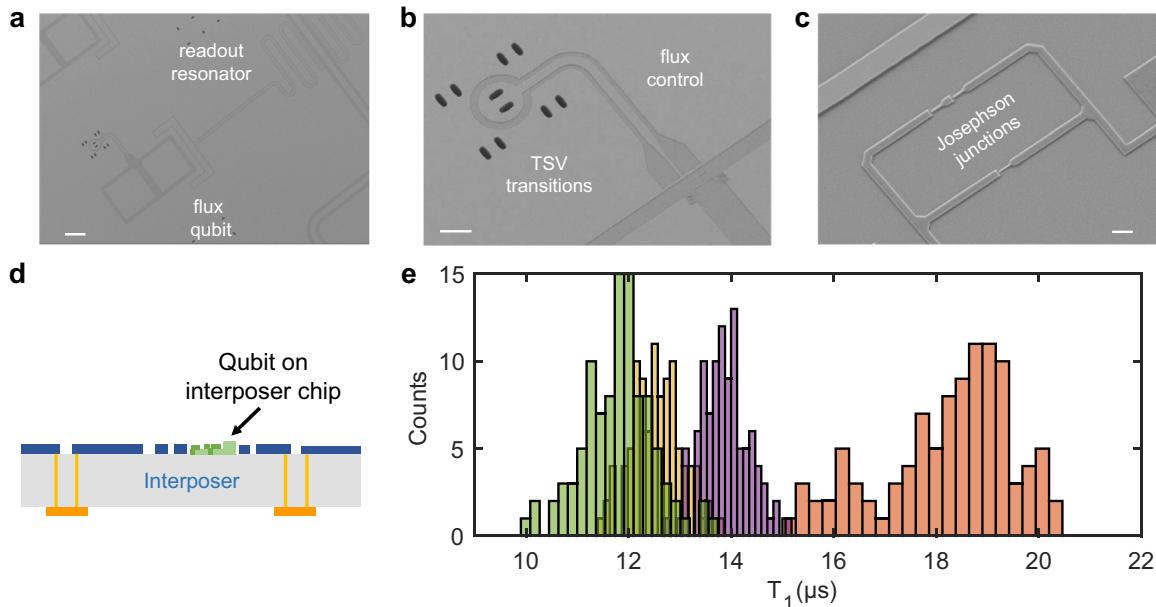
Each interposer wafer is then flipped and bonded to a temporary carrier wafer using a Brewer wafer bond temporary adhesive. The wafer is thinned by a combination of grinding and chemical mechanical polishing to reveal the opposite (top) side of the TSVs shown in blue in Figs. 1–4. TiN is deposited on this newly revealed top surface using physical vapor deposition. Interconnects, bias lines, resonators, and qubit capacitors are defined using subtractive etching. Al/AlO<sub>x</sub>/Al Josephson junctions for qubits and other active elements are fabricated using a Dolan bridge defined by electron-beam lithography and utilizing a double-angle shadow evaporation process<sup>39</sup>. Finally, the wafer is diced and released from the temporary carrier wafer. Additional interposer fabrication details will be published in a forthcoming work by Mallek and Yost, et al.

### Qubit chip fabrication

Qubit chip devices are patterned on 50-mm-diameter high-resistivity ( $>10,000\ \Omega\text{ cm}$ ) silicon substrates. The qubit devices consist of silicon hard-stop spacers<sup>13</sup>, base metal, superconducting qubits, underbump metal, and indium bumps. Base metallization components, including capacitive shunts, ground planes, and on-chip control and readout circuitry, are patterned by subtractive etching into aluminum. The patterned surface is ion milled in situ to remove native aluminum oxide prior to definition of qubit loops and Josephson junctions using double-angle shadow evaporation through Dolan-style bridges<sup>39</sup>. Indium bumps, which are 15  $\mu\text{m}$  in diameter and 5–15  $\mu\text{m}$  tall, are patterned on the qubit chip on top of an underbump metallization layer of titanium/platinum/gold which ensures the indium makes good electrical contact with the underlying aluminum. Additional fabrication details are available in refs. <sup>12,29</sup>.

### Flip-chip integration

Qubit and interposer chips are bump-bonded using thermocompression bonding. For the chips used in this work, indium bumps are used only to connect the ground planes of the two chips; they do not carry active signals. Bump bonding is performed at 105 °C in a commercial thermocompression bonding system with a post-bond lateral accuracy of  $<1\ \mu\text{m}$ . This alignment accuracy, which is verified with post-bond infrared imaging of alignment structures, has a negligible effect on the



**Fig. 4** Qubits fabricated directly on the surface of the TSV-integrated interposer chip. **a–c** SEM images of TSV-integrated qubits. **a** A zoom-out showing the qubit, the readout resonator, and the TSV-integrated flux bias line. Scale bar is 100  $\mu$ m. **b** A zoom-in showing the TSV flux line transition. Scale bar is 30  $\mu$ m. **c** The three Josephson junctions that form the CSFQ loop. Scale bar is 2  $\mu$ m. **d** Schematic of qubits patterned directly on the qubit-chip-facing surface of the interposer chip. **e** A histogram of qubit relaxation times ( $T_1$ ) measured for four qubits. The mean  $T_1$  across all four qubits is 12.5  $\mu$ s.

**Table 1.** Qubit and resonator frequencies for all devices described in this paper, as well as  $T_1$  relaxation times and  $T_{2,\text{Ramsey}}$  and  $T_{2,\text{Echo}}$  as measured at the flux-insensitive point.

Qubit parameters						
Qubit	Qubit location	Qubit freq. (GHz)	Resonator freq. (GHz)	$T_1$ ( $\mu$ s)	$T_{2,\text{Ramsey}}$ ( $\mu$ s)	$T_{2,\text{Echo}}$ ( $\mu$ s)
a	Qubit chip	4.189	7.165	$10 \pm 3$	n/m	n/m
b	Qubit chip	4.091	7.229	$9.1 \pm 0.8$	$7.7 \pm 0.6$	$8.5 \pm 0.6$
c	Qubit chip	3.671	7.259	$10 \pm 3$	n/m	n/m
d	Qubit chip	3.698	7.362	$9 \pm 3$	n/m	n/m
e	Qubit chip	3.718	5.281	$9 \pm 2$	n/m	n/m
f	Interposer	3.359	7.324	$18 \pm 1$	$19 \pm 2$	$27 \pm 2$
g	Interposer	2.483	7.395	$12.6 \pm 0.5$	$1.7 \pm 0.2$	$1.6 \pm 0.2$
h	Interposer	3.788	7.469	$13.8 \pm 0.5$	$2.6 \pm 0.3$	$3.3 \pm 0.5$
i	Interposer	2.576	7.658	$11.8 \pm 0.7$	$3.0 \pm 0.4$	$4.0 \pm 0.6$

The notation “n/m” indicates quantities that were not measured. Error bars represent the standard deviation of repeated measurements over several hours. The differences between the  $T_1$  of the qubits on the qubit chip and on the interposer chip are not statistically significant. The lifetime of flux qubits is typically limited by the size of the SQUID loop: larger loops have lower  $T_1$ , but are also amenable to stronger coupling to neighboring qubits, which has advantages in annealing applications. Planar equivalents of the devices measured here (i.e., designed with identical SQUID loops and capacitances) typically have relaxation times of  $T_1 = 10\text{--}20 \mu\text{s}$ <sup>12</sup>. Because this study focused on  $T_1$ , the measurements of  $T_2$  were typically taken from rough calibration scans and are underestimates of the true coherence of the devices. Samples b and f were fine-tuned to extract the optimal phase coherence for those devices.

coupling between the qubits and elements on the interposer chip. The post-bond vertical spacing between the two chips is 3  $\mu$ m.

#### Measurement

The measurements in Figs. 2–4 are taken using standard dispersive measurement techniques<sup>1</sup>. We couple a CSFQ biased at its flux-insensitive point in the 2–5 GHz range to a CPW  $\lambda/4$  resonator in the 7–8 GHz range. The experiments were performed in a commercial BlueFors XLD-1000 dilution refrigerator operating at a base temperature of 12 mK. The measurement chain incorporates a high-efficiency traveling-wave parametric amplifier that enables high-fidelity readout<sup>27</sup>. In Fig. 2a, we measure the transmission of a resonator that is capacitively coupled to a

CSFQ in a 2-stack architecture. We tune the qubit through several avoided crossings with the resonator and observe the vacuum Rabi splitting between the qubit and the resonator. The periodicity of these avoided crossings provides the effective inductive coupling between the TSV-integrated bias line and the qubit. In Fig. 2b, we measure a separate 2-stack device that incorporates TSV-integrated resonators. We record complex-valued single-shot measurements for 21,000 preparations each of the lowest two energy states  $|0\rangle$  and  $|1\rangle$ , and fit the distribution of those measurements to a Gaussian function. The separation and width of the Gaussian fits allow us to extract the separation fidelity. The  $|0\rangle$ -prepared single-shot data is also used in Fig. 3b to extract the qubit temperature. The data in Fig. 4e are taken from four qubits fabricated on the top side of an interposer chip after TSV fabrication. All readout resonators are coupled

to a common feedline. Each qubit was sequentially biased to its flux-insensitive point, where the  $T_1$  relaxation time was measured 100 times over the course of  $\sim 2$  h and then histogrammed.

Measured qubit parameters, including frequencies and  $T_1$  relaxation times, are recorded in Table 1.

## DATA AVAILABILITY

The data supporting the findings of this study are available within the paper. The data are available from the authors upon reasonable request and with the permission of our US Government sponsors.

## CODE AVAILABILITY

The code used to process data presented in the study is available from the authors upon reasonable request and with the permission of our US Government sponsors.

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D.R.W.Y., J.M., C.S., J.L.Y., M.C., R.D., D.K.K., A.M., and B.M.N. developed processes and executed the fabrication and 3D integration of the devices. D.R. and W.W. designed the devices. M.E.S. performed the cryogenic qubit measurements. D.R.W.Y., M.E.S., D. R., and W.D.O. wrote the paper. M.E.S., D.R., G.C., A.L.D., E.B.G., and W.W. contributed to qubit design, measurement infrastructure, and data analysis. D.R., J.L.Y., A.J.K., and W.D.O. provided technical direction.

## COMPETING INTERESTS

The authors declare no competing interests.

## ADDITIONAL INFORMATION

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