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Characterizing conditional quantum dynamics on superconducting quantum processors

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Abstract The pursuit of practical quantum computation relies on the precise implementation and characterization of high-fidelity entangling gates. We present a detailed experimental characterization of the controlled-NOT (CX) and controlled-phase (CZ) gates on a noisy intermediate-scale quantum (NISQ) superconducting processor using full quantum process tomography and direct state measurements. The gates were benchmarked against a noise-free quantum simulator to isolate hardware-induced errors. The CX gate, implemented as a native gate, achieved an average process fidelity of $\mathcal{F}_p^{\mathrm{CX}} = 93.02\%$ and correctly prepared the target state with $P_{00}^{\mathrm{CX}} = 92.40\%$ probability. The CZ gate, decomposed into a sequence of single-qubit and CX gates, achieved $\mathcal{F}_p^{\mathrm{CZ}} = 92.59\%$ with superior state-preparation fidelity of $P_{00}^{\mathrm{CZ}} = 97.08\%$. Remarkably, the compiled CZ gate outperformed the native CX gate in state preservation by 4.68-percentage points, demonstrating the effectiveness of hardware-aware compilation. Our analysis provides a comprehensive benchmark of these essential gates, revealing that compilation strategy can be as crucial as native hardware performance for reliable quantum circuit execution in the NISQ era.

1 Introduction

The development of practical quantum computers [1, 2] hinges on the high-fidelity implementation of entangling operations [3–5], which are essential for generating the quantum correlations that enable computational advantage [6–8]. These operations exemplify *conditional quantum dynamics* [9]—a fundamental concept where the quantum evolution of one subsystem (the target qubit) becomes intrinsically dependent on the state of another subsystem (the control qubit) [10]. This conditional dynamics represents a distinct quantum mechanical phenomenon that transcends classical control logic, as it operates coherently on superposed states to generate genuine quantum entanglement.

Within the framework of universal quantum computation [11], the CX and CZ gates serve as canonical implementations of conditional quantum dynamics, forming a complete gate set when combined with arbitrary single-qubit rotations [12]. However, on current NISQ hardware [8], the performance of these gates is substantially limited by decoherence, control inaccuracies, and crosstalk [13–17]. Comprehensive characterization through methods such as quantum process tomography (QPT) [18–20] is therefore critical for benchmarking gate performance, identifying error sources, and informing hardware development [21]. QPT has proved effective for characterizing controlled gates in diverse platforms, from linear optical implementations [22] to photonic time-bin qubits [23]. In superconducting qubits, pioneering early work demonstrated QPT of two-qubit gates using phase qubits, including characterization of the $\sqrt{i\mathrm{SWAP}}$ gate [24] as well as controlled-Z and controlled-NOT gates [25], with reported process fidelities of 63%, 70%, and 56%, respectively. These foundational studies established QPT methodologies for solid-state quantum processors but were constrained by the coherence limitations of first-generation phase qubits [13].

This work extends these characterization techniques to modern superconducting transmon processors [26, 27], which offer significantly improved coherence times and gate fidelities, thereby enabling more precise quantification of gate performance and detailed analysis of error mechanisms [13–17]. This work presents a detailed experimental study comparing the performance of CX and CZ gates on an IBM Quantum's superconducting quantum processor. We employ full QPT to reconstruct the complete process matrix for each gate [18–20], conducting parallel experiments on both a noiseless simulator ('qasm_simulator') and physical hardware to isolate the contribution of noise to gate infidelity [28, 29]. The CX gate was implemented as a native operation, while the CZ gate was realized through a hardware-aware decomposition into single-qubit gates and one CX gate, allowing us to investigate the impact of circuit compilation on gate performance [30–33].

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Our results demonstrate robust performance for both gates, with process fidelities exceeding 92% on hardware. The native CX gate achieved $\mathcal{F}_p^{\mathrm{CX}} = 93.02\%$, slightly outperforming the decomposed CZ gate ($\mathcal{F}_p^{\mathrm{CZ}} = 92.59\%$) in overall process fidelity. However, in state-preparation fidelity, the compiled CZ gate demonstrated superior performance, correctly preparing the target state with $P_{00}^{\mathrm{CZ}} = 97.08\%$ compared to $P_{00}^{\mathrm{CX}} = 92.40\%$ for the native gate—a 4.68-percentage point advantage that highlights the effectiveness of hardware-aware compilation. The consistent fidelity gap of approximately 4–5 percentage points between simulator and hardware quantifies the collective effect of device noise. By correlating these findings with contemporaneous device metrics—including relaxation times (T_1), dephasing times (T_2), and readout errors—we provide insight into the dominant sources of infidelity and offer practical guidance for optimizing quantum circuit design on superconducting platforms [27, 34].

The paper proceeds through the following sections: Sect. 2 lays the theoretical groundwork by examining conditional quantum dynamics, with subsections dedicated to two-qubit entanglement mechanisms 2.1, the canonical CX and CZ gates, and their geometric representation within the Weyl chamber (2.2). Section 3 details the experimental methodology, detailing both the hardware configuration of the superconducting quantum processor and the specific implementation strategies employed for the CX and CZ gates. Section 4 presents a comprehensive analysis of the quantum process tomography results, discussing fidelity metrics, error sources, and performance correlations with device characteristics. Finally, Sect. 5 concludes with a summary of findings and perspectives for future work.

2 Background: conditional quantum dynamics

2.1 Two-qubit gates and entanglement

The computational advantage of quantum information processing [35] stems from the coherent control of multi-qubit entanglement [3]. Two-qubit gates are the fundamental building blocks for generating this entanglement, enabling the non-classical correlations necessary for quantum algorithms to surpass their classical counterparts [35].

The term *conditional quantum dynamics* precisely captures the essential mechanism underlying controlled quantum gates: The quantum dynamics of one subsystem (the target qubit) become conditioned on the state of another subsystem (the control qubit) [9]. This conditioning represents a fundamental departure from classical control logic, as it operates not merely on discrete binary states but on the continuous parameters of quantum superposition and phase [36]. When the control qubit exists in superposition, the conditional dynamics generate coherent entanglement between the qubits, creating quantum correlations that cannot be described by any local hidden variable theory [37].

The CX and CZ gates, in particular, form a universal set for quantum computation when supplemented with arbitrary single-qubit rotations [12, 38]. Their precise implementation is therefore a critical metric for assessing the capabilities of quantum hardware. In fact, any entangling two-qubit gate, supplemented with arbitrary single-qubit rotations, forms a universal set for quantum computation [12, 38]. The CX and CZ gates serve as canonical examples in this context, widely adopted due to their natural emergence in physical platforms (e.g., superconducting qubits, linear optics) and their foundational role in circuit design. Their precise implementation is therefore a critical metric for assessing the capabilities of quantum hardware.

2.2 Canonical controlled gates

The CX gate performs a Pauli-X (bit-flip) operation on the target qubit if and only if the control qubit is in the state $|1\rangle$ [12, 38]. Its unitary representation in the computational basis $\mathcal{B}_2 = \{|00\rangle, |01\rangle, |10\rangle, |11\rangle\}$ is given by:

$$U^{\mathrm{CX}} = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{pmatrix}.$$

This gate is a maximally entangling operator and serves as a standard primitive in quantum circuit design, from quantum error correction to arithmetic operations [39].

The CZ gate (also known as the controlled-phase or CSIGN gate) applies a conditional phase shift, imparting a factor of -1 to the amplitude of the $|11\rangle$ state [10, 12]. Its unitary matrix is:

$$U^{\mathrm{CZ}} = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 \end{pmatrix}.$$

The CZ gate is locally equivalent to the CX gate, related by the transformation $\mathrm{CX} = (\mathbb{I} \otimes H) \cdot \mathrm{CZ} \cdot (\mathbb{I} \otimes H)$, where H is the Hadamard gate [12]. Despite this equivalence, the CZ gate often arises more naturally in many physical implementations, such as in certain superconducting circuit architectures [26, 40] and linear optical quantum computing (LOQC) [41–44], due to its symmetry

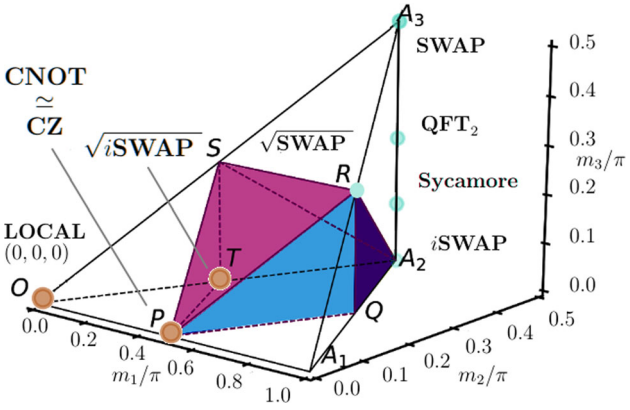

Fig. 1 Geometric representation of two-qubit gates within the Weyl chamber. The chamber is a tetrahedron defined by the local invariants (m_1, m_2, m_3). The positions of the CX, CZ, and other standard gates (e.g., SWAP, iSWAP, $\sqrt{\text{SWAP}}$, $\sqrt{i\text{SWAP}}$, Sycamore, and QFT_2) are shown. The polyhedral region TS$R$$A_2$QP represents the set of perfect entanglers

and the nature of the underlying qubit interactions. It should be noted, however, that in the specific processor used in this work (*ibm_nairobi*), the CX gate is the native entangling operation.

The geometric representation of two-qubit gates in the Weyl chamber [45, 46] further illustrates this relationship: The CX and CZ gates—being locally equivalent—correspond to the same vertex, as shown in Fig. 1. This framework helps visualize gate relationships and entangling power; both CX and CZ lie within the region of "perfect entanglers," confirming their ability to generate maximal entanglement. The positions of the CX, CZ, and other standard gates (e.g., SWAP, iSWAP, $\sqrt{\text{SWAP}}$, $\sqrt{i\text{SWAP}}$ [24], Sycamore [21], and QFT_2 [12]) are also presented.

3 Methods

Complete QPT experiments [18–20, 47] were performed on the *ibm_nairobi* quantum processor, a 7-qubit superconducting device based on IBM's Falcon r5.11H architecture. This processor has a quantum volume [48] of 32 and supports a basis gate set of $\mathcal{G}^{\text{ibm}}_{\text{nairobi}} = \{\text{ID, RZ, SX, X, CX}\}$, consistent with IBM's Falcon-family architecture as documented in the official QPU specifications [49]. The general device's performance metrics are summarized in Table 1. The median 2-qubit (CX) and 1-qubit (SX) gate errors were 7.238×10^{-3} and 2.948×10^{-4}, respectively, with a median readout error of 2.160×10^{-2}. The median energy relaxation and dephasing times were $T_1 = 97.85\,\mu\text{s}$ and $T_2 = 67.56\,\mu\text{s}$ [50]. Qubit drive frequencies ranged from approximately 4.53 to 5.79 GHz. All experiments were conducted in September 2023 on this processor before its retirement; calibration data were logged directly from the system and are provided in Tables 1, 2 and 3. The methodology remains fully reproducible on current superconducting processors with similar gate sets and coherence profiles.

The CX gate was implemented as a native gate directly supported by the hardware's control electronics (Fig. 2). The CZ gate, not natively available on this processor, was decomposed into a sequence of single-qubit gates and one CX gate (Fig. 3). This decomposition inherently makes the CZ gate more susceptible to error accumulation due to its longer duration.

We employed a dual-characterization approach to comprehensively evaluate gate performance. Full QPT was used to reconstruct the complete process matrices and calculate process fidelities. Additionally, direct state measurements were performed by applying each gate to the $|00\rangle$ input state and measuring the output distribution across the computational basis states. This approach provided complementary metrics: QPT quantified overall gate quality, while direct measurements assessed state-preparation fidelity and revealed specific error patterns in the output subspace. All experiments were conducted with a shot count of 4000 per measurement basis; this resulted in a total of 576,000 quantum measurements, to ensure sufficient statistical sampling for tomography and to mitigate the impact of shot noise.

To isolate the error contribution from the gate itself from those of state preparation and measurement (SPAM) [51, 52], the same QPT procedure was also performed on a noiseless state vector quantum simulator to establish a theoretical fidelity upper bound for the given circuit compilation and finite-shot statistical regime. We refer the reader to [47] for a detailed treatment of QPT utilizing the Choi matrix representation in superconducting transmon processors [26].

To contextualize the gate performance results, detailed device metrics are presented in Tables 2 and 3. The former captures system-wide parameters during the initial QPT characterization period, while the latter provides implementation-specific data logged during the actual execution of the CX and CZ gates. These tables reflect typical calibration variations, yet the overall device stability allowed both the QPT and gate-implementation experiments to achieve fidelities exceeding 92%. The consistency in performance despite these variations underscores the reproducible operation of the processor under routine calibration cycles.

Table 1 Summary of key performance metrics for the *ibm_nairobi* processor [50]

Parameter	Median value
Quantum volume	32
CX gate error	7.238×10^{-3}
SX gate error	2.948×10^{-4}
Readout error	2.160×10^{-2}
T_1 (Relaxation time)	97.85 μs
T_2 (Dephasing time)	67.56 μs
Qubit frequency range	4.53 – 5.79 GHz

Table 2 Device properties for the "ibm_nairobi" quantum processor during the QPT experiments

Qubit	T_1 (μs)	T_2 (μs)	Freq (GHz)	Anh (GHz)	Readout Err	P(0|1)	P(1|0)	Readout Len (ns)
Q0	80.779	30.702	5.2605	−0.3398	0.0225	0.0328	0.0122	5560.888
Q1	127.35	105.23	5.1704	−0.3406	0.0263	0.0374	0.0152	5560.888
Q2	101.96	100.78	5.2743	−0.3389	0.0286	0.0438	0.0134	5560.888
Q3	144.12	60.266	5.0267	−0.3425	0.0294	0.0460	0.0128	5560.888
Q4	129.40	79.236	5.1772	−0.3406	0.0188	0.0278	0.0098	5560.888
Q5	99.227	19.777	5.2925	−0.3405	0.0987	0.1414	0.0560	5560.888
Q6	63.208	111.29	5.1287	−0.3404	0.0224	0.0360	0.0088	5560.888

Parameters include relaxation times (T_1), dephasing times (T_2), qubit frequency (Freq (GHz)), anharmonicity (Anh (GHz)), readout error (Readout Err), conditional measurement probabilities (P(0|1) and P(1|0)), and readout length (Readout Len). These metrics define the noise environment for the gate characterization

Table 3 Specification metrics for the qubits used in the experimental implementation of the two-qubit gates (CX and CZ)

Qubit	T_1 (μs)	T_2 (μs)	Freq (GHz)	Anh (GHz)	Readout Err	P(0|1)	P(1|0)	Readout Len (ns)
Q0	119.97	33.18	5.2605	−0.3398	0.0204	0.0294	0.0114	5560.89
Q1	145.91	112.72	5.1704	−0.3406	0.0288	0.0410	0.0166	5560.89
Q2	104.49	137.78	5.2743	−0.3389	0.0311	0.0478	0.0144	5560.89
Q3	99.46	68.28	5.0267	−0.3425	0.0228	0.0356	0.0100	5560.89
Q4	86.87	76.34	5.1772	−0.3406	0.0179	0.0288	0.0070	5560.89
Q5	124.40	22.01	5.2925	−0.3405	0.0595	0.1006	0.0184	5560.89
Q6	81.50	142.77	5.1287	−0.3404	0.0201	0.0334	0.0068	5560.89

These values, logged during the job execution, provide the coherence times and error rates relevant to the gates' performance

4 Results and discussion

4.1 Direct state measurements results

Experimental measurements confirm the correct logical action of both the native CX and compiled CZ gates when applied to the $|00\rangle$ input state. The performance was quantified by measuring the probability of obtaining the correct output state P_{00}, along with analyzing error patterns through the complete output distribution.

For the native CX gate, execution on the noiseless simulator yielded the ideal outcome with $P_{00}^{\text{sim}} = 100\%$. On physical hardware, the gate achieved $P_{00}^{\text{hw}} = 92.40\%$, with the 7.60% infidelity characterized by population leakage into erroneous states. The $|10\rangle$ state was the most prominent error channel (2.85% of outcomes), indicative of specific single-qubit errors on the control or target qubit. The compiled CZ gate exhibited superior performance in state preservation. While the simulation also showed perfect results ($P_{00}^{\text{sim}} = 100\%$), the hardware implementation achieved a notably higher $P_{00}^{\text{hw}} = 97.08\%$ (Fig. 4d). The extremely low population in the $|11\rangle$ state (0.03%) suggests that the dominant error mechanism involves single-qubit errors populating the $|01\rangle$ and $|10\rangle$ states, with very few correlated two-qubit errors.

This analysis demonstrates that both native and carefully compiled gates can achieve high-fidelity operation on superconducting quantum hardware. The CZ gate's 4.68-percentage point higher success probability (P_{00}) compared to the CX gate, despite requiring a non-native decomposition, highlights the remarkable effectiveness of the hardware-aware compilation strategy in minimizing error propagation. It should be noted that the superior state-preparation fidelity of the compiled CZ gate observed here is specific to the $|00\rangle$ input state. A comprehensive benchmark across all two-qubit basis states ($|00\rangle$, $|01\rangle$, $|10\rangle$, $|11\rangle$) would be required to determine

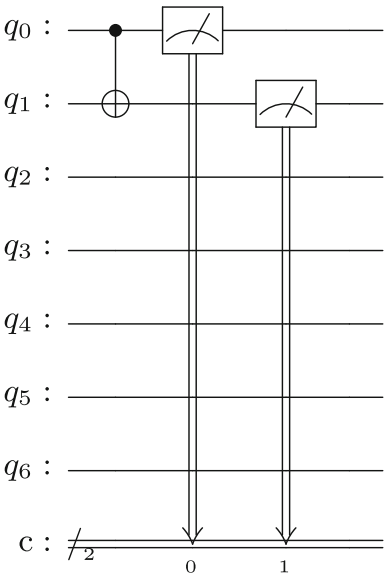

Fig. 2 Experimental quantum circuit for the native CX gate. The gate is native to the target quantum hardware and is applied directly to the target qubits (q_0 as control, q_1 as target) on the superconducting processor, *ibm_nairobi*

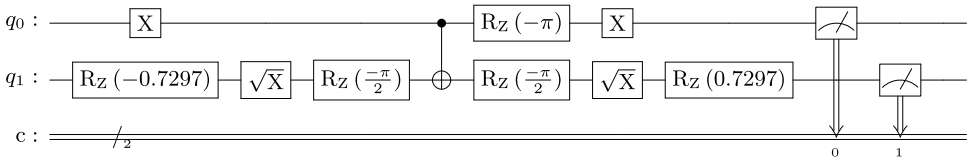

Fig. 3 Hardware-aware quantum circuit for the CZ gate. The non-native gate is implemented using a sequence of single-qubit gates and one CX gate, demonstrating efficient adaptation to superconducting hardware connectivity constraints

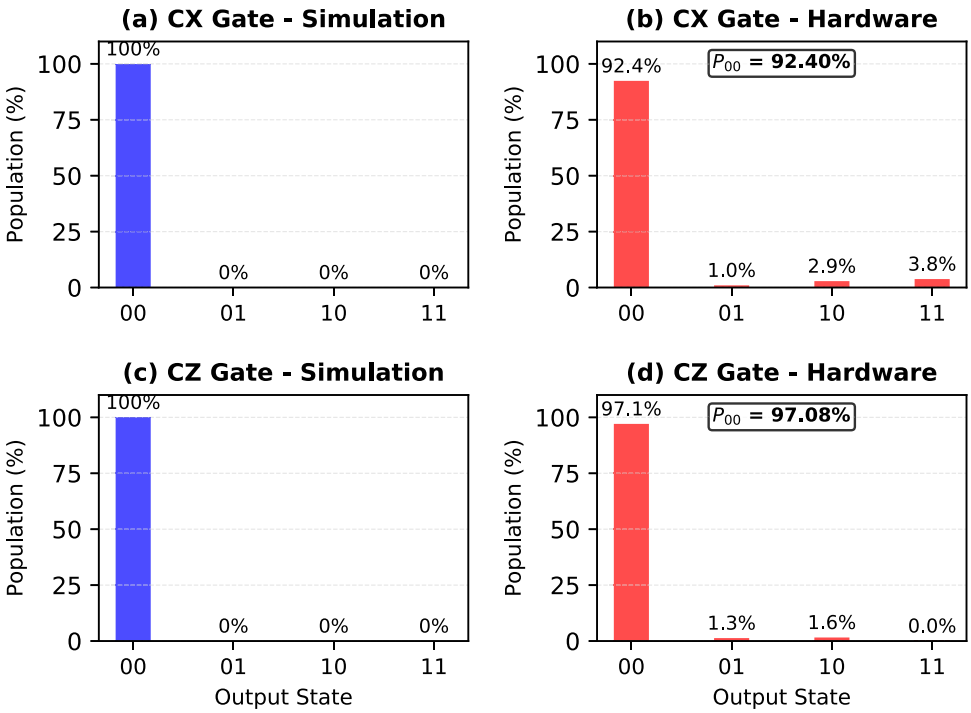

Fig. 4 State population distributions for CX and CZ gates applied to the $|00\rangle$ input state. Output probabilities for the **a** CX gate simulation, **b** CX gate hardware execution, **c** CZ gate simulation, and **d** CZ gate hardware implementation. The ideal simulator confirms correct logical operation (100% $|00\rangle$). Hardware results show the compiled CZ gate achieves higher state preservation ($P_{00} = 97.08\%$) compared to the native CX gate ($P_{00} = 92.40\%$). The CX gate exhibits prominent $|10\rangle$ errors (2.85%), while the CZ gate shows minimal correlated errors ($|11\rangle = 0.03\%$) with dominant single-qubit error channels

whether this advantage extends to arbitrary inputs. Such an extension represents a natural direction for future work, providing a more complete picture of how hardware-aware compilation affects gate performance across the full computational space.

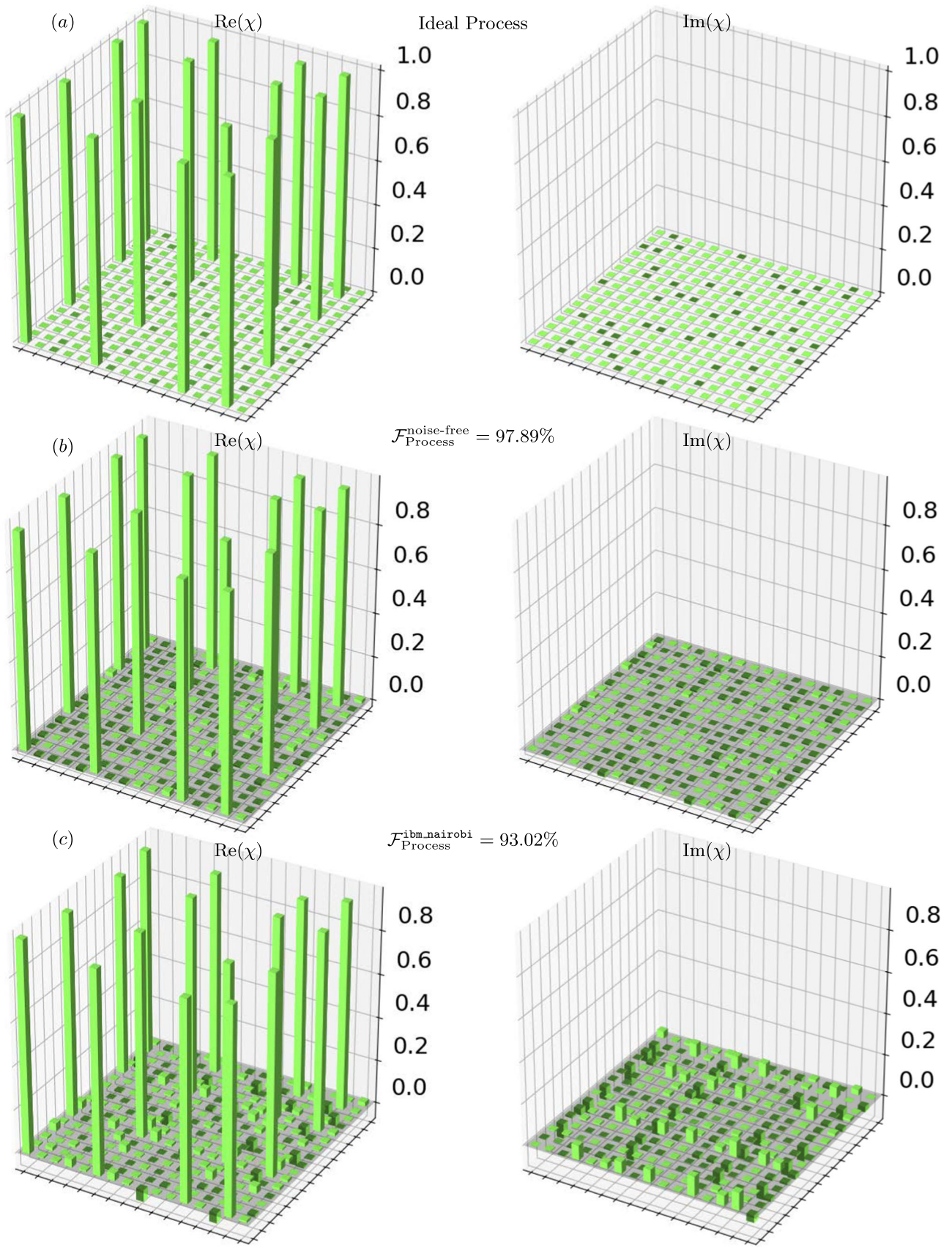

Fig. 5 Quantum process tomography results for the CX gate. **a** Ideal theoretical process matrix ($\mathcal{F}_p^{CX} = 1.0$). **b** Process matrix reconstructed from the noiseless qasm simulator ($\mathcal{F}_p^{CX} = 97.89\%$). **c** Process matrix reconstructed from experiments on the "ibm_nairobi" processor ($\mathcal{F}_p^{CX} = 93.02\%$), showing clear signatures of hardware noise

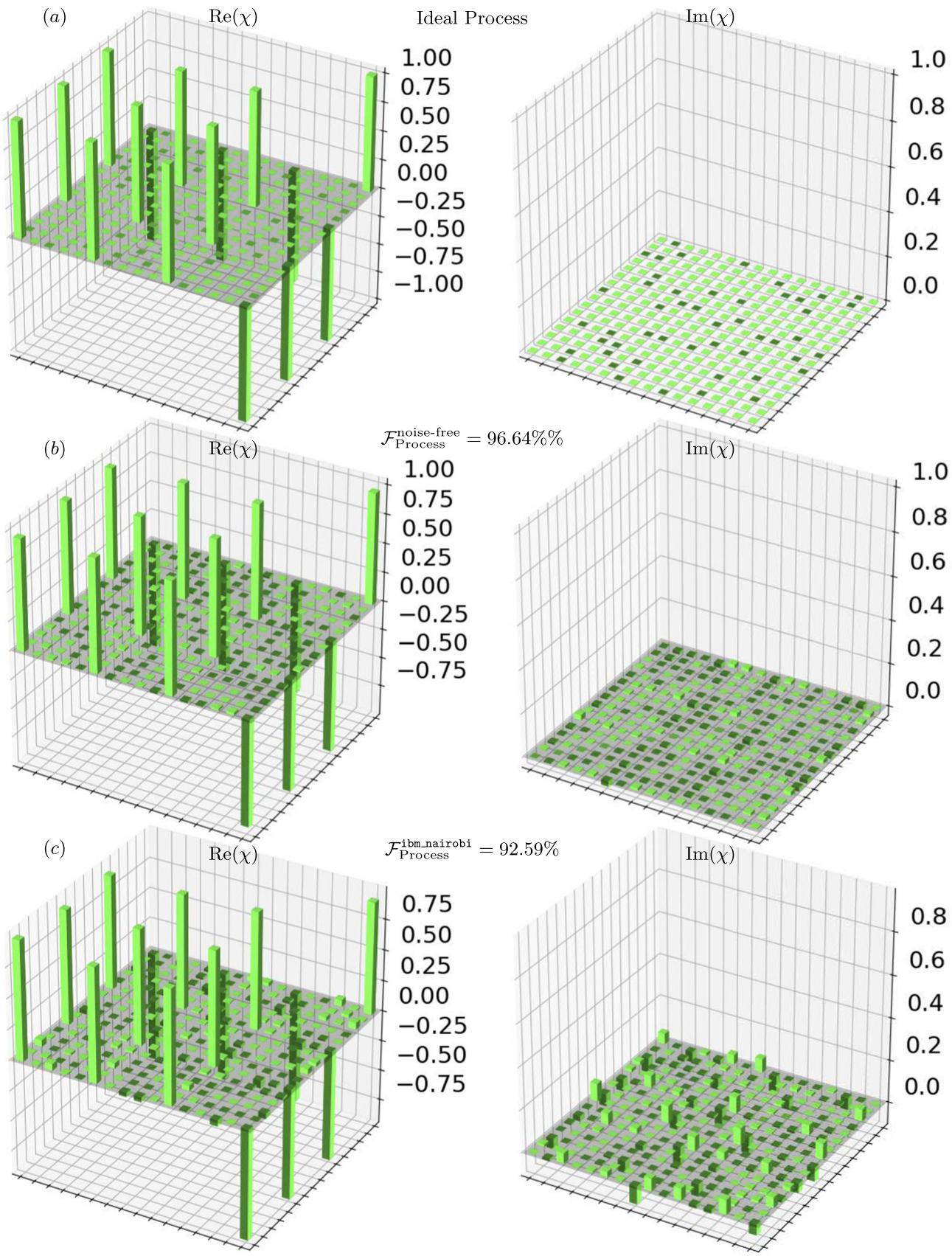

Fig. 6 Quantum process tomography results for the CZ gate. **a** Ideal theoretical process matrix ($\mathcal{F}_p^{CZ} = 1.0$). **b** Process matrix from the noiseless qasm simulator ($\mathcal{F}_p^{CZ} = 96.64\%$). **c** Process matrix from the "ibm_nairobi" hardware ($\mathcal{F}_p^{CZ} = 92.59\%$). The increased infidelity compared to the CX gate is consistent with error accumulation from its longer decomposed sequence

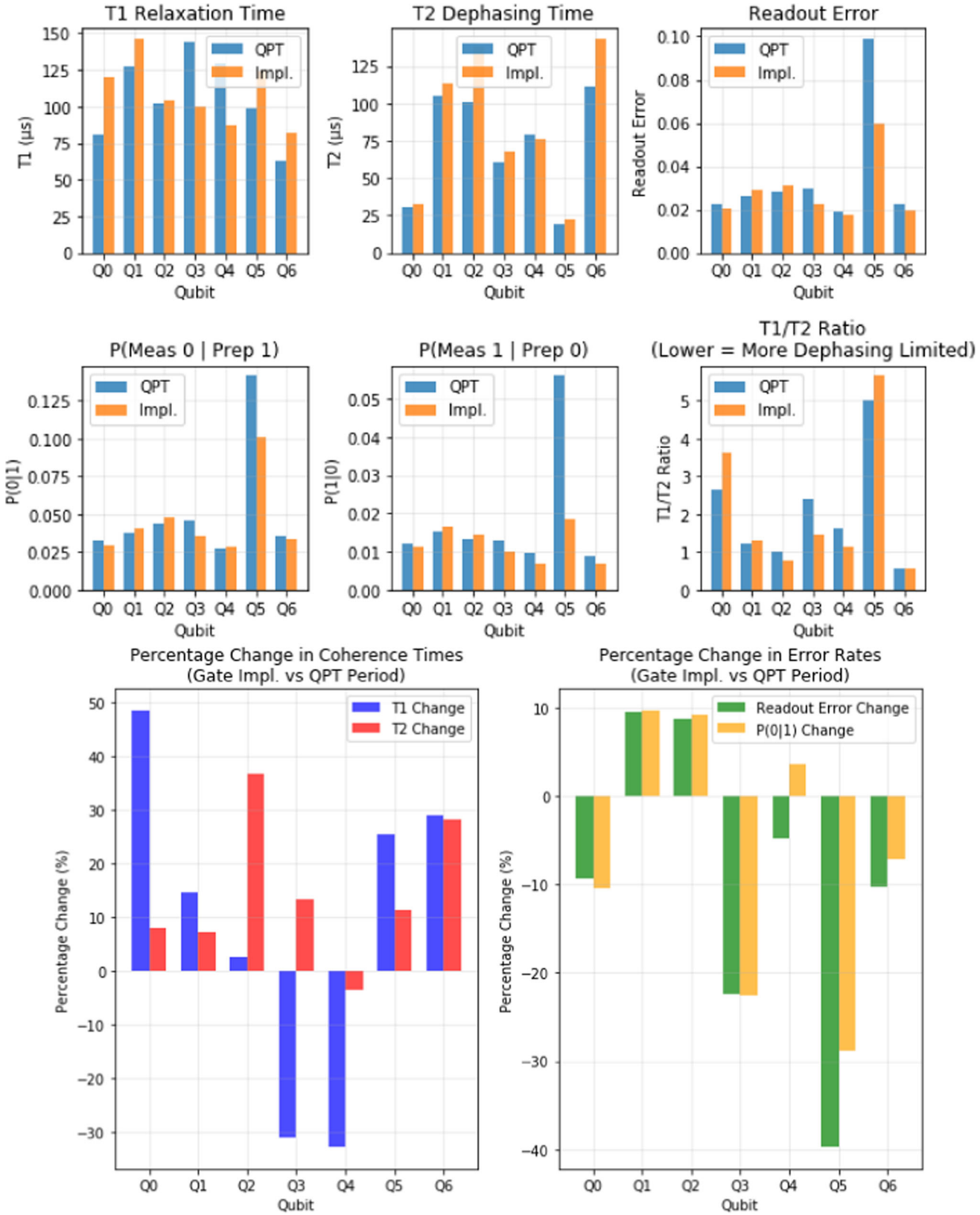

Fig. 7 Comparative analysis of qubit performance metrics between QPT characterization and gate-implementation periods on the quantum hardware, *ibm_nairobi*. Summary statistics show percentage changes in average coherence times (T_1, T_2) and error rates across the 7-qubit processor. The T_2 dephasing time improved by +16.9%, while the T_1 relaxation time remained stable (+2.2%). These temporal improvements in device calibration likely contributed to the enhanced gate performance observed during experimental implementation. Error bars represent the standard deviation across the seven qubits

Table 4 Comprehensive characterization of CX and CZ gates showing quantum process tomography fidelities ($\mathcal{F}_p$) and state-preparation probabilities (P_{00})

Gate	Process fidelity $\mathcal{F}_p$		$\Delta\mathcal{F}_p$	State preparation P_{00}		ΔP_{00}
	Simulator (%)	Hardware (%)	(HW drop) (%)	Simulator (%)	Hardware (%)	(HW drop) (%)
CX (Native)	97.886	93.017	4.87	100.00	92.40	7.60
CZ (Non-native)	96.637	92.587	4.05	100.00	97.08	2.92

While both show similar process fidelity degradation on hardware ($\Delta\mathcal{F}_p \approx 4$–5%), the compiled CZ gate achieves higher state-preparation fidelity (P_{00}), outperforming the native CX gate by 4.68-percentage points. The fidelity drop on hardware quantifies the total effect of decoherence and control errors

4.2 The quantum process fidelity results

The results of the QPT experiments are summarized in Table 4. The process fidelity $\mathcal{F}_p$ was calculated by comparing the experimental process matrix χ_{exp} to the ideal matrix χ_{ideal} [28, 29]. This metric provides a measure of how well the experimental gate implements the desired unitary operation. The $\mathcal{F}_p$ obtained from the quantum simulator were $\mathcal{F}_p^{\text{CX}} = 97.89\%$ and $\mathcal{F}_p^{\text{CZ}} = 96.64\%$, with the non-unit fidelity attributed to finite-sampling error from the 4000 shots per measurement basis. On the quantum hardware, the fidelities were $\mathcal{F}_p^{\text{CX}} = 93.02\%$ and $\mathcal{F}_p^{\text{CZ}} = 92.59\%$, representing a consistent fidelity reduction of approximately $4 - 5$ percentage points compared to the simulated results.

The visual representation of the quantum processes in Figs. 5 and 6 provides qualitative insight into the nature of the hardware imperfections [13]. The experimental process matrices show clear deviations from their ideal counterparts, particularly in the off-diagonal elements which represent phase coherence and entanglement properties [13]. The hardware results exhibit characteristic signatures of decoherence, including diminished off-diagonal components and increased population in non-ideal states [14, 15].

The observed performance gap between simulation and hardware quantifies the collective impact of noise sources present in the superconducting quantum processor [14, 15]. This fidelity reduction can be attributed to several factors: energy relaxation governed by T_1 times, pure dephasing characterized by T_2 times, imperfect gate calibration, residual ZZ crosstalk [16, 17], and readout errors [13–17].

4.3 Quantum hardware characterization

Analysis of the device metrics during the QPT experiments (Table 2) provides insight into the noise environment during tomography. The qubits used for the experiments (Q_0 and Q_1) exhibited markedly different coherence properties: Q_0 had $T_1 = 80.779$ µs and $T_2 = 30.702$ µs, while Q_1 showed $T_1 = 127.35$ µs and $T_2 = 105.23$ µs. The notably shorter T_2 of Q_0, which is substantially less than its T_1, indicates that pure dephasing is a dominant error channel for this qubit. Readout errors during the QPT period were 2.25% for Q_0 and 2.63% for Q_1, adding infidelity to the process reconstruction.

During the gate-implementation period (Table 3), the coherence times improved: Q_0 reached $T_1 = 119.97$ µs and $T_2 = 33.18$ µs, while Q_1 attained $T_1 = 145.91$ µs and $T_2 = 112.72$ µs. Readout errors shifted to 2.04% (Q0) and 2.88% (Q1). Despite these variations, both gates achieved fidelities above 92%, illustrating the processor's robustness under routine calibration cycles. A comparative analysis of all seven qubits (Fig. 7) shows that, on average, T_2 improved by +16.9% between the QPT and implementation periods, while T_1 remained stable (+2.2%). These temporal improvements reflect recalibration and likely contributed to the consistently high gate performance observed in both experimental phases.

5 Conclusion

This work has presented a detailed experimental characterization of two fundamental entangling gates—the CX and CZ—on an NISQ-era superconducting quantum processor using full QPT and direct state measurements. Our results demonstrate robust implementation, with both gates achieving process fidelities exceeding 92% under current NISQ-era conditions. The native CX gate ($\mathcal{F}_p^{\text{CX}} = 93.02\%$) showed a subtle process fidelity advantage over the decomposed CZ gate ($\mathcal{F}_p^{\text{CZ}} = 92.59\%$). However, a more nuanced picture emerged from state-preparation metrics: The compiled CZ gate significantly outperformed its native counterpart, preparing the target state with $P_{00}^{\text{CZ}} = 97.08\%$ fidelity compared to $P_{00}^{\text{CX}} = 92.40\%$.

The observed performance gap of approximately 4–5 percentage points between the noiseless quantum simulator and the physical hardware quantitatively captures the collective impact of decoherence, imperfect control, and readout errors. These findings underscore a critical, refined principle for near-term quantum computing: While the overall process fidelities of the native CX and compiled CZ gates are statistically comparable, the compiled CZ gate achieved a 4.68-percentage point higher *state-preparation fidelity* for the particular input $|00\rangle$. This suggests that, for specific input states and algorithmic primitives, carefully compiled non-native gates can exploit hardware-aware error mitigation to match or even exceed the performance of native gates. However, a full assessment across all possible input states would be required to determine whether this advantage generalizes. This expands

the toolkit for quantum circuit optimization, indicating that fidelity benchmarks should consider both overall process quality and state-specific performance to guide the design of efficient and reliable quantum circuits.

Looking forward, the path toward fault-tolerant quantum computation necessitates further improvements in gate fidelity through several promising directions. Applying advanced error mitigation techniques such as zero-noise extrapolation or probabilistic error cancelation could post-process our results to yield a more accurate estimate of the ideal process matrix, providing deeper insight into the underlying error mechanisms. Extending this tomography-based methodology to other qubit technologies would offer a standardized benchmark for comparing the maturity of different hardware platforms, while investigating the impact of dynamical decoupling sequences during gate operations could help mitigate dephasing noise and boost T_2-limited fidelity. Furthermore, refining pulse-level implementations to develop the CZ gate as a native, high-fidelity operation would be valuable for closing the performance gap with CX gates.

For quantum algorithm designers, our study reinforces the importance of tailoring circuits to a hardware's native interaction graph and gate set to optimize performance. For hardware developers, the results highlight that while significant progress has been made, simultaneous improvements in qubit coherence times, control precision, and readout fidelity are all required to cross the 99% fidelity threshold necessary for advanced quantum error correction codes. This work provides a rigorous, tomography-based benchmark that charts the progress of superconducting quantum processors and outlines the challenges that should be addressed to advance toward practical quantum computation.

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Author contributions M. AbuGhanem was involved in conceptualization, methodology, formal analysis, visualization, investigation, validation, and writing—reviewing and editing. The author approved the final manuscript.

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Data availability The datasets generated during and/or analyzed during this study are included within this article.

Declarations

Conflict of interest The author declares no Conflict of interest.

Ethical approval and consent to participate Not applicable.

Consent for publication All authors have approved the publication. This research did not involve any human, animal, or other participants.

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