

The New Small Wheel High Voltage Infrastructure

I. Drivas-Koulouris *, **Efstathios Karentzos****

*National Technical University of Athens, Physics Department, 9 Heroon Polytechniou, Zografos, Postal code 15780, Athens GR

**Albert-Ludwigs-Universität Freiburg, Fahrenbergplatz, 79085 Freiburg im Breisgau, Germany

E-mail: ioannis.drivas-koulouris@cern.ch, efstathios.karentzos@cern.ch

Abstract. The ATLAS Muon Spectrometer is subjected to a series of upgrades in order to face the High Luminosity era of Phase-II. One of the main projects is the New Small Wheel (NSW), which has replaced the existing Small Wheel (SW), and is a perfect complement to the ATLAS Muon Spectrometer (MS) in the Endcap regions. The NSW is the combination of two prototype detector technologies, the small Thin Gap Chambers (sTGC) and the resistive Micromegas (MM). In order to operate smoothly the two technologies, a dedicated hardware infrastructure has been installed and modified accordingly based on the needs of each muon sub-system. In order to control and monitor the hardware for both technologies a Detector Control System (DCS) has been developed, following the architecture of the legacy Muon sub-systems. Aim of this work is the presentation of the development and implementation of these HV DCS systems under the Point 1 schema.

1. Introduction

The replacement of SW with the NSW in the context of the upgrade of MS [1] brought many changes to all the systems involved. The biggest was on DCS [2] where 2 new technologies were introduced in order to meet the prerequisite upgrades. Along with the automatic control system, where it is based on how it is installed the hardware. The MM system has a direct approach by hosting the CAEN A7038 HV boards [3] on a CAEN SY4527 Mainframe [4], while in total 6 mainframes (3 per side) provide the power and service all the HV channels. The sTGC follows the daisy chain logic, where a CAEN SY4527 Mainframe hosts four CAEN A1676A Branch Controller [5]. Each branch controller handles a CAEN EasyCrate3000 and either one channel of a 48V ACDC Generator; CAEN 3485s for service [6] and 3486 for power [7]. The last element of the chain are the HV boards on the crates. All the HV boards have been validated on surface before the installation at the ATLAS cavern. In order this chain of hardware to be operated successfully, the ATLAS experiment has a dedicated central Detector Control System (DCS), which checks the operational status of different sub-systems and enables the communication between them. Similarly, the NSW follows the same conventions and thus it is being controlled by dedicated projects built with the SIMATIC WinCC Open Architecture (WinCC-OA) [8].



2. Finite State Machine (FSM)

The FSM [9] is an abstract machine that is able to be in only one of a finite number of states at a time; the state can change when initiated by a triggering event or condition (transition state). A particular FSM node is defined by a list of states, and the triggering conditions for the transitions between them. Figure 1 depicts the ATLAS FSM architecture. The Global Control Station (GCS), which is in supervision of the overall operation of the detector, provides high level control and monitoring of all the sub-detectors; the execution of the commands and the data processing are managed at the lower levels. Sub-detector Control Stations (SCSs) constitute

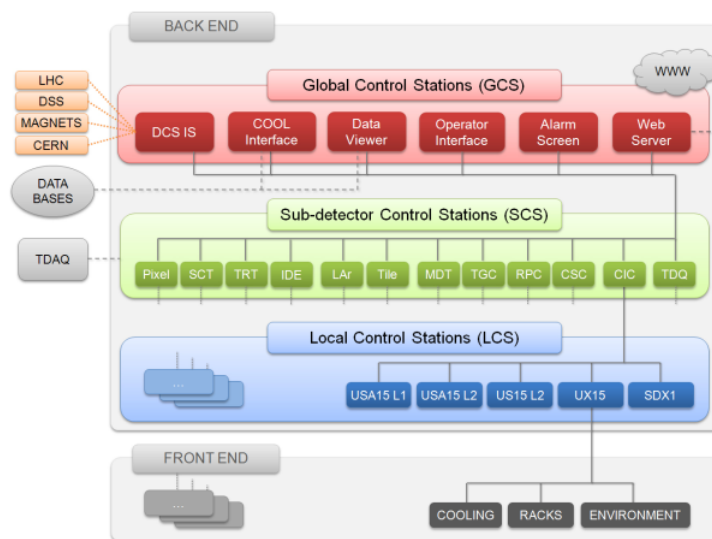


Figure 1. The ATLAS DCS architecture.

the middle level of the “back-end” architecture. The SCS allows the full local operation of a sub-detector.

The DCS activates the supervision of the equipment using commands, processes and actions on the operational parameters of the detector. It is also responsible for the communication between the internal parts of the system and with external control systems. At this level in the hierarchy, the connection with the Data Acquisition (DAQ) system is established in order to guarantee the synchronization between the detector operation and the physics data taking. For this purpose the sub-detector is divided into partitions which are based on the DAQ TTC (Timing, Trigger and Control) zones. Both systems are synchronized via the DAQ-DCS Communication (DDC) software package. The FSM plays an important role, reporting the DCS state of the TTC zones to the DAQ and executing commands received from DAQ. The final part of the FSM hierarchy on the back-end side, is the Local Control Stations (LCSs). This layer provides the low level control and monitoring of the SCS services, executing all the received commands from it and at the same time is able to trigger autonomously predefined actions if necessary. Each LCS is in charge of a certain system within the sub-detector (i.e. HV, LV, Racks, gas, cooling, etc).

The lowest level is composed of Device Units (DUs) which implement the connection layer between the FSM and the hardware, defining in such way the granularity of the system. Everything below these boundaries is not accessible through the FSM.

3. NSW Caen Easy System

The CAEN EASY system is a modular system of LV and HV power supplies developed by CAEN for the LHC experiments; are grouped into two main categories, the radiation-sensitive parts, and the radiation hard parts. Among its core features are the remote control, the scalability, the compatibility with operation under strong magnetic fields, and radiation harsh environments like the ATLAS cavern (UX15).

The MMG HV system consists of three mainframes per side and the HV boards are installed directly onto them. The main difference between them is that the third mainframe is fully equipped with 16 A7038AP boards serving in such a way all 16 sectors, 4 layers, and the first 5 PCBs (8 in total per layer). The other mainframes follow the same “mapping” scheme, where 4 A7038STP HV boards supply the remaining 3 PCBs. The system is completed by two boards of type A7038STN, which supplies the voltages of the drift panels. The FSM tree consists of three nodes dedicated to each mainframe. The graphical user interface (panel), as illustrated in Figure 2, monitors the vitals (fan speed, status, V1/V0 set flag, etc.) of each mainframe along with the visualisation of the installed board and their main status parameters.

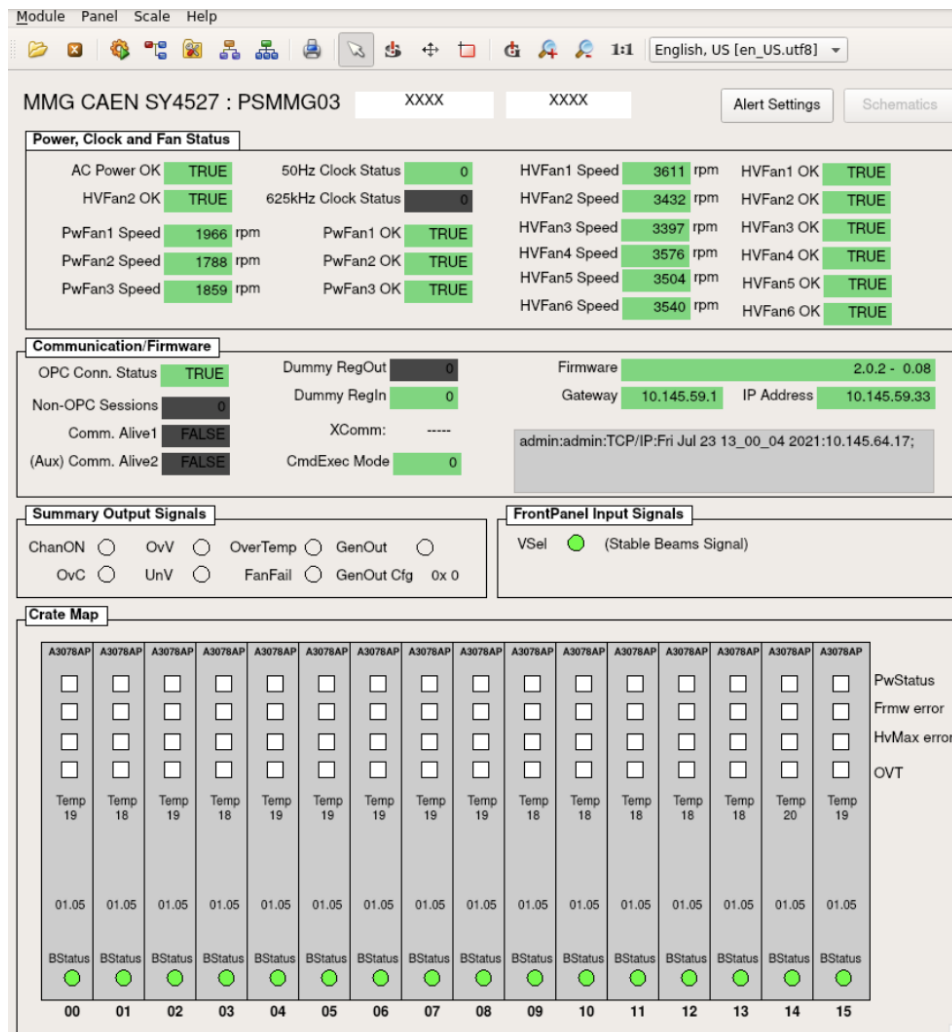


Figure 2. Main FSM MMG panel for the Mainframes

The STG HV system architecture consists of a mainframe, two branch controllers and four crates per side. The branch controllers handles the chain along with the generators. The HV boards are installed in the CAEN EasyCrates and located in the UX15, in a unified format in order to regulate the power consumption per crate. There are two different types of boards, the A3540P and the A3535P serving the 16 STG sectors. There are 4 parts per layer, where the former serves the innermost part of the detector while the other type the rest. The FSM is divided in three nodes :

- one for the mainframe with the main panel similarly to the MMG Tree, but branch controllers' information instead of boards as shown in Figure 3.
- one node branch controllers.
- one node for the crates including also the FSM branch controllers for the HV boards, as shown in Figure 3.

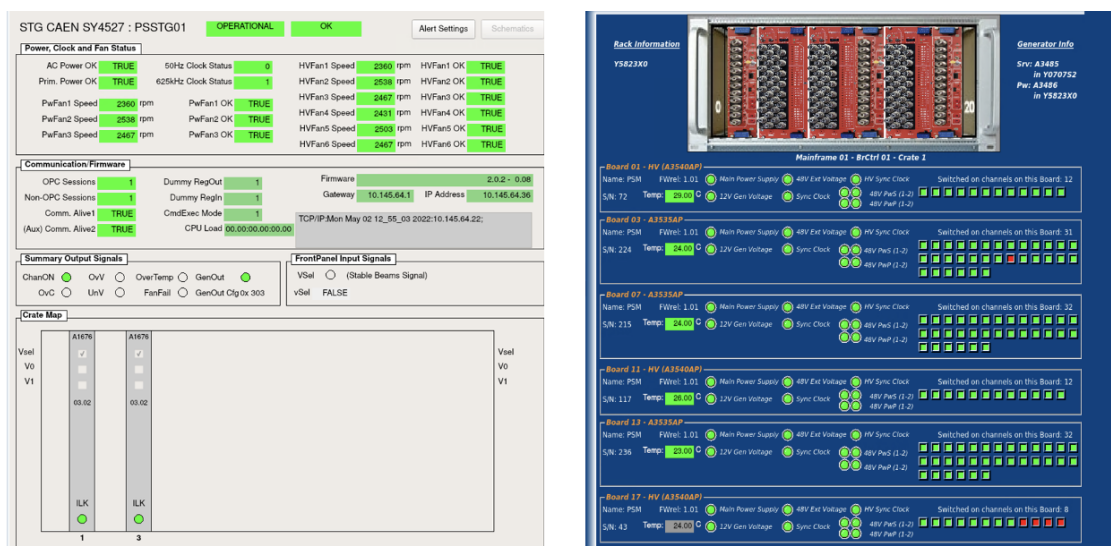


Figure 3. On the left is Main FSM STG panel for the Mainframes. On the right the Main FSM panel for STG crates.

4. NSW (STG) Caen 48V Generators

The 48V generators are used for the STG Sub-detector using the pre-existing muon logic. The crates and boards are supplied with an external DC power of 48V generated by separate AC-DC converters. The system consists of two generators per side of detector. Each generator has two channels. The 48V Service generator is responsible for the control of the easy chain circuitry, distributing the power to the easy crate controllers. The 48V power generator on the other hand is responsible for the output power of the modules up to the channels' level.

Left Figure 4 depicts the associated to the generators rack. Each generator is represented by a rectangle which holds the details about the current, voltage and temperature of every channel. The panel also provides information about the branch controllers and the main logical parameters of the channels as well as supplementary information concerning the connected branch controllers and the generators channels, alongside with a visual representation of the associated to these generators' chambers. The user/expert can select a variety of monitoring controls to perform,

from highlighting the associated to the generator chambers, up to configuring low level elements such as the alert handling. The main STG generators FSM include all these panels, which are associated with the respective nodes. By clicking the state of the nodes, the user can turn on/off the corresponding generators' channels, allowing in such way the control of all or part of the connected hardware.

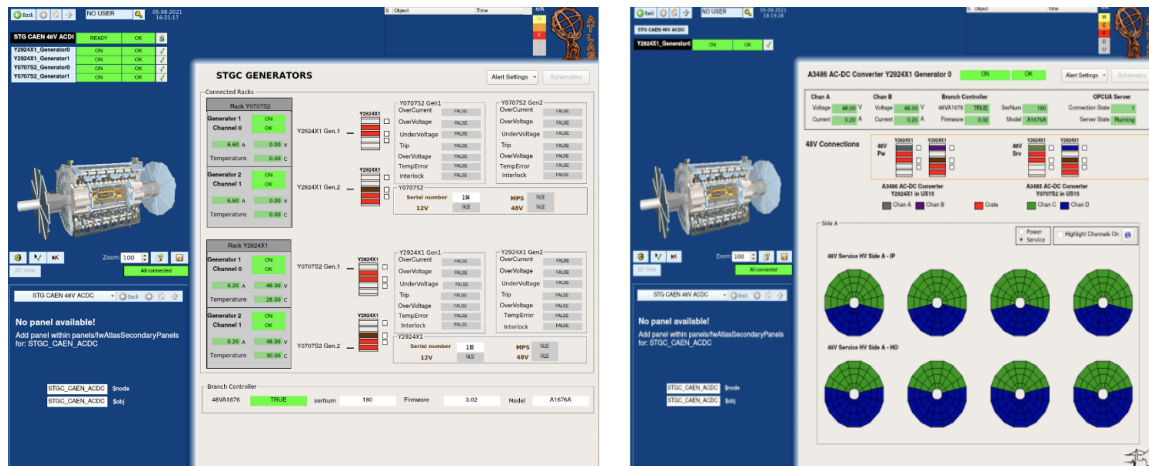


Figure 4. On the left is Main STG generator FSM Panel. On the right Main FSM panel for every individual generator.

5. NSW Reset Network

The CAEN Reset Network was implemented to provide a remote reset during periods without or limited access during beam mode were an actual incident might arise or a clean restart is needed to establish a glitch on power or even communication level. Similarly to the legacy systems, the NSW is using the same logic via the Agilent circuitry [10]. Due to the limitation of the lines in such module, the NSW took some lines from the legacy systems, one from the retired Cathode Strip Chambers (CSC) system, one from the Monitored Drift Tubes (MDT) and one line from the Resistive Plate Chambers (RPC). There the multiplexing of some signals performed in order to include all the hardware of the NSW for both technologies and both board types (LV and HV). A cable is the going from each branch controller to the Agilent module at USA15, where the presence or absence of the 50 Ohm resistor is emulated by a DCS controllable piece of electronics. The Reset Network allows to perform a simultaneous reset of the CAEN mainframes and the branch controllers individually. The MMG FSM has only the mainframe node, shown in Figure 5, where with the “one click” mechanism the expert can reset all the associated to this line mainframes. Unfortunately, due to the limited numbers of lines in the Agilent module, this action will affect all the mainframes of the MMG system for both sides, and thus the expert has to be very careful, communicating to all the affected systems such action in advance.

Similarly to the MMG, the STG reset network has been developed. The possibility of resetting the mainframes of the STG or individually the branch controllers is available. However, the mechanism to independently reset a crate is under development. The FSM of the STG follows explicitly the hardware structure, consisting of two nodes, one for the branch controllers and one for the mainframes as depicted in Figure 6 and 7, respectively. By right clicking the branch controller object element (green circle) the user can perform the following actions:

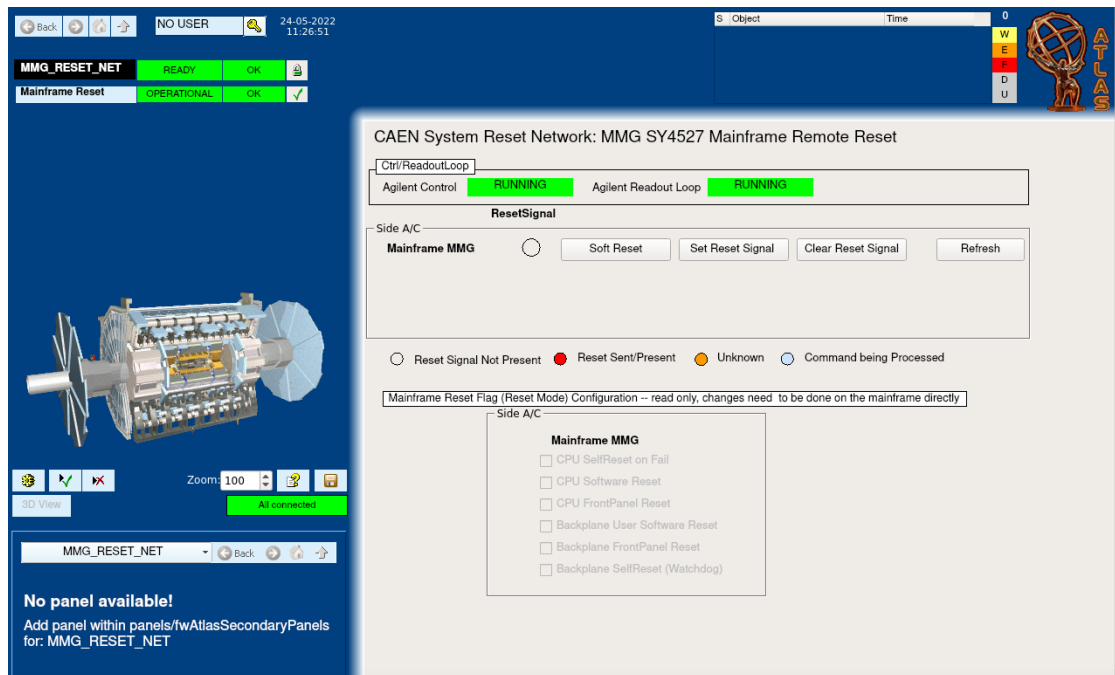


Figure 5. Main panel for MMG Reset Network FSM.

- ENABLE DCS CTRL - Enables reset functionality for this line.
- DISABLE DCS CTRL - Disables reset functionality for this line.
- RESET - Perform the reset for the connected branch controller.
- GET STATUS - Reread the status of the line.
- CANCEL - Abort doing anything on this line.

The STG mainframe Reset panel connects the STG HV with the STG and MMG LV and can be operated by the following actions :

- **Soft Reset:** Reset signal to the mainframe's front-panel reset input is shorter than 1 second, equivalent to shortly depressing the front-panel reset button. A soft reset acts on parts of the mainframe only, as defined in the "Reset Flag" configuration. A soft reset is used to reboot the mainframe CPU without affecting the back plane, i.e. without turning any EASY boards nor any LV/HV channels off.
- **Hard Reset:** This is a full reset, which will turn off all boards and channels controlled of the mainframe. A hard reset occurs if the reset signal is longer than 3 seconds in duration or equivalently, if the reset button is pressed for more than 3 seconds.

The NSW Reset Tree has been tested successfully validating at the same time the mapping of all the NSW Agilent lines between the mainframes and branches of both HV and LV of the systems.

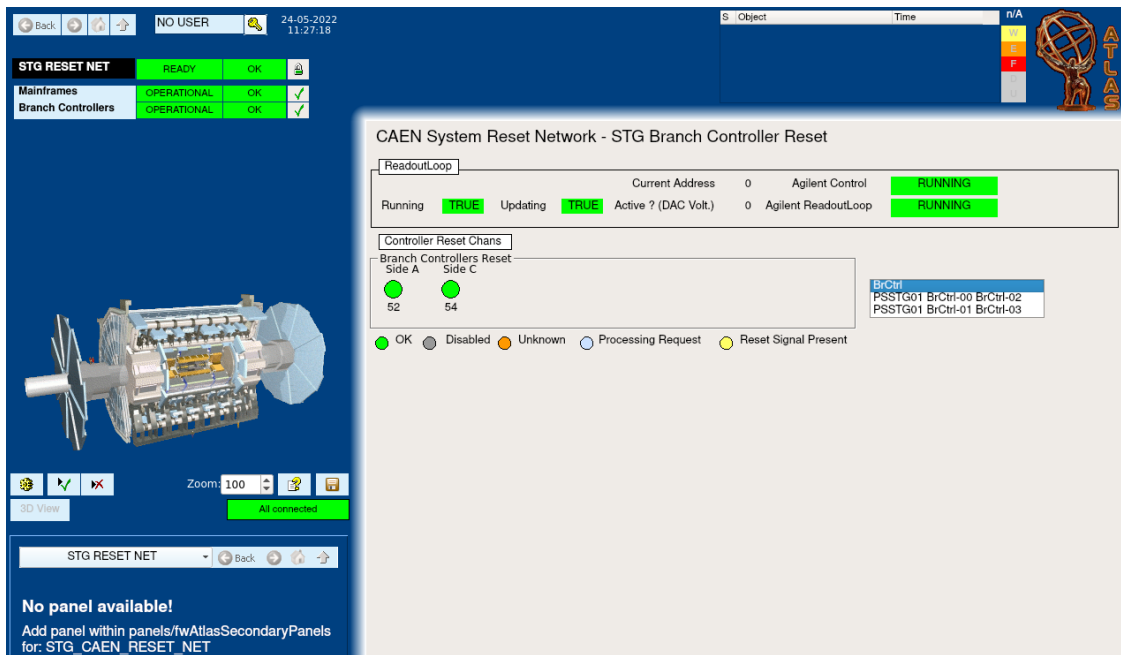


Figure 6. Main panel for STG Reset Network FSM, for controlling the branches.

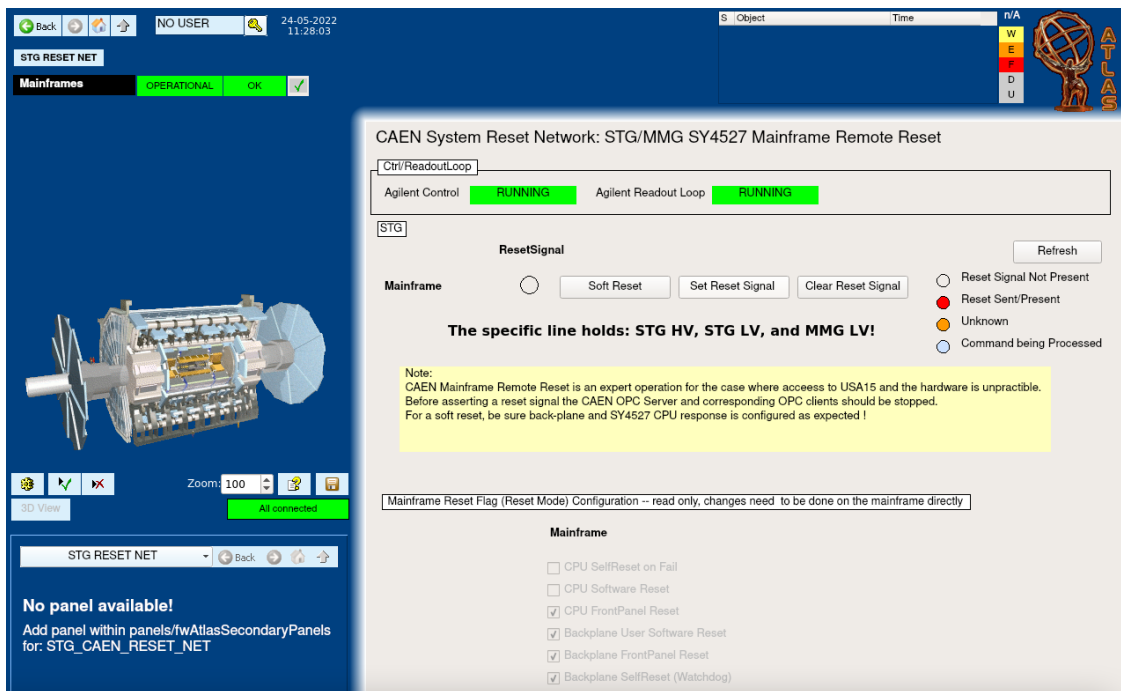


Figure 7. Main panel for STG Reset Network FSM, for controlling the Mainframes

Acknowledgments

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