THE MAGNET POWER SUPPLY FOR PAL-XFEL*

K. H. Park#, Y. G. Jung, D. E. Kim, H. S. Suh, H. G. Lee, S. B. Lee and I. S. Ko.
PAL, POSTECH, Pohang, Korea
W. S. Choi and M.J. Kim. POSTECH, Pohang, Korea

Abstract

A magnet power supply (MPS) for PAL-XFEL was developed, which is the bipolar type with the power capacity of 3.6 KW. The MPS has been implemented by the digital signal processing technology using the DSP, FPGA, ADCs and so on. An embedded module was adapted for the Ethernet connection for EPCIS. The output current stability of the MPS showed about 10 ppm peak-to-peak in long term experiment. The measured accuracy was less than 10 ppm in full range. The other experimental results such as repeatability and zero-cross response were given in this paper.

INTRODUCTION

The Pohang Accelerator Laboratory (PAL) has been carrying out the PAL-XFEL construction project since 2011. It generates 0.1 nm hard X-ray FEL using the 10 GeV S-band linear accelerator [1]. The layout of the linear accelerator was figured hard X-ray and soft X-ray beam lines as well as undulator lines.

The PAL-XFEL accelerator needs many kinds of magnet power supply (MPS). The MPSs are nowadays developed by the digital technologies using digital signal processor (DSP), FPGA, ADC and so on. The DSP was primarily optimised for the various digital signal processing with the fast calculation time such as feedback control, digital filters, stand alone controller etc. And it includes many hardware functions to make it easy to interface the peripheral devices through the SPI, CAN, RS232C, I2C, ADCs etc. Thus the application areas of the DSP increased sharply in the various targets, especially in power conversion systems – high stable power supply, UPS, inverter, etc. The table 1 shows the simple summary of the MPSs required to the PASL-XFEL. There are all switch-mode power supplies except for the quite small power capacity which is less than 10 W for corrector magnets. This will be provided with linear type.

Table 1: MPSs for the PAL-XFEL Accelerator

Magnet	MPS Type	Number	Stability(ppm)
Corrector	Bipolar	424	50
Quadrupole	Unipolar	122	100
	Bipolar	96	
Dipole	Unipolar	24	20
Solenoid	Bipolar	3	100

In this paper, we present the design schemes and experimental results of the high stabile MPS of the PAL-XFEL project.

SYSTEM CONFIGURATION

The system configuration of the designed MPS was similar with others [2]. The input stage was the full rectifier circuits for the delta-wye transformer windings in series of a damped low pass filter. The bandwidth of the input filter should be less than 30 Hz to have a good output performance. The output stage was composed of the H-bridge topology by the four IGBTs with a low pass filter to remove the switching noise, thus it made the output current stable. The gate drivers were isolated to the control circuits by the photo couplers in order to decouple the switching noise influence.

The DSP TMS320F28335 from TI Co was adapted to control the overall power supply system. It has six enhanced PWM modules with 150 ps micro edge positioning [3]. The effective PWM resolutions were increased up to about 18-bit in case of PWM frequency of 20 KHz. The normal PWM resolution is about 13-bit, which does not offer sufficient resolution for the high stability of ~10 ppm to the required MPS. Figure 1 showed the DSP board which was assembled with DSP, FGPA, uC5282 module and other components.

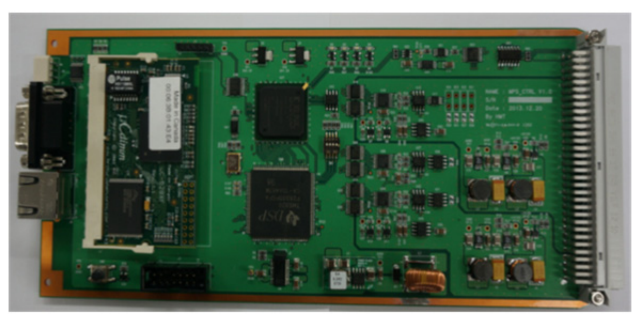

Figure 1: DSP Board that includes DSP, FPGA, ADCs and the other components.

The uC5282 embedded microprocessor module from Arcturus Co. was assembled into the DSP board to support Ethernet.

The output current was measured using DCCT MACC150 from HITEC. This DCCT has features followings: 1) offset error : < 5 ppm, 2) temperature ratio error : < 2 ppm/ºC, and 3) linearity error : < 10 ppm. Its current output was translated to voltage by the burden resistor which also has small temperature coefficient.

Four ADCs are assembled to measure the output current, output voltage, link voltage and so on. The oversampling method was applied to increase the

* Work supported by Ministry of Science, ICT & Future Planning
# pkh@postech.ac.kr

effective bit resolution of the ADC [3]. Oversampling methods for Analog-to-Digital Converters are based on sampling an analog signal at a higher rate, filtering and reducing the sampling rate to the designated frequency depending on the control loop. In an oversample factor of k, quantization noise will be reduced by the factor of k. Since the signal within the given bandwidth is not affected by the filter, this leads to an enhancement of the signal-to-noise ratio (SNR). The formula for the improved SNR is given as following,

$$SNR[dB] \cong 6.02N + 1.76 + 10\log_{10}(k)$$

This leads to improvement of SNR as following table.

Table 2: Oversampling Effectiveness

Factor k	SNR in dB	Extra bits
8	9	1.5

The ADCs are interfaced by the XC3S400 FPGA from the Xilinx Co, which generated SPI control signals for the ADC. The FPGA processed the ADC data and make them ready state to pass to the DSP whenever requested.

The control loops for the designed MPS were consisted of a cascaded current and voltage feedbacks, The inner loop controls the output voltage, and the outer loop controls the output current[4]. The control loops were executed at every PWM switching frequency. The PI compensator was described as following:

$$u(t) = K_p e(t) + K_I \int_0^t e(t)dt$$

where, $e(t)$ is error coming from difference between reference and output signal, K_P and K_I are the proportional and integration gain, respectively. The block diagram of the discrete PI controller was shown in Fig. 2.

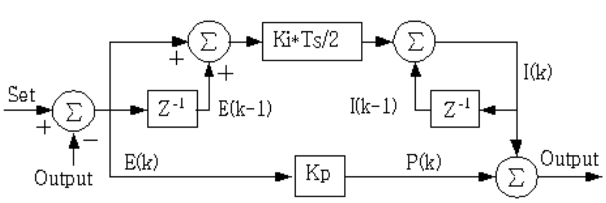

Figure 2: Discrete PI controller block diagram.

Discrete time difference equation for the PI controller :

$$I(k) = (E(k) + E(K-1)) * Ki * Ts / 2 + I(k-1)$$
$$P(k) = Kp * E(k)$$

The output filter with magnet load was simply modelled as Fig. 3, where the R1 and L1 were equivalent circuits for magnetic load, and C2, R2 and L3 for filter construction. The output filter was recommended to have the parallel damped type with condition of $C_2 = 4C_3$ [5].

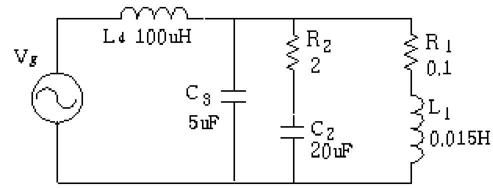

Figure 3: The modelling of the output filter with a magnet load.

The Fig. 4 showed the frequency responses of the output filter with the equivalent magnet load. The cut-off frequency was about 5 KHz. It gives a good dynamic control performance. Two stage output filters were usually adapted in the high stable MPS. But the second filter which had a slightly higher cut-off frequency than that of the first stage was eliminated here, because its effect was not as effective as generally known.

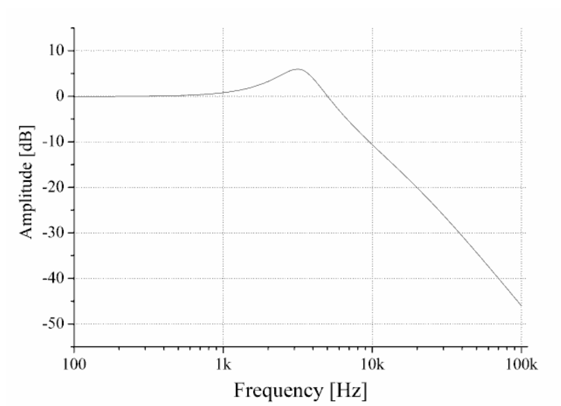

Figure 4: Frequency responses of the output filter with the magnet load.

The whole MPS circuits model including both IGBT switching parts and filter circuits was simulated using the PSIM and its result was shown in Fig. 5. The rising time is less than 40 ms at the magnet load. The full link voltage was applied to the magnet during the rising time and it reduced to DC voltage drop after reaching to steady state.

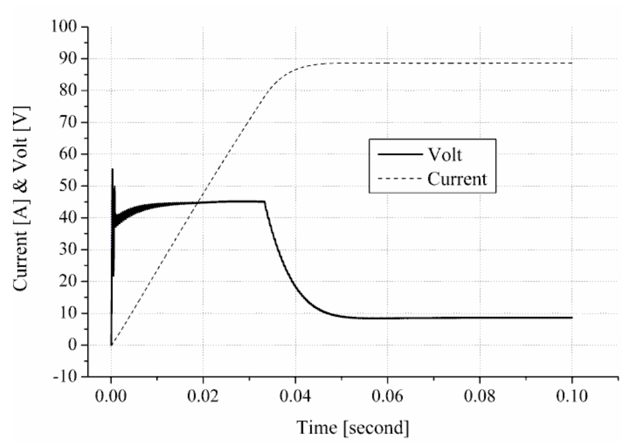

Figure 5: Current output signal simulated by the PSIM to the output filters and a magnet load.

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EXPERIMENTAL RESULTS

Various performances of the MPS were examined. Functions like interlock signal processing, Ethernet & RS232C communication, CSS and so on were tested to this MPS. This MPS included the small web-server to make easy maintenance. The major specifications of the MPS were strictly examined such as short term, step responses at the ring and falling times. The accuracy difference between set and read-back data was measured and the repeatability performance was tested which showed the good results. The long term test results for eight hours with the magnet load was shown in Fig. 6, which was shown the stability less than 10 ppm at the output current of 90 A.

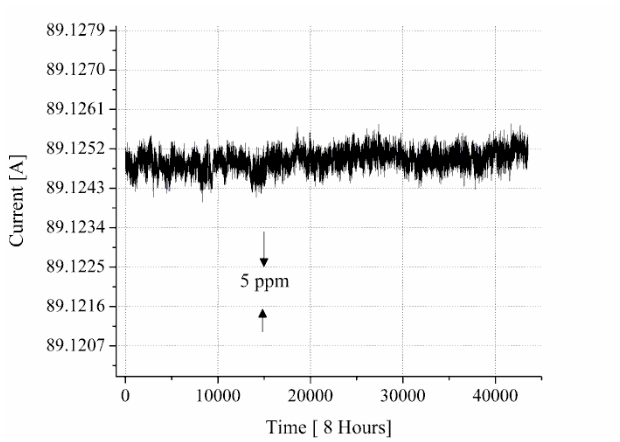

Figure 6: Test results of the long term stability.

Figure 7 shows that the accuracy of the MPS. The differences between set and read-back current were drawn from -90 A to 90 A. It showed less than 10 ppm in full output range.

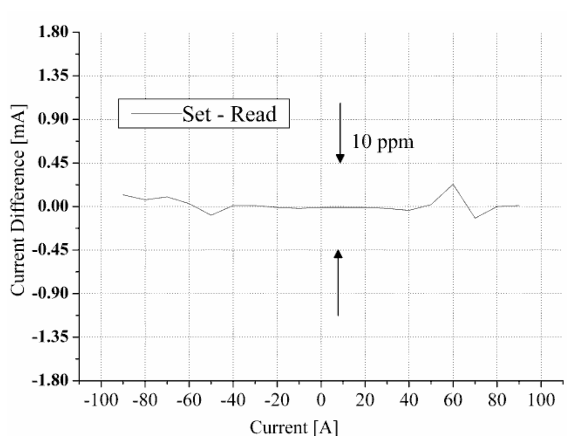

Figure 7: Current difference between set and read-back.

The zero cross response of the MPS was also shown in Fig. 8. When the set current was increased with 5 ppm step from 0.0035 A to -0,0035 A, the MPS showed a good output responses when it crossed the about zero output current.

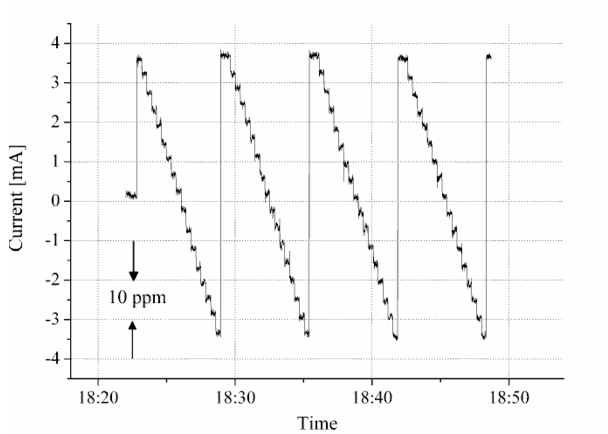

Figure 8: Test results of the zero cross responses.

The repeatability of the MPS was measured. The current was set to 70 A and 5 A with 5 times. It showed that the setting repeatability was within 5 ppm as shown in Fig. 9.

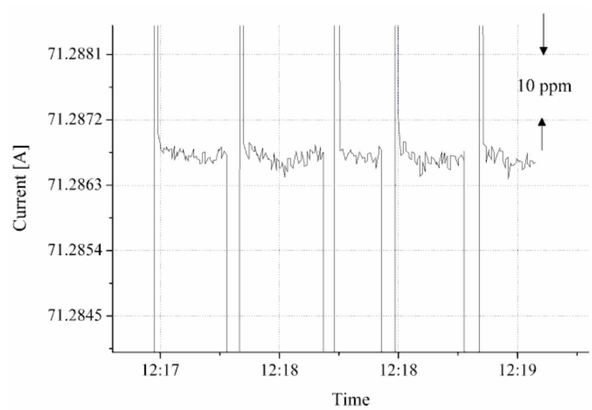

Figure 9: Test results of the repeatability of the MPS.

CONCLUSIONS

This paper described the bipolar power supply for the XFEL dipole magnet. The digital controller for the MPS assembled with a DSP, uC5282 embedded module, FPGA, ADCs and the other analogue and digital circuits. The two control loops in series for the load voltage and the current were implemented. The input stage was assembled by the delta-wye transformer windings, full rectifier circuits and input filter. The output filter was designed and simulated using the PSPICE. The bandwidth of the filter and PI coefficients were decided to have good output stability and step response.

The experimental results with the assembled MPS showed the high stability. The long term stability for eight hours was about 10 ppm and the short term also was less than 10 ppm. The zero cross response of the MPS showed that there was no non-linearity section when crossed the zero output region. The measured accuracy showed less than 10 ppm in the full output range. The repeatability of the MPS was also tested, and it also showed less than 10 ppm.

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