Published by IOP Publishing for Sissa Medialab

Received: *September 28, 2024*
Revised: *December 18, 2024*
Accepted: *January 2, 2025*
Published: *April 2, 2025*

25th International Workshop on Radiation Imaging Detectors
Lisbon, Portugal
30 June – 4 July 2024

Functional tests of the detector assembly demonstration model of the eXTP wide field monitor: system description and results

M. Antonelli,[a,*] **G. Zampa**,[a] **V. Bonvicini**,[a] **D. Cirrincione**,[a] **G. Orzan**,[a] **A. Rachevski**,[a] **I. Rashevskaya**,[i] **N. Zampa**,[a] **G. Aitink-Kroes**,[b] **R. de la Rie**,[b] **J.J.M. in 't Zand**,[b] **P. Laubert**,[b] **F. Zwart**,[b] **R. Tacken**,[c] **F. Ceraudo**,[d] **G. Della Casa**,[d] **Y. Evangelista**,[d] **M. Feroci**,[d] **J.-L. Gálvez**,[e,f] **M. Hernanz**,[e,f] **D. Baudin**,[g] **A. Meuris**,[j] **P. Bellutti**,[h,i] **G. Borghi**,[k] **M. Centis Vignali**,[h,i] **E. Demenev**,[h,i] **F. Ficorella**,[h,i] **G. Pepponi**,[h,i] **A. Picciotto**,[h,i] **A. Samusenko**[h,i] **and N. Zorzi**[h,i]

[a] *INFN Trieste, via A. Valerio 2, Trieste, 34127, Italy*
[b] *SRON Netherlands Institute for Space Research, Niels Bohrweg 4, 2333 CA Leiden, Netherlands*
[c] *Neways Electronics International B.V., P.O. Box 100, 5690 AB Son, Netherlands*
[d] *INAF/IAPS, Via del Fosso del Cavaliere 100, Roma, 00133, Italy*
[e] *Institute of Space Sciences (ICE-CSIC), Carrer de can Magrans, s/n, Campus UAB, Cerdanyola del Vallès (Barcelona), 08193, Spain*
[f] *Institut d'Estudis Espacials de Catalunya (IEEC), Barcelona, Spain*
[g] *IRFU, CEA, Université Paris-Saclay, Gif-sur-Yvette, 91191, France*
[h] *Fondazione Bruno Kessler, Via Sommarive 18, Trento, 38123, Italy*
[i] *TIFPA-INFN, Via Sommarive 14, Trento, 38123, Italy*
[j] *Université Paris-Saclay, Université Paris Cité, CEA, CNRS, AIM, 91191, Gif-sur-Yvette, France*
[k] *Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Milan, 20133, Italy*

E-mail: matias.antonelli@ts.infn.it

Abstract: The Wide Field Monitor is one of the 4 state-of-the-art instruments onboard the enhanced X-ray Timing and Polarimetry mission, which will search for and observe neutron stars, magnetars and black holes to study matter under extreme conditions of density, gravity and magnetism. The wide-field cameras of the Wide Field Monitor are based on large-area silicon drift detectors. Such position-sensitive spectroscopic detectors, together with their front-end electronics, must pass a series of functional tests before proceeding with the mass production of the detector assemblies. This paper describes the test system developed to carry out such measurements, as well as reporting the results of the functional tests together with a preliminary characterisation of the performance of the detector assemblies.

Keywords: X-ray detectors and telescopes; Front-end electronics for detector readout; On-board space electronics; Control and monitor systems online

*Corresponding author.

https://doi.org/10.1088/1748-0221/20/04/C04010

2025 JINST 20 C04010

Contents

1 **Introduction** 1

2 **WFM detector assembly** 2

3 **Test system** 3

4 **Results and discussion** 4

5 **Conclusions** 7

2025 JINST 20 C04010

1 Introduction

The enhanced X-ray Timing and Polarimetry mission (eXTP)[1] is a scientific space mission aimed at studying the behaviour of matter under extreme conditions that cannot be attained on Earth. In particular, the main objectives are the study of matter in ultra-dense conditions, the physics and astrophysics of strong magnetic fields, and the physics of accretion in the strong-field limit of gravity. These objectives will be achieved through searching for and observing some primary targets such as neutron stars, magnetars and black holes [1–3]. To that end, the eXTP satellite will be equipped with an unprecedented suite of state-of-the-art instruments enabling the simultaneous spectral-timing-polarimetry studies of cosmic sources in the energy range from 0.5 to 30 keV and beyond.

The payload includes four instruments (figure 1): the Spectroscopic Focusing Array (SFA), i.e. a set of 9 co-aligned focusing X-ray telescopes with a small array of Silicon Drift Detectors (SDDs) at their focus, with an effective area (dependent on photon energy) reaching a maximum of about 0.8 m^2 at 2 keV and a FWHM spectral resolution better than 180 eV at 6 keV; the Large Area Detector (LAD), i.e. a set of 640 large-area SDDs, combining to an energy-dependent effective area with a maximum of 3.4 m^2 at 8 keV and achieving an energy resolution of 200 eV at 6 keV [4]; the Polarimetry Focusing Array (PFA), consisting of 4 focusing X-ray telescopes based on gas pixel detectors with an energy resolution better than 25% at 6 keV and polarimetric capabilities; finally, a set of 3 coded-mask, wide-field-of-view camera pairs based on position-sensitive SDDs called Wide Field Monitor (WFM) [5, 6].

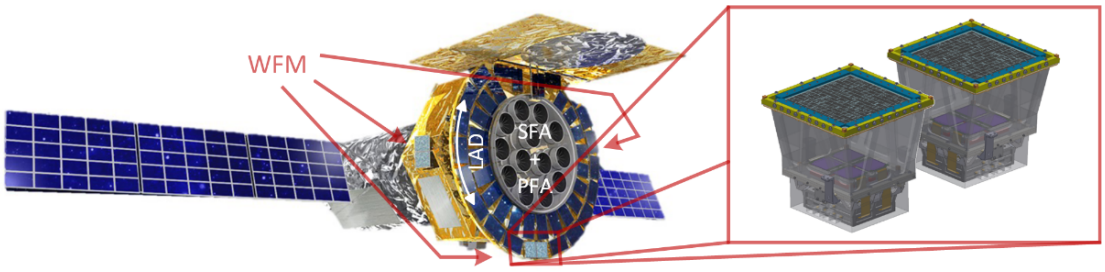

Figure 1. Depiction of the eXTP concept satellite, with a magnified view of a camera pair of the WFM (right inset).

[1] In the course of the process for the final mission adoption of the enhanced X-ray Timing and Polarimetry mission, the Chinese Academy of Sciences required the removal of all programmatic uncertainties for the mission implementation, the largest residing in securing the European provision of the Large Area Detector and the Wide Field Monitor payloads. As a result, these two payloads are now optional instruments for such mission, which at the time of submitting this paper only includes the Spectroscopic Focusing Array and the Polarimetry Focusing Array. The study reported here is based on the work carried out on the Wide Field Monitor for the original payload, as presented at iWoRiD 2024 in the previous operational framework.

The main purpose of the WFM is to detect new X-ray transients and known X-ray sources undergoing spectral state changes, allowing for follow-up observations with the other pointing instruments of eXTP. Therefore, the WFM is designed to cover, in a single observation, a portion of the sky of about 3.7 sr with a 1-day sensitivity of 4 mCrab in the 2–50 keV range.

As will be explained in more detail later, the WFM consists of 3 pairs of coded-mask cameras, each having 4 Detector Assemblies (DAs). Each DA hosts a large-area SDD featuring two drift regions each having 384 anodes, whose readout is performed by twenty-four 32-channel Application-Specific Integrated Circuits (ASICs) mounted on the Front-End Electronics (FEE) Printed Circuit Board (PCB). The DAs are then controlled by the so-called Back-End Electronics (BEE).

Before proceeding with the mass production of these cameras, a number of DA Demonstration Models (DMs) must pass a series of reduced and full functional tests aimed at qualifying the design and the assembly procedures by operating the DA DMs through test electronics. Therefore, a dedicated, yet versatile, test system has been developed, which can be connected to the DA DMs and operated from a Personal Computer (PC).

The Electrical Ground Support Equipment (EGSE) that acts as a test BEE consists of a mixed-signal Interface Board (IB), a Field-Programmable Gate Array (FPGA) board for control and communication, and a PC software (SW) with a Graphical User Interface (GUI). This system enables the detector developers to efficiently perform series of tests on the DA DMs and to collect and analyse several types of data through its convenient GUI.

This paper will continue with a section dedicated to the components of the DA, followed by another one providing a detailed description of the EGSE developed for the functional tests of the DA DMs. A final section will report the main results of such tests together with some preliminary performance characterisation.

2 WFM detector assembly

As mentioned above, the WFM consists of 3 pairs of coded-mask cameras (figure 1), each having 4 DAs (figure 2, left part) with the SDDs oriented orthogonally to those in the accompanying camera in the same pair, achieving a FWHM angular resolution better than 4.3 arcmin and an energy resolution better than 500 eV at 6 keV. Each DA mounts a detector on its FEE PCB (made of Al_2O_3 to improve the matching of the thermal expansion coefficient with the Silicon detector thus minimising thermal distortions), forming the so-called sandwich (figure 2, central part), and a mechanical/thermal interface attached to the sandwich, allowing for cooling and fine positioning of the whole DA [7].

The detector is a large-area SDD whose active volume is divided in two halves featuring 384 anodes each, with a pitch of 169 µm, for a total effective area of 6.50×7.00 cm^2 (figure 2, right part). This technology [8, 9] is characterised by a fine spatial resolution in one direction and a coarse resolution in the orthogonal one. In fact, one coordinate of the incident photon can be obtained directly from the centroid of the anode readout, while the other (the coarse one) is estimated from the charge spread over the anodes. This is also the reason for the orthogonal arrangement of the DAs in each camera pair.

The readout of the 768 anodes of the SDD is carried out by twenty-four 32-channel ASICs (the so-called IDeF-X [10]), which are mounted on the FEE and connected via wire-bonding. The DA is then connected to the BEE (or to the IB of the EGSE, in the case of the DA DM) through a rigid-flex PCB by means of two high-density 100 pin Z-ray interposers, and to the high- and mid-voltage power supplies through coaxial cables.

2025 JINST 20 C04010

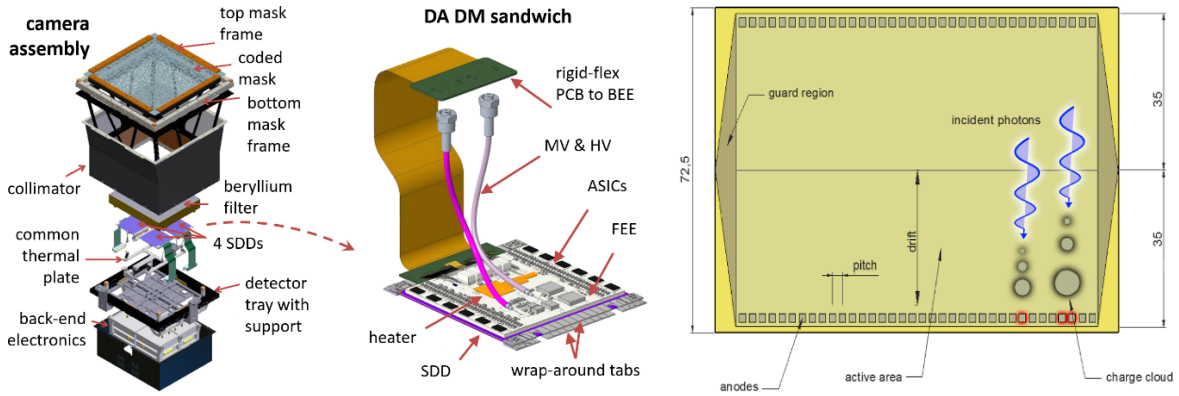

Figure 2. Breakdown of the modules of the WFM: left part, a single camera assembly; central part, the sandwich of the DA DM; right part, the layout of the large-area SDD.

3 Test system

In order to verify their functionality, the DA DMs have to be operated by a test BEE. The EGSE developed for this purpose makes it possible to configure and control each component of the FEE, as well as acquiring analogue and digital data related to the behaviour and the performance of the SDD and the FEE itself.

Analysing the acquisition chain as depicted in figure 3, the first element downstream from the FEE is the aforementioned IB. This board embeds a number of different analogue and digital sections to fully operate and characterise the DA DM. It is equipped with several signal-conditioning stages for buffering, level shifting, gain adjustment, impedance matching and differential-to-single-ended conversion. Four 8-channel, 1.5-Msps, 16-bit Analogue-to-Digital Converters (ADCs) enable the simultaneous acquisition of the analogue output of the 24 ASICs together with those of temperature and power-consumption monitors. A 12-bit Digital-to-Analogue Converter (DAC)-based pulser allows a test charge to be injected into the ASIC preamplifiers, to simulate detector signals and assess the response of each input channel. The IB also hosts a Pulse Width Modulation (PWM) driver for the FEE heater, plus voltage regulators and ancillary electronics to ensure the proper power supply of some FEE components and of the IB itself. It is worth mentioning that this board can be connected to both the FEE and an auxiliary setup, which is particularly convenient for preliminary testing and debugging while the DAs are under production.

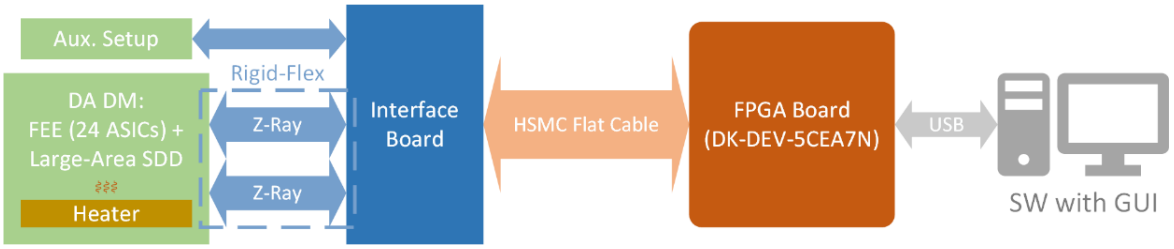

Figure 3. Block diagram of the test system connected to the DA DM (and to the auxiliary setup).

The FPGA board is connected to the IB through an HSMC cable and to a PC via USB. This arrangement allows for testing the mixed-signal interface of the EGSE and the DA DM enclosed together in a climatic chamber while the FPGA is at some distance. The FPGA runs a rather complex

2025 JINST 20 C04010

firmware (FW) that performs the continuous low-level control of the IB and the FEE, as well as acquiring and transmitting the data to the PC. More specifically, the FW is responsible for the control of the test injections, for the FEE temperature regulation (with a Proportional-Integral-Derivative controller driving the PWM section of the IB), for the communication with the ASICs and for the control of the ADCs.

The PC SW comes with a fully featured GUI which allows the user to program the entire set of 24 ASICs of the DA and to carry out tests on them, while constantly checking the status of the system. In more detail, the SW enables the user to set all the parameters and the operating modes of the ASICs, such as peaking time, threshold, test injection and acquisition mode; then, it can test the DA DM either with clocked acquisitions (sweeping either the pulser amplitude or the peak-holder delay) or with X-ray acquisitions, waiting for SDD events. Furthermore, the SW keeps FEE temperatures, currents and voltages under continuous surveillance, as well as checking the single-event-upset alarm of the ASICs.

The measurements can be performed either as single tasks (e.g. pulser-amplitude sweeping) or as specific automated test sequences, which make it possible to collect several types of data with a single user action. More precisely, such automated sequences measure four important quantities for each channel of the ASICs, namely, the response pedestal, the Equivalent Noise Charge (ENC), the response linearity and the triggering threshold. These procedures have been used to collect most of the data presented in the next section.

4 Results and discussion

The EGSE has successfully carried out all the operations it had been developed for. As a first step, the functional tests have verified the full operability of the ASICs as well as the compliance of a series of measurements related to bias and power consumption. It must be pointed out that, owing to the limited availability of some crucial components (ASICs and FEE boards) in this pre-mass-production stage, only two DA DMs have been assembled (labelled DA_DM_04 and _05, respectively), each mounting 3 of the 24 ASICs in just as many significant positions on the FEE. Nonetheless, the EGSE has tested all the required features as it had been designed to cope with any number of missing elements.

The main results of these compliance tests are summarised in table 1. It is important to note that the values reported for DA_DM_04 refer to the assembly either before or after the SDD had been mounted on the FEE. On the other hand, DA_DM_05 has been partially tested only without its SDD, since, after mounting the detector, an electrical issue in the PCB of the sandwich prevented the second series of measurements to be completed. Nevertheless, this DA DM is still available for further tests of its electronics not directly involving the SDD.

The results reported in table 1 are all compliant with the expected or required values, the only exception being the ASIC power consumption per channel in the case of DA_DM_04 with the SDD. This overrun of the limit imposed by the mission will be addressed with the future optimisations of the ASIC for eXTP. In any case, in the current stage of the WFM development, such slight excess will not prevent that assembly from undergoing the next phases of the qualification tests and providing relevant results.

A note should be made also about the High-Voltage (HV) power consumption of DA_DM_04 (marked with an asterisk). Its value is well below the required limit; however, it has been measured at room temperature (in this case, 27.4 °C), but the requirement must be met at a temperature of −26 °C, at which such consumption is estimated to be about 57.5 mW.

2025 JINST 20 C04010

Table 1. Results of the functional test of the DA DMs (at room temperature).

feature	expected/required result	DA_DM_04 result w/o SDD	DA_DM_04 result with SDD	DA_DM_05 result w/o SDD
mid-voltage bias current	$\geq 21.58\,\mu A$ $\leq 22.02\,\mu A$	NA	22.00 µA	NA
HV power consumption	≤ 56 mW	NA	37.7 mW*	NA
ASIC power consumption/ch.	≤ 1 mW	0.94 mW	**1.03 mW**	0.98 mW
ASIC operability	OK	OK	OK	OK
temperature sensor resistance	$\geq 1058\,\Omega$ $\leq 1117\,\Omega$	1102 Ω	1102 Ω	1105 Ω
heater resistance	$\geq 17.8\,\Omega$ $\leq 23.1\,\Omega$	22.6 Ω	22.6 Ω	18.8 Ω

In addition to the results just listed, thanks to the SW procedures mentioned in section 3, a preliminary characterisation of the performance of the DA DMs has been obtained with this EGSE. For the sake of brevity and clarity, only the results of DA_DM_04 will be reported here. Indeed, they are also representative of other DA DMs, since the measured values do not deviate significantly from those of DA_DM_05, except for those specific parts of the tests that do not apply to DAs without the SDD.

The linearity of the ASIC response has been assessed by sweeping the pulser amplitude for each peaking time available in the shapers of the ASIC. The top part of figure 4 shows that response for 2 channels of each ASIC, for the minimum and the maximum peaking times (τ_p), respectively.

By calculating the slope and the intercept of the lines interpolating these data it is possible to estimate the gain of each channel (figure 4, bottom left part) and its true output pedestal, respectively (the ASIC channels use peak detectors whose minimum output corresponds to the noise peak value when no signal is injected). The ASIC gains obtained from this procedure are in line with the design specification of 200 mV/fC.

The pedestals have been measured also with their dedicated SW procedure, obtaining the results reported in the bottom right graph of figure 4. Since these values are shifted by the peak noise around the true pedestal, they can be compared with those extrapolated from the linearity data to have a cross-check estimation of the ENC.

The results of the dedicated ENC measurement for DA_DM_04 are reported in figure 5 for both the case with the SDD and that without it. It can be clearly seen that the presence of the detector adds a parallel-noise component, as expected. In such conditions the minimum ENC is of about 30 electrons rms, which is again in line with the expected performance for this preliminary version of the ASIC that is not yet complying with the WFM specifications. In the figure the ENC of the DA before the installation of the SDD is higher than after the assembly of the sensor in the peaking time range between 2 and 4 µs: this is due to ambient noise being captured by the ASIC inputs that could not be shielded properly during the test.

2025 JINST 20 C04010

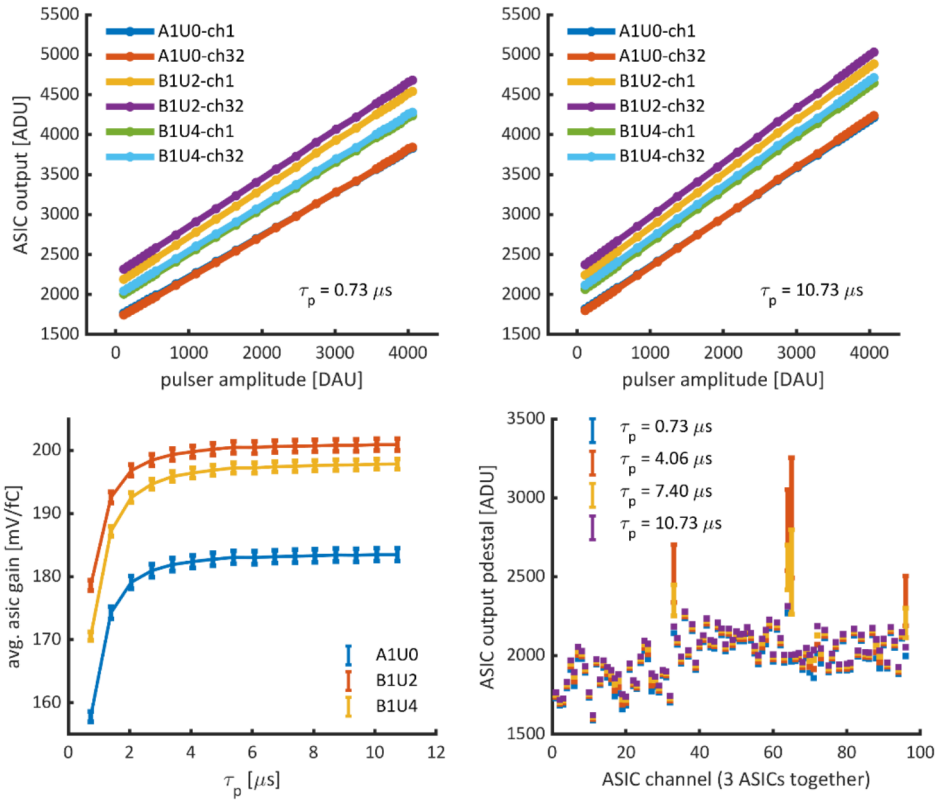

Figure 4. Automated linearity measurements for DA_DM_04 for minimum and maximum τ_p (top graphs), in ADC Units (ADU) vs DAC Units (DAU). Average ASIC gain as a function of τ_p (bottom left) and output pedestal of each channel for 4 different peaking times (bottom right), both for DA_DM_04.

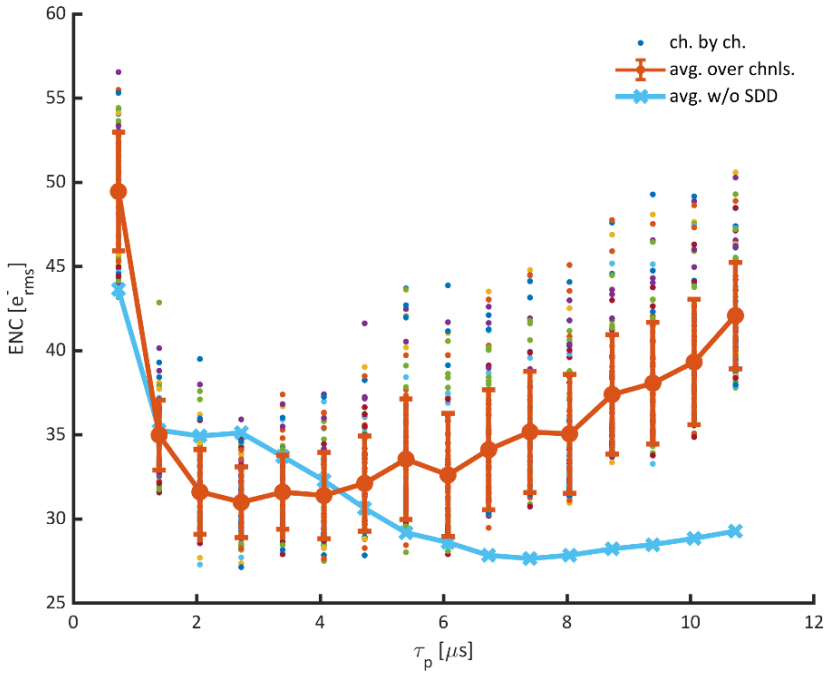

Figure 5. Equivalent noise charge of DA_DM_04 as a function of peaking time, for the case with the SDD (the red line with error bars refers to the average over all channels and each coloured dot represents a channel) and for that without the detector (the blue line with x markers is the average over all channels).

2025 JINST 20 C04010

Finally, the automated threshold test provides yet another way to verify the ENC measurement. Such procedure estimates the triggering probability of every threshold available in the ASIC by repeatedly checking the trigger interrupt while stepping through each threshold value. Once the thresholds are calibrated, the deviation of the distribution obtained in this way can be used as an estimation of the ENC.

5 Conclusions

The system presented in this paper, namely the EGSE, has been developed for the functional tests of the DA DMs of the WFM for the eXTP mission. The EGSE has worked successfully, allowing the users to operate the FEE of 2 DA DMs and to carry out the required tests on them.

The results obtained with DA_DM_04 meet all the requirements for this phase, with the only exception of the power consumption per channel of the ASICs, exceeding the limit specified for the mission by 3%. DA_DM_05 has produced similar results, meeting all the requirements in those parts of the test that could be performed before mounting the SDD. In fact, as reported above, this DA DM could not be tested with a biased SDD because of an electric problem in its FEE.

The information gathered with all these measurements will be crucial for the qualification of the procedure to be adopted for the mass production of the DAs. In addition, the EGSE has been utilised to collect data on the performance of the ASIC; such results show values in line with its preliminary design objectives, in particular concerning the gain and the ENC.

The EGSE will be used for the next phases of the tests with DA_DM_04, which are about to begin; these will include acquisitions with the SDD under X-ray irradiation and operations at low temperature, with the assembly enclosed in a climatic chamber.

Given the results of these tests, the next version of the ASIC will address the slight excess of power while being optimised for this application in terms of both ENC and readout parallelisation. In the meanwhile, the FW of the EGSE might be upgraded to speed up the communication with the PC in view of the upcoming X-ray measurements.

References

[1] eXTP collaboration, *eXTP — enhanced X-ray Timing and Polarimetry Mission*, *Proc. SPIE* **9905** (2016) 99051Q [arXiv:1607.08823].

[2] eXTP collaboration, *The enhanced X-ray Timing and Polarimetry mission — eXTP*, *Sci. China Phys. Mech. Astron.* **62** (2019) 29502 [arXiv:1812.04020].

[3] eXTP website, https://www.isdc.unige.ch/extp/.

[4] M. Feroci et al., *The large area detector onboard the eXTP mission*, *Proc. SPIE* **12181** (2022) 121811X.

[5] M. Hernanz et al., *The wide field monitor onboard the Chinese-European x-ray mission eXTP*, *Proc. SPIE* **12181** (2022) 121811Y.

[6] M. Hernanz et al., *The Wide Field Monitor (WFM) of the China-Europe eXTP (enhanced X-ray Timing and Polarimetry) mission*, *Proc. SPIE* **13093** (2024) 130931 [arXiv:2411.03050].

[7] F. Zwart et al., *The detector/readout-electronics assembly of the eXTP wide field monitor*, *Proc. SPIE* **12181** (2022) 1218167.

2025 JINST 20 C04010

[8] A. Rachevski et al., *Large-area linear Silicon Drift Detector design for X-ray experiments*, 2014 *JINST* **9** P07014.

[9] ALICE collaboration, *Large area silicon drift detector for the ALICE experiment*, *Nucl. Instrum. Meth. A* **485** (2002) 54.

[10] D. Baudin et al., *IDeF-X HDBD: Low-Noise ASIC for Imaging Spectroscopy With Semiconductor Detectors in Space Science Applications*, *IEEE Trans. Nucl. Sci.* **69** (2022) 620.