Tests with beam setup of the TileCal phase-II upgrade electronics

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Tests with beam setup of the TileCal phase-II upgrade electronics

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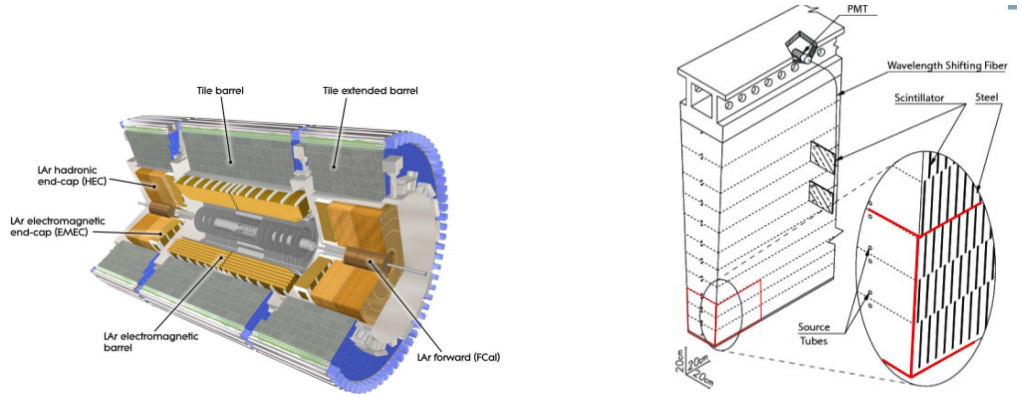
Abstract. The LHC has planned a series of upgrades culminating in the High Luminosity LHC which will have an average luminosity 5-7 times larger than the nominal Run-2 value. The ATLAS Tile calorimeter plans to introduce a new readout architecture by completely replacing the back-end and front-end electronics for the High Luminosity LHC. The photomultiplier signals will be fully digitized and transferred for every bunch crossing to the off-detector Tile PreProcessor. The Tile PreProcessor will further provide preprocessed digital data to the first level of trigger with improved spatial granularity and energy resolution in contrast to the current analog trigger signals. A single super-drawer module commissioned with the phase-II upgrade electronics is to be inserted into the real detector to evaluate and qualify the new readout and trigger concepts in the overall ATLAS data acquisition system. This new super-drawer, so-called hybrid Demonstrator, must provide analog trigger signals for backward compatibility with the current system. This Demonstrator drawer has been inserted into a Tile calorimeter module prototype to evaluate the performance in the lab. In parallel, one more module has been instrumented with two other front-end electronics options based on custom ASICs (QIE and FATALIC) which are under evaluation. These two modules together with three other modules composed of the current system electronics were exposed to different particles and energies in three test-beam campaigns during 2015 and 2016.

1. Introduction

The Large Hadron Collider (LHC) is a proton-proton collider with 14 TeV center of mass energy and design luminosity of $10^{34} cm^{-2} s^{-1}$ [1]. A series of upgrades culminating in the High Luminosity LHC (HL-LHC) have been planned which will result in an increased average luminosity 5-7 times larger than the nominal Run-2 value. The ATLAS detector (A Toroidal LHC Apparatus) [2] is one of the two general purpose particle detectors at the LHC, and it consists of multiple sub-detectors (Figure 1a) which are designed to detect interesting particle physics events in 40 million bunch-crossings per second [3]. The hadronic Tile Calorimeter (TileCal) is the central region of the ATLAS detector and is used to measure energies and directions of hadrons, jets, τ and leptons. Particles pass through the plastic scintillating tiles (Figure 1b) which emit light that is transferred to the photomultiplier tubes (PMTs). This provides the means to measure energy and direction of hadrons. These light signals are directed to the on-detector front-end (FE) electronics where they are converted to electrical signals and digitized, and then processed as first level (L0/L1) trigger events [4]. Data from the FE electronics is further transferred to the off-detector back-end (BE) for further processing and readout to permanent storage. The TileCal FE and BE will be completely redesigned to adopt a new readout strategy to adhere to the HL-LHC parameters [5]. A series of test-beam campaigns during 2015 and 2016 were performed to test and assess the performance of the new prototype electronics

for the phase-II upgrades. This article presents the firmware and software developed explicitly for the tests with beam setup and shows preliminary performance analysis for different types of particles and energies as well as for calibration data.



(a) ATLAS Calorimeter system (b) TileCal module

Figure 1: ATLAS Detector and a TileCal module.

2. TileCal Phase-II Upgrade

The LHC has envisaged a series of upgrades in the machine in order to reach the design center of mass energy ($\sqrt{s} = 14$ TeV) and to increase the peak luminosity up to 5 times the nominal value($\mathcal{L}_{peak} = 5$ x $10^{34} cm^{-2} s^{-1}$) in 2023. The TileCal detector components (absorber, scintillating tiles, fibers, and PMTs) are largely in good shape and do not have to be replaced. The readout electronics are to be completely redesigned to provide full-granularity digital data to the Level-0/1 triggers at 40 MHz. The present on-detector electronics are designed to output digital data at the maximum rate of about 100 kHz with the digital data stored on detector in a 6.4 μs long pipeline (Figure 2), and are basically not compatible with the HL-LHC TDAQ (Trigger and Data Acquisition) architecture [6]. Most of the components have aged (time & radiation) and some of them have even been discontinued. The main difference between the present and the upgrade readout architectures is that all the digital data is transmitted off-detector at 40 MHz (Figure 3). The data is pipelined and processed in the off-detector Tile PPr (PreProcessor).

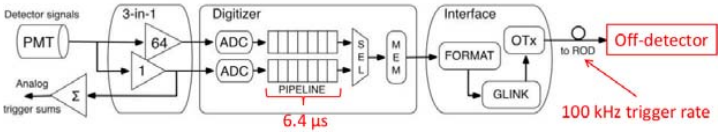


Figure 2: Current readout architecture.

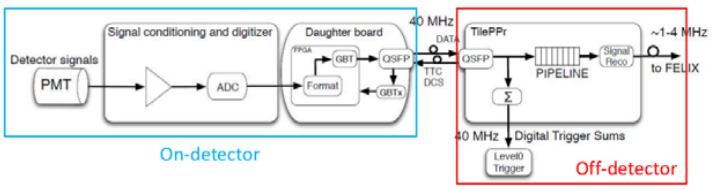


Figure 3: Upgrade readout architecture.

The Demonstrator project aims at testing the long term performance of the upgrade system without compromising the present data taking. This is to be achieved by adding to the upgrade design the analog trigger signal output. Digital transformation will translate TTC (Timing, Trigger and Control) signals into upgrade commands and translate upgrade outputs to a format acceptable by the present RODs (Read Out Drivers). The super-drawer Demonstrator module is composed of four independent mini-drawers (Figure 4), each of them are equipped with:

- 12 FE boards: 1 out of the 3 different options.
- 1 Main Board (MB): for the corresponding FE option.
- 1 Daughter-board (DB): single design.
- 1 HV (High Voltage) regulation board: 1 out of 2 options viz. Remote HV and HVOpto.
- 1 adder base board plus 3 adder cards for the summation of the analog trigger signals to send to the L0/1 event accept.
- New LVPS (Low Voltage Power Supply) architecture that provides redundancy and Point Of Load regulators - LVPS v.8.01 [7].

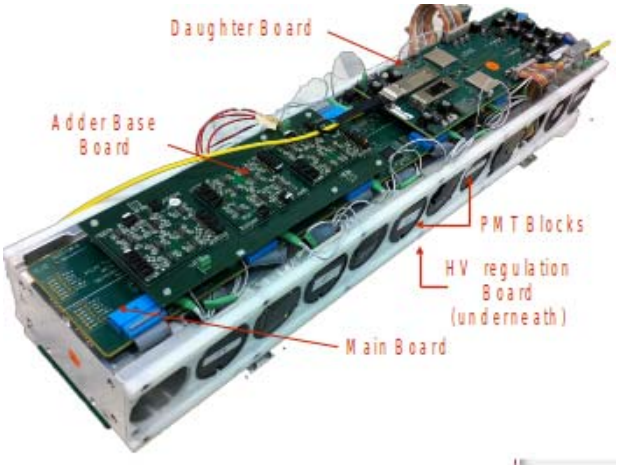


Figure 4: The Demonstrator mini-drawer.

3. Test-beam campaigns

Three test-beam campaigns took place in 2015 and 2016 with the aim of testing the phase-II upgrade electronics prototypes and to assess their performance. Several TileCal modules were equipped with the phase-II upgrade electronics and exposed to different beam particles (electrons, muons and hadrons) during these test-beam campaigns. The primary objective was to assess the status of the Demonstrator based on the modified 3-in-1 FE baseline option, attention and help was also given to the two alternative FE options viz. the QIE (Charge Integrator and Encoder) [8] and the FATALIC (Front-end ATLas TIle Circuit.) [9]. The results from these campaigns provide the necessary performance analysis to aid the 2017 FE option down-selection. The module configuration for the test-beam campaigns is depicted in Figure 5 below.

There is new hardware components available as of the 2016 test-beams, this include the DB version 4 which uses the new GBTx (GigaBit Transceiver) chip [10] instead of the CDCE chip for clock recovery and remote FPGA (Field Programmable Gate Arrays) programming [11, 12]. The MB version 2 which provides a frame and bit clock for ADC de-serialization, correct channel orientation and new 3-in-1 cards. The PPr prototype with no auxiliary boards and operates at 40.08 MHz (4,8 Gbps - 9,6 Gbps) with optimized firmware versions. The PCIe (Peripheral Component Interconnect Express) module for

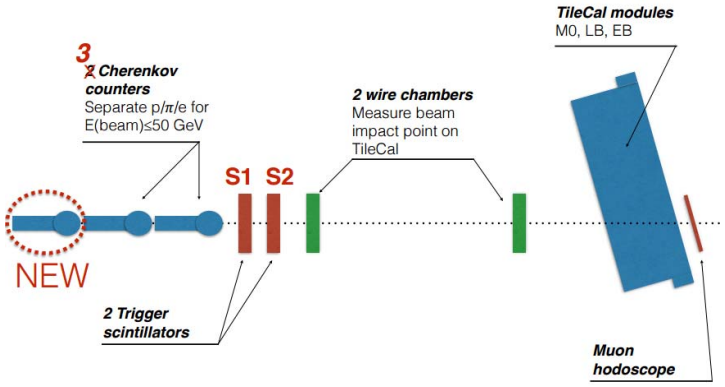
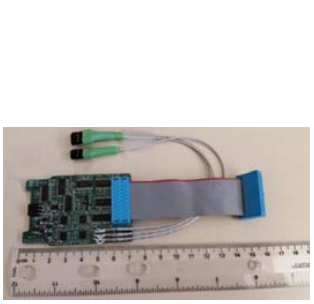


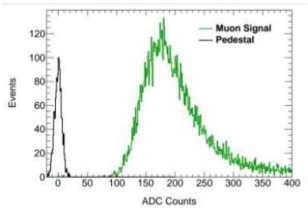
Figure 5: Test-beam configuration with TileCal modules.

readout to the basic pseudo-FELIX(Front-End LInk eXchange) [13] through the PCIe-GBT link data format. A new mobile Cs-137 calibration unit to perform in-situ Cesium calibrations. The 3 FE options under evaluation were all operated in parallel for the entire test-beam period. New software for the TDAQ and the DCS (Detector Control Systems) to improve the communication through IPbus with PPr was developed and provides; improved PPr memory stability for multiple application access, monitoring the link status and FE option configuration at the beginning of every data taking session. The DCS software has been updated to work with the official IPbus OPC server [14] that provides better HV and temperature monitoring. Calibration runs (CIS, CIS mono, Ped and LED) have been successfully integrated as well.

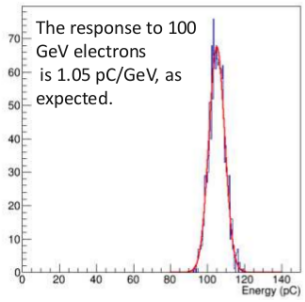
The 3-in-1 cards (Figure 6a) are built with discrete commercial off-the-shelf components. The shaped pulses from 12 FE cards are digitized on the MB. The upgrade brings an improved digitized signal resolution: 12 bit ADCs instead of 10 bits, modern, better performing components. It also brings even lower electronic noise than the present system. The new 3-in-1 system is compatible with the analog trigger and can be installed into TileCal before the HL-LHC upgrade. As mentioned before, the new 3-in-1 system was calibrated and evaluated with test beams hadrons, muons (Figure 6b), and electrons (Figure 6c) in 2015 and 2016. The results illustrate a strong performance for the upgrade system.



(a) 3-in-1 FE board.



(b) Muon signal response.

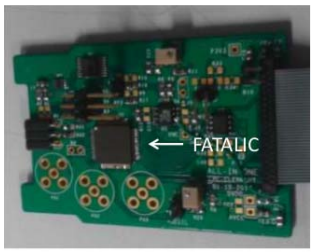


(c) Electron signal response.

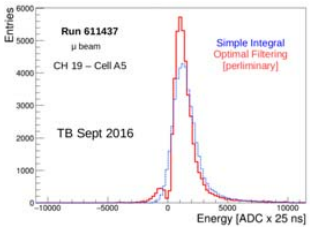
Figure 6: Sample Test-beam analysis results for the 3-in-1

The FATALIC (Figure 7a) is a new technology for TileCal, it is implemented as an AISC (Application Specific Integrated Circuit) slightly different from the 3-in-1. The FATALIC approach also uses shaping like the 3-in-1 but the pulse shape is different. The digitization is done inside the chip. Simulated performance for FATALIC_5 IC is within specifications. Work is ongoing on signal reconstruction and simulations. The FATALIC system was calibrated and evaluated with test beams hadrons, muons (Figure 7b), and electrons

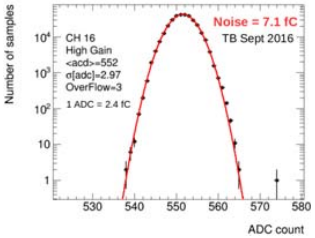
(Figure 7c) in 2016. The results also speak in favor of the strong performance of the FATALIC system.



(a) FATALIC FE board.



(b) Muon signal response.

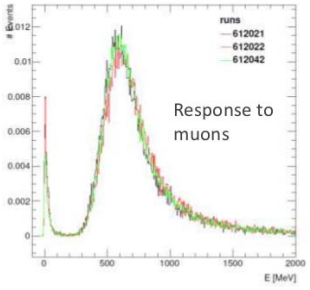


(c) Response from electron signals.

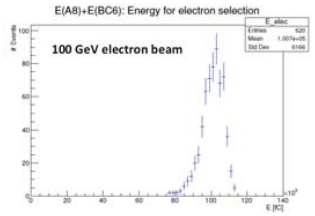
Figure 7: Sample Test-beam analysis results for the FATALIC

The QIE circuit (Figure 8a) is an ASIC which does not shape the PMT pulse to digitization at 40 million samples per second. Instead, it directly integrates the PMT anode current in 25 ns intervals and gives two sample signals viz. (i) charge (current integrated over a 25 ns period) and (ii) time (when current crossed a threshold at 1 ns resolution). The total charge of a PMT pulse (energy) is obtained as a sum of two or three QIE samples. The PMT current is integrated in a bank of capacitors that are time-multiplexed for lossless operation at 40 MHz. The current splitter is used to achieve the required dynamic range (>17 bits). The QIE12 ASIC is designed to be radiation tolerant and tailored for TileCal. All the signal processing (integration and digitization) is done in the FE boards. QIE main boards have mostly point-to-point signal connections and power distribution [15]. The QIE system was calibrated and evaluated with test beams hadrons, muons (Figure 8b), and electrons (Figure 8c) in 2016. The results also speak in favor of the strong performance of the QIE system.

(a) QIE FE board.



(b) Muon signal response.



(c) Response from electron signals.

Figure 8: Sample Test-beam analysis results for the QIE12

4. Conclusions

Upgrade activities are progressing well with the goal of test-beams to do performance analysis for the 2017 option down-selection. The reliability and stability of the system has been visibly improved with respect to the 2015 test-beam. The FE-BE links have been optimized for better stability, improved latency and FE clock recovery. The Demonstrator analog trigger signals output has been integrated successfully into the TDAQ infrastructure for the commissioning of the hybrid Demonstrator. The FE and HV option final selection process has been defined based on extensive comparison of the performances and other criteria. The TileCal community plans to complete the R&D and take a decision by the end of summer.

References

[1] The ATLAS Collaboration. *ATLAS detector and physics performance: Technical Design Report, 1.* Technical Design Report ATLAS. CERN, Geneva, 1999.
[2] The ATLAS Collaboration. The ATLAS Experiment at the CERN Large Hadron Collider. *J. Instrum.*, 3:S08003. 437 p, 2008. Also published by CERN Geneva in 2010.
[3] The ATLAS Collaboration. Letter of Intent for the Phase-II Upgrade of the ATLAS Experiment. Technical Report CERN-LHCC-2012-022. LHCC-I-023, CERN, Geneva, Dec 2012. Draft version for comments.
[4] Matthew Spoor and Oscar Kureba and Charles Sandrock. Development of a high data-throughput ADC board for the PROMETEO portable test-bench for the upgraded front-end electronics of the ATLAS TileCal. *Journal of Physics: Conference Series*, 645(1):012027, 2015.
[5] F Carrio and V Castillo and A Ferrer and L Fiorini and Y Hernndez and E Higon and B Mellado and L March and P Moreno and R Reed and C Solans and A Valero and J A Valls. The sROD module for the ATLAS Tile Calorimeter Phase-II Upgrade Demonstrator. *Journal of Instrumentation*, 9(02):C02019, 2014.
[6] O. Solovyanov. Performance of the ATLAS Tile Hadronic Calorimeter at LHC in Run 1 and planned upgrades. *Journal of Instrumentation*, 9(10):C10006, 2014.
[7] ATLAS Tile Collaboration. Initial Design for the Phase-II Upgrade of the ATLAS Tile Calorimeter System. Technical Report ATL-COM-TILECAL-2016-054, CERN, Geneva, Dec 2016.
[8] Gary Drake and Alexander Paramonov. Controls and read-out of QIE12 front-end cards. Technical Report ATL-COM-TILECAL-2016-043, CERN, Geneva, Oct 2016.
[9] Laurent Royer. FATALIC: A Dedicated Front-End ASIC for the ATLAS TileCal Upgrade. Oct 2015.
[10] P Moreira, S Baron, S Bonacini, O Cobanoglu, F Faccio, S Feger, R Francisco, P Gui, J Li, A Marchioro, C Paillard, D Porret, and K Wyllie. The GBT-SerDes ASIC prototype. *Journal of Instrumentation*, 5(11):C11022, 2010.
[11] Kai Chen, Hucheng Chen, Weihao Wu, Hao Xu, and Lin Yao. Optimization on fixed low latency implementation of GBT protocol in FPGA. Technical Report arXiv:1608.08916, CERN, Aug 2016.
[12] S Muschter, C Soos, C Bohm, J-P Cachemiche, and S Baron. Optimizing latency in Xilinx FPGA implementations of the GBT. *J. Instrum.*, 5:C12017, 2010.
[13] J T Anderson et al. FELIX: a PCIe based high-throughput approach for interfacing front-end and trigger electronics in the ATLAS Upgrade framework. Technical Report ATL-DAQ-PROC-2016-022. 12, CERN, Geneva, Nov 2016.
[14] Soare Cristian-Valeriu. OPC UA IPbus server. Sep 2015.
[15] Gary Drake, Alexander Paramonov, James Proudfoot, Robert Stanek, and Sergei Chekanov. QIE12: A New High-Performance ASIC for the ATLAS TileCal Upgrade. *ATLAS*, Oct 2015.