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DETAILED CONCEPT REVIEW OF THE DATA PUSH ARCHITECTURE TEST CHIP ANALOG DESIGN*

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I. INTRODUCTION

This document is an attempt to list the specifications for the analog behavior of the Data Push Architecture (DPA) test chip to be developed by Adept IC Design over the next few months. During the detailed design process, trade-offs must, of necessity, be made. This is an attempt to guide the design should these trade-offs result in behavior characteristics which have not been discussed in detail elsewhere. Within this document, we will discuss the justification for some of the more important specifications and assign priorities. At this time our priority list is as follows:

1. Throughput
2. Noise
3. Power

II. SPECIFICATION SUMMARY

TABLE 1. DPA TEST CHIP SPECIFICATIONS

PARAMETER	SPECIFICATION	GOAL
1. Pixel size (μm^2)	50×150	< 40×120 I 35×100 II
2. Throughput (ns/hit)	200	100
3. Power budget (μW/pixel)	30	20
4. Time walk (4–50 ke^-) (ns)	250	32
5. Noise (input referred) (e^-)	200	100
6. Gain ($\mu V/e^-$) (10 fF feedback cap)	16	16
7. Maximum signal (e^-)	50 k	50 k
8. Pixel comparator reset time (ns)	< 100	< 50
9. Chip reset time (ns)	< 1000	< 500
10. Pileup (Min I hits w/o preamp reset)	3	3
11. Settling accuracy (bits or %)	4 bits or 6%	5 bits or 3%
12. Threshold for pixel comp (e^-)	800–2400	800–2400
13. Gain uniformity (neighbors) (%)	3	2

III. DISCUSSION OF INDIVIDUAL SPECIFICATIONS

1. PIXEL SIZE: 50 μm × 150 μm

The maximum pixel size has been chosen to conform to the detector PIN diode arrays already fabricated by Steve Holland at LBL. This specification will easily be achieved, as there are only 14 FETs, 5 caps, and 14 lines in the DPA pixel design compared to 22 FETs, 7 caps, and 20 lines in the CHIP 5 design. An estimate of the

achievable size of the layout is given by setting the goal of 40×120 μm^2 (GOAL I), however, not much a priori work has gone into this estimate. GOAL II is just a guess at the size achievable with the TI 0.8 μm SOI process, and is not relevant to this design round.

Whatever size is eventually achieved will be placed on a 50×150 μm^2 pitch so that the eventual large array can be bonded to our diodes should we choose to do so. Our initial 4×4 array will be close-packed in order to check crosstalk.

2. THROUGHPUT: 200 ns/HIT

Throughput, as defined here, is the minimum time between two hits on the analog output port of the chip. Each hit is considered to be three pixels, a central hit, and two neighbors. Each of the three analog signals from the hit must have settled to the accuracy specified in specification 11, viz., 4 bits or 6%; thus this specification refers to the maximum time necessary to read out three pixels per hit on separate columns.

At a forward *B* spectrometer at the SSC, the working luminosity is ten times less than SSC design luminosity. Even when we evaluate performance at radii close to the beam line—e.g., at 1 cm—the expected data rates, averaged over an array, are about 1 per cm^2 per μs. Thus, at this first specification of 200 ns, there is at least a factor of five in time safety. All background and noise hits must be sent off-chip along with the data. There is presently no estimate of this rate, however, so when this effect is coupled with statistical fluctuations in so-called average rates, the assumed safety factor is essential. At a SLAC *B* factory, the data rates are down at least another factor of five at the beam pipe radius of 2.5 cm.

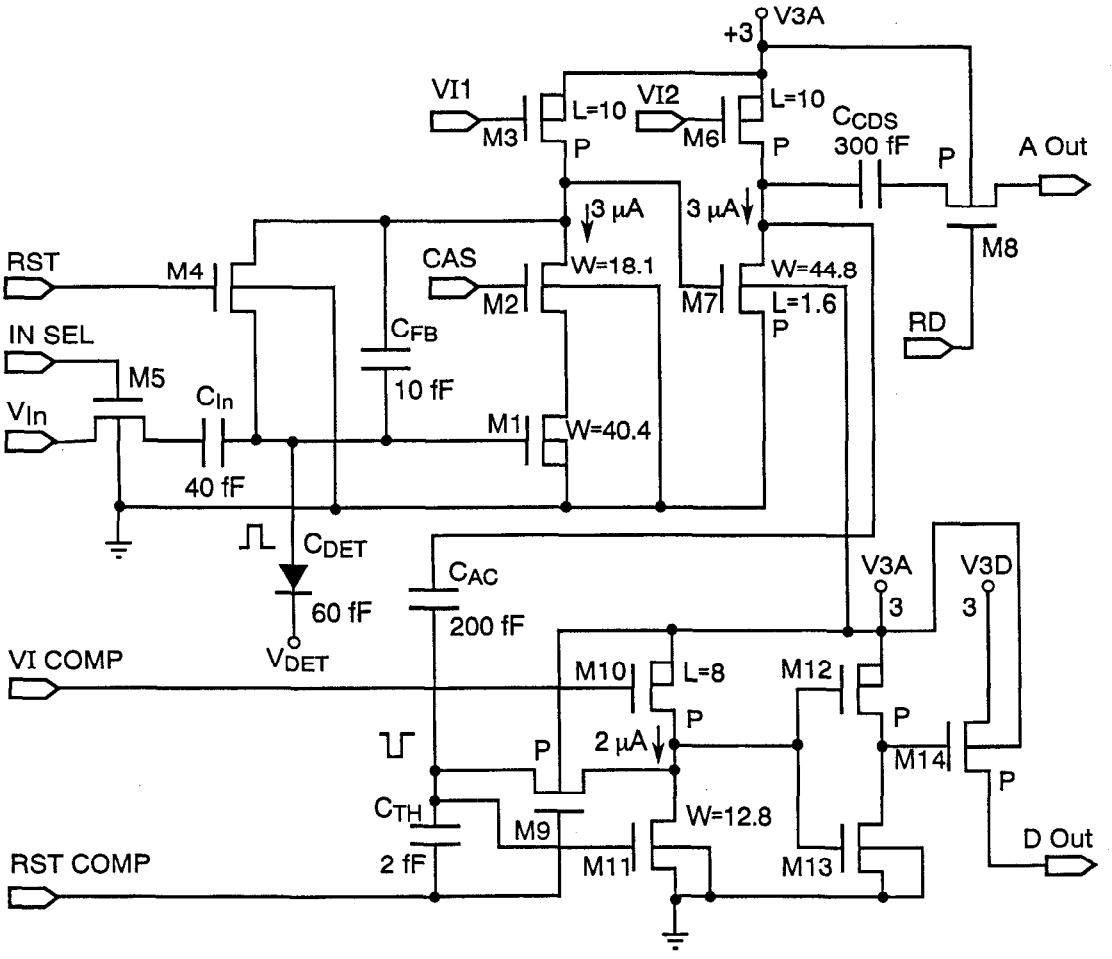
By specifying throughput, we can leave the details of the individual logical blocks to the designer, and not get bogged down in details of bandwidth and reset times. These will be discussed later as informational issues, and our biases at the start of the design process will be mentioned.

3. POWER: 30 μW/PIXEL

This power figure is meant to include both the power generated within the pixel and a prorated portion of the power generated by the analog electronics on the periphery. The goal of keeping the power dissipation to 0.5 Watts per cm^2 is implied. There is no estimate of the power needed by the digital periphery, but it will be amortized over 15,000 pixels. The present pixel design goals include 3 V voltage swings and standing currents allocated as follows:

TABLE 2. STANDING CURRENTS	
Preamp	3 μA
Source follower	3 μA
Comparator	2 μA

Figure 1 Is a schematic of the proposed pixel circuit; SLAC–TN–92–2 provides additional detail of the design trade-offs to date.



1. All transistors are N unless marked P
2. W, L in microns
3. Default L = 1.2 µm, W = 2.4 µm

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Figure 1. A transistor level schematic of the data push unit cell showing 14 FETs, 5 capacitors, and 14 lines.

4. Time Walk: 250 ns from 4–50 ke⁻ Input Signal

Time walk is defined as the difference in time between the beginning of the charge pulse at the preamp and the appearance of the current pulse at the output of the comparator (D_OUT) as a function of the size of the charge pulse.

Time walk is not a problem for multiple hits within a column, or for the neighbor readout, as the largest hit in the column will trigger that column's logic to start the readout, and its time tag will be recorded. Time walk occurs in the pixel comparator—small signals take forever to trigger because they have little "overdrive." Within a column, not too much time is needed for the preamp to stabilize its output level onto the correlated double sampling capacitor C_{cds}. This depends on preamp characteristics. Within a column, the column may be reset before its smallest signals trigger their comparators. This is fine, as the logic will read out these small "neighbors" without their comparators ever firing.

The effect of time walk is felt most for particles which cross multiple columns. Small pulses will appear as hits, at times later than their particle's arrival time at the PIN diode detector—by hundreds of nanoseconds in some cases. This time-of-arrival error

can be corrected by either using a timing algorithm built into the detector analog periphery or by using a simple ASIC containing the amplitude-dependent corrections off-chip.

Data on this effect fortunately was acquired in the testing of Hughes CHIP 4, plotted in Fig. 2a. The time walk for 4,000 to 25,000 e^- is about 275 ns. This data was acquired with a threshold setting of 2,000 e^-. The preamp current was 1 μA and the comparator current was 0.4 μA. Our test chip will be designed with more standing current, and will surely be faster and result in less time walk. However, even this poorly performing comparator is adequate for our needs using the DPA ideas. We have the analog information at our disposal for developing a timing correction. Figure 2b demonstrates that, even with the CHIP 4 comparator, if we measure the charge to 6% (±3%), we can achieve 30 ns time resolution. The outer two curves represent the ±3% bounds.

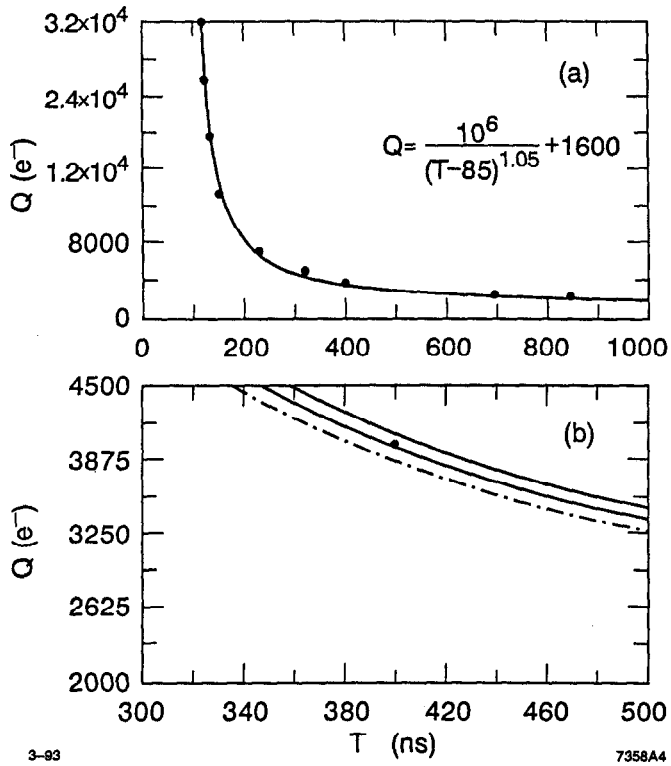

Figure 2. (a) plot of time walk versus input charge representing data taken from the Hughes CHIP 4, and (b) plot showing that the effect of measuring pulse height to four bits (±3%) is adequate to resolve the time-of-arrival to about 30 ns, even if the time walk is as bad as that of CHIP 4.

The 30 ns goal represents a time resolution adequate for full luminosity detectors and *B* factories, and is more than adequate to forward spectrometer designs at the SSC where interactions happen, on average, every 100 ns.

5. NOISE (INPUT REFERRED): 200 e^-

Noise, in this definition, refers only to the noise generated by the preamp/PIN diode composite prior to any radiation. We want to set our pixel comparator threshold as low as possible, while still retaining a good rejection of "noise"-induced hit pixels. As we expect about 15,000 pixels per cm^2 in this first design, and as there is always the interaction between signal size, threshold, and noise, we have set our maximum noise

specification at 200 e^- to allow a 10:1 threshold-to-noise margin. This may appear too high to some—and may in fact be too high—but it will allow us to lower the threshold value later, to improve time walk. This noise floor of 200 ns will be challenged quickly once we start irradiating the chip, and shot noise generated by the leakage current grows.

A noise estimate for our pixel design has been made using a number of "reasonable" assumptions:

TABLE III. PIXEL DESIGN ASSUMPTIONS	
Temperature	300 K
C_{DET}	80 fF
BW	30 MHz
RST_COMP	$\langle 1/(64\ \mu s)\rangle$ = 15,600 Hz
I (preamp)	3 μA
Process parameters for 1.2 μm CMOS	

With this set of assumptions, Fig. 3 is an estimate of input noise as a function of driver (M_1) gate width. A broad minimum is seen at widths of 20 to 35 μm of approximately 140 e^-. It should not be too difficult to exceed our specification and reach a number closer to our goal at first pass. The dashed and dotted lines represent the thermal and the 1/f noise components of the solid total-noise curve.

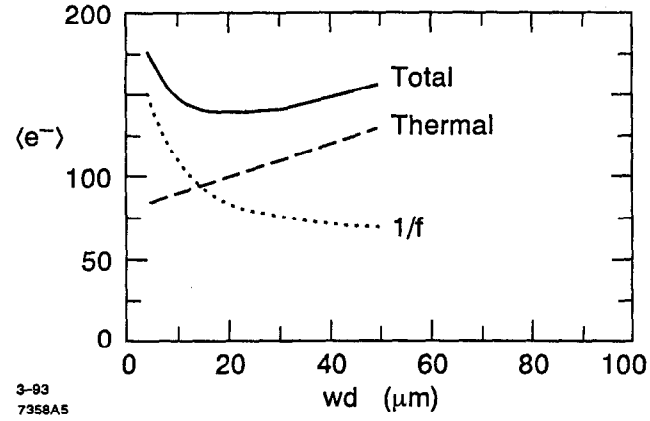

Figure 3. Computer simulation of the expected input referred noise showing that for our choice of input gate width 150 e^- noise is predicted.

6. GAIN: 10 fF FEEDBACK CAPACITOR

The feedback capacitor has been chosen to be 10 fF as a conservative value providing ample overall gain. The comparator threshold settings of about 40 mV will be easy to maintain, and the output referred noise will be about 3 mV, a comfortable value.

Reducing the feedback capacitor is equivalent to increasing the gain of the preamp. The input capacitance of the pixel is $C_{det} + C_{IN} + C_{M1}$ = 60 fF + 40 fF + 40 fF = 140 fF; thus, we have a gain of about 14. The present design of the preamp employs a bandwidth of 30 MHz. We believe this design, as presently envisioned, will be adequate to meet the throughput, noise, and power specifications, without increasing the gain.

7. MAXIMUM SIGNAL: 50 ke⁻

The dynamic range should be read to mean that a minimum ionizing particle traversing 300 μm of silicon will produce 25,000 electron–hole pairs, and we will collect one or the other of them. Landau scattering can fake twice-minimum ionizing particles or higher, with decreasing probability. We ask of our circuit that it record with fidelity (linearity <3%) the charge deposited by particles from the noise floor of 200 e^- to 50 ke^-; the DPA design handles this automatically.

8. PIXEL COMPARATOR RESET TIME: 100 ns

The comparator will be reset after each analog read. In the case of the forward spectrometer, with an average hit rate of one per array per μs, this is every 64 μs since there are 64 columns in our proposed array. This specification does not affect the throughput of the array, since the analog circuit on the periphery contains a ping-pong sample and a hold circuit that allows the simultaneous resetting of the previously hit column while reading the current column. Figure 4 is a block diagram of the analog chain. The throughput will be largely determined by the speed with which the charge-to-voltage (Q–V) converter and the ghost discriminator (GD)—both on the row periphery—can be reset, and on the interaction between the preamp and the Q–V converter circuit in transferring the charge to the sample-and-hold capacitor to the desired accuracy.

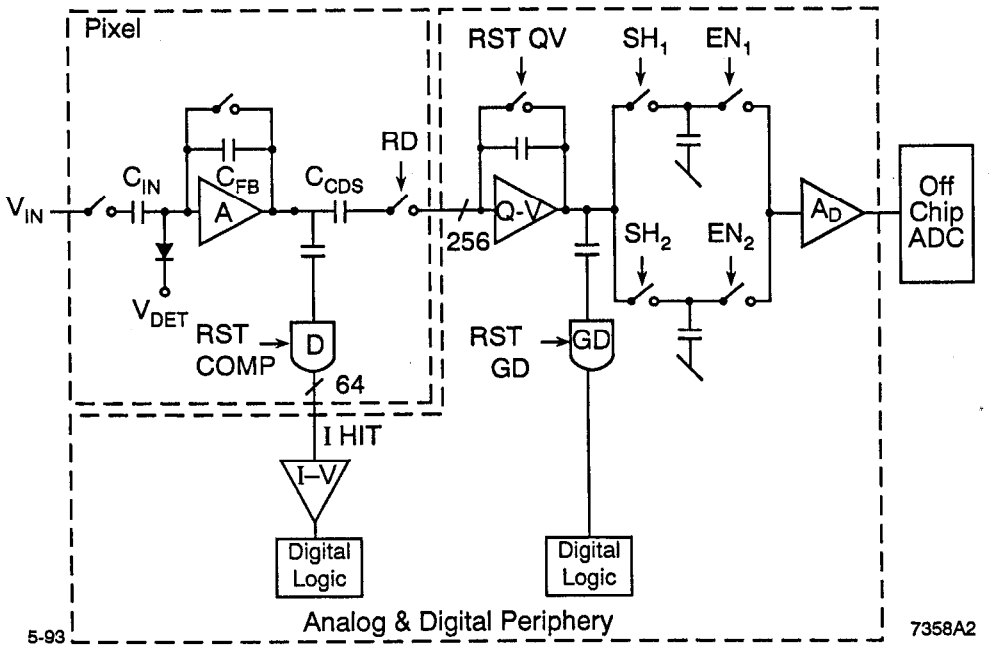

Figure 4. Block diagram highlighting the data push architecture analog design.

This specification is set by dead time considerations after radiation levels of 1 MRad. Though not thought of as a specification, we are attempting to hold chip dead time to about 1% at this level of radiation exposure. With radiation, PIN detector leakage currents grow, causing effective threshold shifts in the pixel comparator. To combat this effect, we have postulated that we can reset the comparator asynchronously every 10 μs, limiting the threshold shifts to the current collected over that short time interval. If the reset time is 100 ns, then we have a 1% dead time under these conditions.

9. CHIP RESET TIME: 1000 ns

The chip reset time, too, does not affect array throughput.

The preamp should be reset only when a pixel has been hit two to three times. Due to statistical fluctuations, during the wait for an average (across the chip) of two to three hits per pixel, some pixels will be hit as many as five times. As there are about 15,000 pixels per chip, with each hit affecting about three of them, we will initially reset about every millisecond for an assumed hit rate of $5/cm^2/\mu s$. Once again, it is the behavior of the array after a radiation dose of 1 MRad that drives this specification. Leakage current collected on the feedback capacitor will affect the size of the signal necessary to cross the comparator threshold. If we asynchronously reset the entire array every 100 μs, then an array reset time of 1 μs will result in a dead time of 1%.

10. PILEUP: 3 PER PIXEL

The preamplifier is AC coupled to both the analog chain and the comparator, so the DC level of the input to these AC coupling capacitors does not affect the performance of the readout. A minimum-ionizing (Min I) particle traversing 300 μm of silicon generates 24,000 electron hole pairs. This circuit is designed to collect holes. The feedback capacitor is 10 fF, resulting in a 0.4 V level change for a Min I particle. There is about 2.0 V of headroom before the drain of transistor M_1 approaches ground and M_1 ceases to operate, allowing 3 to 5 hits/pixel if they are all 0.4 V hits. Landau scattering will surely make some of them larger, but a specification of three per pixel will still be easy to accommodate by resetting every millisecond or so. This specification is not a severe one, and after fabrication of the prototype, the headroom can possibly be reduced, with a potential saving in power.

11. SETTLING ACCURACY: 4 BITS OR 6%

If we are to improve our measurement of spatial resolution by measuring the charge shared by two neighboring pixels, we must specify the accuracy needed for this measurement. A requirement for high accuracy will be translated into a specification for a long settling time. How long should we wait before latching a voltage level for digitization? This involves both the signal and the reset level settling time. To first order, the time to settle is proportional to RC where C is the capacitor on which the signal (or reset level) is stored, and R is the effective resistance of the transistor interrogating this capacitor: $R = 1/gm = 1/\sqrt{I}$ Thus, achieving a fast settling time requires a high standing current. To be more specific, for a fixed time response, for a number of bits accuracy (n), the current I is proportional to ln (2^n), or n.

To estimate the accuracy needed, we need only build a simple model with two neighboring pixels: pixel A with a large pulse height "a" and the neighboring pixel B, with a smaller pulse height "b." The passage of a charged particle somewhere in pixel A causes the charge deposition. Defining the position X from the edge of pixel A as positive in the direction of the center gives the relationship

$$X = \frac{L}{2}\,\frac{a-b}{a+b},$$

where L is the width of the pixel and $0 < b < a$.

$$\delta x = \left[\left(\frac{\partial X}{\partial b} \right)^2 \delta b^2 + \left(\frac{\partial X}{\partial a} \right)^2 \delta a^2 \right]^{1/2} , \qquad (1)$$

$$\delta x = \frac{L}{(a+b)^2} \left[a^2 \delta b^2 + b^2 \delta a^2 \right]^{1/2} , \qquad (2)$$

where δx is the rms error in X, and δa and δb are the measurement errors of the two pulse heights, which depend on:

1. The electronic noise of about $\langle 200\ e^- \rangle$.
2. Binning error of an 8 bit ADC; if one adjusts 50,000 electrons to be full scale, 50,000/256 = 200 e^-; however, this is a square distribution, and for combination with other Gaussian errors it must be adjusted to be the equivalent Gaussian value of $200/\sqrt{12}$ or $\langle 65\ e^- \rangle$.
3. The settling error: e.g., 4 bits or 6 %.
4. The shot noise of the leakage current for zero radiation = 0.

If one considers the example of the particle striking at the interface between the two pixels, then,

$$a = b = 12{,}000\ e^- .$$

Thus,

$$\delta a = \delta b = .06\ (12{,}000) \quad \text{or} \quad \langle 720\ e^- \rangle ,$$

and Eq. (2) becomes

$$\delta x = \frac{L}{\sqrt{2}} \frac{D}{24{,}000}$$

where

$$D = \sqrt{200^2 + 65^2 + 720^2} = \langle 750\ e^- \rangle .$$

If L = 50 μm, then δx = 1.1 μm.
If one considers a second example where

$$a = 22{,}000\ e^- \quad \text{and} \quad b = 2000\ e^- ,$$

then

$$\delta a = \sqrt{200^2 + 65^2 + 1320^2} = \langle 1336\ e^- \rangle ,$$

and

$$\delta b = \sqrt{200^2 + 65^2 + 120^2} = \langle 242\ e^- \rangle .$$

Eq. (2) results in δx = 0.5 μm.

These examples assume that the charge cloud is spread out over more than L/2 or 25 μm. Not true, but close enough for now. We've assumed an 8-bit ADC to allow adequate dynamic range and low binning error. This can be reexamined at a later time.

The lesson learned from these examples is that, with only four bits accuracy (6 %) we can match or exceeds the accuracy achievable, because of the effects of Landau

scattering. Data from our test run using the Hughes 256x256 arrays (with 30 μm^2 pixels) showed 2 to 3 μm spatial resolution—we can surely not do better with larger pixels.

12. Threshold for Pixel Comparator: 800–2400 e^-

The threshold for the pixel comparator is presently envisioned to be set at ten times the noise specification. As the noise performance is improved, this threshold can be reduced to improve the overdrive for the time walk specification. However, as radiation damage will increase the effective noise of the system, it is more likely that the threshold will be increased with time.

On the other hand, in a low radiation environment, as the performance of the readout chip is improved viz., as we reach 100 e^- noise, the threshold can be reduced to 1000 e^- and the PIN diodes can be made thinner.

13. Gain Uniformity [Neighbors]: 3%

Gain nonuniformity would, if uncorrected, result in an inaccurate measurement of the charge sharing necessary for the spatial resolution. We have specified a 6% settling specification, and a gain nonuniformity of much less than this percentage would be dominated by this number. However, we have the ability to do a gain map of the array, and apply corrections if necessary. More to the point, the gain is dependent of the feedback capacitor, and neighboring capacitors should vary by only about 1% using standard fabrication and layout techniques.

IV. INFORMATIONAL COMMENTS

1. Delay

The delay between the incoming hit and the appearance of an analog pulse at the periphery of the chip is comprised of a number of delays, which will be described here. This delay is not specified above, because to first order it is the same for all incoming particles (time walk notwithstanding).

The incident-particle pulse shape is determined by the collection time of the holes; that is, the thickness of the silicon diode, and the voltage applied. The bandwidth of the preamp will determine the speed with which the output pulse is presented to Ccds and the comparator (risetime $\tau = 0.35/f_{-3\,dB}$). Within a column, the timing will be determined by the largest pulse (since it will have the minimum time walk), and the D OUT pulse so generated will be presented to the current-to-voltage converter (I–V) on the column periphery. The I–V converter will add a bit of delay as well. Simulations to date imply a total delay of about 100 ns from Idet to HIT_COL for a Min I particle.

Another delay chain occurs at the time of the analog read request, RD. After a bit of digital logic delay to identify the hit column, store its address, and priority select the first column to read, an RD instruction is sent. This enables an interaction between the preamplifier and the charge-to-voltage converter. The delay to a stable voltage stored on the sample-and-hold capacitor is dependent on both the bandwidth of the two amplifiers and the accuracy to which we want the measurement. In parallel with this, the ghost discriminator will trigger, allowing the digital row logic on the periphery to identify the relevant row, add neighbors, and start the transfer from the sample-and-

hold capacitors to the ADC (off chip). Simulations to date show this delay to also be on the order of 100 ns.

Figure 5 is a timing diagram of the read cycle, for three simultaneous hits in one array. The timing assumptions are those listed in the specification column, rather than the goal column. The 200 ns throughput specification is illustrated. An indication of timing delays caused by the digital logic is hinted at by the shaded sections. No calculations of these delays have been attempted here.

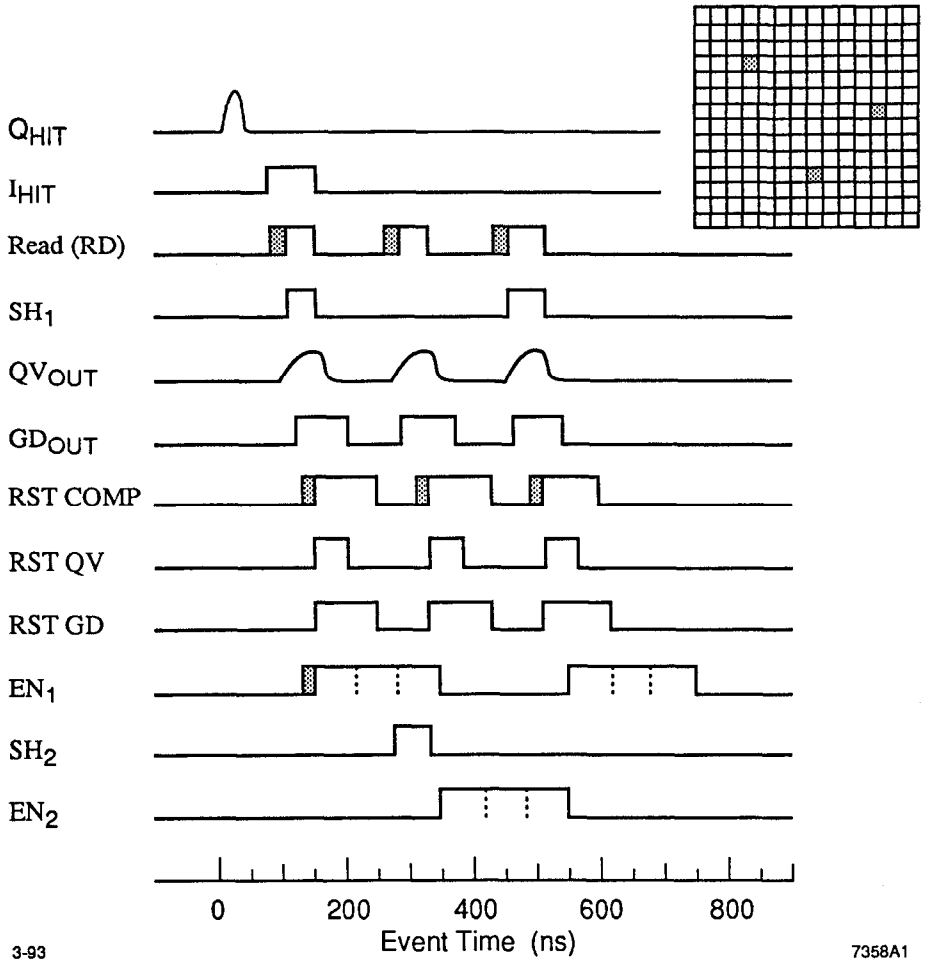

Figure 5. Timing diagram of the read cycle, for three simultaneous hits in one array. The 200 ns throughput specification is illustrated, as are the timing delays caused by the digital logic.

2. Open Loop Gain of the Preamplifier

Simulation has this at 750. A minimum of 200 can be thought of as necessary for proper preamp performance.

3. Ghost Discriminator

The ghost discriminator noise contribution should be small compared to the 3 mV output referred noise of the front end. Nevertheless, the threshold should be set high to trigger on only the central pixel of a cluster, neighbors being added for digitization by the digital peripheral logic.

4. BANDWIDTH CONSIDERATIONS

There are two modes of operation of the preamp. During the write cycle, the Ccds capacitor doesn't exist, as M_8 is open; therefore, the amplifier is only weakly loaded with the comparator, and its bandwidth is thus 30 MHz. During the read cycle, Ccds is grounded (by the virtual ground of the Q–V) and the preamp drives a load of about 300 fF, reducing the bandwidth to 10 MHz. The cascoded preamp loaded by Ccds has a gain bandwidth product of 150 MHz; unloaded it is 400 MHz. Similarly, the source follower when loaded has a $f_{-3\,dB}$ of 16 MHz, while loaded it has a $f_{-3\,dB}$ of 60 MHz.

5. NOISE [OUTPUT REFERRED]: >3 mV

This specification is set to indicate a sensitivity to off chip and system considerations of environmental effects. Our input referred noise specification translates to about 3 mV (200 e^-×16 $\mu V/e^-$) of output noise. We expect that the environmental noise may be as large as this. We would like our signal-to-noise ratio to be set by our input parameters of 25,000 e^- signal and 200 (or 100) e^- noise. If we succeed in lowering our input referred noise to 100 e^-, it would be the equivalent of about 1.5 mV, output referred, and this specification is interpreted to mean that gain should be added on-chip to overcome the environmental noise off chip.

6. RADIATION TOLERANCE: > 2 MRad

The prototype array, to be designed and delivered by this summer, will be fabricated in a nonradiation hard process. However, SLAC–TN–92–2 discusses the issue of radiation hardness. A rad-hard process—such as the TI 0.8 μm SOI process—will be chosen for the next rototype.

The detector is DC coupled to the readout electronics, and the leakage current, therefore, emulates a low level signal. With radiation damage the leakage current grows, and a charge, equal to it and opposite in sign, must be applied to the readout electronics to reduce it. This is done with a ramp input through VIN. However, as there are pixel-to-pixel variations, this will only reduce the effect. To eliminate the charge build up one must reset the comparator in an asynchronous fashion. If we reset it every 5 μs, and if the reset is effected in as little as 50 ns (our goal), the dead time caused by this will be no greater than 1% and the fluence tolerated with no loss in efficiency will be approximately 2 MRad.

Between resets pixel nonuniformity may be a problem. We envision a pixel ``kill'' circuit to eliminate pixels that are exceptionally effected by radiation. We also envision a leakage current sensing circuit which can be enabled at high radiation doses that can inject an opposite charge (per pixel). Both of these circuits are envisioned to be added to the pixel during the next design phase.

7. RESET CONSIDERATIONS

(a) Column crosstalk during comparator reset

We would like the crosstalk and other synchronous effects to be on the order of 10% of the comparator thresholds—in this case, 200 e^-. The placement of the RST_COMP line in the center of the pixel places it far from the sensitive front end of the pixel on the

one hand, and separated by six metal lines from the front end of the neighboring pixel. Capacitance to other layers can be calculated only with great difficulty and, hence, the crosstalk that occurs via other layers cannot be calculated easily. However, this particular effect will be kept in mind during the layout. To remain below the desired 200 e^- requires a $C_{crosstalk}$ of about 10 aF (10^{-17} F), too small to trust calculations.

(b) Comparator threshold uniformity

Once again, 10% of the threshold value is the goal. In this case, the uniformity—which is dependent on the ratio of two capacitors—would be a nonissue; viz., it would be only a few percent if both capacitors were of the same type. As one of the capacitors is exceptionally small (2 fF), making them both by the same technique is difficult. One capacitor will be metal-poly, and the other will be poly–N well. Thus, the dielectrics will be different and a uniformity of about 10% (~200 e^-) is expected.

(c) Accuracy of the comparator threshold

We would like to settle to within 10% of the threshold value. We would also like to effect the reset function in about 100 ns. The 200 fF capacitor C_{AC} (more like 300 fF when stray parasitics are included) is reset through the g_m of M_9. This is about 20 μMho for a time constant of about 15 ns. Thus, 100 ns is about six time constants, and we should consistently reset to a few percent.

(d) Remnant charge on the analog readout

As we reset the ghost discriminator and the Q–V converter, we will leave a bit of charge unreset. This will appear as a form of crosstalk as we progress in the readout to the next column read. The gain bandwidth product of the Q–V will determine the reset time. But in this mode, i.e., the reset mode, we will be shorting the feedback capacitor and reducing the gain of the device, so that it will surely react faster than the canonical 15 ns speed in effect during Read. Five time constants—or 75 ns—is about six bits, or about 1.5% settling accuracy—about 300 e^-, better than 10% of the ghost discriminator threshold (4 ke^-). The ghost discriminator will surely be set to a higher threshold than the pixel discriminator, and 4000 e^- is a good estimate at this time.

8. Temperature Considerations

We are designing this device for approximately room temperature operation. should we decide to operate at significantly lower temperatures, the pixel and periphery will work *better*. Mobilities will increase, resulting in greater device speed.

This issue is mentioned for three reasons, all desireable features of a cold system:

- The heat removal technique is not yet firm—a cool gas system is likely.
- Secondly, the cooling of the detector will reduce leakage currents dramatically.
- Thirdly, the operation of beam pipes and rf shields at cryogenic temperatures reduces their resistivity, and increases the number of skin depths of rf shield we have for a fixed thickness of material at a constant bandwidth.

9. THE ANALOG CIRCUITS ON THE PERIPHERY

The analog circuits on the periphery are described in the Figs. 6, 7, and 8.

Figure 6. is a schematic of the charge-to-voltage converter (Q–V). It employs 40 μA of standing current in its input stage, and 17 μA standing in the output stage. The open loop gain is calculated to be about 500, and the gain-bandwidth product is calculated to be 250 MHz. The closed loop gain is the ratio of Cin to Cfb or about 17.

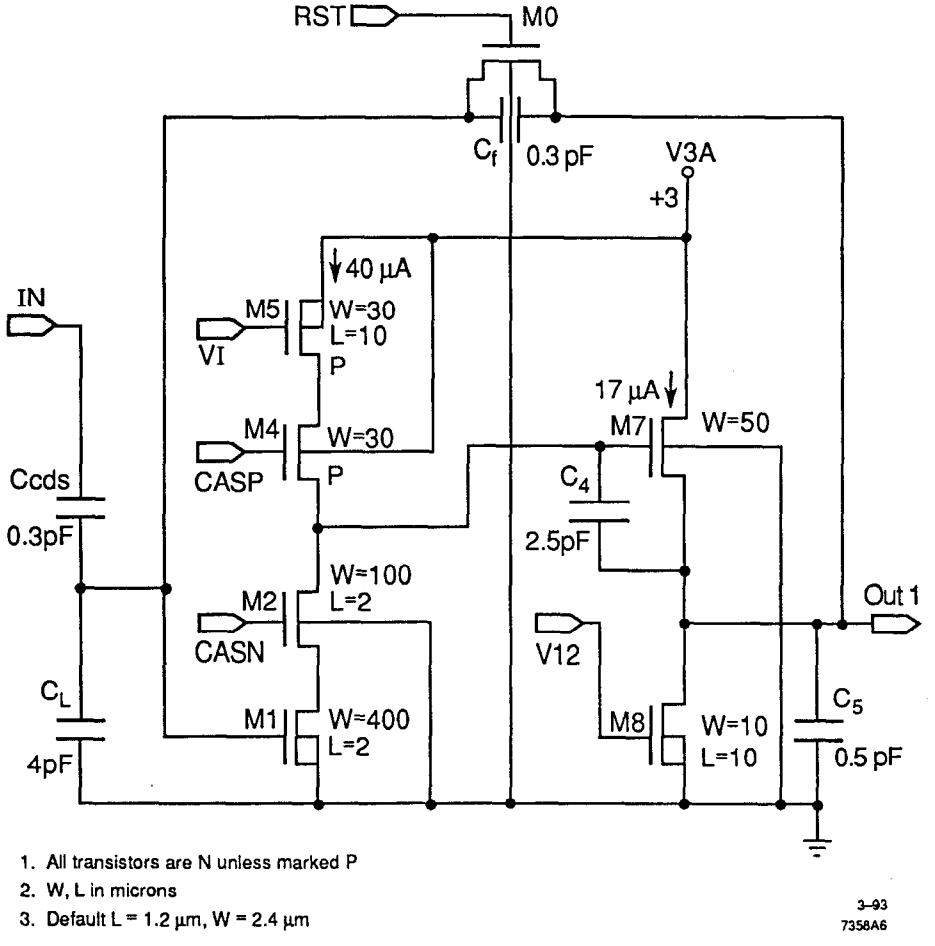

Figure 6. Schematic of the charge-to-voltage converter (Q–V), which employs 40 μA of standing current in its input stage, and 17 μA standing in the output stage.

Figure 7 is a schematic of the current-to-voltage converter (I–V). Simulation shows its conversion time to be 15 ns.

Figure 8 is a schematic of the ghost discriminator (GD).

V. BIBLIOGRAPHY

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2. E. L. Atlas, S. Shapiro, and D. Cords, "Design of a Pixel Cell Optimized for a Data Push Architecture Readout," SLAC–TN–92–2 (1992).

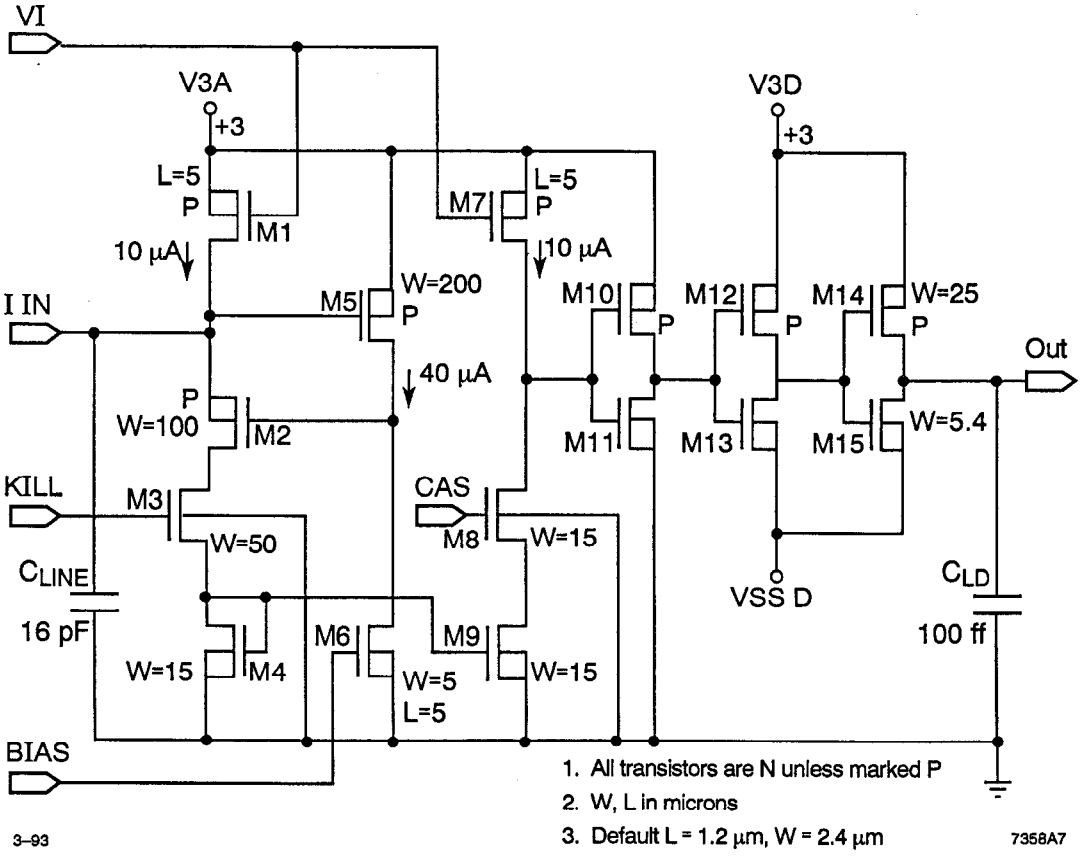

Figure 7. Schematic of the current-to-voltage converter (I–V).

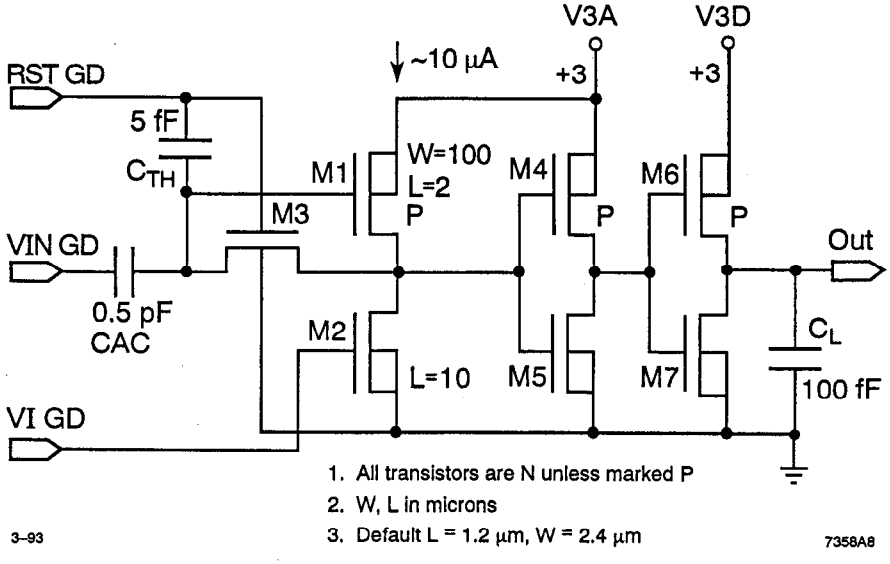

Figure 8. Schematic of the ghost discriminator (GD).