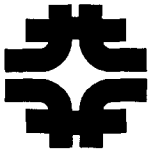

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The MASDA-X Chip - A New Multichannel ASIC for Readout of Pixelated Amorphous Silicon Arrays

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The MASDA-X chip is designed specifically for reading out large amorphous silicon pixel arrays used in medical imaging research. Instrumenting these arrays requires a set of digital row addressing chips to sequentially select the pixel rows for readout, and a set of column readout chips to collect and process the analog charge transferred to each column by the selected pixels. A 32 channel column readout chip, MASDA-R, has previously been designed and successfully implemented by Fermilab and the University of Michigan [1]. However, new arrays require an updated readout chip design with much tighter input channel pitch for direct mating to arrays. A new 128 channel chip, MASDA-X, has been designed at Fermilab. This chip incorporates performance improvements along with tighter channel pitch. MASDA-R was designed in the H. P. 0.8 micron process, which will no longer be available. Therefore, MASDA-X has been designed in the H. P. 0.5 micron 3.3V process.

General Operation

MASDA-X has 128 identical channels which are spaced at a pitch of 80 microns, comparable to that of the new arrays, so that the chips may be directly wirebonded or TAB bonded to the arrays without fanout. A functional block diagram of the chip is shown in Figure 1. Each of the 128 channels consists of a charge integrator with programmable charge gain and bandwidth, two sets (A and B) of two sample capacitors for performing pipelined correlated double samples on the integrator output, and an analog multiplexer for sequential differential analog readout. Correlated double sampling is achieved by taking "before" signal and "after" signal samples with a given set of two capacitors. This has several advantages: the effect of low frequency noise at the input is greatly reduced, integrator reset noise and charge injection is rejected, common mode noise after the integrator is rejected, and a differential output is naturally formed for driving a balanced transmission line off-chip. Pipelined operation is achieved by acquiring the signal with one set of sample capacitors while the other set is being read out. For example, during a given integration period, if the A set of capacitors is sampling the integrator signal, the B set (which holds the double sample of the previous integration period) is routed by the Precharge/Mux circuit to the output buffers for readout. During the next integration period, the B set will be acquiring the signal while the A set is being read out. Pipelining thus allows continuous signal acquisition and avoids deadtime due to readout.

Readout is performed by sequentially multiplexing channel outputs onto a common differential output bus. Since this must happen concurrently with the signal integration period (due to the pipelined architecture), all 128 channels must be read out (and digitized externally) within one

integration period. Since it may be impractical to complete the sequential readout of all 128 outputs on one differential bus within this time period, the chip is divided for readout purposes into groups of either 16 or 64 channels, selectable by the user. If 64 channel mode is selected, as depicted in Figure 1, then there will be two sets of active output buffers. While the top set is reading out channels 0-63, the bottom set concurrently reads out channels 64-127. Thus 64 readout clock cycles will be required to read out all channels. If 16 channel mode is selected, then there will be 8 active sets of output buffers, each concurrently reading out 16 channels. Only 16 readout clock cycles are then required. In either case, channel readout direction (low to high numbered or high to low numbered) is selectable.

Single Channel Operation

1. Acquisition

A more detailed diagram of a single channel is shown in Figure 2. The integrator charge gain is programmable via eight binary weighted feedback capacitors. The maximum total feedback capacitance is approximately 5 pF, and the integrator dynamic range is at least 2 V, giving a maximum charge capacity of at least 10 pC. The integrator design is optimized for negative input charge. If the input is positive charge, then VREF can be raised for opposite polarity operation, although the total available range will be reduced. An on-chip input charge injection circuit is included at the integrator input which can be used to cancel the charge injection of transistor switches on the pixel array. The integrator output feeds the sample capacitors through a resistor whose value is programmable via the BW1-3 control input lines. The resultant time constant (RC) determines the effective system bandwidth. The integrator output risetime is designed to be fast compared to RC so that the system risetime and noise bandwidth will be determined to first order only by the bandwidth setting, and not by the input capacitance or bias current. Of course, the total equivalent input referred noise of MASDA-X depends on several factors, including noise bandwidth, total input capacitance, and integrator input transistor bias current.

Figure 3 is a timing diagram which shows the important signals during typical operation. A high level of the control signal indicates closure of the associated switch on Figure 2. Four external logic signal inputs are necessary for signal acquisition: ABSEL (pipeline A/B select, which determines the internal routing of the other control signals to the A or B set of capacitors), IRST (integrator reset), SBEF (before sample), and SAFT (after sample). At the start of a cycle, IRST should be raised for at least 1 us to fully reset the integrator. Depending on the state of ABSEL, either RSTA or RSTB is derived from IRST so that the A or B set of capacitors is reset along with the integrator. In like manner, SBEFA and SBEFB are generated internally from SBEF, and SAFTA and SAFTB are generated from SAFT, depending on the state of ABSEL. SBEF should be held high during integrator reset and lowered to take the before sample only when the voltage on the sample capacitor has settled after integrator reset release (at least 3RC). This time thus depends on the programmed bandwidth. Failure to observe this rule will result in higher noise. At least 2 ns after SBEF is lowered, SAFT is raised to connect the after sample capacitor to the integrator. At the same time, the pixel is connected to the input, applying the signal to the integrator. After integrating for the desired time period, SAFT is lowered to take the after sample. This completes one acquisition cycle, and ABSEL is toggled in order to proceed with the next cycle on the

other set of capacitors.

If integrator input charge injection is desired in order to cancel charge injection associated with the switch on the pixel array which connects the pixel to the integrator input, a DC voltage difference should be supplied between the VINJP and VINJN pins. A voltage step of this magnitude is then automatically applied through a 1.5 pF injection capacitor to the input at the time when SAFT goes high.

2. Readout.

While signal acquisition is occuring on one set of capacitors, the other set of capacitors must be multiplexed to a common differential output bus for all channels sequentially. The simplest approach would be to just connect a desired capacitor via a switch to the common output bus at the appropriate time. However, this results in errors which can greatly reduce accuracy. An output bus has a significant parasitic capacitance, which would result in a charge sharing "memory error" due to the voltage remaining on the bus from the previous channel's capacitor readout. Even without memory errors, the parasitic bus capacitance is a nonlinear function of voltage, and would cause nonlinear charge sharing between a sample capacitor and the bus. In order to preserve accuracy and linearity, the scheme shown in Figure 2 is implemented. Precharge amplifiers (one for each bus per channel) are used to precharge an output bus to the sample capacitor voltage, within some uncertainty, with minimal disturbance of the value of the capacitor voltage. The amplifier is then disconnected from the bus and the capacitor itself is connected directly to the bus, which ideally brings the bus voltage to exactly the capacitor voltage. This method eliminates any memory error due to the previous voltage on the bus. Also, there will be no charge sharing error if the bus is precharged to exactly the capacitor voltage. However, there is an uncertainty in the bus precharge voltage due to random amplifier noise and a random but relatively constant amplifier offset voltage. The final bus voltage will be in error by the amount of the precharge uncertainty divided by the factor (Csample/Cbus). Since Csample is substantially larger than Cbus, the amplifier noise portion of the uncertainty is reduced by this factor to a level well below the intrinsic integrator noise. The offset portion of the uncertainty is also reduced by this factor and simply becomes part of the pedestal, to be absorbed by external calibration. Nonlinear charge sharing errors apply only to the small offset, and not to the full capacitor voltage. Therefore, even with a nonlinear bus capacitance, the errors have been reduced to an acceptably small value and the linearity preserved.

The MASDA-R chip used a precharge scheme in which each of the four capacitors per channel had its own precharge amplifier. This is a simple approach, but a drawback is that there are pedestal differences between the A and B capacitors of a given channel, caused by the precharge amplifier offsets. In the MASDA-X chip, the A and B capacitors use the same precharge amplifier, so that only one gain and offset calibration is needed per channel. However, this is a more complicated arrangement which requires additional switching. Also, there is a memory error effect between the A and B capacitors at the precharge amplifier input! Thus the amplifier input is always discharged to a constant reference voltage before being connected to a capacitor. The amplifiers are therefore designed to have low and constant input capacitance, so that significant charge sharing errors are not introduced when connecting the capacitor to the amplifier input.

The MASDA-X bus precharge scheme is more complicated than that of the MASDA-R chip, but this is actually transparent to the user. As with MASDA-R, readout of all channels is accomplished with a single CLK line. The required switching is all controlled with internal logic. As shown in Figure 3, toggling the CLK input after changing the state of ABSEL will multiplex the proper capacitors to the output. When CLK is high, a channel which is being read out is in *bus precharge* mode. This mode should be held until the chip outputs have finished slewing. Then CLK is lowered, placing the channel in *mux* mode, which quickly brings the output to its final value. Since each clock cycle reads out one channel, 64 cycles are required to read out the complete chip in 64 channel mode. When all channels have been read out, the state of ABSEL can be changed to begin readout on the other set of sample capacitors. The required duty cycle of the CLK input depends on how long it takes the outputs to slew in precharge mode (CLK high, ~ 500 ns maximum) and how long the final value needs to be held for an external digitizer (CLK low).

Since the precharge amplifiers are always started from an internal reference voltage, there will be slewing back and forth between this reference voltage and the actual output voltages of the channels on the "after" output bus. To avoid unnecessary slewing, a selectable option exists which uses a comparator to sense when the "after" precharge amplifier output is near its final value. This comparator is used to control when the amplifier output is connected to the bus. The "after" output then slews only from one channel's output level to the next, and not back to the reference voltage. This option is enabled by default, and can be disabled by grounding the CPSEL pin.

Pad Assignments

Channel input pads are distributed on the west side of the chip on an effective 80 micron pitch. A continuous column of pads is provided for tab bonding, and two staggered columns of pads are provided for wire bonding. Channels are stacked north-south on an 80 micron pitch. All other chip inputs and outputs (power, control, analog outputs, etc.) are on the east, or "control" side. The chip layout dimension is approximately 11026 microns (north-south) by 4704 microns (east-west). The final cut dimension will be slightly larger. There are 49 control pads on the east side evenly spaced at 225 micron pitch. These are numbered 1-49, starting in the northeast corner of the chip and proceeding south. Following is a listing of all of the control pads, including detailed information about required connections, signal levels, bias, etc.

1. **AGND1**: Analog ground. Tie directly to common low impedance ground plane.

2. **AVDD1**: Analog VDD = +3.5V. Absolute maximum = +3.6V. Should be bypassed to ground close to the chip.

3. **VREF**: DC reference voltage input which sets the integrator reset point. Supplied externally with resistive divider, bypassed with 0.1uF. Thevenin resistance must be < 1K. With negative integrator input signal polarity, set VREF voltage as low as possible for linear operation (approximately .8V). For positive input signal polarity, VREF should be set higher (up to approx. 2.1V) to allow the integrator output to swing negative. The signal range available for this polarity is reduced.

4. **VREF2**: Can be used in conjunction with the VREF pin to form a temperature compensated reference voltage to maintain the maximum possible range. Leave floating if unused. To use, connect 6.8K resistor from VREF to AVDD, and 0.1uF bypass from VREF to ground. Connect appropriate resistor from VREF2 to ground to obtain desired VREF voltage (approx. 250 ohms).

5. **ISET**: Bias current set for integrator. Connect appropriate resistor from ISET pin to ground. May require bypass from ISET to AVDD. Maximum bias current (800 uA) is achieved with a 2.5K resistor.

6-8. **BW1-3**: Integrator bandwidth select pins. If unconnected, they will be pulled high internally, giving minimum bandwidth. Grounding the BW pins increases the bandwidth. The three pins have binary weighted significance, with BW1 being the LSB.

9-16. **PG1-8**: Integrator programmable charge gain select pins. If unconnected, they will be pulled high internally. Grounding a PG pin inserts a capacitor into the integrator feedback loop, decreasing the gain and increasing the charge capacity. The capacitors associated with the PG pins have binary weighted significance, with PG1 being the MSB. The PG1 capacitor is nominally 2.56 pF, and the PG8 capacitor is nominally 0.02 pF.

17. **OUT1-**: Analog minus output for channels 0 - 15. The minus output presents the result of the integrator "before" sample. If the chip is in 64 channel mode, OUT1- is inactive. All the analog outputs (OUT1-8) can drive 2K ohms in parallel with 200 pF.

18. **OUT1+**: Analog plus output for channels 0 - 15. The plus output presents the result of the integrator "after" sample. If the chip is in 64 channel mode, OUT1+ is inactive.

19-20. **OUT2-,+**: Analog output for channels 16 - 31. If the chip is in 64 channel mode, OUT2-,+ presents the output for channels 0 - 63.

21-22. **OUT3-,+**: Analog output for channels 32 - 47. If the chip is in 64 channel mode, OUT3-,+ is inactive.

23-24. **OUT4-,+**: Analog output for channels 48 - 63. If the chip is in 64 channel mode, OUT4-,+ is inactive.

25. **OBVDD**: Output buffer VDD. Absolute maximum = +3.6V. OBVDD can share the same external power supply as AVDD if they are brought together only at a bypass capacitor.

26: **OBGND**: Output buffer ground. Tie directly to common low impedance ground plane.

27-28. **OUT5-,+**: Analog output for channels 64 - 79. If the chip is in 64 channel mode, OUT5-,+ is inactive.

29-30. **OUT6-,+**: Analog output for channels 80 - 95. If the chip is in 64 channel mode, OUT6-,+ presents the output for channels 64 - 127.

31-32. **OUT7-,+**: Analog output for channels 96 - 111. If the chip is in 64 channel mode, OUT7-,+ is inactive.

34-34. **OUT8-,+**: Analog output for channels 112 - 127. If the chip is in 64 channel mode, OUT8-,+ is inactive.

35. **16/64**: 16 or 64 channel multiplexer mode select. If unconnected, the pin is pulled high internally, selecting 64 channel operation. In this mode, only the OUT2 and OUT6 analog outputs are active. Grounding the 16/64 pin selects 16 channel operation. In this mode, all analog outputs OUT1-8 are active.

36. **DIR**: Channel readout direction select. Unconnected, the pin is pulled high internally, and sequential channel readout progresses from low to high numbered channels. If grounded, readout progresses from high to low numbered channels.

37. **ABSEL**: A/B select control pin. The chip is pipelined with two sets (A and B) of sample and hold capacitors for each channel. When ABSEL = +3.5V (high), the A set of S/H's is read out while the B set of S/H's acquires the signal. When ABSEL = 0V (low), the situation is reversed. After bringing ABSEL from low to high the first time after power up, the chip is able to acquire data on the B sample and holds, but the analog data that is read out is invalid (since none has been acquired yet on the A side).

38. **IRST**: Integrator reset. Bringing IRST high resets all integrator outputs. Minimum reset time required = 1 us.

39. **SBEF**: Sample and hold "before" sample control. Internally routed to whichever set of sample and holds is selected for acquisition by the ABSEL line. Holding SBEF high connects the appropriate before sample capacitor to the integrator output. Lowering SBEF disconnects the capacitor, taking the sample. SBEF should be raised high with IRST and lowered after IRST falls and the integrator has had time to settle (3-5 RC after IRST falls, see Risetime Specifications).

40. **SAFT**: Sample and hold "after" sample control. Should be held low until at least 2 ns after SBEF falls, then raised high to connect the after sample capacitor to the integrator output. Pixel input signal should be applied to the input when SAFT is raised. Typical integration period (SAFT high) is 30 us. Lowering SAFT takes the "after" sample.

41. **CLK**: Readout clock. When the sense of the ABSEL line is changed, the readout logic is reset, readying the channels for readout. The clock should be low when ABSEL is changed. Thereafter, each positive transition of the clock multiplexes the next channel's analog data to the output for readout. When the clock is high, the readout section is in precharge mode, which charges the internal multiplexer buses to approximately the sample cap voltages and causes the output drivers to slew. This mode MUST be held until the outputs are done slewing (approximately 500 ns) in order to avoid internal errors due to charge sharing. When CLK is brought low, the sample caps are then directly connected to the internal multiplexer buses, and the outputs will be valid in a short time (<100 ns). The duty cycle of the clock thus depends on the precharge time and the readout rate.

42: **DVDD**: Digital VDD = +3.5V. Absolute maximum = +3.6V. DVDD can share the same external power supply as AVDD if they are brought together only at a bypass capacitor.

43: **DGND**: Digital ground. Tie directly to common low impedance ground plane.

44. **CPSEL**: Option which enables internal comparators that prevent the internal analog multiplexer buses from being precharged until the precharge amplifiers have reached close to final value. Prevents needless slewing by the analog outputs. If unconnected, CPSEL is pulled high internally and the option is enabled. Grounding CPSEL disables the option.

45-46. **VINJP, VINJN**: Charge injection set voltage. At the time of SAFT going high, a negative charge of magnitude (VINJP - VINJN) * (1.5pf) will be injected into the input of the integrator. Typically VINJN should be tied to ground, and VINJP tied to a positive DC reference voltage (no larger than +3.5V). If positive charge injection is desired, VINJN and VINJP should be reversed. If no charge injection is desired, both VINJP and VINJN should be grounded.

47. **SUBS**: Chip substrate. Tie directly to common low impedance ground plane.

48. **AVDD2**: Analog VDD = +3.5V. Absolute maximum = +3.6V. Should be bypassed to ground.

49. **AGND2**: Analog ground. Tie directly to common low impedance ground plane.

Risetime and Noise Specifications

The risetime at a sample/hold capacitor is limited by the simple RC filter formed by the sample capacitor and a resistor whose value is programmed by the BW1-3 pins. The nominal time constants of the filter are as follows:

BW = 0: RC = 180 ns
BW = 1: 360 ns
BW = 2: 540 ns
BW = 3: 720 ns
BW = 4: 900 ns
BW = 5: 1080 ns
BW = 6: 1260 ns
BW = 7: 1440 ns

For a given BW setting, the SBEF line should not drop low (taking the before sample) until at least 3RC after IRST drops in order to keep the noise as low as possible (>5RC offers no improvement).

The equivalent input noise of the integrator is predicted by HSPICE simulations with Cfb = 0.16 pF and Cin = 70 pF. To first order, the equivalent input noise should be linearly related to Cin but

should not be affected by Cfb.

For BW = 0: Noise = 125 e + 12.5 e/pF.

For BW = 1: Noise = 100 e + 9 e/pF.

For BW = 3: Noise = 80 e + 6.4 e/pF.

For BW = 7: Noise = 65 e + 5 e/pF.

Power Consumption

The current draw for different sections of the chip is as follows (3.5V supply):

Integrator: (2Iset + 210 uA)/channel
Precharge amplifiers: 200 uA/channel
Driver: 4.6 mA/driver (applies to one differential output driver). Eight drivers are active in 16 channel mode, two are active in 64 channel mode.

Note that if the integrator bias current (ISET) is set to its maximum value of 800 uA, the total chip power dissipation will be approximately 930 mW for one chip in 64 channel mode. If ISET is instead set to 400 uA, the noise performance will be somewhat worse but the chip power dissipation is a much lower 530 mW. Unless the lowest possible noise is required, ISET should be set at lower than the maximum value to avoid heat problems.

Static Protection

All analog inputs have back biased diodes per H.P. recommendations for ESD protection. Digital inputs have back biased diodes plus a series resistance feeding a secondary protection element. Secondary protection cannot be used on the analog inputs due to an unacceptable increase in the noise.

Even though all inputs have some protection, ESD safe handling precautions should always be observed, since the chip can still be susceptible to damage.

References

[1]. R. Yarema, et. al., "A Programmable, Low Noise, Multichannel ASIC For Readout of Pixelated Amorphous Silicon Arrays," presented at the 8th European Symposium of Radiation Detectors, June 14-17, 1998, Schloss Elmau, Germany. Submitted to NIM.

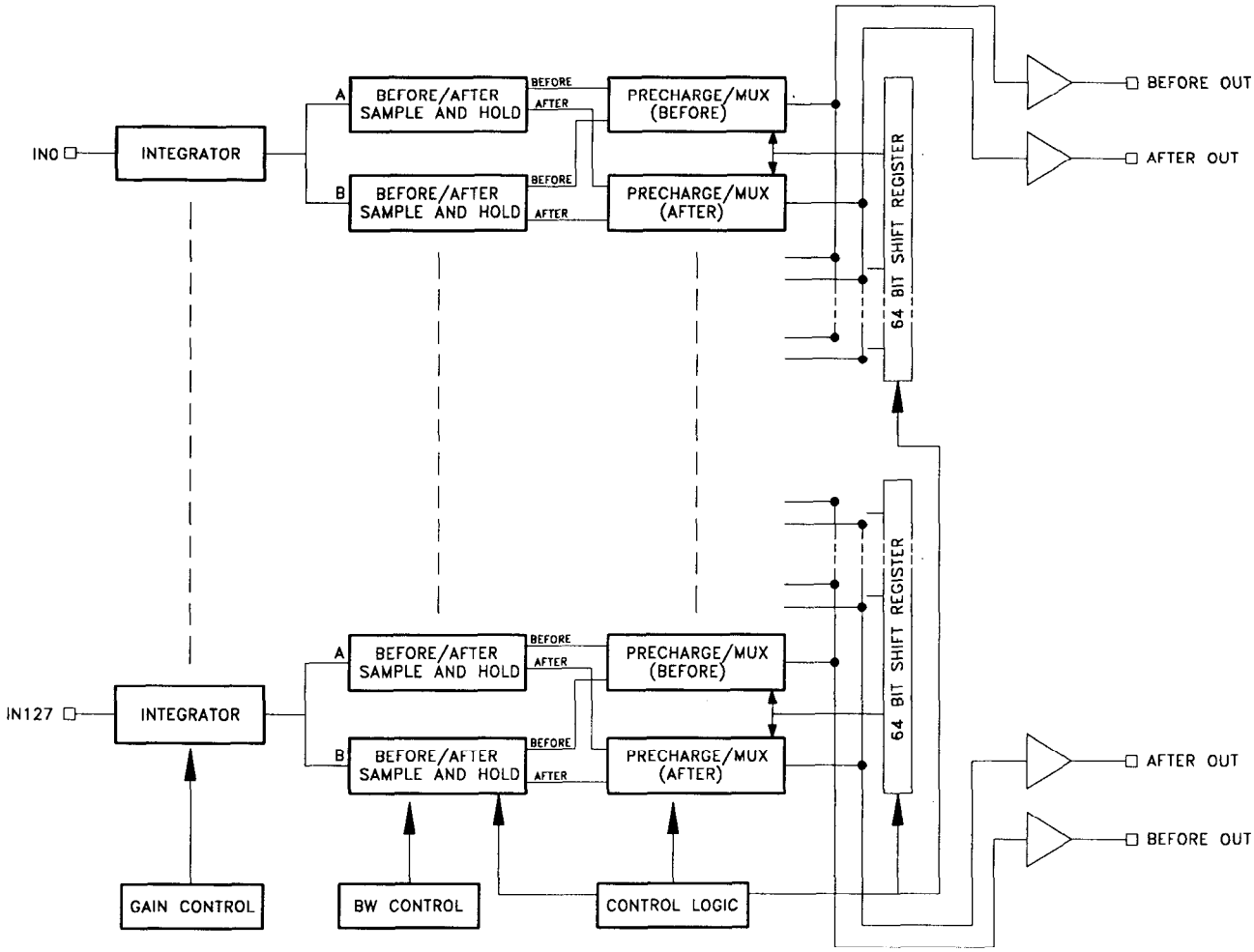


FIGURE 1. MASDAX BLOCK DIAGRAM

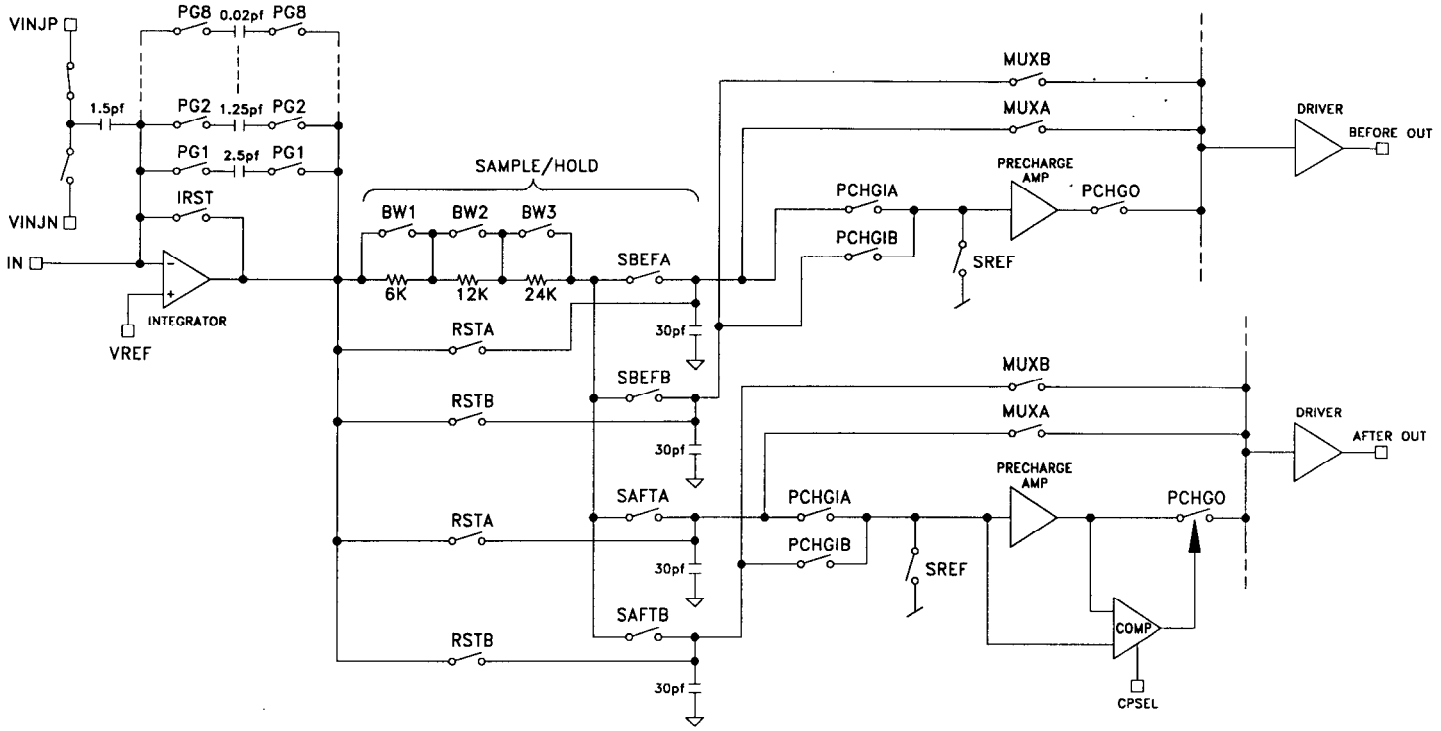
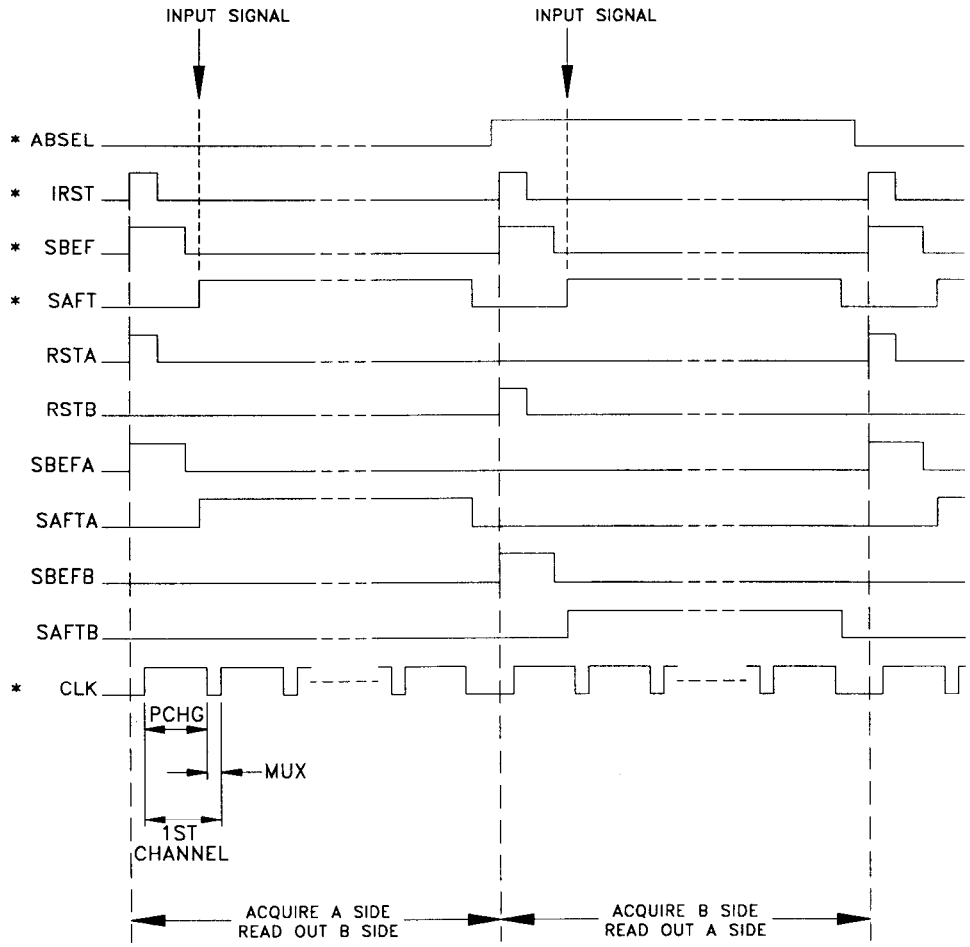
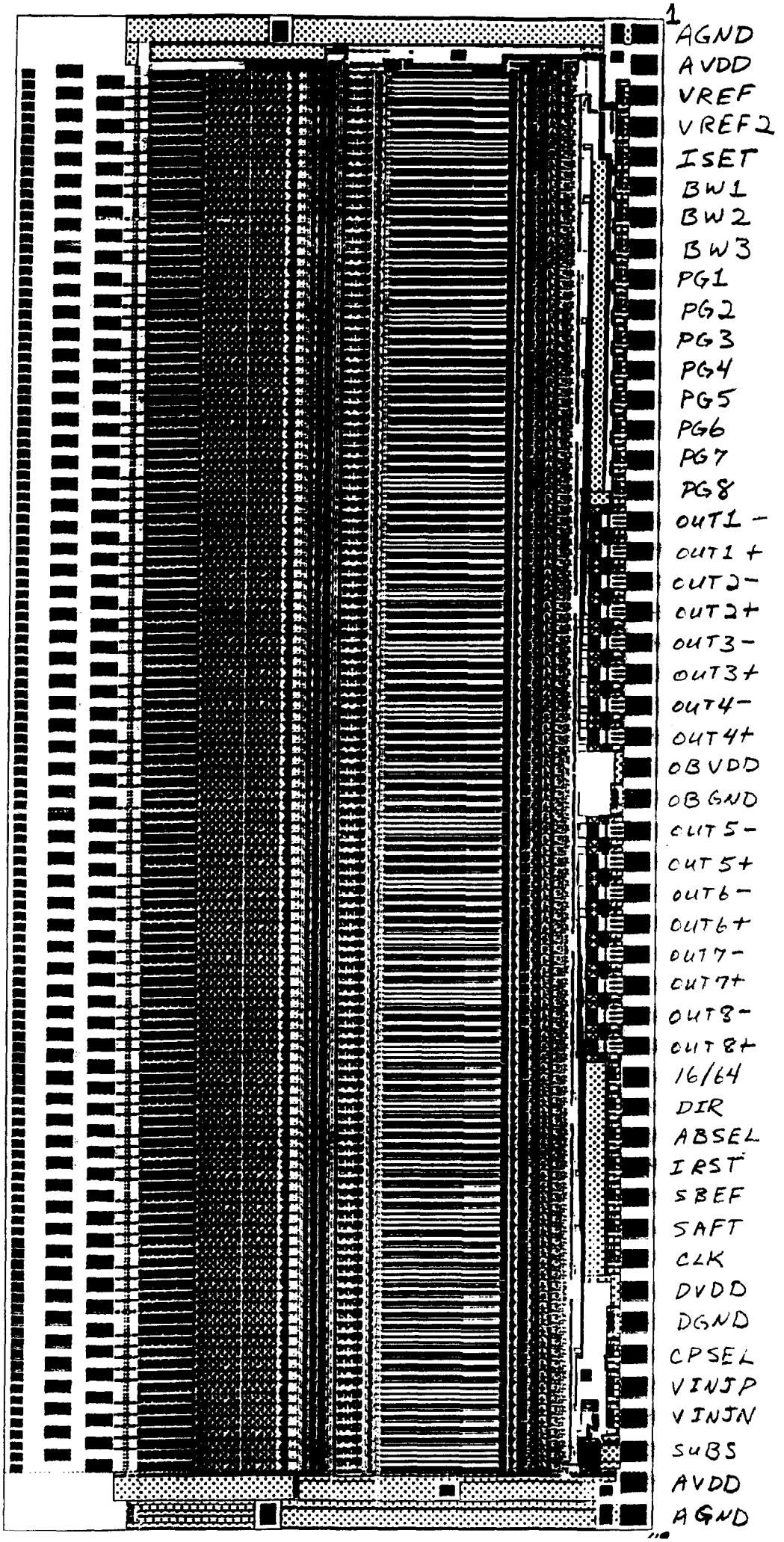


FIGURE 2. SINGLE CHANNEL



* = CHIP INPUT CONTROL SIGNAL

FIGURE 3. TIMING DIAGRAM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AGND
AVDD
VREF
VREF2
ISET
BW1
BW2
BW3
PG1
PG2
PG3
PG4
PG5
PG6
PG7
PG8
OUT1 -
OUT1 +
OUT2-
OUT2+
OUT3-
OUT3+
OUT4-
OUT4+
OBVDD
OBGND
OUT5-
OUT5+
OUT6-
OUT6+
OUT7-
OUT7+
OUT8-
OUT8+
16/64
DIR
ABSEL
IRST
SBEF
SAFT
CLK
DVDD
DGND
CPSEL
VINJP
VINJN
SUBS
AVDD
AGND