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K. Tsoukalas,[1,a)] F. Schupp,[1] L. Sommer,[1] I. Bouquet,[2] M. Mergenthaler,[1] S. Paredes,[1] N. Vico Triviño,[1] M. Luisier,[2] G. Salis,[1] P. Harvey-Collard,[1] D. Zumbühl,[3] and A. Fuhrer[1]

AFFILIATIONS

[1]IBM Research Europe – Zürich, Säumerstrasse 4, 8803 Rüschlikon, Switzerland
[2]Integrated Systems Laboratory, ETH Zürich, 8092 Zürich, Switzerland
[3]Department of Physics, University of Basel, Klingelbergstrasse 82, 4056 Basel, Switzerland

[a)]**Author to whom correspondence should be addressed:** kts@zurich.ibm.com

ABSTRACT

Metal contacts in semiconductor quantum electronic devices can offer advantages over doped contacts, primarily due to their reduced fabrication complexity and lower temperature requirements during processing. Some metals can also facilitate ambipolar device operation or form superconducting contacts. Furthermore, a sharp metal–semiconductor interface allows for contact placement in close proximity to the active device area avoiding damage caused by dopant implantation. However, in the case of gate-defined quantum dots in intrinsic silicon, the formation of a Schottky barrier at the silicon–metal interface can lead to large, nonlinear contact resistances at cryogenic temperatures. We investigate this issue by examining hole transport through metal oxide-semiconductor transistors with platinum silicide contacts on intrinsic silicon substrates. We extract the contact and channel resistances as a function of temperature and improve the cryogenic conductance of the device by more than an order of magnitude by implementing meander-shaped contacts. In addition, we observe signatures of enhanced transport through localized defect states, which we attribute to platinum clusters in the depletion region of the Schottky contacts that form during the silicidation process. These results showcase the prospects of silicide contacts in the context of cryogenic quantum devices and address associated challenges.

Metal oxide-semiconductor field effect transistors (MOSFETs) with doped contacts have been widely used in the semiconductor industry. However, the stochastic nature of the dopant implantation processes might impose limitations on further scaling, for example, the channel length. Metallic contacts could be a viable alternative since they can form atomically abrupt interfaces with the semiconductor channel.[1] In addition, transistors with metallic contacts show lower parasitic source–drain resistance[2,3] and require lower thermal budgets in a simpler fabrication process. Some material combinations can also enable ambipolar contacts such that a single device can operate in the hole or electron regimes.[3,4] For transistor applications, metallic contacts are mostly used in novel devices made from, for example, organic materials,[5] 2D materials,[6,7] or carbon nanotubes.[8,9] The contact resistance in these devices can be relatively low because the Schottky barrier (SB) formed at the interface between the metal and semiconductor is either thin, yielding high transmission of the relevant charge carriers, or low compared to their thermal energy, for example, due to Fermi level pinning.[10,11]

At cryogenic temperatures, the combination of SB contacts and a low thermal energy of the charge carriers can result in large contact resistances. While this can render metallic contacts less attractive for cryogenic MOSFETs, other types of cryogenic devices can benefit, for example, when superconducting contacts are required[12–14] or when the SBs themselves serve as the confinement barriers of a quantum dot.[15]

In silicon quantum dots, metal contacts have enabled ambipolar operation[16] of spin qubit devices that exhibited high fidelity spin control.[17,18] However, the contact resistance of these devices has been very high, even compared with the large resistance of the quantum dots.[16,19] This makes it difficult to measure Coulomb blockade in transport at low bias, and for charge sensing it decreases the readout bandwidth and the signal-to-noise ratio.[20] As silicon is one of the leading host materials for spin qubits, and it is known that doping can have detrimental effects,[21,22] a thorough investigation of metal silicide contacts for intrinsic silicon is needed. Previous studies have discussed contacts with nickel silicide[23] at room temperature and aluminum

silicide[19] at cryogenic temperature. Although platinum silicide (PtSi) forms a lower SB for holes than nickel or aluminum, it has only been studied in doped silicon substrates in the context of classical electronics applications.[23–25]

We investigate PtSi contacts to intrinsic silicon substrates at cryogenic temperatures with the prospect of integration in spin qubit devices. Figure 1(a) shows a spin qubit device consisting of two silicide contact regions next to two lead gates (LG1, LG2), which are used to accumulate carriers between the contacts and the active area of the device.[17] Between the lead gates, nanoscale plunger gates (P1, P2) define the electrostatic potential that confines single carriers (holes) into QDs [Fig. 1(b)]. In order to study and optimize the cryogenic behavior of the silicide contacts, we fabricate simplified test devices where we omit the plunger gates and instead use a single large gate, as in a SB metal oxide field effect transistor (SBMOSFET) [Fig. 1(d)]. We focus on PtSi contacts fabricated on a (100) near-intrinsic silicon substrate ($\rho > 10\,000\,\Omega\,\mathrm{cm}$) and incorporated in MOSFET devices, as a testbed for integration with silicon hole spin qubits.[17,18]

Silicide contacts are defined using electron-beam lithography (EBL); a patterned polymethyl methacrylate (PMMA) resist serves as an etch mask to selectively remove a 7 nm-thick thermally grown silicon dioxide (SiO_2) in the contact regions using hydrofluoric acid, followed by evaporation and liftoff of a 20 nm-thick platinum film. Silicidation is achieved with a rapid thermal anneal. Subsequently, an isolation dielectric (7 nm HfO_2 then 4 nm SiO_2) as well as the gate metal (20 nm TiN) are grown by atomic layer deposition. The resulting stack is shown in Fig. 1(f). The gate is patterned by EBL using hydrogen silsesquioxane (HSQ) resist followed by a metal etch in an HBr inductively coupled plasma, with the dielectric below serving as an etch stop. The chip is packaged in 100 nm of SiO_2 deposited with plasma enhanced chemical vapor deposition. Finally, tungsten bondpads are connected to the silicide contacts and the gate with vias that are patterned by EBL and reactive ion etching. The device geometry includes sufficient overlap of the gate and the silicide to ensure direct gating of the silicide–silicon interface, independently of variations in the gate-to-contact alignment or lateral silicide growth. Using EBL allows us to quickly assess various meander-shaped contact geometries, as shown in Figs. 1(d) and 1(e), that can increase the interface length and decrease the contact resistance while retaining the footprint of the contact.

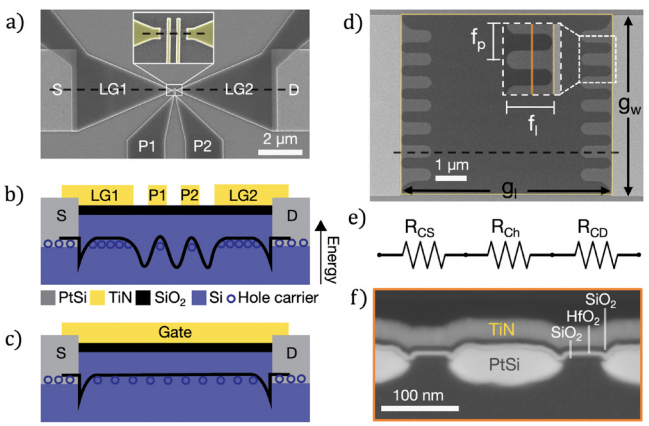

FIG. 1. (a) Scanning Electron Microscope (SEM) image of a silicon FinFET double QD device. (b) Schematic cross section along the black dashed line in (a), of a double QD device with a sketch of the valence band profile when the device is tuned into the few hole regime for both QDs. S and D denote the source and drain contacts, respectively, while LG1 and LG2 denote the lead gates and P1 and P2 the plunger gates. (c) Cross section of the SBMOSFET device used to characterize contacts. (d) SEM image of a SBMOSFET with meander contacts. The device dimensions are indicated as follows: gate width (g_w), gate length (g_l), meander finger pitch (f_p), and meander finger length (f_l). The gate boundary is highlighted with a yellow line. (e) Equivalent circuit of a SBMOSFET consisting of the contact resistances (R_{CS}, R_{CD}) of the source and drain as well as the channel resistance (R_{Ch}). (f) Transmission electron microscope cross section of a single meander finger of a meander contact with $f_p = 200$ nm.

Platinum silicide forms from a platinum surface layer in two stages, starting with a metastable Pt_2Si phase before converting into a stable PtSi phase.[26,27] The atomic diffusion and reaction rates are controlled mainly by the annealing temperature.[28,29] The stable PtSi phase is expected to form a lower SB with silicon than Pt_2Si.[25,30,31] To verify complete silicidation, x-ray diffraction and Kelvin Probe Force Microscopy were performed to map out the stoichiometry and work function of PtSi contacts as a function of different annealing parameters (see the supplementary material). From this analysis, we conclude that the optimal conditions for complete PtSi formation are an anneal duration of 300 s at a temperature of 450 °C. These parameters are used for all the studied SBMOSFET devices below.

To quantify the SB height, we use electronic transport through a SBMOSFET device as a function of measurement temperature and gate voltage. By performing an Arrhenius analysis[32] on the acquired data, we extract a SB height of 170 ± 20 mV (Refs. 11, 33, and 34) (see the supplementary material). This value is lower than the values quoted in the literature, which range from 220 to 250 mV,[25,30,31] but similar to values extracted with the same technique elsewhere.[35] This discrepancy between the techniques can be attributed to the fact that thermally assisted tunneling modifies the temperature dependence of the measured current for gate voltages near flat-band conditions.

Figure 2(a) shows extraction of the contact and channel resistance as a function of temperature using the transfer length method (TLM).[36] We assume an equivalent electrical circuit with source (R_{CS}), drain (R_{CD}), and channel (R_{Ch}) resistances in series, as shown in Fig. 1(e). By comparing devices with identical contacts but varying channel lengths (l_{ch}), and by assuming a linear dependence of R_{Ch} on the channel length l_{ch}, both R_{Ch} and $R_C = R_{CS} + R_{CD}$ can be extracted separately. The channel length is defined as the distance measured from the middle of the source meander to the middle of the drain meander, $l_{ch} = g_l - f_l$. In Fig. 2(a), resistances for meander contact devices with $f_l = 1\,\mu$m, $g_w = 9\,\mu$m, $f_p = 200$ nm are shown, with f_l, g_w, and f_p as defined in Fig. 1(a), for three measurement temperatures at 300, 120, and 4 K. For these measurements, a source–drain bias $V_{ds} = 20$ mV was applied antisymmetrically. As expected, R_{Ch} decreases with more negative gate voltage (due to the increasing hole density) as well as with decreasing temperatures (due to a reduction in phonon scattering).[37] The behavior of R_C as a function of temperature and gate voltage is primarily attributed to thermally activated tunneling through the SB. As the temperature decreases, the tunneling probability diminishes because fewer thermally excited carriers attain an energy level that enables substantial tunneling probability through the SB. This characteristic behavior is exemplified at $V_g = -4$ V, where R_C increases from 5 kΩ at 300 K to 40 kΩ at 4 K. At room temperature, R_{Ch} significantly surpasses R_C, causing the device to behave as a

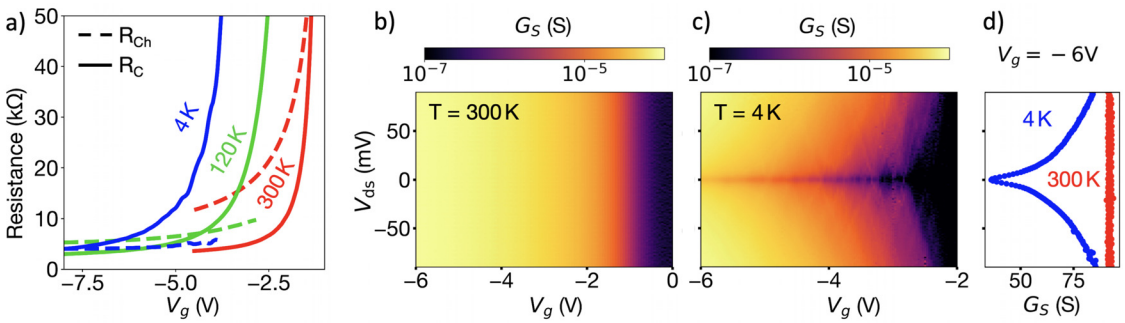

FIG. 2. (a) Channel (dashed curves) and contact resistance (solid curves) as a function of V_g at temperatures of 300 K (red), 120 K (green), and 4 K (blue) extracted using the TLM method. (b) and (c) Differential conductance $G_s = dI_{ds}/dV_{ds}$ at 300 K (b) and 4 K (c). (d) G_s at $V_g = -6$ V at temperatures of 300 K (red) and 4 K (blue).

traditional MOSFET, with resistance predominantly dictated by the channel, while the contact resistance remains orders of magnitude lower. However, at 4 K, R_{Ch} has stabilized around 4–6 kΩ, whereas R_C exhibits a strong dependence on V_g, spanning resistances from 5 to at least 50 kΩ. This dependence of the contact resistance on the gate voltage arises from the fact that in intrinsic substrates (with negligible doping densities) the width of the SB, near threshold, is to first order determined by the electric field between the gate and the contact. This electric field scales with $\Delta V_{d(s)-g} = V_{d(s)} - V_g$, and therefore the tunneling probability through the SB increases with decreasing gate voltage, leading to a reduction in contact resistance. It is important to note that this dependance of contact resistance on V_g is present even at 300 K, indicating that tunneling is significant even at higher temperatures.

To further analyze the impact of the SB contacts on device resistance, we turn to measurements of the differential conductance $G_s = dI_{ds}/dV_{ds}$ as a function of V_g and V_{ds}. Figure 2(b) shows a map of G_s for a device with $f_l = 1\,\mu$m, $f_p = 0.75\,\mu$m, and $g_w = l_{ch} = 6\,\mu$m at 300 K, where the conductance is dominated by the channel resistance and is therefore constant as a function of V_{ds}.

At cryogenic temperatures, however, where tunneling through the barrier is the predominant transport mechanism, there is a clear suppression of the conductance at low V_{ds} [see Figs. 2(c) and 2(d)] because the SB width depends on $\Delta V_{d(s)-g}$.[19,25] This suppression persists even at gate voltages far away from turn-on, for example, at $V_g = -6$ V, as shown in Fig. 2(d). The SBs therefore still add significantly to the contact resistance R_C at large negative gate voltages where one might expect the strong electric field to induce a thin enough barrier resulting in $R_{Ch} \gg R_C$. One reason for this weak tunability of the barrier width with the gate voltage is the screening of the electric field between gate and contact due to charge accumulation in the channel. Furthermore, it was suggested that depending on the shape of the metallic contact interface, the local electric field distribution may be unfavorable for efficient tuning of the Schottky barrier width with gate voltage.[3,38,39] We exclude electron–electron interaction effects[40] as the primary cause of the low bias conductance dip, since the observed conductance suppression persists at temperatures significantly above 4 K and at strong gate overdrive voltages, i.e., at very high carrier densities. In addition, the dip is absent in identical devices when using doped contacts [see supplementary material Fig. S3(c)].

To mitigate the high contact resistance, we adapt the shape of the contact to increase the SB interface length with the channel without increasing the device footprint. We choose a meander-shaped contact geometry where the width of a silicide finger is equal to the gap between two fingers with pitch f_p [see inset in Fig. 1(d)]. SBMOSFETs with straight contacts are fabricated as a control along with SBMOSFETs with meander-shaped contacts with varying f_p between 200 nm and 1 μm. The length of a silicide finger is fixed at $f_l = 1\,\mu$m. Figure 3 (left) shows the differential conductance at T = 4 K and $V_g = -6$ V for the low bias regime. As expected, we find that smaller pitches lead to a higher conductance and smaller contact resistance. Figure 3 (right) shows the conductance at $V_{ds} = 0$ mV and $V_{ds} = 0$ mV from the same measurements plotted against the interface length between contact and channel (L_C). For larger pitches, the conductance increases linearly with the interface length, as expected, but for pitches below 350 nm the conductance saturates. This is likely related to screening of the gate electric field in the narrow channel regions between the silicide meanders, leading to a partial overlap of the depletion regions. As a result, the SB cannot be tuned efficiently in these regions with increasing interface length, leading to a saturation of the contact resistance.

In Fig. 2(c), we also observe signatures of transport through localized states i.e., resonant transport peaks in the low source–drain bias

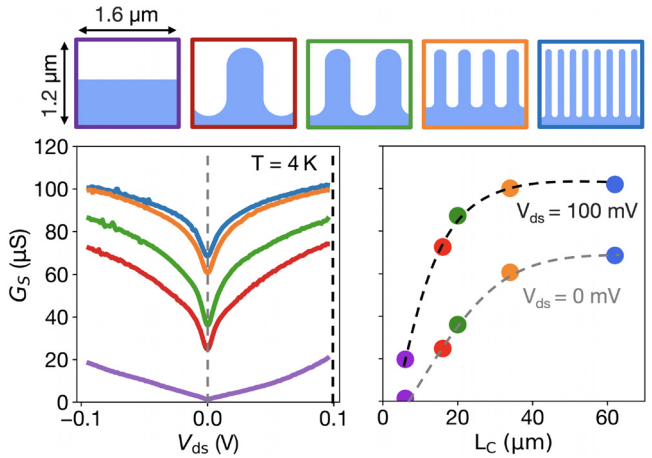

FIG. 3. Left: G_s as a function of V_{ds} at $V_g = -6$ V for different meander pitches: blue 200 nm, orange 350 nm, green 750 nm, red 1 μm, purple: straight. Right: G_s as a function of contact length L_C for $V_{ds} = 0$ mV and $V_{ds} = 100$ mV. The gray and black dashed curves are guides to the eye to illustrate the behavior of G_s vs L_C. The channel width l_{ch} of these devices is 6 μm.

regime at cryogenic temperatures. This becomes more evident when we take the numerical derivative with respect to the gate voltage, as is shown in Fig. 4 for three different devices with varying contact geometries. We consistently find similar resonances in various types of SBMOSFETs with PtSi contacts as well as in SBMOSFETs with nickel silicide contacts (see the supplementary material). On the other hand, we do not observe such resonances in devices with doped contacts (see the supplementary material), where the channel is the same but where no SB is present. Furthermore, in SBMOSFETs at cryogenic temperatures, the turn-on is dominated by the contact resistance and the channel is already highly accumulated in the gate-voltage region displaying the resonances [Fig. 2(a)]. We therefore exclude localized states in the channel as the source of these resonant features, meaning that the associated localized states must be in the vicinity of the SB depletion region.

Localized states in the barriers could originate from fixed charges in the nearby ALD oxide, atomic defects in the semiconductor, or Pt clusters that build up in the depletion region of the SB during the silicidation process. The latter was suggested previously in Refs. 41 and 42. To investigate the impact of trapped charges in the oxide, we have also measured a set of devices with various gate oxides featuring different ratios of HfO_2 to SiO_2 (see the supplementary material). Here, we do not observe more resonances in devices with higher HfO_2 content, even though HfO_2 is expected to have a much higher trap density.[43,44] This allows us to conclude that charges in the oxide are unlikely to be linked to the localized states in the barriers.

A critical difference between atomic defects and Pt clusters is that the former is energetically bound to the valence band edge while the latter can be charged and therefore have an independent chemical potential similar to a QD. In order to differentiate the two, we compare their gate lever arm (α_{gl}) to the one calculated for the valence band edge ($\alpha_{gv} = \frac{\Delta E_V}{\Delta V_g}$). From the resonant lines in Fig. 4, we extract α_{gl} in the range of 140–170 meV/V close to the turn-on voltage (see the supplementary material). This is of the same order of magnitude as the lever arm of Pt islands reported previously.[24,45] In contrast, we estimate the lever arm of the gate to the valence band edge in accumulation to be $\alpha_{gv} = 7.5$ meV/V for $m_h = 0.49\, m_0$ and $d_{ox} = 16$ nm [see supplementary material Eq. (S2)]. It is therefore unlikely that the observed resonances originate from localized states with energies tied to the valence band (e.g., lattice defects[42]). Instead, our findings are consistent with, for example, charged metallic clusters where the capacitive coupling to the environment determines the tunability as a function of gate– and source–drain bias voltage. We also note that the extracted α_{gl} reduces to a range of 70–100 meV/V for more negative gate voltages where the channel is highly accumulated. We interpret this as an increased capacitance of the localized states to the accumulated channel of the device, hence decreasing the ratio of the gate capacitance to the total capacitance. In addition, upon measuring SBMOSFETs with NiSi contacts, we find fewer signatures of localized states but similar lever arms (see the supplementary material) compared with the devices with PtSi contacts. We therefore suspect that the shape of the SB for NiSi or the diffusion properties during NiSi formation produces fewer silicide clusters in the SB depletion region.

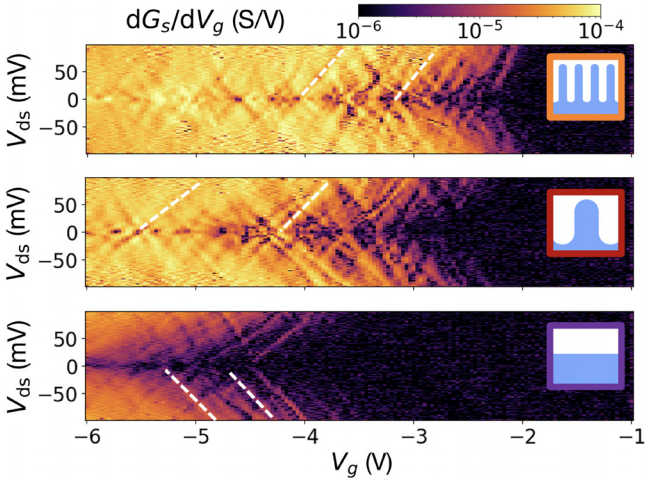

FIG. 4. Derivative of the conductance with respect to V_g as a function of V_g and V_{ds} in three devices with different contact geometries shown in the respective insets at 4 K. Top: 350 nm meander pitch. Middle: 1 μm meander pitch. Bottom: straight contact device. Dashed white lines indicate selected resonance lines that were used for lever arm extraction. The difference in the turn-on voltages between the plots originates from the different contact interface lengths of the devices.

In summary, we have developed and characterized PtSi SBMOSFETs with a focus on achieving low contact resistance at small source–drain bias and at cryogenic temperatures, a regime suitable for silicon spin qubits. After optimizing silicide formation conditions, we studied contributions of contact and channel resistance with decreasing temperature. We found that the SB resistance increases drastically with decreasing temperature, consistent with thermally assisted tunneling being the main transport mechanism. At cryogenic temperatures the implementation of meander-shaped contacts reduces contact resistance by more than an order of magnitude by increasing the effective SB interface length while preserving the device footprint. We also found that transport at low bias is enhanced by tunneling through localized states. This behavior persists in devices with different oxide stacks and for NiSi but disappears in devices with doped contacts. We argue that these localized states are not related to atomic defects but rather to Pt or PtSi clusters near the PtSi–silicon interface as indicated through gate lever arm characterization. Given that the devices are fabricated using intrinsic Si substrates, it is also unlikely that the localized states are linked to boron clusters as discussed in previous work.[46]

Our findings lead to a mixed conclusion on the potential of silicide contacts for quantum electronic devices. On the positive side, engineering the shape of the contacts, for example, with a meander-shaped interface or intentionally incorporating localized states in the SB depletion region could effectively reduce contact resistance. This can be achieved through diffused clusters from the silicide or the diffusion of dopants into the contact region near the silicide-to-channel interface.[47,48] While the latter approach involves a much higher thermal budget associated with activation anneals, it can be advantageous in avoiding implantation damage.[49,50] An alternative approach to improve the barrier transparency might be to further engineer the gate field distribution at the contact with a suitable three-dimensional contact shape, i.e., increasing the sharpness of the meander features used in our work. Here, the challenge is to concentrate the field in the semiconductor near the silicide and thus reduce the SB width while staying below any breakdown fields of the involved materials such as the gate oxide. These strategies hold the promise of creating high-transparency

contacts while also enabling interesting silicide contact properties such as superconductivity or ambipolarity. On the flip side, the presence of randomly distributed localized states can make the conductance of the device susceptible to mesoscopic voltage or charge fluctuations. Such fluctuations are expected to lead to noisy signals, particularly in applications like charge sensing with a single electron transistor. Additionally, the presence of random metallic islands or dopants near the semiconductor–silicide interface may hinder dense integration of quantum electronic devices since the requirement of maintaining a minimum distance between the pristine quantum channel and the disordered contact limits integration density.

See the supplementary material for additional data regarding the SB height estimation techniques, other dielectric and contact materials used as well as details on the lever-arm extraction.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Konstantinos Tsoukalas: Conceptualization (equal); Data curation (lead); Formal analysis (equal); Investigation (equal); Methodology (equal); Visualization (lead); Writing – original draft (equal); Writing – review & editing (equal). **Felix Julian Schupp:** Data curation (supporting); Formal analysis (equal); Investigation (supporting); Methodology (equal); Writing – original draft (lead); Writing – review & editing (equal). **Lisa Sommer:** Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Writing – original draft (supporting). **Ilan Bouquet:** Formal analysis (supporting); Software (equal). **Matthias Mergenthaler:** Investigation (equal); Methodology (supporting); Supervision (supporting); Writing – original draft (supporting). **Stephan Paredes:** Investigation (equal); Methodology (equal). **Noelia Vico Triviño:** Investigation (supporting); Methodology (supporting); Supervision (supporting). **Mathieu Luisier:** Investigation (supporting); Methodology (equal); Software (supporting); Supervision (supporting). **Gian Salis:** Formal analysis (supporting); Funding acquisition (supporting); Software (supporting); Supervision (supporting); Writing – review & editing (equal). **Patrick Harvey-Collard:** Resources (equal); Supervision (supporting); Writing – original draft (supporting); Writing – review & editing (equal). **Dominik Max Zumbühl:** Conceptualization (supporting); Funding acquisition (supporting); Supervision (supporting); Writing – review & editing (supporting). **Andreas Fuhrer:** Conceptualization (lead); Formal analysis (equal); Funding acquisition (lead); Methodology (equal); Supervision (lead); Writing – original draft (supporting); Writing – review & editing (lead).

DATA AVAILABILITY

The data that support the findings of this study are openly available in a Zenodo at (Ref. 51).

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