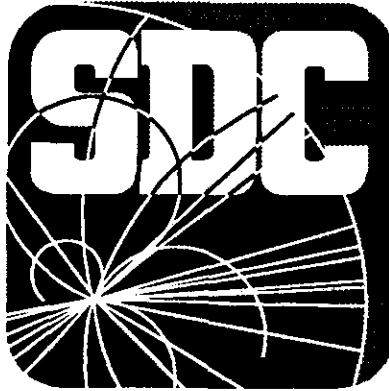




SDC SOLENOIDAL DETECTOR NOTES
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REVISED SDC TRIGGER COST

March 20, 1992

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1 Introduction

This document describes the Work Breakdown Structure (WBS) and Cost Estimate for the SDC Trigger System (WBS 5.3). This represents a revision of the previous cost estimate for the SDC Trigger System[7]. The SDC trigger system costed here is based on a particular implementation of the SDC trigger group conceptual design report [1]. The design has been revised[10] from the original described in [5]. The design has several subsystems. These include the Level 1 Decision Logic[9, 4, 2], the Level 2 Decision Logic[5] and the Trigger Clock and Control System[11]. The basic Level 1 Trigger system interfaces to front-end electronics crates on the detector for the calorimeter, shower max, tracking and muon subsystems. These are connected with optical fibers[8] to the counting house on the surface, which contains the level 1 decision processing crates. These include the Calorimeter Summation crates, the Track/Shower Max Match crates, the Electron Match crates, the Energy Sum/Jet Threshold crate[3], the Muon Trigger Crates, and the Final Decision crate.

The front-end electronics and trigger crates together form a pipeline structure in which data flows off of the detector crates on 1 Gbit/sec optical fibers into the Calorimeter Summation, Track/Shower Max Match and Muon Trigger crates. Data is transmitted from these crates to the Electron Match and Energy Sum/Jet Threshold crates[4] for further correlation before it is sent to the Final Decision crate. The Muon Trigger crates correlate muon segments with outer tracker segments and with quiet calorimeter regions and send this data to the Final Decision crate[2]. The trigger decision pipeline ends at the Final Decision crate[9], where a Level 1 Accept/Reject is generated and transmitted to the Global Clock/Control Crate for subsequent distribution to all DAQ and Level 1 Trigger crates. The Level 1 Crates which receive raw data directly from the front end trigger hardware on the detector contain Level 2 Interface Cards. These cards store copies of the raw data for which Level 1 Accepts were generated to be transmitted to the Level 2 Trigger. Each crate in the system has a backplane processor interface bus. This VME or similiar-type bus is used by the DAQ Interface/Processor card in each crate to program, control and monitor all of the cards in the system. Each crate in the system also has a Level 1 Clock/Control Board (L1CCB). This card receives the level 1 clock and trigger control information from the Global Level 1 Processor and distributes it to the cards in the crate.

2 Cost Estimate

2.1 Methodology

The cost for the trigger system was calculated by determining the numbers of ASIC's, boards, crates, and cables. Each electronics board was costed at 2 K\$, with 1.2 K\$ for parts, .4 K\$ for the board, and .4 K\$ for assembly. This cost is based on vendor quotes for manufacture and assembly of 270 9U x 400 mm deep 12-layer 83 MHz VME Trigger Boards built for the Zeus experiment. The quotes are attached as Appendix B. The cost for the SDC boards is increased somewhat to account for stricter impedance control necessary at anticipated speeds up to 125 MHz. Each crate was costed at 10 K\$, with 2.5 K\$ for hardware, 2.5 K\$ for power supplies, and 5 K\$ for the crate processor. Fiber optic links were costed at \$ 300 per link with 35% contingency. Each rack was assumed to contain three crates apiece and cost 8 K\$.

ASIC's and boards were divided into "easy", "average" and "hard" categories. Easy designs were estimated to take 1 man-year (MY) of engineering time. Average designs were estimated to take 2 MY and hard designs were estimated to take 3 MY of engineering time. In addition, each MY of engineering time was assumed to also use a MY of technician time, as well as 12.5 K\$ of expenses for travel, supplies and computing (i.e. CAD).

The trigger electronics was assumed to be contained in rows of racks in the counting house on the surface. The Level 1 cable paths between crates were based on the assumption that the Level 1 crates were contained in two rows 4 feet apart of 15 racks, with cables between non-nearby racks set to the length of the maximum path between the farthest crates, estimated to be 20 m. Cables between adjacent racks were estimated at 6 m and cables between crates in the same rack at 1 m. The cables and connectors were costed as shielded twisted pairs capable of operating at 63 MHz at a price of \$2 per pair per meter, plus a connector cost of \$2 per pair . In the WBS, the cable costs have been assigned to the driving end.

2.2 Interfaces

There are a number of boundaries in the cost responsibilities between the trigger and front end electronics systems. These have been established in joint consultation with front end electronics groups. For central and muon tracking systems, the segment finding is costed with the front end electronics and the segment linking and all that follows is costed with the trigger. For calorimetry, the front end electronics costs all generation of the 8-bit hadronic and electromagnetic sums and the trigger pays for the optical link to bring the data up to the counting house. For the boundary between Level 1 and Level 2, Level 1 pays for the transmission of the data to the Level 2 Interface card (including crate and backplane), while Level 2 pays for the card. For the boundary between DAQ and trigger, the trigger pays for its crate and processor cards, while the DAQ pays for all the links that connect to the processor cards.

2.3 Contingency

The costs listed in the budget estimate are the base costs of producing each item correctly the first time. There are also explicit costs listed for prototyping where required. The cost contingency is the cost required beyond the base cost to ensure successful completion. The calculation of contingency has been done for each WBS item. Each item has been assigned a technical risk factor, a cost risk factor and a schedule risk factor. Items that involve a new design that differs from established designs, but use existing technology received a technical risk factor of 6. Items that represent new designs that require R&D, but do not advance the state of art of the technology were assigned a technical risk factor of 8. Items with cost based on in-house estimates based on similar previous experience, were assigned a cost risk factor of 4. Items with cost based on in-house estimates based on minimal actual experience, but related to existing capabilities, were assigned a cost risk factor of 6. All trigger elements were assigned a schedule risk factor of 1 since they do not delay completion of other subsystems. Each risk factor was assigned a weight. The technical risk factor was assigned a weight of 4% since it involves a risk in both design and manufacturing. The cost risk factor was assigned a weight of 2% since it involves risk in both material cost and labor rate. The schedule risk factor used was 1%. Each risk was multiplied by its weighting factor and the total of these products was used as the total contingency for each item.

3 WBS Dictionary

- **5.3** This is the Work Breakdown Structure (WBS) for the Trigger System. There are three main sections to the WBS. Section 5.3.1 contains the Level 1 Trigger, section 5.3.2 contains the Level 2 Trigger, and section 5.3.3 contains the overall Trigger Project Management.
- **5.3.1** This is the WBS for the Level 1 Trigger. Section 5.3.1.1 contains the Level 1 Outer Tracking Trigger, section 5.3.1.2 contains the Level 1 Calorimeter Trigger, section 5.3.1.3 contains the Level 1 Muon Trigger, section 5.3.1.4 contains the Level 1 Silicon (inner) Tracking Trigger, section 5.3.1.5 contains the Level 1 Trigger Global Decision Logic, and section 5.3.1.6 contains the Level 1 Clock and Control System.
- **5.3.1.1** This is the WBS for the Level 1 Tracking Trigger. Section 5.3.1.1.1 contains the Local Processing for the Trigger, which is done in crates located on the detector. Section 5.3.1.1.2 contains the Regional Processing for the Trigger, which is done in the counting house on the surface.
- **5.3.1.1.1** This is the WBS for the Local, or on-detector, Processing for the Level 1 Barrel and Intermediate Tracking Triggers. The cost of the Barrel Trigger includes that of interfacing the front end and DAQ of the Tracking electronics to the trigger system clock and control by placing a Level 1 Clock and Control Board (L1CCB)[5, 11] in each front end crate. Additionally, it includes the cost of the 1 data optical fiber and 3 Clock and Control optical fibers for the L1CCB in each of the 16 barrel tracking crates. The cost of the Intermediate Tracking Detector (ITD) trigger includes the connection of a network of 20,800 slow speed (63 MHz) optical fibers from the ITD to

2 electronics crates, each containing 16 Tracking Boards that receive 650 fibers in 25 bundles of 26 fibers, where each bundle is brought to one of 25 ITD Trigger ASIC's that service 48 ϕ ITD strips. The crates also contain one ITD Tracking Trigger Control Board apiece. The crates also contain an L1CCB and its optical fibers. The ITD Tracking ASIC is considered to be a hard design (3 MY engineering). The ITD Tracking Trigger Board is considered to be an easy design (1 MY engineering). The ITD Tracking Control Board is considered to be an average design (2 MY engineering).

- **5.3.1.1.2** This is the WBS for the Regional, or counting-house, Processing for the Level 1 Tracking Trigger. This processing is contained in the 2 Track/Shower Max Match Crates. These Crates contain 16 Track/Shower Max Boards, which are estimated to be hard (3 MY engineering). The crates also contain a L1CCB. The cable costs represent the connections from the Track/Shower Max Match cards to the Electron Region Match Cards, and to the Correlated Muon Logic Cards.
- **5.3.1.2** This is the WBS for the Level 1 Calorimeter Trigger. Section 5.3.1.2.1 contains the Local Processing for the Trigger, which is done in crates located on the detector. Section 5.3.1.2.2 contains the Regional Processing for the Trigger, which is done in the counting house on the surface.
- **5.3.1.2.1** This is the WBS for the Local, or on-detector, Processing for the Level 1 Calorimeter and Shower Max Trigger. The cost includes that of interfacing the front end and DAQ of the Calorimeter and Shower Max electronics to the trigger system clock and control by placing a L1CCB in each front end crate. The Calorimeter front end electronics includes in its cost the circuitry to find energies in trigger towers to the inputs of 28, 52, or 32 optical fiber drivers for each Barrel, Intermediate, or Forward Calorimeter crate, respectively. The Shower Max front end electronics includes in its cost the circuitry to provide hits over threshold on the inputs to 1 or 2 optical fiber drivers for each Barrel or Intermediate Calorimeter crate, respectively. The trigger assumes the cost of transmitting the Calorimeter and the Shower Max information on optical fibers to the Calorimeter and Track trigger processing. An additional 3 optical fibers link the L1CCB to the Trigger Clock and Control system, for a total of 32, 57, and 35 fiber optic links per Barrel, Intermediate, and Forward Calorimeter front end crate, respectively.
- **5.3.1.2.2** This is the WBS for the Regional, or counting-house, Processing for the Level 1 Calorimeter Trigger. While Calorimeter Regional Processing comprises the most expensive subsystem in the trigger system, it participates in all four major Level 1 Triggers (Muon, Electron/Photon, E_T /Missing E_T , and Jets), and forms the backbone of three of those triggers. The regional processing is contained in the 31 Calorimeter Summation Crates and the 1 Energy Sum/Jet Threshold Crate. The Calorimeter Summation crates contain 8 Memory Lookup Boards, which have 9 Adder ASICs each. The crates each contain a single Calorimeter Energy Board, which continues the summation of energies from the Memory Lookup Boards, and also contains 9 Adder ASICs, for a total of 81 in each crate. These Crates also contain 2 Calorimeter Pattern Recognition Cards, which have 6 Pattern Recognition ASICs apiece. The Memory Lookup Board, Energy Board, and Pattern Recognition ASIC designs are considered to be average (2 MY engineering apiece), while the Pattern Recognition

Cards and Adder ASIC designs are considered to be easy (1 MY). This yields 8 MY total engineering for the Summation Crate system. The Energy Sum/Jet Threshold Crates contain 4 Energy Summation Cards and 4 Jet Threshold Summation Cards. The Energy Summation Cards also use 9 Adder ASICs each. Both boards are estimated to be average designs (2 MY engineering apiece), yielding 4 MY engineering for the Energy Sum/Jet Threshold Crates. All 31 of the Calorimeter Trigger Regional Processing crates contain an L1CCB. The cable costs reflect the connections from the Calorimeter regional crates to the Electron Region Match Cards, and to the Energy Sum and Jet Threshold Sum cards.

- **5.3.1.3** This is the WBS for the Level 1 Muon Trigger. Section 5.3.1.3.1 contains the Local Processing for the Trigger, which is done in crates located on the detector. Section 5.3.1.3.2 contains the Regional Processing for the Trigger, which is done in the counting house on the surface.
- **5.3.1.3.1** This is the WBS for the Local, or on-detector, Processing for the Level 1 Muon Trigger. The cost to the Trigger System includes only that of the 1 data optical fiber and 3 Trigger Clock and Control system optical fibers, plus a L1CCB, for each front-end crate.
- **5.3.1.3.2** This is the WBS for the Regional, or counting-house, Processing for the Level 1 Muon Trigger. There are 4 Muon Trigger Crates that contain 8 Correlated Muon Logic Cards (CMLC cards) and 4 Muon Histogram Summation Cards (HSC Card) each. The CMLC cards each contain 4 FIFO Delay ASICs. The Muon Logic Card is estimated to be a average design (2 MY engineering). As the requirements for the HSC card are fundamentally driven by the Electron Trigger, Engineering for the HSC card is budgeted in the Global System, Regional Processing WBS, Section 5.3.1.5.1, where the HSC card is used for Electron Detection. The ASICs are costed in Section 5.3.1.5.2, Global Processing Final Decision, with their engineering budgeted there. The crates also contain a L1CCB. The cable costs reflect the connections between the CMLC and HSC cards within each Muon Trigger Crate and the connections to the Final Decision crate.
- **5.3.1.4** This is the WBS for the Level 1 Silicon Tracking Trigger System. Since the Silicon tracking system does not provide information for the Level 1 Trigger, there is no processing of trigger information. Therefore, this WBS only contains the local processing sufficient to interface the Level 1 Trigger clock and control to the 64 Crates of the Silicon Tracking System in the counting house.
- **5.3.1.4.1** This is the WBS for the Local Level 1 Silicon Tracking Trigger System. This consists only of the circuitry to interface the Level 1 Clock and Control system to the Level 1 Tracking system. This includes one L1CCB per Silicon Tracking Electronics Crate. These electronics are located on the electronics counting house on the surface.
- **5.3.1.5** This is the WBS for the Global Level 1 Trigger system. Section 5.3.1.5.1 contains regional processing of Level 1 Triggers. Section 5.3.1.5.2 contains global processing of Level 1 Triggers. These electronics are located in the counting house on the surface.

- **5.3.1.5.1** This is the WBS for the Regional Processing of the Global Level 1 Trigger System. This processing is contained in the 8 Electron Match Crates. The Electron Match Crates each contain 8 Electron Region Match Cards (RMC Cards) and 3 Electron Hit Summation Cards (HSC Cards). Each Electron RMC Card also contains 3 FIFO Delay ASICs. Both boards are estimated to be average designs (2 MY engineering apiece). The engineering for the FIFO Delay ASIC is budgeted in Section 5.3.1.5.2, Final Decision Global Processing, which is the primary application for this ASIC. These crates also include an L1CCB.
- **5.3.1.5.2** This is the WBS for the Global Processing of the Global Level 1 Trigger System. This processing is contained in the Final Decision Crate. This Crate contains 7 total HSC Cards for Electron and Muon summations, an Energy Summation Card, and a Jet Threshold Summation Card. Each of these cards is also used in Regional Trigger processing and their engineering costs are assigned to the appropriate regional processing categories. Two cards must be designed for the Final Decision Crate. These are the Final Decision Memory Lookup Card and the Final Decision Logic Card. These cards are both average designs (2 MY engineering apiece). The Final Decision Memory Lookup Card also contains 9 FIFO Delay ASICs. This ASIC is considered a hard design (3 MY engineering).
- **5.3.1.6** This is the WBS for the Level 1 Trigger Clock and Control System. Section 5.3.1.6.1 contains regional distribution of the clock and control. Section 5.3.1.6.2 contains global processing of the clock and control.
- **5.3.1.6.1** This is the WBS for the Regional Distribution of the Level 1 Trigger Clock and Control. This includes 8 Local Clock/Control Crates which provide Clock and Control Signals for up to 64 Crates apiece, providing these signals for the 274 Front End Crates and 47 Trigger Crates. (There are a total of 56 Crates in the Global Level 1 Processor, 9 of which are for Global/Local Clock and Control, with the remaining 47 used for the Trigger Decision.) The Front End Electronics Systems are responsible for the the cost of the optical fiber links and L1CCB's in their crates. Each Local Clock/Control Crate contains a L1CCB and 16 Level 1 Clock and Control Fanouts (L1CCF). The L1CCB and L1CCF are average designs (2 MY engineering apiece). The engineering budget in this section also includes 2 MY for optic fiber link technology development.
- **5.3.1.6.2** This is the WBS for the Global Processing of the Level 1 Trigger Clock and Control. This is contained in the Global Clock/Control Crate. This Crate contains a Machine Clock Interface Card, a Beam Pickup Interface Card, a Deadtime Monitor Card, a Final Decision Interface Card, a Global Clock Master Card and a Global Control Master Card. Each of these boards is an easy design (1 MY engineering apiece) for a total engineering time of 6 MY. The crate also contains 4 L1CCF's and a L1CCB.
- **5.3.2** This is the WBS for the Level 2 Trigger. Section 5.3.2.1 contains the Level 2 Outer Tracking Trigger, section 5.3.2.2 contains the Level 2 Calorimeter Trigger, section 5.3.2.3 contains the Level 2 Muon Trigger, section 5.3.2.4 contains the Level 2 Silicon (inner) Tracking Trigger, and section 5.3.2.5 contains the Level 2 Trigger Global Decision Logic.

- **5.3.2.1** This is the WBS for the Level 2 Outer Tracking Trigger. This system consists of 12 Level 2 Interface Cards that reside in the 12 Level 1 Trigger Track/Shower Max Match Crates, as well as 4 Regional Crates with 16 Regional Cards and one Regional Master Card apiece.
- **5.3.2.2** This is the WBS for the Level 2 Calorimeter Trigger. This system consists of 24 Level 2 Interface Cards that reside in the 24 Level 1 Trigger Calorimeter Summation Crates, as well as 4 Regional Crates with 16 Regional Cards and one Regional Master Card apiece.
- **5.3.2.3** This is the WBS for the Level 2 Muon Trigger. This system consists of 6 Level 2 Interface Cards that reside in the 6 Level 1 Trigger Muon Crates, as well as 4 Regional Crates with 16 Regional Cards and one Regional Master Card apiece.
- **5.3.2.4** This is the WBS for the Level 2 Silicon Inner Tracking Trigger. This system consists of 4 racks with 8 crates containing printed circuit boards with 3 custom integrated circuits (Associate Memory Chip 1, Associate Memory Chip 2, L2TC Chip) and ECL logic. This is the WBS for the Overall Level 2 Trigger System.
- **5.3.2.5** This is the WBS for the Global Level 2 Trigger system. Section 5.3.2.5.1 contains regional processing of Level 2 Triggers. Section 5.3.2.5.2 contains global processing of Level 2 Triggers. These electronics are located in the counting house on the surface.
- **5.3.2.5.1** This is the WBS for the Regional Interface of the Global Level 2 Trigger System. This consists of 4 Regional Crates with 16 Regional Cards and 1 Regional Master apiece. This WBS contains the engineering for the Regional Cards and Regional Master Cards. Due to the system engineering involved, these are both hard designs (3 MY engineering apiece).
- **5.3.2.5.2** This is the WBS for the Global Processing of the Global Level 2 Trigger. This consists of a Global Processing Crate with 16 Global Logic Cards and a single Global Logic Master. Due to the system engineering involved, these are both hard designs (3 MY engineering apiece).
- **5.3.3** This is the WBS for the Project Management of the Trigger System. This involves engineering for system, resource, cost, schedule, and integration of the trigger system.

4 Hardware Requirements for the Level 1 Trigger System

4.1 Global Level 1 Processor Crate Counts

Table 1: Summary of Track/Shower Max Match Crate Usage (WBS 5.3.1.1.2)
Per Crate Coverage

Region	η	ϕ	Quantity
Central/Int. $0 < \eta < 3.0$	3.0	6.4	1
Central/Int. $-3.0 < \eta < 0$	3.0	6.4	1
Total Crates:			2

Table 2: Summary of Calorimeter Crate Usage (WBS 5.3.1.2.2)
Per Crate Coverage

Region	η	ϕ	Quantity
Barrel/Intermediate $-2.4 < \eta < 2.4$	0.8	1.6	24
Intermediate $2.4 < \eta < 3.0$	0.4	3.2	2
Intermediate $-3.0 < \eta < -2.4$	0.6	1.6	4
Forward $ \eta > 3.0$	3.0	6.4	1 [†]
Total Crates:			31

[†]Total Energy only provided for forward regions of the Calorimeter. Isolated Electron and Jet Threshold Triggers provided only out to $|\eta| < 3.0$.

Table 3: Summary of Energy Sum/Jet Threshold Crate Usage (WBS 5.3.1.2.2)
Number of crates for for entire Total/Missing Energy and Jet Trigger Coverage: 1

Table 4: Summary of Electron Match Crate Usage (WBS 5.3.1.5.1)

Region	Per Crate Coverage		Quantity
	η	ϕ	
Barrel $ \eta < 1.6$	1.6	3.2	4
Intermediate $1.6 < \eta < 3.0$	1.4	3.2	4
Total Crates:			8

Table 5: Summary of Muon Trigger Crate Usage (WBS 5.3.1.3.2)

Region	Per Crate Coverage		Quantity
	η	ϕ	
Barrel/Int./Forward $0 < \eta < 2.5$	2.5	3.2	2
Barrel/Int./Forward $-2.5 < \eta < 0$	2.5	3.2	2
Total Crates:			4

Table 6: Summary of Final Decision Crate Usage (WBS 5.3.1.5.2)

Number of crates for Final Decision Calculation: 1

Table 7: Summary of Global Clock and Control Crate Usage (WBS 5.3.1.6.2)

Number of crates for Global Clock and Control generation: 1

Table 8: Summary of Level 1 Distribution Crate Usage (WBS 5.3.1.6.1)

Subsystem	Quantity
Level 1 Decision Logic	2
Calorimeter Front End	2
Tracker Front End	1
Muon Front End	2
Silicon Front End	1
Total Crates:	8

4.2 Global Level 1 Processor Card Counts

Table 9: Calorimeter MLU Card Counts (WBS 5.3.1.2.2)

Crate Description	Per Crate Usage	Number of Crates	Card Quantity
Barrel/Intermediate Cal $-2.4 < \eta < 2.4$	8	24	192
Intermediate Cal $-3.0 < \eta < -2.4$	8	4	32
Intermediate Cal $2.4 < \eta < 3.0$	8	2	16
Forward Cal $ \eta > 3.0$	2	1	2
Total Cards:			242

Table 10: Calorimeter PRA Card Counts (WBS 5.3.1.2.2)

Crate Description	Per Crate Usage	Number of Crates	Card Quantity
Barrel/Intermediate Cal $-2.4 < \eta < 2.4$	2	24	48
Intermediate Cal $-3.0 < \eta < -2.4$	2	4	8
Intermediate Cal $2.4 < \eta < 3.0$	2	2	4
Forward Cal $ \eta > 3.0$	0	1	0
Total Cards:			60

Table 11: Calorimeter Energy Card Counts (WBS 5.3.1.2.2)

Crate Description	Per Crate Usage	Number of Crates	Card Quantity
Barrel/Intermediate Cal $-2.4 < \eta < 2.4$	1	24	24
Intermediate Cal $-3.0 < \eta < -2.4$	1	4	4
Intermediate Cal $2.4 < \eta < 3.0$	1	2	2
Forward Cal $ \eta > 3.0$	1	1	1
Total Cards:			31

Table 12: Track/Shower Max Match Card Counts (WBS 5.3.1.1.2)

Crate Description	Per Crate Usage	Number of Crates	Card Quantity
Central/Int. Track/Shower Max Match	16	2	32
Total Cards:			32

Table 13: Electron RMC Card Counts (WBS 5.3.1.5.1)

Crate Description	Per Crate Usage	Number of Crates	Card Quantity
Iso Electron Match $ \eta < 1.6$	8	4	32
Iso Electron Match $1.6 < \eta < 3.0$	8	4	32
Total Cards:			64

Table 14: Electron HSC Card Counts (WBS 5.3.1.5.1)

Crate Description	Per Crate Usage	Number of Crates	Card Quantity
Iso Electron Match $ \eta < 1.6$	3	4	12
Iso Electron Match $1.6 < \eta < 3.0$	3	4	12
Muon Trigger Crates	4	4	16 [†]
Final Decision Crate	7	1	7 [‡]
Total Cards:			47

[†]Card costs charged to Muon Trigger (WBS 5.3.1.3.2)

[‡]Card costs charged as follows: 3 cards to Electron Trigger (WBS 5.3.1.3.1), and 4 cards to Muon Trigger (WBS 5.3.1.3.2).

Table 15: Total/Missing Energy ESC Card Counts (WBS 5.3.1.2.2)

Crate Description	Per Crate Usage	Number of Crates	Card Quantity
Energy Sum/Jet Threshold	4	1	4
Final Decision	1	1	1
Total Cards:			5

Table 16: Jet Threshold JTSC Card Counts (WBS 5.3.1.2.2)

Crate Description	Per Crate Usage	Number of Crates	Card Quantity
Energy Sum/Jet Threshold	4	1	4
Final Decision	1	1	1
Total Cards:			5

Table 17: Correlated Muon Logic Card Counts (WBS 5.3.1.3.2)

Crate Description	Per Crate Usage	Number of Crates	Card Quantity
Barrel/Int./Forward Muon	8	4	32
Total Cards:			32

Table 18: Level 1 Clock/Control Fanout Card Counts

Crate Description	Per Crate Usage	Number of Crates	Card Quantity
Global Clock and Control	4	1	4
Level 1 Distribution	12	8	96
Total Cards:			100

Table 19: Level 1 Clock/Control Board Counts

Crate Description	Per Crate Usage	Number of Crates	Card Quantity
Global Level 1 Processor	1	56	56
Calorimeter Front End [†]	1	98	98
Tracker Front End [†]	1	16	16
Muon Front End	1	96	96
Silicon Front End	1	64	64
Total Cards:			330

4.3 Global Level 1 Processor ASIC Counts

4.3.1 Isolated Electron Pattern Recognition ASIC

The Pattern Recognition ASIC (PRA) is used to perform Isolated Electron detection on $.8\eta \times .8\phi$ regions of the calorimeter. It operates on the Encoded Tower Type (ETT) codes for each $.1\eta \times .1\phi$ trigger tower. This code identifies the tower as being quiet, at one of the six isolation thresholds, or as occupying a non-electromagnetic energy state (i.e., hadronic). Each Calorimeter PRA card contains 6 PRAs, one for each of the candidate isolation threshold levels.

Table 20: Pattern Recognition ASIC per Board Counts (WBS 5.3.1.2.2)

Card Description	Per Card Usage	Per Crate Usage	Number of Cards	Total Card Usage
Calorimeter PRA Card	6	12	60	360
Total ASICs:				360

4.3.2 12-bit Adder ASIC

The 12-bit Adder ASIC is used to sum 4 fixed point 12-bit sources to a single result. This ASIC is used to sum total and transverse energies in the Calorimeter to support the Total/Missing Energy and Jet Threshold triggers. The ASIC may be pipelined, with a fundamental clock and data accept rate of 16 nsec. This ASIC is used on numerous cards as shown in Table 21.

Table 21: 12-bit Adder ASIC per Board Counts (WBS 5.3.1.2.2)

Card Description	Per Card Usage	Per Crate Usage	Number of Cards	Total Card Usage
Calorimeter Energy Card	9	- - [†]	31	279
Calorimeter MLU Card	9	81 [†]	242	2178
Total/Missing Energy ESC Card	9	36	5	45
Total ASICs:				2566

[†]Adder ASIC totals per Calorimeter crate are given in the Per Crate Usage column for the Calorimeter MLU Card. Both card types reside in the Calorimeter Trigger Crate.

4.3.3 Pipeline Delay FIFO

The Pipeline Delay FIFO is conceived of as a 16-bit x 128 location FIFO Memory with simultaneous read/write capability, and a cycle time of 16 nsec. This FIFO will be used throughout the SDC Global Level 1 Processor to supply variable pipeline delays. These delays are used for the alignment of trigger data for correlation between trigger subsystems.

The FIFO is used in the various Level 1 Trigger Decision cards described in Table 22, and may also find use in front end or other subsystems.

Table 22: Pipeline Delay FIFO per Board Counts (WBS 5.3.1.5.2)

Card Description	Per Card Usage	Per Crate Usage	Number of Cards	Total Card Usage
Electron RMC	3	24	64	192
Correlated Muon Logic Card	4	32	32	128
Final Decision MLU Card	9	9	1	9
Total FIFOs:				329

4.4 Global Level 1 Processor Fiber Optic Cable Counts

Table 23: Summary of Calorimeter Trigger Primitive Optical Fiber Usage (WBS 5.3.1.2.1)

Region	Per Fiber Contents	η/ϕ Bin Quantity
Barrel $ \eta < 1.4$	EMC/HAC for $(.1)^2$ Towers	$28 \times 64 = 1792$
Int. $1.4 < \eta < 2.6$	EMC/HAC for $(.1)^2$ Towers	$24 \times 64 = 1536$
Int. $2.6 < \eta < 3.0$	EMC/HAC for $(.2)^2$ Towers	$4 \times 32 = 128$
Forward $3.0 < \eta < 6.0$	E_{TOTAL} for $(.8)^2$ Towers	$8 \times 8 = 64$
Total Optical Fibers:		3520

Table 24: Summary of Tracker Trigger Primitive Optical Fiber Usage (WBS 5.3.1.1.1)

Region	Per Fiber Contents	η/ϕ Bin Quantity
Central Half $\eta < 0$	4 3-bit p_T hits per cable, 1 η bin $\times$ 0.1ϕ per hit.	$1 \times 16 = 16$
Central Half $\eta > 0$	4 3-bit p_T hits per cable, 1 η bin $\times$ 0.1ϕ per hit.	$1 \times 16 = 16$
Int. End $\eta < 0$	4 3-bit p_T hits per cable, 1 η bin $\times$ 0.1ϕ per hit.	$1 \times 16 = 16$
Int. End $\eta > 0$	4 3-bit p_T hits per cable, 1 η bin $\times$ 0.1ϕ per hit.	$1 \times 16 = 16$
Total Optical Fibers:		64

Table 25: Summary of Shower Max Trigger Primitive Optical Fiber Usage (WBS 5.3.1.1.1)

Region	Per Fiber Contents	η/ϕ Bin Quantity
Barrel Half $-1.4 < \eta < 0$	14 1-bit hit flags per cable, $.2\eta \times .1\phi$ per hit.	$1 \times 32 = 32$
Barrel Half $0 < \eta < 1.4$	14 1-bit hit flags per cable, $.2\eta \times .1\phi$ per hit.	$1 \times 32 = 32$
Endcap End $-3.0 < \eta < -1.4$	16 1-bit hit flags per cable, $.2\eta \times .1\phi$ per hit.	$1 \times 32 = 32$
Endcap End $1.4 < \eta < 3.2$	16 1-bit hit flags per cable, $.2\eta \times .1\phi$ per hit.	$1 \times 32 = 32$
Total Optical Fibers:		128

Table 26: Summary of Muon Trigger Primitive Optical Fiber Usage (WBS 5.3.1.3.1)

Region	Per Cable Contents	η/ϕ Bin Quantity
Barrel Half $-1.0 < \eta < 0$	Top 2 p_T s with η ϕ location to $.2 \times .2$ in $1.0\Delta\eta \times .4\Delta\phi$ region	$1 \times 16 = 16$
Barrel Half $0 < \eta < 1.0$	Top 2 p_T s with η ϕ location to $.2 \times .2$ in $1.0\Delta\eta \times .4\Delta\phi$ region	$1 \times 16 = 16$
Int. End $-1.4 < \eta < -1.0$	Top 2 p_T s with η ϕ location to $.2 \times .2$ in $.4\Delta\eta \times .4\Delta\phi$ region	$1 \times 16 = 16$
Int. End $1.0 < \eta < 1.4$	Top 2 p_T s with η ϕ location to $.2 \times .2$ in $.4\Delta\eta \times .4\Delta\phi$ region	$1 \times 16 = 16$
Forward End $-2.5 < \eta < -1.4$	Top 2 p_T s with η ϕ location to $.2 \times .2$ in $1.1\Delta\eta \times .4\Delta\phi$ region	$1 \times 16 = 16$
Forward End $1.4 < \eta < 2.5$	Top 2 p_T s with η ϕ location to $.2 \times .2$ in $1.1\Delta\eta \times .4\Delta\phi$ region	$1 \times 16 = 16$
Total Optical Fibers:		96

Table 27: Summary of Clock, Control and Status Cable Optical Fiber Usage

Crate Type	Quantity
Calorimeter	98
Tracker	16
Muon	96
Silicon	64
Total Clock Cables:	274
Total Control Cables:	274
Total Status Cables:	274

† Each Front End crate has a single control fiber and status fiber link to the Global Clock and Control distribution system.

Table 28: Summary of Local Calorimeter Crate Optical Fiber Counts (WBS 5.3.1.2.1)

Region	Total					
	Cal. Fibers	Sh. Max Fibers	Clk/Cntrl Fibers	Per Crate Fibers	Number of Crates	Total Fibers
Barrel	28	1	3	32	64	2048
Int.	52	2	3	57	32	1824
Forward	32	0	3	35	2	70
Total Local Calorimeter Crate Optical Fibers:						3942

4.5 Global Level 1 Processor Electrical Cable Counts

Table 29: Electrical Interconnect Cable Summary

Level 1 Trigger Subsystem	Cable Description	Signal Pairs	Number of Cables	Approx. Length [†]
Electron/Photon	PRA card to RMC card	36	60	20 m
Electron/Photon	PRA card to RMC card	12	120	20 m
Electron/Photon	PRA card to RMC card	3	60	20 m
Electron/Photon	TSM card to RMC card	24	120	20 m
Electron/Photon	RMC card to Iso. HSC card	19	24	1 m
Electron/Photon	Iso. HSC to F.D. Iso. HSC	19	24	20 m
Muon	TSM card to CMLC card	24	32	20 m
Muon	RMC card to CMLC card	8	120	20 m
Muon	CMLC card to Muon HSC card	6	128	1 m
Muon	Muon HSC to F.D. Muon HSC	8	16	6 m
E _T /Missing E	Cal. Energy Card to ESC card	36	31	20 m
E _T /Missing E	reg. ESC to F.D. ESC card	36	4	6 m
Jets	Cal. Energy Card to JTSC card	24	30	20 m
Jets	reg. JTSC to F.D. JTSC card	40	4	6 m
Final Decision	Iso HSC card to FDM card	19	3	1 m
Final Decision	Muon HSC card to FDM card	6	4	1 m
Final Decision	JTSC card to FDM card	40	1	1 m
Final Decision	ESC card to FDM card	36	1	1 m
Final Decision	FDL card to Gbl. Clk & Cntrl.	10	1	6 m
Global Clk & Cntrl	Clock to Local L1CCBs	1	8	6 m
Global Clk & Cntrl	Control to Local L1CCBs	16	8	6 m
Global Clk & Cntrl	Status from Local L1CCBs	16	8	6 m
Local Clk & Cntrl	Clock to L1 Dec. Crates	1	46	20 m
Local Clk & Cntrl	Control to L1 Dec. Crates	16	46	20 m
Local Clk & Cntrl	Status from L1 Dec. Crates	16	46	20 m

[†]Cable lengths are estimates only, as follows: intra-crate connections are estimated at 1 m, intra-rack and nearby/adjacent rack connections are estimated at 6 m, and non-nearby/adjacent inter-rack connections are estimated at 20m.

5 Crate and Card Usage in the Level 2 Trigger System

5.1 Crate Summary

Summary of Crate Usage in the Level 2 Trigger System:

Crate Type	Quantity
Calorimeter	4
Track	4
Muon	4
Silicon	8
Regional	4
Global	1
Total Crates:	25

5.2 Card Summary

Summary of Card Usage in the Level 2 Trigger System:

Card Type	Nominal per Crate Usage	Total Quantity	Comments
Regional Cards	16	256	
Regional Master	1	16	
L2TC Cards	30	240	
Global Cards	16	16	
Global Master	1	1	

6 Cost Breakdown

Appendix A gives the detail cost breakdown for the SDC Trigger System. The WBS numbers follow the description given in the WBS section above. The total cost is 22,498 K\$ plus 7,213 K\$ contingency, giving a total project cost of 29,711 K\$. Of this total project cost, 20,328 K\$ is for Level 1, 8,670 K\$ is for Level 2 and 712 K\$ is for project management.

7 Schedule

The schedule for the trigger system is driven by the following needs:

- The complete trigger system must be installed by January, 1999 to allow sufficient time for completion of system integration and testing before data taking in October, 1999.

- The integration of subsystems into the trigger system must begin with partial subsets of these subsystems in 1997 since this must be done one subsystem at a time.
- Operation of the trigger system with the DAQ system must be started in 1996 in order to have trigger and DAQ systems ready for operation with front end systems in 1997.
- Test stand-alone trigger systems must be available for test-beam running and bench test of front end systems in 1993.

These considerations lead to the schedule shown in the schedule below. The time lines associated with this schedule are shown in Appendix C.

MAJOR MILESTONES – Level 1 Trigger

Completion of Trigger System Design Specs. (incl. Technical Choices)	Dec. '93
Test Trigger System for use in front end & DAQ system bench and test beam operations (incl. simulation of clock & control)	May '93
Start Final Design of Global & Subsystem Triggers	Jan. '93
Final Design Review of Global & Subsystem Trigs.	Jan. '95
Complete Design of Global & Subsys. Trigs.	June '95
Delivery of Prototypes of Global & Subsys. Trigs.	June '96
Initial Delivery of Trigger Interfaces to Front End and DAQ.	June '96
Delivery of Trigger System Begins	Jan. '97
Integration and Test of Subsystem and Global Trigger Systems begins	June '97
Integration and Test of Trigger with Final DAQ/FE Systems begins	Jan. '98
Commissioning of Trigger System Completed	Oct. '99

MAJOR MILESTONES – Level 2 Trigger

Completion of Trigger System Design Specs. (incl. Technical Choices)	Dec. '94
Test Trigger System for use in front end & DAQ system bench and test beam operations (incl. simulation of clock & control)	May '93
Start Final Design of Global & Subsystem Triggers	Jan. '94
Final Design Review of Global & Subsystem Trigs.	Jul. '95
Complete Design of Global & Subsys. Trigs.	Dec. '95
Delivery of Prototypes of Global & Subsys. Trigs.	June '96
Initial Delivery of Trigger Interfaces to Front End and DAQ.	June '96
Delivery of Trigger System Begins	Jan. '97
Integration and Test of Subsystem and Global Trigger Systems begins	June '97
Integration and Test of Trigger with Final DAQ/FE Systems begins	Jan. '98
Commissioning of Trigger System Completed	Oct. '99

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APPENDIX A:

SDC TRIGGER WBS 5.3

Level 1 & 2 Trigger 3/19/92

WBS	Element Name	ENG	TECH	PROC	EXP	TOTAL	Ct%	tc	cs	sc	tw	cw	sw	Cont. \$	TOTAL
5.3	Trigger Systems	6,832,800	5,694,000	8,354,302	980,000	21,861,102								6,964,059	28,825,161
5.3.1	First Level Trigger	4,399,200	3,666,000	5,867,410	655,000	14,587,610								4,854,747	19,442,357
5.3.1.1	Tracking Systems	842,400	702,000	980,700	180,000	2,705,100								965,809	3,670,909
5.3.1.1.1	Local Processing	561,600	468,000	663,700	120,000	1,813,300	39	8	6	1	4	1	1	707,187	2,520,487
5.3.1.1.2	Regional Processing	280,800	234,000	317,000	60,000	891,800	29	6	4	1	4	1	1	258,622	1,150,422
5.3.1.2	Calorimeter Systems	1,123,200	936,000	3,132,270	150,000	5,341,470								1,690,706	7,032,176
5.3.1.2.1	Local Processing	0	0	1,416,800	0	1,416,800	39	8	6	1	4	1	1	552,552	1,969,352
5.3.1.2.2	Regional Processing	1,123,200	936,000	1,715,470	150,000	3,924,670	29	6	4	1	4	1	1	1,138,154	5,062,824
5.3.1.3	Muon Systems	280,800	234,000	523,600	37,500	1,075,900								342,731	1,418,631
5.3.1.3.1	Local Processing	0	0	307,200	0	307,200	39	8	6	1	4	1	1	119,808	427,008
5.3.1.3.2	Regional Processing	280,800	234,000	216,400	37,500	768,700	29	6	4	1	4	1	1	222,923	991,623
5.3.1.4	Silicon Tracking	0	0	128,000	0	128,000								37,120	165,120
5.3.1.4.1	Local Processing	0	0	128,000	0	128,000	29	6	4	1	4	1	1	37,120	165,120
5.3.1.5	Global System	1,029,600	858,000	510,340	137,500	2,535,440								847,648	3,383,088
5.3.1.5.1	Regional Processing	374,400	312,000	387,300	50,000	1,123,700	39	8	6	1	4	1	1	438,243	1,561,943
5.3.1.5.2	Global Processing	655,200	546,000	123,040	87,500	1,411,740	29	6	4	1	4	1	1	409,405	1,821,145
5.3.1.6	Clock Control System	1,123,200	936,000	592,500	150,000	2,801,700								970,733	3,772,433
5.3.1.6.1	Regional Distributor	561,600	468,000	477,800	75,000	1,582,400	39	8	6	1	4	1	1	617,136	2,199,536
5.3.1.6.2	Global Processing	561,600	468,000	114,700	75,000	1,219,300	29	6	4	1	4	1	1	353,597	1,572,897
5.3.2	Second Level Trigger	2,152,800	1,794,000	2,486,892	287,500	6,721,192								1,949,146	8,670,337
5.3.2.1	Tracking Systems	0	0	378,000	0	378,000	29	6	4	1	4	1	1	109,620	487,620
5.3.2.2	Calorimeter Systems	0	0	522,000	0	522,000	29	6	4	1	4	1	1	151,380	673,380
5.3.2.3	Muon Systems	0	0	306,000	0	306,000	29	6	4	1	4	1	1	88,740	394,740
5.3.2.4	Silicon Tracker	1,029,600	858,000	796,892	137,500	2,821,992	29	6	4	1	4	1	1	818,378	3,640,369
5.3.2.5	Global System	1,123,200	936,000	484,000	150,000	2,693,200								781,028	3,474,228
5.3.2.5.1	Regional Interface	561,600	468,000	308,000	75,000	1,412,600	29	6	4	1	4	1	1	409,654	1,822,254
5.3.2.5.2	Global Processor	561,600	468,000	176,000	75,000	1,280,600	29	6	4	1	4	1	1	371,374	1,651,974
5.3.3	Project Management	280,800	234,000	0	37,500	552,300	29	6	4	1	4	1	1	160,167	712,467

5.3 TRIGGER SYSTEMS

.1 FIRST LEVEL TRIGGER

5.3.1.1 TRACKING SYSTEMS

5.3.1.1.1	Local Cent. Tracker Processing	Unit	Cost/unit	Total	Cost/Unit	Labor Rate
	Central Tracker Crates					
	Clock Control Board	1	2,000		2,000	
	Fiber Optic Links	7	300		2,100	
	Cost per Crate				4,100	
	TOTAL CRATE COST	8	4,100		32,800	
	Local Int. Tracker Processing					
	Intermediate Tracking Crates					
	Slow Fiber Optic Links	10,400	19		197,600	
	Tracker Boards	16	2,000		32,000	
	Tracker ASIC	400	85		34,000	
	Tracker Control Board	1	2,000		2,000	
	Clock Control Board	1	2,000		2,000	
	Fiber Optic Links	3	300		900	
	Crate Hardware	1	2,500		2,500	
	Power Supplies	1	2,500		2,500	
	Cost per Crate				273,500	
	TOTAL CRATE COST	2	273,500		547,000	
	Prototype Crate (1/2)	1	75,900		75,900	
	Racks	1	8,000		8,000	
	Engineering in Man Years	6	93,600		561,600	360
	Technical in Man Years	6	78,000		468,000	300
	Misc. Expenses					
	Travel				30,000	
	Computing				60,000	
	Supplies				30,000	
	TOTAL LOCAL PROCESSING				1,813,300	

Level 1 & 2 Trigger 3/19/92

5.3.1.1.2	Regional Processing	Unit	Cost/unit	Total Cost/Unit	Labor Rate
	Track/Sh. Max Match Crate				
	Trk./Sh. Max Match Card	16	2,000	32,000	
	Clock/Control Board	1	2,000	2,000	
	Crate Hardware	1	2,500	2,500	
	Power Supplies	1	2,500	2,500	
	Cost per Crate			39,000	
	TOTAL CRATE COST	2	39,000	78,000	
	Prototype Crate	1	78,000	78,000	
	Racks	1	8,000	8,000	
	Cables			153,000	
	Engineering in Man Years	3	93,600	280,800	360
	Technical in Man Years	3	78,000	234,000	300
	Misc. Expenses				
	Travel			15,000	
	Computing			30,000	
	Supplies			15,000	
	TOTAL REGIONAL PROCESSING			891,800	

5.3.1.2 CALORIMETER SYSTEM

5.3.1.2.1	Local Processing	Unit	Cost/unit	Total Cost/Unit	Labor Rate
	Barrel Crates:				
	Fiber Optic Links	32	300	9,600	
	Clock Control Board	1	2,000	2,000	
	Total Barrel Crates	64	11,600	742,400	
	Intermediate Crates:				
	Fiber Optic Links	57	300	17,100	
	Clock Control Board	1	2,000	2,000	
	Total Intermediate Crates	32	19,100	611,200	
	Forward Crates:				
	Fiber Optic Links	35	300	10,500	
	Clock Control Board	1	2,000	2,000	
	Total Forward Crates	2	12,500	25,000	
	Total Crates	98		1,378,600	
	Prototype	1	38,200	38,200	
	TOTAL LOCAL PROCESSING			1,416,800	

Level 1 & 2 Trigger 3/19/92

5.3.1.2.2	Regional Processing	Unit	Cost/unit	Total Cost/Unit	Labor Rate
	Isolation/Summation Crate				
	Calorimeter MLU Board	8	2,000	16,000	
	Calorimeter Energy Board	1	2,000	2,000	
	Adder ASIC	81	70	5,670	
	Calorimeter PRA Card	2	2,000	4,000	
	PRA ASIC	12	300	3,600	
	Clock/Control Board	1	2,000	2,000	
	Crate Hardware	1	2,500	2,500	
	Power Supplies	1	2,500	2,500	
	Cost per Crate			38,270	
	Total Crate Cost	31	38,270	1,186,370	
	Prototype	1	76,540	76,540	
	Egy Sum/Jet Thresh Crate				
	Energy Sum Card	4	4,000	16,000	
	Adder ASIC	36	70	2,520	
	Jet Thresh Sum Card	4	4,000	16,000	
	Clock/Control Board	1	2,000	2,000	
	Crate Hardware	1	2,500	2,500	
	Power Supplies	1	2,500	2,500	
	Total Crate Cost	1	41,520	41,520	
	Prototype	1	83,040	83,040	
	Racks	11	8,000	88,000	
	Cables			240,000	
	Engineering in Man Years	12	93,600	1,123,200	360
	Technical in Man Years	12	78,000	936,000	300
	Misc. Expenses				
	Travel			60,000	
	Computing			60,000	
	Supplies			30,000	
	TOTAL REGIONAL PROCESSOR COSTS			3,924,670	

5.3.1.3 MUON SYSTEMS

5.3.1.3.1	Local Processing	Unit	Cost/unit	Total	Cost/Unit	Labor Rate
	Fiber Optics	4	300		1,200	
	Clock/control Board	1	2,000		2,000	
	Total Cost per Unit				3,200	
	Barrel Crates	56	3,200		179,200	
	Inter Crates	8	3,200		25,600	
	Forward Crates	32	3,200		102,400	
	Total Crate Cost	96	3,200		307,200	
	TOTAL LOCAL PROCESSING				307,200	

5.3.1.3.2	Regional Processing	Unit	Cost/unit	Total	Cost/Unit	Labor Rate
	Muon Trigger Crate					
	Correlated Muon Logic Card	8	2,000		16,000	
	Muon HSC Card	4	2,000		8,000	
	FIFO Delay ASIC	32	50		1,600	
	Clock/Control Board	1	2,000		2,000	
	Crate Hardware	1	2,500		2,500	
	Power Supplies	1	2,500		2,500	
	Cost per Crate				32,600	
	Total Crate Cost	4	32,600		130,400	
	Prototype	1	65,200		65,200	
	Racks	2	8,000		16,000	
	Cables				4,800	
	Engineering in Man Years	3	93,600		280,800	360
	Technical in Man Years	3	78,000		234,000	300
	Misc. Expenses					
	Travel				15,000	
	Computing				15,000	
	Supplies				7,500	
	TOTAL REGIONAL PROCESSING SYSTEM				768,700	

5.3.1.4 SILICON TRACKING

5.3.1.4.1	Local Processing	Unit	Cost/unit	Total	Cost/Unit	Labor Rate
	Clock Control card	1	2,000		2,000	
	Cost per Crate				2,000	
	Total Crate Cost	64	2,000		128,000	
	TOTAL LOCAL PROCESSING				128,000	

5.3.1.5 GLOBAL SYSTEM

5.3.1.5.1	Regional Processing	Unit	Cost/unit	Total	Cost/Unit	Labor Rate
	Isolated Electron Match Crate					
	Isolated Electron RMC	8	2,000		16,000	
	Isolated Electron HSC	3	2,000		6,000	
	FIFO Delay ASIC	24	50		1,200	
	Clock/Control Board	1	2,000		2,000	
	Crate Hardware	1	2,500		2,500	
	Power Supplies	1	2,500		2,500	
	Cost per Crate				30,200	
	Total Crate Cost	8	30,200		241,600	
	Prototype	1	60,400		60,400	
	Racks	3	8,000		24,000	
	Cables				61,300	
	Engineering in Man Years	4	93,600		374,400	360
	Technical in Man Years	4	78,000		312,000	300
	Misc. Expenses					
	Travel				20,000	
	Computing				20,000	
	Supplies				10,000	
	TOTAL REGIONAL PROCESSING				1,123,700	
5.3.1.5.2	Global Processing	Unit	Cost/unit	Total	Cost/Unit	Labor Rate
	Final Decision Crate					
	Isolated Electron HSC	3	2,000		6,000	
	Energy Sum Card	1	4,000		4,000	
	Jet Thresh Sum Card	1	4,000		4,000	
	Muon HSC Card	4	2,000		8,000	
	Final Decision MLU Card	1	4,000		4,000	
	Adder ASIC	9	70		630	
	FIFO Delay ASIC	9	50		450	
	Final Decision Logic	1	4,000		4,000	
	Clock/Control Board	1	2,000		2,000	
	Crate Hardware	1	2,500		2,500	
	Power Supplies	1	2,500		2,500	
	Cost per Crate				38,080	
	Total Crate Cost	1	38,080		38,080	
	Prototype	1	76,160		76,160	
	Racks	1	8,000		8,000	
	Cables				800	
	Engineering in Man Years	7	93,600		655,200	360
	Technical in Man Years	7	78,000		546,000	300
	Misc. Expenses					
	Travel				35,000	
	Computing				35,000	
	Supplies				17,500	
	TOTAL GLOBAL PROCESSING				1,411,740	

5.3.1.6 CLOCK/CONTROL SYSTEM

5.3.1.6.1	Regional Distribution	Unit	Cost/unit	Total	Cost/Unit	Labor Rate
	Local Clock/Control Crate					
	Clock Control Board	1	2,000		2,000	
	Clock Control Fanout	16	2,000		32,000	
	Crate Hardware	1	2,500		2,500	
	Power Supplies	1	2,500		2,500	
	Cost per Crate				39,000	
	Total Crate Cost	8	39,000		312,000	
	Prototype	1	78,000		78,000	
	Racks	3	8,000		24,000	
	Cables				63,800	
	Engineering in Man Years	6	93,600		561,600	360
	Technical in Man Years	6	78,000		468,000	300
	Misc. Expenses					
	Travel				30,000	
	Computing				30,000	
	Supplies				15,000	
	TOTAL REGIONAL DISTRIBUTION				1,582,400	
5.3.1.6.2	Global Processing	Unit	Cost/unit	Total	Cost/Unit	Labor Rate
	Global Clock/Control Crate					
	Mach. Clock Interface	1	4,000		4,000	
	Beam Pickup Interface	1	4,000		4,000	
	Deadtime Monitor	1	4,000		4,000	
	Final Decision Interface	1	4,000		4,000	
	Global Clock Master	1	4,000		4,000	
	Global Control Master	1	4,000		4,000	
	Clock Control Fanout	4	2,000		8,000	
	Crate Hardware	1	2,500		2,500	
	Power Supplies	1	2,500		2,500	
	Cost per Crate				37,000	
	Total Crate Cost	1	37,000		37,000	
	Prototype	1	74,000		74,000	
	Cables				3,700	
	Engineering in Man Years	6	93,600		561,600	360
	Technical in Man Years	6	78,000		468,000	300
	Misc. Expenses					
	Travel				30,000	
	Computing				30,000	
	Supplies				15,000	
	TOTAL GLOBAL PROCESSING				1,219,300	
	GRAND TOTAL LEVEL 1				14,587,610	

5.3.2 SECOND LEVEL TRIGGER**5.3.2.1 TRACKING SYSTEMS**

	Unit	Cost/unit	Total	Cost/Unit	Labor Rate
Regional Processing					
Level 2 Interface Cards	12	2,000		24,000	
Regional Crate	1	5,000		5,000	
Regional Cards	16	2,000		32,000	
Regional Master	1	2,000		2,000	
Total Regional Crates	4	63,000		252,000	
Prototype	1	126,000		126,000	
TOTAL REGIONAL PROCESSING SYSTEM				378,000	

5.3.2.2 CALORIMETER SYSTEM

	Unit	Cost/unit	Total	Cost/Unit	Labor Rate
Regional Processor					
Level 2 Interface Cards	24	2,000		48,000	
Regional Crate	1	5,000		5,000	
Regional Cards	16	2,000		32,000	
Regional Master	1	2,000		2,000	
Total Regional Crates	4	87,000		348,000	
Prototype	1	174,000		174,000	
TOTAL REGIONAL PROCESSOR COSTS				522,000	

5.3.2.3 MUON SYSTEMS

	Unit	Cost/unit	Total	Cost/Unit	Labor Rate
Regional Processing					
Level 2 Interface Cards	6	2,000		12,000	
Regional Crate	1	5,000		5,000	
Regional Cards	16	2,000		32,000	
Regional Master	1	2,000		2,000	
Total Regional Crates	4	51,000		204,000	
Prototype	1	102,000		102,000	
TOTAL REGIONAL PROCESSING SYSTEM				306,000	

Level 1 & 2 Trigger 3/19/92

5.3.2.4	SILICON TRACKER	Unit	Cost/unit	Total	Cost/Unit	Labor Rate
	L2TC Chips	10,000	20	200,000		
	Assoc. Mem. Chip 1	10,000	15	150,000		
	Assoc. Mem. Chip 2	10,000	15	150,000		
	PC Boards	240	300	72,000		
	ECL Chips	120	100	12,000		
	Card Assy./Test	240	125	30,000		
	Crates and Power Supp.	8	12,750	102,000		
	Racks	4	750	3,000		
	Total Equipment			719,000		
	Spare	24	2,996	71,900		
	Prototype	1	5,992	5,992		
	Engineering	11	93,600	1,029,600		360
	Technician	11	78,000	858,000		300
	Travel			55,000		
	Computing			55,000		
	Supplies			27,500		
	TOTAL SILICON TRACKER SYSTEM			2,821,992		

5.3.2.5	GLOBAL SYSTEM					
5.3.2.5.1	Regional Interface	Unit	Cost/unit	Total	Cost/Unit	Labor Rate
	Regional Crate	1	10,000	10,000		
	Regional Cards	16	2,000	32,000		
	Regional Master	1	2,000	2,000		
	Total Regional Crates	4	44,000	176,000		
	Spare	1	44,000	44,000		
	Prototype	1	88,000	88,000		
	Engineering	6	93,600	561,600		360
	Technician	6	78,000	468,000		300
	Travel			30,000		
	Computing			30,000		
	Supplies			15,000		
	TOTAL REGIONAL PROCESSING SYSTEM			1,412,600		

5.3.2.5.2	Global Processing	Unit	Cost/unit	Total	Cost/Unit	Labor Rate
	Global Crate	1	10,000	10,000		
	Global Cards	16	2,000	32,000		
	Global Master	1	2,000	2,000		
	Total Global Crates	1	44,000	44,000		
	Spare	1	44,000	44,000		
	Prototype	1	88,000	88,000		
	Engineering	6	93,600	561,600		360
	Technician	6	78,000	468,000		300
	Travel			30,000		
	Computing			30,000		
	Supplies			15,000		
	TOTAL GLOBAL PROCESSING SYSTEM			1,280,600		

GRAND TOTAL LEVEL 2

6,721,192

Level 1 & 2 Trigger 3/19/92

5.3.3	PROJECT MANAGEMENT	Unit	Cost/unit	Total	Cost/Unit	Labor Rate
	Engineering	3	93,600		280,800	360
	Technician	3	78,000		234,000	300
	Travel				15,000	
	Computing				15,000	
	Supplies				7,500	
	TOTAL PROJECT MANAGEMENT				552,300	
	GRAND TOTAL PROJECT MANAGEMENT				552,300	
	GRAND TOTAL TRIGGER				21,861,102	

APPENDIX B:

VENDOR QUOTES FOR PC BOARDS AND ASSEMBLY



May 13, 1991

Pat Leggett
Purchasing Agent
University of Wisconsin - Madison
Purchasing Services
750 University Avenue, 2nd Floor Reception
Madison, Wisconsin 53706-1490

RE: Bid Number 91-0623

Dear Pat:

I am pleased to provide price and delivery information for the following part:

<u>QTY</u>	<u>PART/DESCRIPTION</u>	<u>U/P</u>	<u>TOTAL PRICE</u>
272	TRIGGER ENCODER CARD	\$298.00	\$81,056.00
257	SAME	298.00	76,586.00
1	TOOLING	930.00	930.00
1	<u>ELECTRICAL/IMPEDANCE TEST</u>	<u>4,500.00</u>	<u>4,500.00</u>
<u>Bld Total</u>			<u>\$163,072.00</u>

General Provisions

- Delivery will be made in two releases, 272 pieces in 5 weeks with the balance of 257 pieces on your dock in 6 weeks. Either quantity, if placed as a single order, can be shipped to arrive on your dock in 5 weeks.
- Terms: Net 30, F.O.B. Destination.
- Customer references will gladly be supplied upon request.

Technical Provisions

- Soldermask type will be DuPont Vacrel 8130. Other processes are available.
- Our Excellon Laser Plotter's largest aperture is one-half an inch.
- Automated optical inspection of layers before lamination is performed on a 100% basis at Spectra, in all cases.
- Impedance characteristics shall be maintained through the following procedure:

- 1) The design will be analyzed using Spectra proprietary software. This analysis will determine if any adjustments to the copper weight, trace widths, or dielectric thicknesses are required, in relation to the specific materials to be used and process parameters at Spectra.
- 2) Any adjustments will be discussed and approval sought from the customer before fabrication.
- 3) 100% of the finished boards will be tested for the specified impedance characteristics using TDR analysis. Certificates of compliance will be provided.

Please call me if you or members of your staff have any questions. I thank you for the opportunity to bid on this requirement.

Regards,

A handwritten signature in black ink, appearing to read 'Erik Clark', with a stylized, flowing script.

Erik Clark
Sales Representative

Ms. Pat Leggett
Purchasing Services
University of Wisconsin-Madison
750 University Ave.
Madison, Wisconsin 53706

October 7, 1991

QUOTATION NO: Q-910081

QUOTATION

This quotation will provide pricing for the Trigger Encoder Card assembly. All components are to be provided by the University of Wisconsin Physical Sciences Laboratory.

Subject to the attached terms and conditions, we are pleased to provide the following quotation for contract services for this assembly.

<u>ITEM</u>	<u>DESCRIPTION</u>	<u>QUANTITY</u>	<u>U/M</u>	<u>UNIT PRICE</u>
1.	Surface Mount and Leaded assembly.	264	ea.	\$346.62
2.	Set up charges	1	ea.	\$275.00
3.	Non-recurring Engineering charges	1.	ea.	\$1135.00

Please see below for the assumptions used for this quotation and more detail on each of the items quoted above.

ASSUMPTIONS

1. University of Wisconsin Physical Sciences Laboratory to provide PWB's and all components.
2. All Components to be on Tape and Reel, in conductive tubes, or in waffle packs.
3. All components to be cleaned in Flux Off E series or water unless specified.
4. University of Wisconsin Physical Sciences Laboratory to provide complete assembly documentation.
5. University of Wisconsin Physical Sciences Laboratory to provide artwork generation for solder stencil.

PCB ASSEMBLY SERVICE

Thor Technology will provide the following services:

1. Procurement of all process materials
2. Assembly and soldering of components to the circuit board.
3. 100% visual inspection of solder joints.
4. Cleaning in Fluxoff E series or water.
5. Packing for shipment.

THOR TECHNOLOGY
C O R P O R A T I O N

NONRECURRING ENGINEERING CHARGE

The following NRE charges apply to this quotation:

- a. Placement machine program.
- b. Solder Stencil.
- c. Wave Solder Tooling

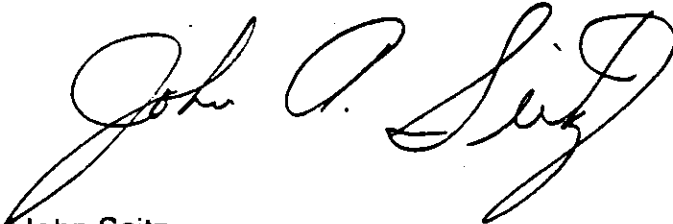
SETUP CHARGES

A \$275.00 set-up charge is uncured each time a production release is run. This covers the cost of installing the materials on our placement machines, logging the transactions and doing a first piece inspection of the populated board.

DELIVERY: Based on a pre-arranged production schedule. It is possible to deliver 40 assemblies 2 weeks ARO providing that artwork needed for a solder stencil and the components are provided along with the purchase order

F.O.B: University of Wisconsin Physical Sciences Laboratory
3725 Schneider Drive, Rt 4
Stoughton, Wisconsin 53589

QUOTATION TO REMAIN FIRM FOR 30 DAYS.

A handwritten signature in black ink, appearing to read "John A. Seitz". The signature is fluid and cursive, with the first name "John" being more prominent.

John Seitz
Contract Sales Manager

JAS/wam

Enclosure

cc: File
P.R.I.S.M.

APPENDIX C:

SDC TRIGGER SCHEDULE

