Published by IOP Publishing for Sissa Medialab

Received: *October 16, 2025*
Accepted: *January 14, 2026*
Published: *February 13, 2026*

Topical Workshop on Electronics for Particle Physics
Rethymno, Crete, Greece
6–10 October 2025

An 11-Gbps CMOS-logic serializer core for high-energy physics experiments

X. Li[a], **Q. Wu**[a,b], **Q. Zhu**[a,c], **W. Wei**[a], **X. Yan**[a,d,*], **J. Chen**[a] and **J. Ye**[a]

[a] *Institute of High Energy Physics Chinese Academy of Sciences, 19B Yuquan Road, Beijing 100049, China*
[b] *Department of Physics, NanJing University, 22 Hankou Road, Gulou District, Nanjing 210093, China*
[c] *School of Physics and Electronic Information, Gannan Normal University, 1 Shida South Road, Ganzhou 341000, China*
[d] *School of Physical Sciences, University of Chinese Academy of Sciences, 19A Yuquan Road, Beijing 100049, China*

E-mail: yanxb@ihep.ac.cn

Abstract: High-speed serial transmitters are commonly used in various fields, including high energy physics experiments, where the data volume has significantly increased due to detector upgrades. In this paper, we present a CMOS-logic serializer core designed in a 55-nm bulk CMOS technology for front-end detector data transmission. The prototype design features a 32-to-1 binary-tree multiplexer, an LC-based phase-locked loop, and a standard current-mode logic driving stage with a 5-stage pre-amplifier. The measured total jitter at 10.24 Gbps and 11.09 Gbps is approximately 24.5 ps and 30 ps, respectively, with total power consumption of 96.2 mW and 97.4 mW. The internal timing margin accommodates a power supply variation from 1.15 V to 1.4 V. However, further improvements are required in the driving capability and power consumption of the driver, which currently accounts for nearly 45% of the total power consumption.

Keywords: Analogue electronic circuits; Electronic detector readout concepts (solid-state); Front-end electronics for detector readout; Pixelated detectors and associated VLSI electronics

*Corresponding author.

https://doi.org/10.1088/1748-0221/21/02/C02013

Contents

1 Introduction

In high energy physics experiments, current ASIC design trends indicate a shift towards front-end electronics, focusing on increasing integration density [1, 2]. Serial transmitters play a vital role in digital detector data transmission, whether in pixelated readout electronics [3, 4] or universal data links [5, 6]. For front-end detector readouts, the system usually has limited space and requires low power consumption along with a high single-channel data rate.

This paper presents the first prototype design in a 55-nm bulk CMOS technology aiming to the timing verification of the serializer core. The core is based on a CMOS-logic binary-tree structure, which comprises an LC-tank phase locked loop (LC-PLL), and a fully-CMOS-logic multiplexer (MUX32t1) including a current-mode logic (CML) driver. The PLL and multiplexer cores consume a minimal amount of current, with the majority of the power being consumed by high-speed clock transmission and serial data driving.

2 Circuit design of the serializer

Figure 1(a) shows the architecture of the serializer. The LC-PLL is based on a previously validated circuit design [7], with minor modifications. To achieve a data rate exceeding 10 Gbps, the MUX32t1 utilizes a cascaded binary-tree structure comprising 5 stages [6]. In order to minimize power consumption, CMOS logic is favored over current-mode logic, despite the latter's faster operation. Customized basic logic cells have been carefully optimized. The initial four stages of MUX32t1 are constructed using a standard 2:1 cell, while the final stage, functioning at 5.12 GHz, employs a high-speed 2:1 cell. As shown in figure 1(c), the high-speed 2:1 cell incorporates progressively enhanced inverters (INVs) to maintain the swift edges of the CMOS clocks. Nevertheless, employing a long chain of INVs, in comparison to employing differential clock transmission, could introduce duty cycle distortion (DCD) to the CMOS clocks. This distortion may also arise when transferring a differential clock pair to two CMOS clocks. Since the MUX32t1 operates at half rates, utilizing both clock edges for data processing, any distortions could potentially result in significant variations in the size of the data eyes between adjacent bits. Consequently, duty cycle correction (DCC) circuits have been inserted at two critical nodes [4].

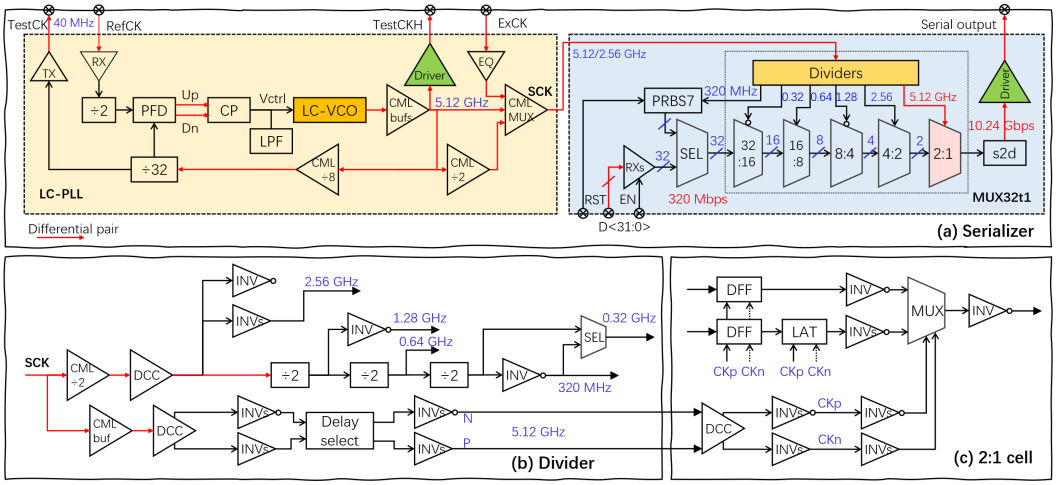


Figure 1. Schemes of the serializer.

The standard 2:1 cell also needs to account for DCD, although its demand is not as stringent as that of the high-speed 2:1 cell. It employs a single-to-differential circuit that relies on varying sizes and quantities of inverters in two paths [8], in order to align two complementary clocks. Each D-flip-flop and latch in the 2:1 cell utilizes complementary clocks.

The divider, a crucial component of MUX32t1 as depicted in figure 1(b), controls the serialization timing. The estimated upper frequency limit of a CMOS by-2 divider is less than 5 GHz at the worst corner in simulation, unless using extremely oversized transistors. Consequently, the initial by-2 sub-divider is implemented using CML, while the subsequent dividers utilize CMOS cells. The DCC circuit aligns two CMOS clocks with 50% duty cycle by transferring a differential pair. Timing for the first three stages of MUX32t1 is relatively straightforward. However, with the 4:2 stage, the clock signal must traverse an extended chain of inverters, leading to a propagation delay that is compatible with the preceding data path. Consequently, the overall timing also enables MUX32t1 to operate below 10 Gbps. The chain of inverters also provides a corresponding timing adjustment for different process corners.

The current data driver comprises a CML driving stage and a 5-stage pre-amplifier. The total current is 38 mA, with a static output current of 4.8 mA. The driving efficiency is notably low. For the upcoming iteration, a source-series-terminated (SST) driving stage [9–11], along with pre-emphasis technique [4, 9–11], will be considered. Since the initial design utilized a traditional CML driver, the driving capability was limited. The analog IO supported by the foundry displays a total parasitic capacitance of about 800 fF. However we estimated the final load capacitance to be around 1 pF, a figure to encompass both the driver and wiring contribution, which significantly impacted the data transmission bandwidth. To address this issue, a customized IO pad was implemented to reduce the capacitance load. The final total load on the chip amounts to around 560 fF. Short bonding wires of around 1.5 mm were employed to mitigate the inductance.

3 Measurements

Figure 2 shows the test setup, where the serializer chip is wire-boned on a printed circuit board (PCB). The total power consumption for the chip, excluding testing blocks, is around 96.2 mW at 10.24 Gbps, with 23, 6 and 67.2 mW for the PLL, clock buffers and MUX32t1 respectively.

2026 JINST 21 C02013

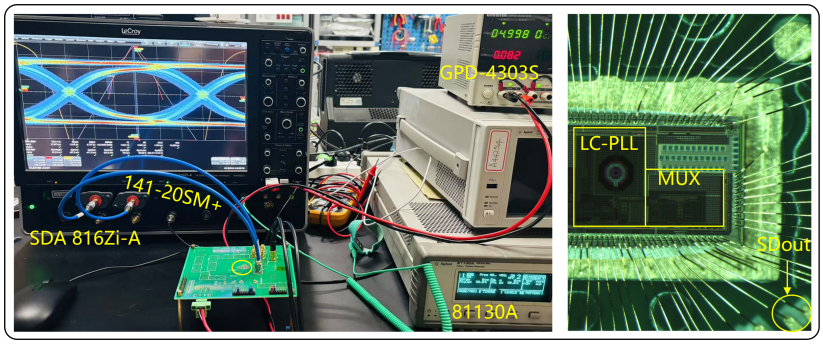
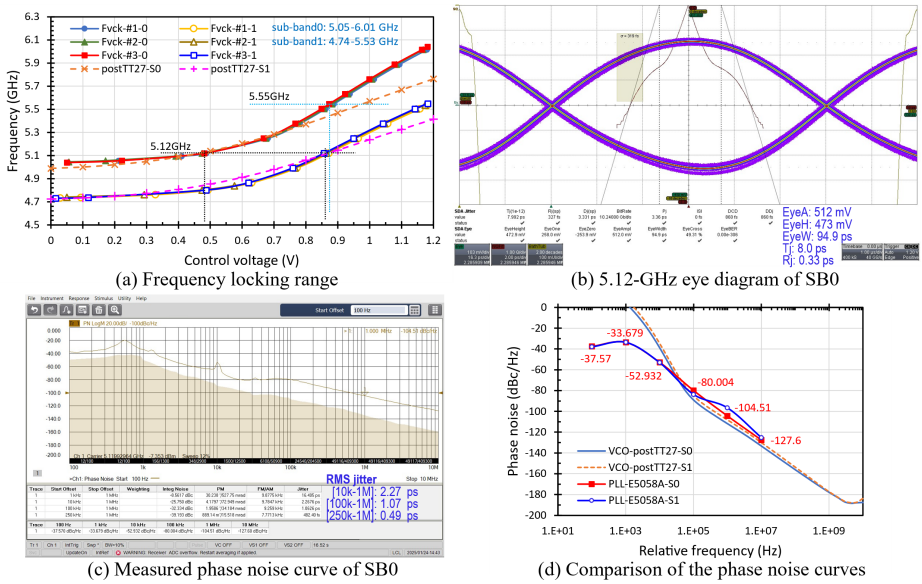


Figure 2. Test setup.

3.1 PLL characterization

The PLL has two frequency tuning curves to cover the entire frequency range, with the upper and lower frequency curves representing subband 0 (SB0) and subband 1 (SB1), respectively. The frequency locking range is measured by adjusting the reference clock, and the results align with the simulations. In a previous study, it was observed that subband 1 (SB1) with metal-oxide-metal capacitors (MOM-CAPs) deviated from the simulation results, potentially due to inaccuracies in the extracted models [7], which may not be entirely accurate. It was found that using transistor-level extraction for the MOM-CAP could result in repeated extractions, which could explain why the simulated frequency of SB1 is much lower than the measured values. In practice, for most analog circuit designs, transistor-level extraction is more precise and preferable. This also depends on the technology used. However, following the guidance from the foundry, gate-level extraction combined with hcell and xcell models is recommended, leading to almost consistent results as shown in figure 3(a). Figure 3(b) shows the measured eye and jitter performance.



(a) Frequency locking range

(b) 5.12-GHz eye diagram of SB0

(c) Measured phase noise curve of SB0

(d) Comparison of the phase noise curves

Figure 3. Performance of the LC-PLL.

2026 JINST 21 C02013

We also used a signal source analyzer (Keysight E5058A) to measure the phase noise performance of the 5.12 GHz clock. Figure 3(c) shows the results, including several spot phase noise and integrated root mean square jitter (RMSj) values. The RMSj_{1k-1M}, RMSj_{10k-1M}, $\mathrm{RMSj}_{100k-1M}$, and $\mathrm{RMSj}_{250k-1M}$ are about 16.41, 2.27, 1.07, and 0.49 ps, respectively, where 250 kHz represents the smallest loop bandwidth of the PLL. The low offset-frequency part is noted to make a substantial contribution to the phase noise, possibly originating from the reference components such as the clock source, PFD, CP, and feedback dividers. The separate tests of the 40-MHz clock from the Agilent 81130A confirmed this, with the RMSj_{1k-1M}, RMSj_{10k-1M}, and $\mathrm{RMSj}_{100k-1M}$ values of about 18.33, 2.19, and 0.42 ps, respectively. A spurious peak was observed at the 10 kHz offset frequency, which also originated from the reference clock. Figure 3(d) compares the measured spot phase noise with the simulated phase noise of the free-running VCO.

3.2 Serializer characterization

Figure 4 displays eye diagrams of the serial data stream captured by the oscilloscope. Panels (a) and (b) show cases of 5.12 Gbps and 10.24 Gbps measured through 0.5-m cables, with the total jitter (Tj) measured at 16.1 and 24.6 ps, and the random jitter (Rj) at 0.45 and 0.47 ps, respectively. Their output eye heights and eye widths measure 874 mV and 581 mV, and 0.92 unit intervals (UI) and 0.75 UI, respectively.

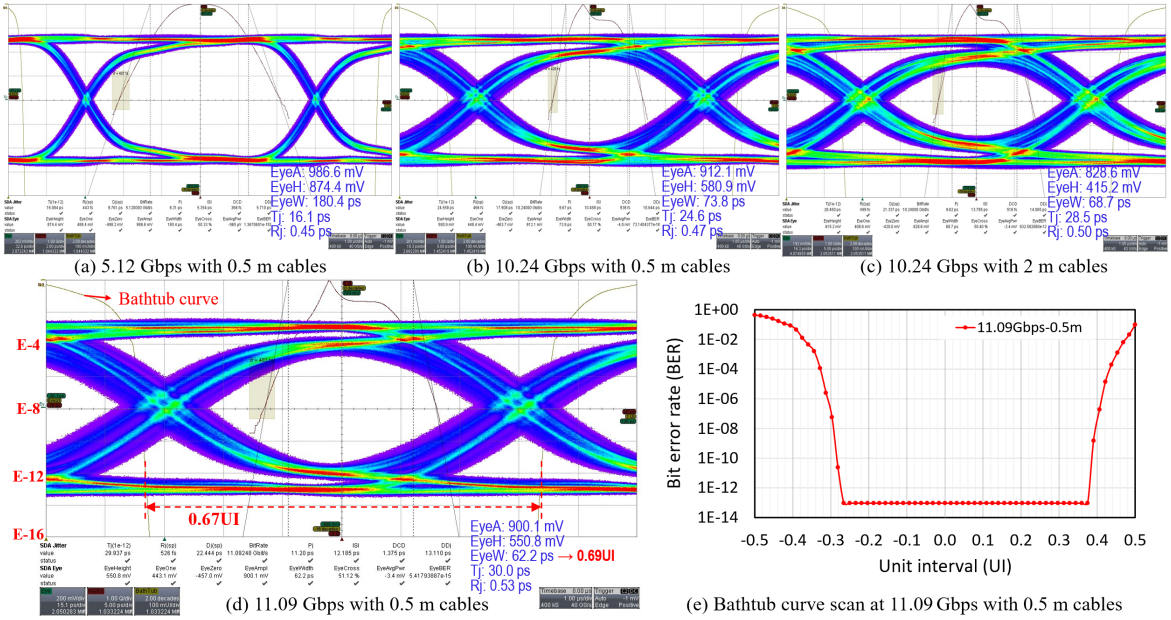


Figure 4. Eye-diagram, jitter performance and bathtub curve measurements at different data rates and cable lengths.

When using 2-m cables at 10.24 Gbps, as shown in panel (c), the Tj and Rj increase by 15.9% and 6.4% compared to the case with 0.5-m cables. Panel (d) presents the measurement at 11.09 Gbps through 0.5-m cables, with the Tj and Rj measuring 30.0 and 0.53 ps. These measurements suggest that for higher data rates and longer transmission distances, the driving capability should be further improved.

2026 JINST 21 C02013

An FPGA evaluation board (KC705) was also used to check data and count the error bits at 11.09 Gbps. When using 0.5-m cables, no error bits occurred over 10^{14} bits. In contrast, with 1-meter cables, no error bits were observed over 3×10^{12} bits. A bathtub curve was measured based on 0.5-m cables to evaluate the bit error rate (BER) performance, as shown in figure 4(e), where the BER is less than 1×10^{-12} at a 99.9% confidence level.

3.3 Influence of supply voltage

Bypassing the on-board 1.2-V LDOs, the power supplies of the PLL and MUX32t1 were connected together and directly provided from the GPD-4303S. Various performance variations were measured by adjusting the supply voltage, and the results are illustrated in figure 5. Panel (a) and (b) depict the total and random jitter variations of the PLL clock, respectively, both showing opposite trends in response to changes in the supply voltage. The PLL remained locked during the power adjustment, with an increasing variation of the control voltage in relation to the supply voltage, as shown in figure 5(c).

An interesting phenomenon was observed. The PLL could remain locked when the supply voltage decreased from normal to below 1.1 V (SB1). However, at this moment, it failed to work when the VCO was re-enabled or re-powered on. If the PLL attempts to work directly with a low-voltage power-on, the supply voltage should be over 1.107 V for SB0 and 1.123 V for SB1, respectively. The probable reason could be that the oscillator stops working at a low supply voltage. However, when there is a disturbance from the previous oscillation or reference inputs, it could trigger the oscillator to start working again in this low-voltage critical region.

Figure 5(d) and (e) present the total and random jitter variations at 10.24 Gbps. Figure 5(f) shows the total current consumption of the serializer core, with a proportional change to the supply voltage. The measurements suggest that the serializer core can maintain correct timing and exhibit slightly better jitter characteristics when enabling the delay select block shown in figure 1(c), which adds an extra delay of about 20~30 ps.

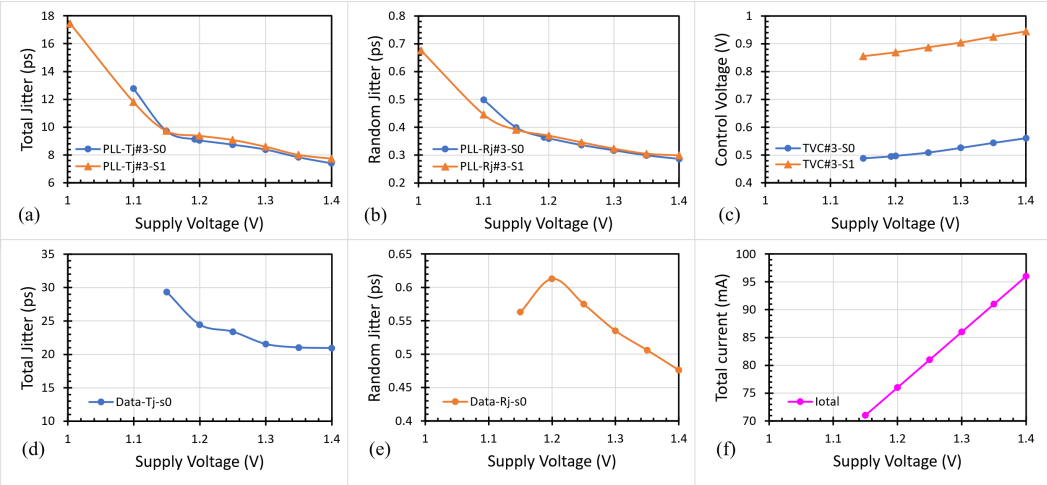


Figure 5. Measurements at different power supply voltages (0.5-m cables): (a) and (b) show the total jitter and random jitter of the PLL clock; (c) illustrates the variations of the PLL control voltage versus supply voltage; (d) and (e) present the total and random jitter of the serial output data; and (f) depicts the variations in total current.

2026 JINST 21 C02013

Table 1. Performance comparison of the recent serializer cores.

	This work	2024 [9]	2024 [10]	2021 [11]	2024 [6]	2024 [4]
Technology	55 nm	28 nm	28 nm	65 nm	130 nm	180 nm
Supply (V)	1.2	0.9	0.9	1.25	1.2	1.8
Data rate (Gbps)	10.24	25.6	8	12.5	5.12	6.25
FFE	No	3-taps	3-taps	2-taps	No	3-taps
Tj (UI)	0.252	0.333	~0.2@5 Gbps	0.623	0.234	0.284
Power (mW/ch)	96.2	225	80	30*	120	173.75
Efficiency (pJ/bit)	9.40	8.79	10	2.4*	23.44	27.8

*Only serializer power consumption.

4 Conclusion

This paper presents a prototype design and measurements of a serializer core using a CMOS-logic binary-tree architecture in a 55-nm bulk CMOS technology. It can be configured to operate at 5.12 Gbps or 10.24 Gbps for a 40-MHz system clock, and 5.55 Gbps or 11.09 Gbps for a 43.33-MHz system clock. The operating data rate depends on the specific application. The measured total jitter is around 0.252 UI, with a power consumption of about 96.2 mW. The internal timing margin is sufficient for a power supply variation from 1.15 V to 1.4 V. Table 1 shows a comparison of the recent serializer designs. In the next iteration, an optimised driver using pre-emphasis SST scheme has been integrated and taped out, to further improve the power consumption and driving capability.

Acknowledgments

This work was partially supported by the YeMinghan Foundation (No. X21520601) of the University of Chinese Academy of Sciences Education Foundation, the Independent Deployment Project of the Institute of High Energy Physics, Chinese Academy of Sciences (No. 2023000134), and the National Natural Science Foundation of China (No. 12005245).

References

[1] CEPC Study Group collaboration, *CEPC Technical Design Report — Reference Detector*, IHEP-CEPC-DR-2025-01, IHEP-EP-2025-01 (2025) [arXiv:2510.05260].

[2] CEPC Study Group collaboration, *CEPC Technical Design Report: Accelerator*, *Radiat. Detect. Technol. Methods* **8** (2024) 1 [arXiv:2312.14363].

[3] Y. Zhang et al., *Development of a CMOS pixel sensor prototype for the high hit rate CEPC vertex detector*, *Nucl. Instrum. Meth. A* **1042** (2022) 167442.

[4] J. Guo et al., *A 4×6.25-Gb/s Serial Link Transmitter Core in 0.18-μm CMOS for High-Speed Front-End ASICs*, *IEEE Trans. Nucl. Sci.* **72** (2025) 309.

[5] P. Moreira and S. Kulis, *Radiation-hard ASICs for data transmission and clock distribution in High Energy Physics*, *Nucl. Instrum. Meth. A* **1053** (2023) 168364.

[6] X. Li et al., *A 5.12-Gbps serializer circuit for front-end fast readout electronics of silicon pixelated detectors*, *Nucl. Instrum. Meth. A* **1063** (2024) 169310.

2026 JINST 21 C02013

[7] X.-T. Li et al., *A 5.12-GHz LC-based phase-locked loop for silicon pixel readouts of high-energy physics*, *Nucl. Sci. Tech.* **33** (2022) 82.

[8] M. Shoji, *Elimination of process-dependent clock skew in CMOS VLSI*, *IEEE J. Solid-State Circuits* **21** (1986) 875.

[9] A. Klekotko et al., *A Radiation-Tolerant 25.6-Gb/s High-Speed Transmitter in 28-nm CMOS With a Tolerance of 1 Grad*, *IEEE Trans. Nucl. Sci.* **71** (2024) 2124.

[10] B. Liang et al., *SEE and TID characterization of an 8 Gbps SST transmitter in a 28 nm bulk CMOS technology*, *Microelectron. Reliab.* **142** (2023) 114909.

[11] B. Liu, Z. Wang, T. Zhang and L. Zhang, *A 12.5Gbps Novel SerDes Transmitter for JESD204B Physical Layer*, in the proceedings of the *2021 5th International Conference on Communication and Information Systems*, Chongqing, China (2021), p. 6–12 [DOI:10.1109/ICCIS53528.2021.9646011].

2026 JINST 21 C02013