The HELIX128 Readout Chip Family for Silicon Microstrip Detectors and Microstrip Gaseous Chambers

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Abstract

This paper presents a description of the HELIX128-2 frontend chips that are used for the readout of the silicon microstrip detectors and the microstrip gaseous chambers in the HERA-*B* experiment. Tests in the laboratory and in the experiment show good performance characteristics and full compliance with specifications including moderate radiation tolerance.

A newer version 3.0 is under development and will also be used by the ZEUS experiment.

I. The HELIX128-2.2 and HELIX128-3.0 Chips

HELIX128-2.2 and HELIX128-3.0 are 128 channel pipelined readout chips [1] used for the HERA-*B* Silicon Vertex Detector, the microstrip gaseous chambers (*MSGC*) of the HERA-*B* Inner Tracking Detector and the ZEUS Microvertex Detector. The HERMES experiment will also use this chip for a vertex detector upgrade. A stripped-down version (without pipeline and analog readout) called *CIPix* will be used for H1's Central Inner Proportional Chamber upgrade. The chip is manufactured in the AMS CYE (0.8 μm CMOS) process and features the same architectural concept as the FElix chip [2] developed by the RD20 collaboration.

As depicted in Fig. 1, each input channel features a low-noise, low-power charge sensitive preamplifier (*CSA*) frontend and a shaper. These folded cascode [3] designs are optimized for 100 ns fall time to comply with the HERA bunch-crossing clock of 10 MHz. The output of each frontend channel feeds its signal into a capacitor array (*pipeline*) and into an AC-coupled differential amplifier type comparator circuit with a common reference voltage for all 128 channels. The outputs of these comparators are *OR*ed together in groups of 4 channels, latched and brought off-chip via open drain pads to derive a level-1 trigger signal. The pipeline consists of 141 cells per channel, which allows a maximum trigger latency of 128 samples and implements a derandomizing buffer for 8 triggered events. The oldest triggered event is read out of the pipeline via a resetable CSA (*pipeamp*). The signals are then serialized and brought off-chip by means of a 2-stage multiplexer and a current driver. The output stages operate at up to 40 MHz readout clock frequency. All amplifier stages feature forced bias currents to ensure a sufficient radiation tolerance. These currents, as well as the voltages that adjust the feedback resistances of CSA, shaper, and the comparator threshold, are generated with on-chip digital to analog converters (8 bit resolution). The DACs, together with digital circuits adjusting the trig-

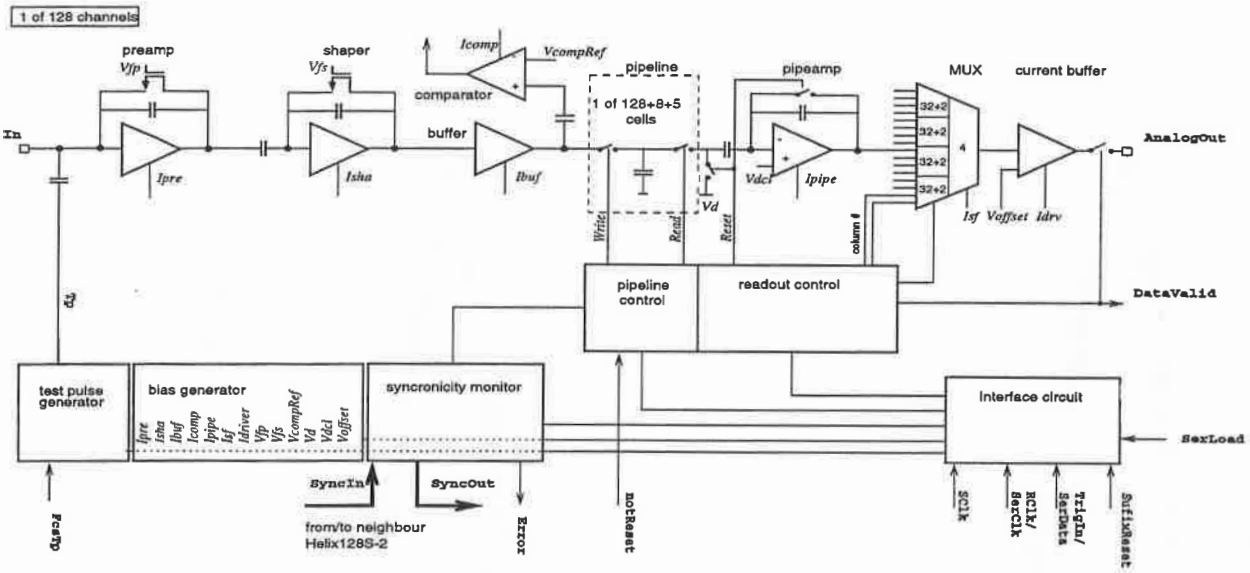

Figure 1: Schematic of the HELIX128-2 and HELIX128-3.0 chips

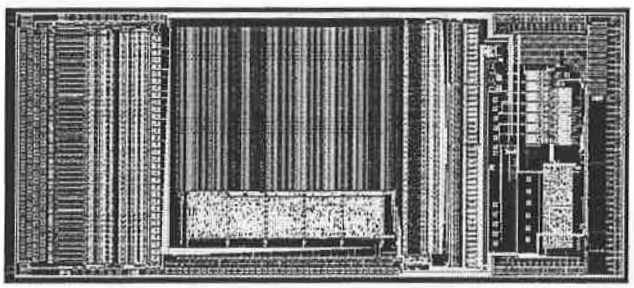

Figure 2: Layout of the HELIX128-2.2 chip

ger latency or the pause between the readout of two triggered events, are programmed via a serial interface using the trigger line for data input. The clock inputs for readout, sampling and the comparator latching, as well as the trigger inputs are equipped with receivers for LVDS signals. Pads for token and monitoring signals allow the daisy-chained readout of two or more chips and the monitoring of their synchronous operation. The HELIX128-3.0 chip, which is intended to be submitted in Oct '98, also implements a fail safe token scheme, that overcomes (non-adjacent) dead chips in a readout daisy-chain. Figure 2 shows the layout of the chip. The die size is $14.4 \times 6.2\,\mathrm{mm}^2$.

II. Performance and Radiation Tolerance

Pulse shape measurements under different input load conditions have been made. These measurements cover the full range of preamp bias currents and shaper feedback control voltages. The results (Figs. 3 and 5) show that an undershoot-free pulse with 100 ns fall time can be achieved for input load capacitances up to $\approx$30 pF. With the recommended receiver circuit, the gain of the chip was measured as 110 mV/MIP without load, dropping to 75 mV/MIP for 16 pF load. I_{pre} was adjusted to preserve a fall time of $\approx$100 ns. The measured noise characteristic of $338\,e^- + 38.4\,e^-/pF$ is depicted in Fig. 4. It closely resembles the simulated value of $287\,e^- + 35\,e^-/pF$ [5].

The comparator threshold resolution was measured to correspond to an input charge of $267\,e^-$ [6], which is small compared to the nominal signal of $35000\,e^-$ for the HERA-*B* MSGCs. In previous versions severe crosstalk between the switching comparators and the analog input was observed. Improvements in the power supply and the guardring structures healed this problem. Fig. 6 shows pulse shapes that correspond to an input charge of one MIP for different levels of threshold and different channels.

Three chips from different HELIX128 revisions were irradiated up to 2 kGy with a ^{137}Cs-source. Except for the HELIX128-2.1, whose pipeamp required a special clock pattern, all chips were fully functional after the irradiation. A fourth chip recovered to functionality after 60 hrs of annealing at 85°C. This chip was further irradiated up to 4 kGy and proofed fully functional thereafter. The pulse shape of this chip is depicted in Fig. 7. The power consumption of the chips was found to increase with the accumulated dose from 2.2 mW/ch before irradiation to 2.4 mW/ch at 2 kGy as shown in Fig. 8. The discharge of the pipeline storage capacitors due to leakage currents was found to be unaffected by irradiation up to 4 kGy (Fig. 9). More detailed tests are under way.

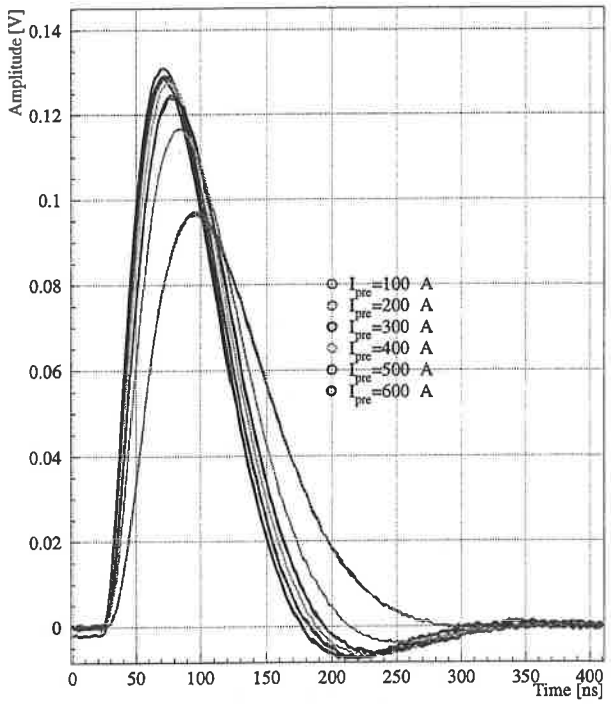

Figure 3: Pulse shapes of a HELIX128-2.2 chip at the input load capacitance of 1.6 pF for different bias currents of the preamplifier

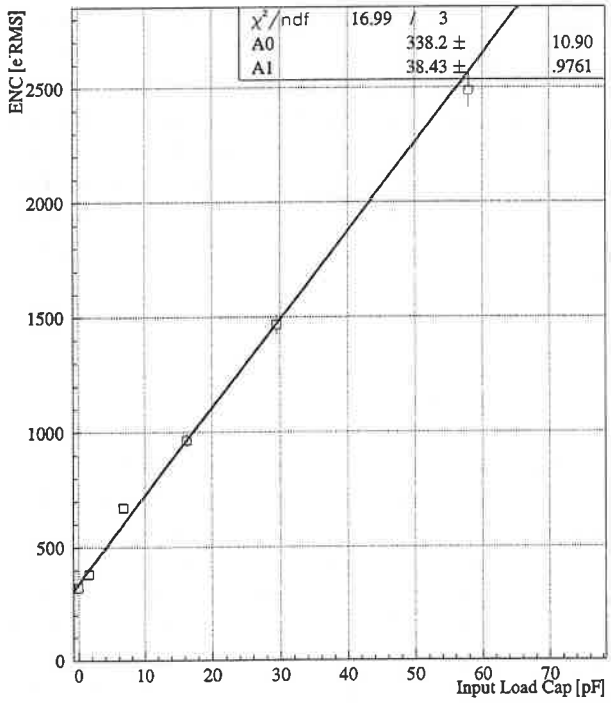

Figure 4: The equivalent noise charge (*ENC*) of a non-irradiated HELIX128-2.2 chip as function of the capacitive input load

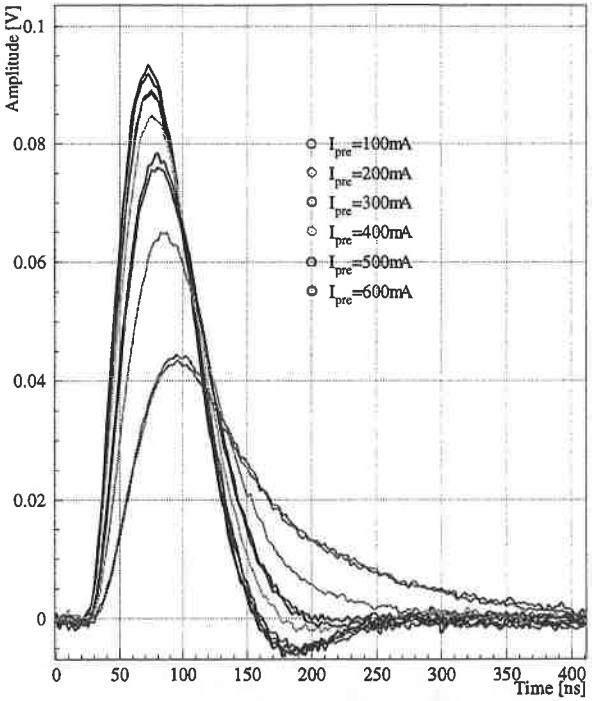

Figure 5: Pulse shapes of a HELIX128-2.2 chip at the input load capacitance of 16.3 pF for different bias currents of the preamplifier

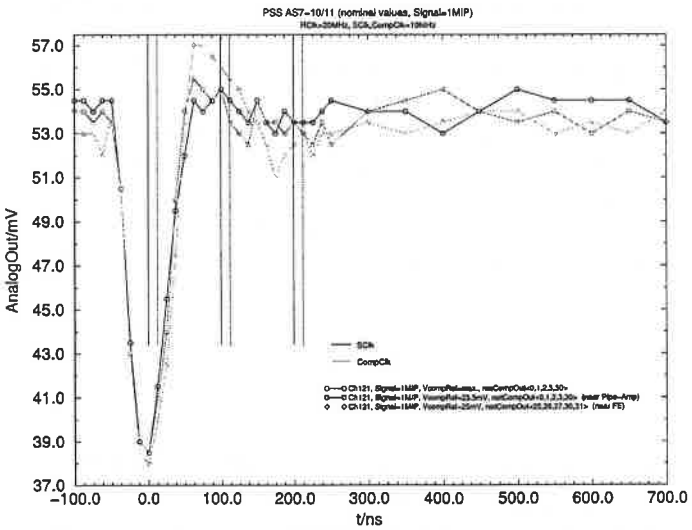

Figure 6: Scans of HELIX128-2.2 output signals for the input equivalent to that of a minimum ionizing particle (*MIP*) with (light curves) and without (dark curve) switching comparators. Vertical lines indicate the edges of the sampling (left) and comparator (right) clocks

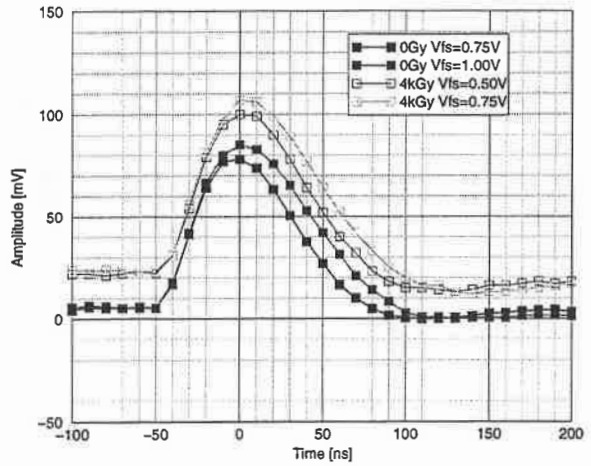

Figure 7: Pulse shapes of a HELIX128-2.2 chip before and after irradiation (4 kGy) at different V_{fs} shaper settings

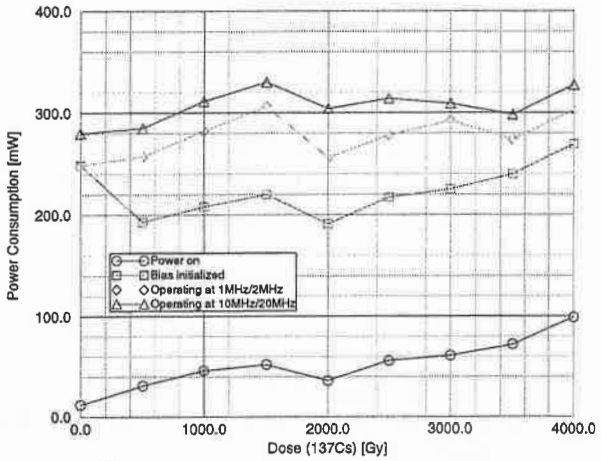

Figure 8: Power consumption of a HELIX128-2.2 chip as a function of dose at different operating conditions (from bottom to top):(a) after switching the power on, (b) after initializing the bias currents and voltages, and running the sampling and readout clocks at (c) 1 MHz resp. 2 MHz, and (d) 10 MHz resp. 20 MHz

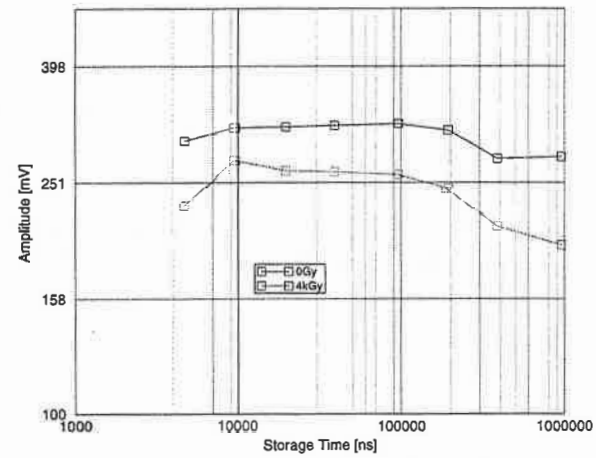

Figure 9: Discharge of HELIX128-2.2 pipeline storage capacitors before (top) and after (bottom) irradiation (4 kGy)

III. Design of Detector Readout Systems

The Inner Tracking and the Silicon Vertex Detector Systems of HERA-*B* exhibit the identical DAQ front-end architecture: a central Front End Driver (*FED*) controller provides the digital control signals (sampling and readout clocks, trigger and reset signals) for the chips, while individual 12 channel FED modules are used to digitize the analog data. In both systems pairs of HELIX128-2 chips are daisy-chained resulting in a total of more than 1000 analog signal paths. Both the digital and analog signal lines are implemented by optical links.

A MSGC tracking superlayer of the HERA-*B* Inner Tracking System consists of 4 MSGC planes; superlayers issuing also a level-1 trigger consist of 8 planes. One quadrant of a MSGC detector plane is shown in Fig. 10. The plane is read out by 3 pairs of HELIX128-2 chips, and each pair is mounted in chip-on-board technology on a multilayer printed circuit board. The connections between detector and chips are implemented with flexible microadaptors and thin film hybrids that integrate also the resistors for spark protection.

The HERA-*B* Vertex Detector System will have 7 superlayers that are implemented as a Roman pot system within a 2.5 m long conical shaped vacuum vessel. Each quadrant of a superlayer is housed in a removable pot and consists of two double-sided silicon detector modules with readout electronics. A 150 μm thick Al cap separates the HERA ring vacuum from the secondary Si detector vacuum and serves as protection against rf pick-up from the beam. A partial view of the n-side of a detector module is shown in Fig. 11. The 1280 n-side strips are connected by a 4 cm flexible microadaptor to 10 HELIX128-2.1 readout chips that are mounted together with blocking capacitors onto a 3-layer Alumina hybrid produced in thick film technology. The whole assembly is water-cooled. The three Kapton cables that are just visible at the r.h.s. of the figure connect the n- and p-side (1024 strips, 8 readout chips) hybrids via vacuum feed-thrus to the outside. Prototypes of such modules have been successfully operated at HERA-*B* since May '98. At present (Oct '98), 17 detector modules with a total of 290 readout chips are installed in the HERA-*B* Silicon Vertex Detector. Event data from one of these detector modules are shown in Fig. 12.

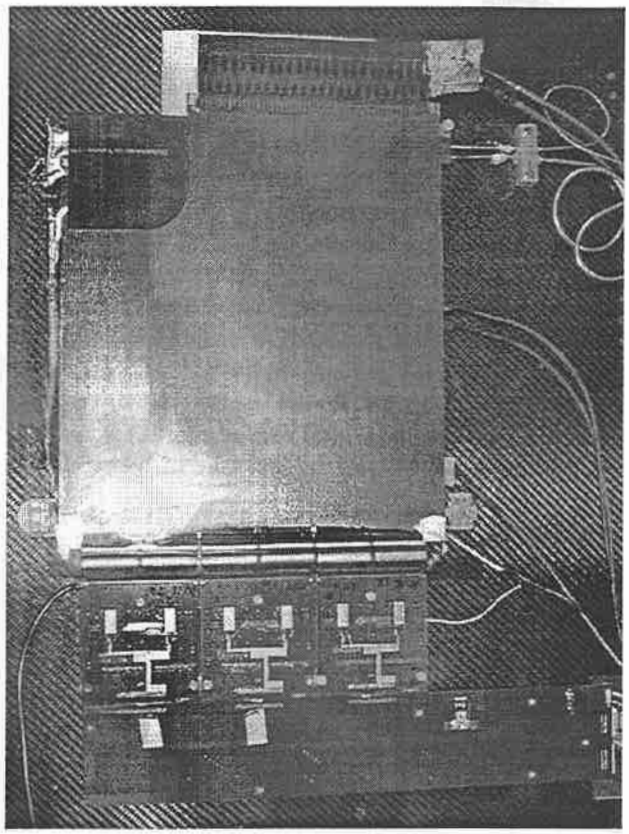

Figure 10: One quadrant of a HERA-*B* MSGC detector with HELIX128-2.2 based readout system

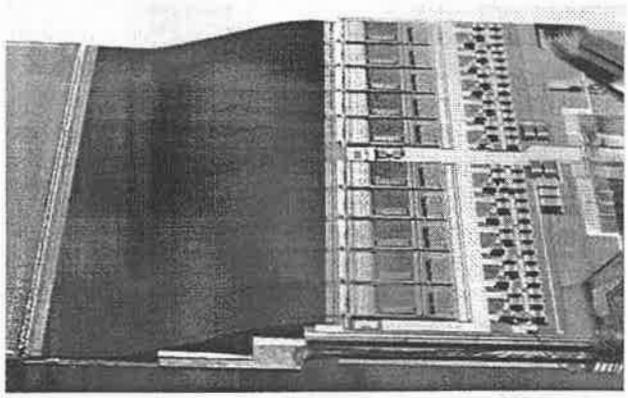

Figure 11: A partial view of a HERA-*B* double-sided Si detector module (from left to right): detector, flexible microadaptor, readout chips and blocking capacitors mounted on n-side hybrid and Kapton cables for power and signal transmission. The detector and the hybrids have different cooling paths.

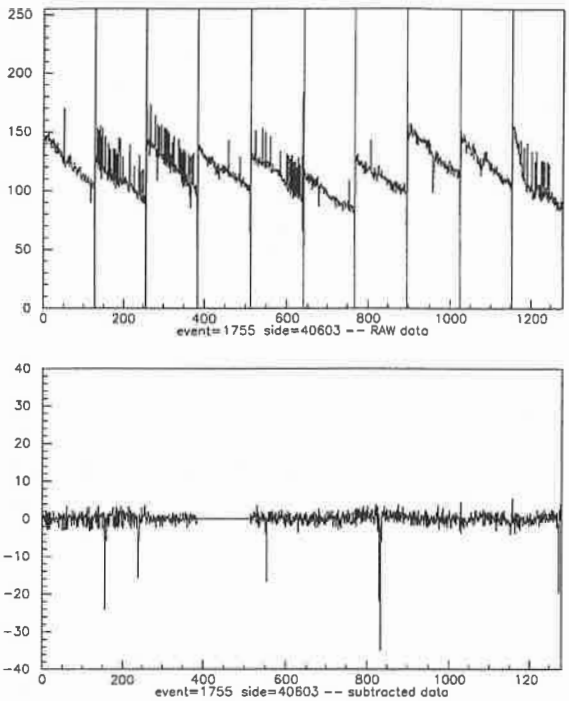

Figure 12: Raw (top) and pedestal corrected (bottom) event data from an n-hybrid of a Silicon Vertex Detector Module installed at HERA-*B*. Five hits in the processed data are clearly visible.

References

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