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The CMS Barrel Calorimeter Processor near production (BCP V2) board evaluation

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Abstract: The Barrel Calorimeter Processor (BCP), based on ATCA blade architecture, has been developed for the readout of the electromagnetic calorimeter (ECAL) and hadron calorimeter (HCAL) subdetectors of the CMS experiment. The BCP supports 120 optical receive channels of up to 25 Gbps, 72 optical transmit channels of up to 25 Gbps, an AMD XCVU13P UltraScale+ FPGA, and an embedded AMD Zynq UltraScale+ SoC. The near production BCP V2 is currently undergoing testing. This presentation highlights key testing results, such as high-speed link performance, power integrity, thermal performance and clock phase alignment as well as lessons for the design of the upcoming production BCP V3.

Keywords: Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases); Digital electronic circuits

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1 Introduction

In order to support physics data taking with the High Luminosity LHC (HL-LHC), where pile-up is expected to be as high as 200, the Electromagnetic Barrel Calorimeter (EB) of the Compact Muon Solenoid (CMS) detector [1] must tighten its timing resolution to 30 ps, increase its sampling rate from 40 MSps to 160 MSps and increase its trigger granularity from single towers of 25 crystals to single crystals [2]. In order to achieve this, new on-detector electronics for the phase 2 upgrade of the CMS detector are required. Additionally, new off-detector electronics are needed to support the increase in data volume and tighter timing resolution. This new off-detector, or back-end, electronics is called the Barrel Calorimeter Processor (BCP).

On the roadmap to a final hardware platform, the BCP near production board, or BCP V2, has been produced. This hardware (shown in figure 1) has been designed to fulfill the production back-end board specifications of both the EB as well as the Hadronic Barrel Calorimeter (HB) of the CMS experiment along with the interface specifications of the Trigger, Acquisition and control subsystems. The notable specifications for BCP V2 are:

- Compliance with the Advanced Telecom Computing Architecture (AdvancedTCA) [3] including modifications as specified by CMS [4];
- Serial data link, 120 receive and 72 transmit, running Pseudo-Random Bit-sequence (PRBS-31) at 25.78 Gbps, in external loop-back with a bit-error ratio lower than 10^{-15};
- Distribution of the system clock from the LHC accelerator, or more simply the "LHC clock", to the detectors with a Time-Interval Error (TIE) of the jitter (as measured at the EB Front-End (FE)) with a standard deviation smaller than 5 ps. This precision on the clock is well below the total 30 ps precision target required for photon timing [2]. It represents the BCP contribution to the full system;

The BCP V2 hosts one AMD/Xilinx Virtex UltraScale+ VU13P Field Programmable Gate Array (FPGA) [5] and provides optical links that are designed to run any serial protocol that is synchronous or asynchronous to the "LHC clock" within line rates 80 Mbps to 25.78 Gbps.

In this paper, we present the BCP V2's design specifications, some of the implementation challenges encountered, and its performance under test conditions aimed at verifying the design of the BCP V2.

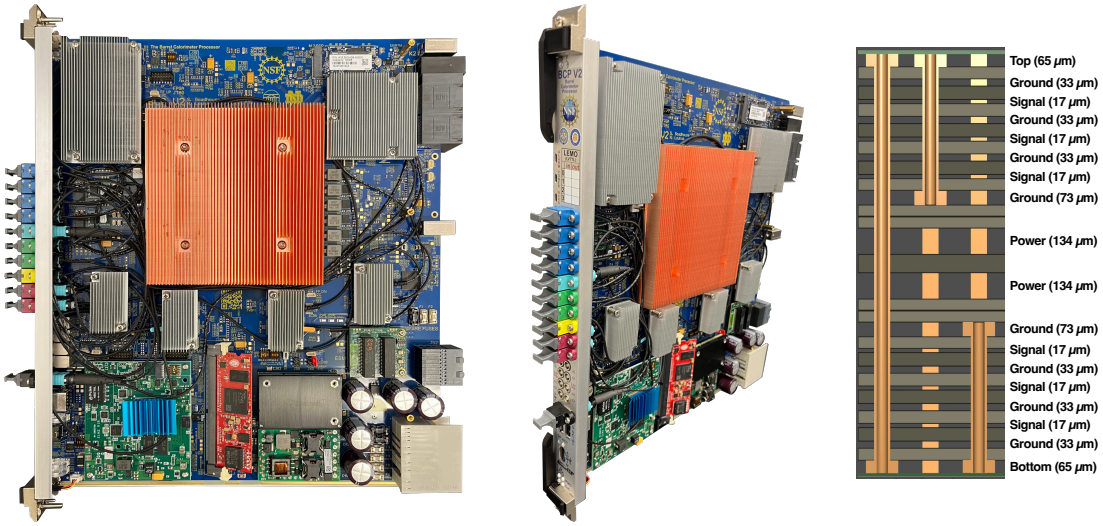

Figure 1. The Barrel Calorimeter Processor - Version 2 in multiple views including PCB stack-up with copper layer thicknesses, where 33 µm is 1 oz/ft^2. Note the extra thick copper in the middle of the PCB for the high current power rails.

2 Board design and specifications

The design of the BCP V2 adheres to the CMS ATCA Crate Specification [4], which builds on top of the AdvancedTCA Base Specification [3]. The BCP V2 has been demonstrated to adhere to: a) the crate mechanics — by successfully installing into an ATCA crate, b) the backplane interconnections — by successfully communicating to a hub card and c) the communication protocols — by testing the links as described in the next sections.

The processing power of the board is based on the XCVU13P-2FLGA2577E FPGA. The FPGA is used to receive synchronous or asynchronous data from the ECAL or HCAL detectors, uncompress any data that is compressed, generate trigger primitives (TPGs) from the data, send the TPGs to the trigger system while buffering all received data events, and write out to the data acquisition system (DAQ) the trigger-selected events while flushing the undesired events. The on-board controller for the BCP V2 is based on an AMD/Xilinx UltraScale+ ZYNQ system-on-chip (SoC) running Linux OS (Embedded Linux Mezzanine, ELM2[1]). Finally, the IPMC mezzanine is based on a ZYNQ7000 which monitors the various power rails on the BCP V2 through its programmable logic (PL) and shuts down the power within 400 µs in case of fault [6, 7].

The board is designed to support up to 20 bidirectional optical links operating up to 25.78 Gbps per link for data acquisition and BCP-to-BCP data transfer. It supports up to 24 optical transmit links, also operating up to 25.78 Gbps for Trigger. For connections with the detectors, the BCP supports up to 96 receive optical links operating between 1 and 10.24 Gbps and up to 24 transmit optical links operating between 2.4 and 2.56 Gbps. For optical transceivers, the BCP uses Samtec FireFly™ [8] in speeds 14 Gbps, 16 Gbps and 25 Gbps, along with the CERN-specified CERN-B flavor [9]. The BCP also electrically supports the 28 Gbps 12-channel flavor at the maximum 25.78 Gbps link speed.

To support the HCAL Outer sub-detector, its clock and fast control is received on 80 Mbps, single-mode optical links. The BCP does not directly support transmission over single-mode fiber

[1]Based on UW's ELM [6] and designed by Alex Madorsky while at University of Florida.

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nor a data rate lower than 1 Gbps. In order to meet this requirement, a Rear Transition Module (RTM) was designed for the BCP to support 80 Mbps over single-mode SFP modules. See section 3 for more information on the RTM.

As the BCP is responsible for delivering clocks to the on-detector electronics that all match in frequency and phase, it hosts a DDMTD that monitors the clock phase so that corrective actions can be taken if the phase is out of specification. DDMTD stands for Digital Dual Mixer Time Difference [10] and is a digital circuit that combines high-speed discrete flip-flops and the Zynq SoC to measure clocks with a precision of 1 ps.

During the design of the BCP V2, several challenges were encountered. One major design challenge was ensuring the power integrity of the board. Given the high current and low noise demands, a detailed power integrity analysis of the high-power rails was performed using the ANSYS Siwave software simulator tool [11] as well as physical measurements on evaluation demonstrator boards for the power circuits. This analysis identified multiple changes to the V2 design that reduced the temperature rise of the PCB and reduced the inductance on the power rails. These improvements resulted in a V2 design with more thermal margin, which allows for more performance from the FPGA, and resulted in less noise on the power rail, which allows for high-speed, error-free communications up to 25.78 Gbps.

The next stage in the design of the BCP is the production version, or V3. In addition to updates identified during V2 verification, the V3 design will be manufactured using halogen-free PCB material, per CERN safety instruction [12, 13]. Also, the system-on-module (SOM) Embedded Linux Module (ELM) will be replaced in the design by the widely used, low-cost and widely available off-the-shelf AMD/Xilinx Kria K26 System-on-Module (SOM) [14, 15].

3 Rear Transition Module (RTM)

The Rear Transition Module (RTM),[2] as shown in figure 2, is an accessory electronic board that adds several interfaces to the BCP. It was designed as a single mainboard with four interchangeable mezzanines for maximum flexibility. The 10G SFP+ mezzanine provides a high-speed optical path for signals from the FPGA and ELM. The SMA mezzanine provides a similar electrical path for these signals that can reach up to 10 Gbps and can also handle slower speed signals like the 40 MHz "LHC clock". The DDMTD & 1 GbE mezzanine is a double-width mezzanine that provides another DDMTD circuit to the FPGA on the BCP and also provides a 1 Gb Ethernet port for cases, such as test beams and radiation testing, where backplane Ethernet is not available. These three mezzanines provide interfaces to be used during development, testing and test stands, as needed. The fourth

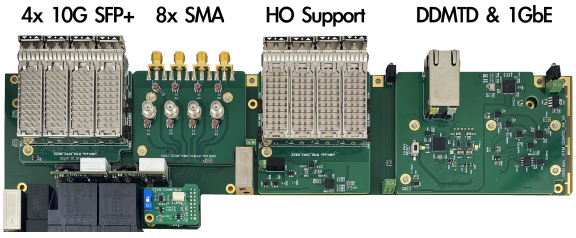

Figure 2. The Rear Transition Module - V3.

mezzanine, the HO Support mezzanine, provides quad SFPs capable of sending an 80 Mbps clock

[2]Designed by Erich Frahm at the University of Minnesota.

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and fast control to the HCAL Outer (HO) over single-mode (SM) fiber. The HO requires support for this obsolete technology because the front-end electronics have not been upgraded and are the same electronics installed during the construction of CMS. HO requires 36 SM links, so nine RTMs will be installed on nine BCPs to interface with the HO sub-detector on CMS at point 5.

4 Board evaluation and performance

One key aspect of the board evaluation is the performance of the optical links. The BCP V2 has shown excellent results in terms of error-free communication, with bit error ratios (BER) of 10^{-15} or better across all 120 optical links operating at 25.78 Gbps, meeting the design specification. Figure 3 illustrates the eye diagrams for the optical links, confirming robust performance. For these tests, all links were looped back optically, the PRBS31 data sequence was used along with a scan depth of 8. Clock Data Recovery (CDR) was enabled on all channels as is the normal operating procedure for 25G FireFly operating at 25.78 Gbps.

As detailed in section 2, there are many data rates specified for the different BCP links depending on which sub-detector is being interfaced, with the maximum specified data rate of 25.78 Gbps. For these eye diagrams, instead of only qualifying the links to their specified data rates, all links were configured for 25.78 Gbps, which exceeds many of the specifications. This was done in order to push the limits of the hardware and assess the performance margins. As can be seen, all links can operate without error at this maximum data rate.

In order to evaluate the thermal performance of the BCP V2, a single BCP was installed into an ATCA crate with firmware that allows us to manually increase the power consumption of the FPGA and has all of the multi-gigabit transceivers (MGTs) configured for integrated bit error ratio tester (iBERT [16]). The FireFly attached to the MGTs were connected in optical loopbacks. The total power consumption of the BCP was increased step-by-step until reaching 348W total consumption, of which the FPGA consumed 225W. This is the maximum power consumption expected, based on simulation and firmware power estimates. At this stage, the ATCA crate was running the fans at 14, which is one less than their highest speed, in order to keep the FPGA under 85°C. The FPGA must be kept under 85°C to meet the manufacturer recommendation for operating for over 20 years [17]. During this test, the maximum FPGA temperature was 84.3°C and the maximum FireFly temperature was recorded as 48°C. Interestingly, when the fan speed was automatically increased to keep the FPGA under 85°C, the maximum FireFly temperature dropped to 43°C. The FireFly are required to be under 50°C in order to meet their performance specifications for over 20 years of operation [18] and this test shows that they meet this specification. The three high power DC/DC converters for the FPGA core (VCCINT), FPGA MGT core (MGTAVCC) and FPGA MGT termination (MGTAVTT) power rails were recorded at maximum temperatures 62°C, 48°C and 60°C, respectively. This is well under the respective maximum component ambient operating temperatures of 125°C [19], 105°C [20] and 105°C [20]. Additionally, the BCP has three ambient board temperature sensors with one at the forced cooling air inlet at the bottom edge of the board, one 25 mm from the FPGA and near the middle of the board and one at the forced air outlet at the top edge of the board. During this thermal test, the bottom sensor measured 28.5°C, the middle measured 40.2°C and the top sensor measured 40°C, which is at most a 11.7°C ambient board temperature rise and meets the specification of 30°C maximum rise. In order for the MGT eye diagrams to be sufficiently open and the BER tests to meet specification, the power rails for the FPGA and the FireFly must have very low voltage ripple noise. Xilinx specifies noise for power rails MGTAVCC, MGTAVTT and MGTVCCAUX must all be less than 10 mV_{pp} [21, p. 341–342].

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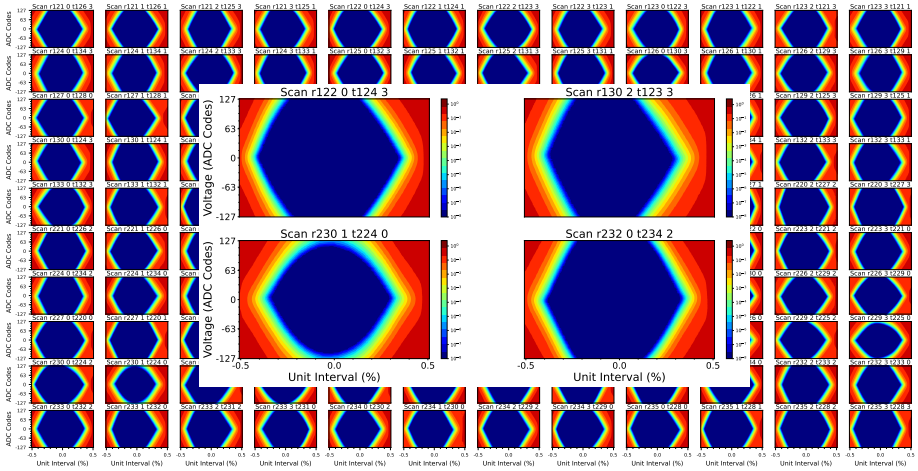

Figure 3. BCP V2 Eye Diagrams: all 120 channels from a single BCP with 4 representative channels superimposed. The dark blue open area of the eyes is the region where no error occurred during data transmission of 10^8 bits.

Additionally, VCCINT must be less than 32 mV_{pp} in order to stay within the specified voltage range [5, p. 3]. For the FireFly power, the noise ripple is specified by Samtec to be less than 50 mV_{pp} [22]. For the power rails on the FPGA, Xilinx recommends to probe them as close to the FPGA as possible and over the bandwidth 10 kHz to 80 MHz [21, p. 339]. With the BCP powered and running firmware that exercises the FireFly in optical loopbacks while consuming a typical 280W for the entire board, the voltage noise of these power rails was measured with an oscilloscope using this recommended measurement configuration. The measured MGTAVCC voltage noise was 5 mV_{pp}, MGTAVTT noise was 7 mV_{pp}, MGTVCCAUX noise was 2 mV_{pp}, VCCINT noise was 6 mV_{pp} and the FireFly power rail noise was 4 mV_{pp}. All of these results are below the minimum specification, 10 mV_{pp}, and thus, the power rail voltage noise specification was met for these critical, low-noise power rails.

The DDMTD circuit [10] of the BCP utilizes the FPGA transceiver's RXRECCLKOUT clock [21], a path which bypasses FPGA fabric and provides an accurate timing reference of the master link driving the BCP. It has been confirmed that the BCP can measure the recovered clock phase using its DDMTD circuit with a peak-to-peak error of 1 ps with respect to the reference master clock. Additionally, the BCP hardware jitter contribution to the synchronizing "LHC clock" of the upgraded ECAL front-end system has been measured to be less than 1 ps of RMS jitter.

Finally, the optical links of the RTM hardware were evaluated and found to provide better than 10^{-15} bit error ratio (BER) at the maximum data rate of 10 Gb/s. The SMA RF outputs of the RTM were used to evaluate jitter performance of the BCP and the RTM Gigabit Ethernet circuit was used to connect the on-board Linux controller to the ethernet network. Therefore, the RTM meets its design specifications.

5 Conclusions

The performance of the BCP V2 optical links were shown to meet the design specification. Moreover, the V2 hardware was shown to meet its power integrity, thermal performance and clock phase alignment specifications. The results of the continued testing of BCP V2, as guided by the QA/QC Test Plan [23], will inform updates to the design for the final V3 version.

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Acknowledgments

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