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# A NEW TIMING SYSTEM FOR PETRA IV

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*Abstract*

At DESY an upgrade of the PETRA III synchrotron light source towards a fourth-generation, low emittance machine PETRA IV is currently being actively pursued. The realization of this new machine implies a new design of the timing and synchronization system because requirements on beam quality and controls will significantly change from the existing implementation at PETRA III. As of now the technical design phase of the PETRA IV project is in full swing.

For the timing system the design process of the overall system as well as the evaluation of individual components have been started as of last year. Given the success of the at DESY developed MicroTCA.4-based timing system for the European XFEL accelerator it has been chosen to serve as a basis for the PETRA IV timing system development as well.

We present first design ideas of the major timing system hardware component, a MicroTCA.4-based AMC for distributing clocks, triggers and further bunch-synchronous information within the accelerator complex and to user experiments. First steps of an evaluation process for designing the AMC hardware are briefly illustrated.

## THE PETRA IV PROJECT

The PETRA IV project comprises the replacement of the existing 3rd generation synchrotron radiation source PETRA III with a state-of-the-art Multi-Bend Achromat (MBA)-based ultra-low emittance storage ring. This includes the upgrade of the storage ring infrastructure with a circumference of 2304 m as well as the redesign of the current pre-accelerator chain and construction of new beamlines. The 6 GeV storage ring will be operated at an RF frequency of 500 MHz as PETRA III used to be. However, the run modes will have an improved timing mode with a fill pattern of 80 bunches and 96 gaps in the ring and a brilliance mode with 1600 bunches and 20 gaps at a bunch spacing of 4 ns. In the brilliance (or coherence) mode the total bunch current will be 200 mA [1].

The present booster synchrotron DESY II will be replaced by a new one, DESY IV, to meet the requirements of a low emittance beam injected into PETRA IV. While the LINAC section will be kept, the gun will be upgraded and the old PIA ring won't be used as an accumulator anymore. The option of keeping DESY II for test beam production has to be taken into account when designing the timing and synchronization system even if this is not considered to be part of the baseline layout of the PETRA IV project. The entire facility is shown in Fig. 1.

Furthermore, the front-end electronics for diagnostics and instrumentation will be completely overhauled and based on the MTCA.4 standard. This effectively leads to the necessity to redesign the entire timing and synchronization system for the storage ring as well as for the pre-accelerator chain.

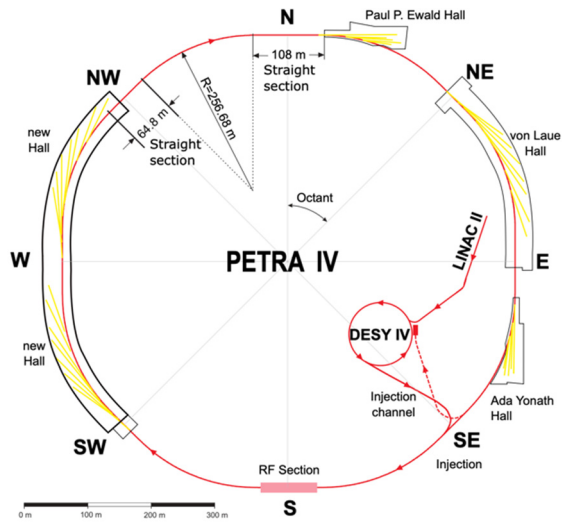


Figure 1: The PETRA IV facility layout with its experimental halls and pre-accelerators.

## THE TIMING SYSTEM DESIGN

The new timing and synchronization system for the PETRA IV project will be based on the following guidelines:

- MTCA.4 [2] will be used as the standard for the timing system electronics specifically for the transmitter and receiver module.
- Since MTCA.4 has been successfully introduced and established when constructing and commissioning the European XFEL accelerator timing system, the design of its transmitter and receiver Advanced Mezzanine Card (AMC) [3] will be used as a basis for the new PETRA IV MTCA.4 timing module.
- The design will be kept such that adaptions and modifications of the overall functionality can be implemented easily during the life-cycle of the accelerator.
- Essential to a successful realization is the expertise from both the machine beam controls and machine controls system groups, being the developers of the timing and synchronization systems for the FEL and synchrotrons at DESY.

### *Key Requirements*

The key requirements for the timing and synchronization system of which the latter is crucial for the proper RF reference and signal distribution are given as follows:

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- Distribution of a continuous RF reference signal.
- Provision of low-jitter clocks for ADC sampling.
- Distribution of timing signals, clocks and trigger events.
- Provision of beam-synchronous data such as:
  - High-resolution timestamp.
  - Revolution counter(s).
  - Beam modes.
  - Bunch pattern.
  - Bunch current.
  - Information on bunch trains to be swapped out / in.

Further, it has been proven at the EuXFEL that a common MTCA.4 module acting as a transmitter and/or as a receiver is a quite flexible and convenient concept [4].

A dedicated optical fiber network with drift compensation along the lines will be used. The topology follows the storage ring layout to make use of temperature-controlled media shafts and facilities. The storage ring, the booster and the LINAC with its gun will have its own timing system, however, being synchronized across the overall facility. Beamline experiments will have the possibility to connect to the machine timing system via the same MTCA.4-based AMC module.

### *Integration into The Control System*

An important part of the PETRA IV control system will be to provide all relevant data not only to control and monitor the entire accelerator but also to analyze its performance and proper functioning. This requires the timing system to provide the corresponding functionality. Beam-synchronous information like a high-resolution timestamp, revolution counters and a bunch pattern will be utilized by:

- Post-mortem analysis.
- Transient recorder.
- Event archives.
- Bunch-resolved data acquisition (for detailed analysis).

A possible layout is shown in Fig. 2.

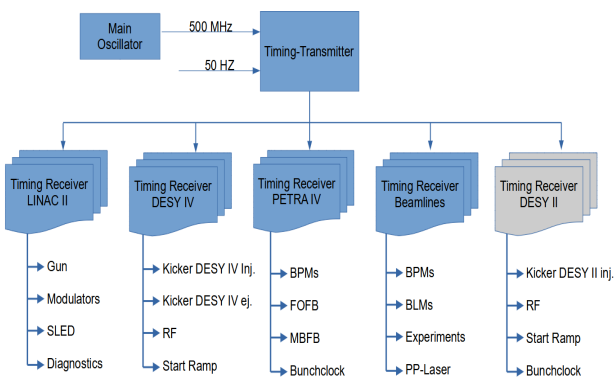


Figure 2: A possible design for the PETRA IV timing and synchronization system.

## PROJECT STATUS

### *Organization*

The timing and synchronization system project is well embedded into the overall PETRA IV project management. A work-breakdown structure as well as a product-breakdown structure with all of its deliverables have been set up. The PBS represents a hierarchical view of all PETRA IV components:

- Define the scope “What will be built?”.
- Organization of design and specification data.
- Integration of the subsystem into the overall project.

Requirements are derived for each PBS item and classified:

- Design, Interface, Functional.
- Design can be validated against requirements.
- Requirements are linked to PBS items.

### *MTCA.4 Electronics Design*

Currently we are in the evaluation phase doing pre-tests in our lab. On one side with the existing X2-Timer hardware as shown in Fig. 3 and on base of Xilinx ZYNQ Evaluation boards as shown in Fig. 4.

Here the main goal is to test the clock and trigger generation function, as used in PETRA III, and to measure the jitter quality of generated clock and trigger signals at the output.

Also, we are evaluating components for the distribution of the incoming and outgoing clock and trigger signals on the AMC-Card. Those components must have a very low additive jitter as well. Therefore, we built up a test stand for measuring their signal jitter.

Figure 3: MTCA-Setup with X2-timers.

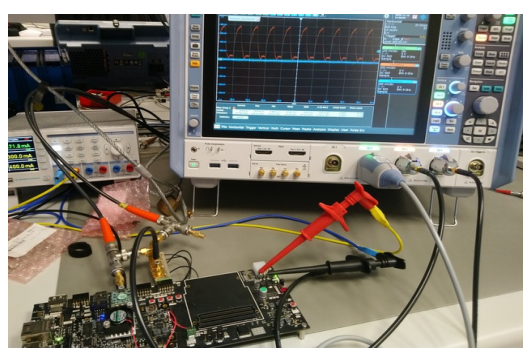

Figure 4: FPGA Evaluation board measurement setup.

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Further on we are in the process of testing new concepts for the advance delay calculation which is required to target individual buckets inside the PETRA ring. Also, we are working on different methods for the FPGA control system interface.

Our next step will be the integration of the aforementioned functionality into the existing DAMC-FMC1Z7IO AMC-Card. This MTCA.4 component is being developed by the DESY MSK group and the MTCA Technology lab.

In this step we will also test the optical fiber interconnection with its beam information distribution and clock recovery on the receiver side.

The next major development step will be to produce a prototype of an MTCA.4 AMC-Card called X3Timer. The exact design of this card is already in the specification phase and will be based on results of the requirements engineering in progress.

## OUTLOOK AND ROADMAP

Actually, we are in the TDR phase as shown in Fig. 5 where research and development for the later technical design report is being made.

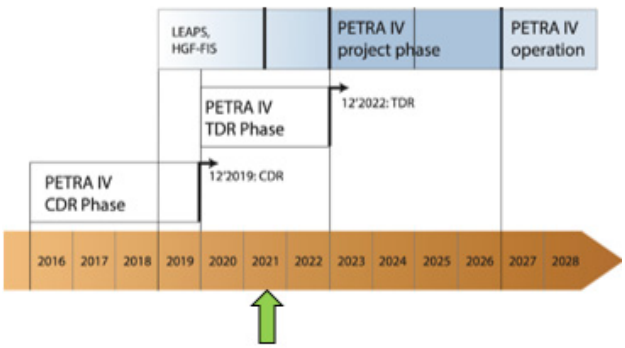


Figure 5: PETRA IV Roadmap.

Our next milestones for the for the TDR phase until end of 2022 are:

- Specify Requirements.
- Derive MTCA AMC- and RTM-Card architecture and interfaces from requirements.
- Adapt AMC- Design for X3Timer prototype.
- Hardware development and Production.
- Firmware development.
- Server and high-level controls development.

## CONCLUSION

The renewal of the timing system for PETRA IV is mandatory and in full swing. Our current pre-studies show a clearer overall picture of how the system will look like.

We are still at the beginning of the development process. The requirements from all affected groups must be collected and included in the overall system design.

Our goal within the TDR phase is to fully specify the requirements of the PETRA IV timing system and bring up a full functional prototype of the X3Timer hardware until the end of 2022.

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