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THE DIAMOND BEAM LOSS MONITORING SYSTEM AT CERN LHC AND SPS

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Abstract

The Large Hadron Collider (LHC) and the Super Proton Synchrotron (SPS) accelerators are equipped with 17 pCVD diamond based Beam Loss detectors at strategical locations where their nanosecond resolution can provide insights into the loss mechanisms and complement the information of the standard ionization chamber type detectors. They are used at the injection and extraction lines of the LHC and SPS, to analyse the injection or extraction efficiency, and to verify the timing alignment of other elements like kicker magnets. They are used at the betatron collimation region and are being also explored as detectors to analyse slow extractions. The acquisition chain was fully renovated during the second LHC long shutdown period (from December 2018 to July 2022) to provide higher resolution measurements, real-time data processing and data reduction at the source as well as to integrate seamlessly to the controls infrastructure. This paper presents the new hardware platform, the different acquisition modes implemented, the system capabilities and initial results obtained during the commissioning and operation at the beginning of the LHC's Run 3.

INTRODUCTION

The LHC is currently equipped with 12 pCVD diamond beam loss detectors (dBLM), and 5 more are installed at the SPS. Their time response, in the order of a few nanoseconds, complements the information provided by the standard ionisation chambers, which deliver very sensitive but much slower measurements (from 40 µs at LHC to 5 ms at SPS). Since the minimum LHC bunch spacing is 25 ns, pCVD detectors can provide bunch-by-bunch beam loss measurements. This time resolution is of particular interest at the injection and extraction regions, where the presence of unbunched beam or ghost bunches on the abort gap, can induce high and fast losses during the kicker ramps. This is the reason why half of the LHC diamond BLM detectors and most of the SPS detectors are located in those regions. The complete topology of the dBLM detectors can be seen in Fig. 1 where their locations are represented by green dots.

The second area of high interest equipped with three detectors per beam, is the LHC betatron collimation region, in IR7, where the LHC global aperture limit is located. On that area, bunch-by-bunch losses can be monitored along the full proton fill, and the loss distribution along the batches can provide additional information on the loss causes (electron cloud, long-range beam-beam interactions, etc) [1].

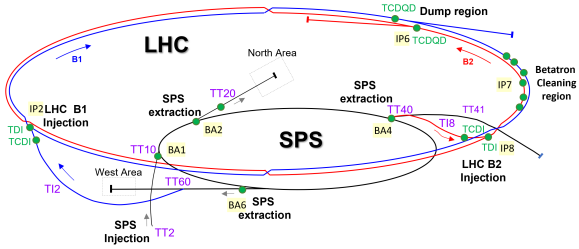

Figure 1: Location of diamond detectors at SPS and LHC.

This paper presents the recent changes that were implemented on the diamond BLM system installed in the CERN accelerator complex as well as some recent measurements to highlight their performances.

DIAMOND BLM HARDWARE

The diamond beam loss monitors consist of pCVD diamond detectors, 10 mm x 10 mm x 0.5 mm in size with gold electrodes of 8 mm x 8 mm on both sides. They are operated with a bias voltage of 500 V, which corresponds to an electric field strength of 1 V/µm. The detectors are connected to a splitter, which provides one DC and two AC outputs. Each of the two AC outputs is either amplified or in some cases attenuated in order to obtain two overlapped operational ranges, thus extending the full dynamic range. Amplifiers consist of either 20 or 40 dB gain, 2 GHz bandwidth, and can withstand up to 1 MGy TID [2].

These three elements are commercial components from CIVIDEC Instrumentation GmbH, and are mounted on a metallic support which positions the detector above or below the beam pipe, downstream of a collimator. Figure 2 shows a typical installation of one of those detectors installed by the end of one the SPS to LHC transfer lines. The acquisition

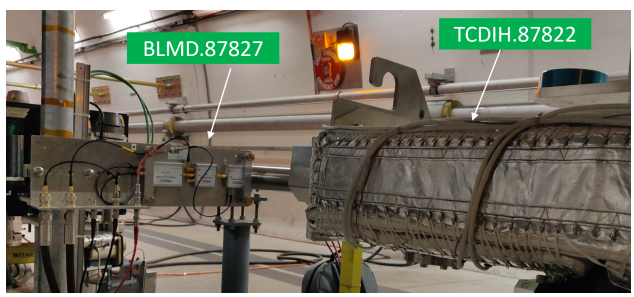

Figure 2: Photo of a dBLM detector installed at the end of the TI8 LHC injection line.

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electronics are located in the auxiliary galleries at LHC or in the surface buildings at SPS installations, where the expected radiation levels are significantly lower.

In previous runs, those detectors were readout using fast oscilloscopes or CIVIDEC's ROSY DAQ systems. However, during the second LHC long shutdown period, the acquisition system has been migrated to the standard back-end hardware platform used by the CERN Beam Instrumentation group, a 6U VME64x FMC carrier card (VFC-HD) [3]. As shown in Fig. 3, this card has been equipped with a commercial mezzanine from Innovative Integration (FMC-1000), hosting a two-channel 14-bit 1250 MSPS ADC (AD9680) and 16-bit 1250 MSPS DAC (DAC38J82). Unfortunately, the maximum operational sampling frequency is limited to 650 MSPS, due to the ARRIA V GX transceivers of the VFC-HD card [4]. This digitiser is DC coupled and its bandwidth extends from DC to 500 MHz. This migration, has been motivated by the need to homogenize the hardware and software diversity of acquisition systems among CERN beam instrumentation devices, and to reduce the maintenance and integration effort with the different CERN control layers.

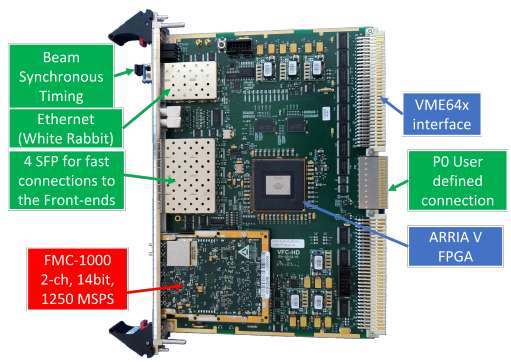

Figure 3: Photo of the VFC-HD card with a FMC-1000 card.

The current hardware platform provides a certain number of advantages, but also some inconveniences. It provides a higher resolution (14 bit instead of 8 bit ADC) and a larger bandwidth (500 MHz vs 250 MHz), but a lower sampling rate (650 MSPS vs 1.25 GSPS) and a reduced input range (±0.45 V vs ±20 V) [5] than previously tested systems. Nevertheless, the most practical advantage is the flexibility to add or adapt new acquisition methods, triggering mechanisms or correction algorithms in-house.

One important feature is that each VFC-HD card receives and decodes the CERN beam synchronous timing (BST) [6] via an optical link, providing turn and bunch clocks, triggers, and other machine information like the energy, beam mode, etc. This is of particular importance since it allows to trigger simultaneously multiple devices in the machine, with minimal skew, as well as tagging the samples as belonging to particular bunches.

ACQUISITION MODES

The FPGA hosted on the VFC-HD card has been programmed to provide several acquisition modes in parallel, from which five buffers publish data continuously and one in a triggered mode. The detectors positioned in transfer or dump lines use the triggered mode as the beam passes only once, while detectors located in rings provide data continuously, typically published and logged by the software layer at 1 Hz. The next paragraph provides a brief description of the different modes implemented:

- **Loss arrival time histogram** This acquisition mode provides the distribution of the losses arrival time along an LHC turn. The digitizers bin each LHC turn in slots of 1.53 ns (corresponding to the 650 MSPS sampling frequency). Each bin, has an associated counter which is increased if in that bin the rising edge of the loss signal crosses a programmable threshold. The counts are accumulated over a programmable time period, generally 1 s. That is, for one LHC turn, 57802 counters with 16-bit depth are used.
- **Bunch loss integral** This acquisition accumulates the digitised samples corresponding to the same bunch, during a programmable number of turns. The resulting array is published and logged by the software every second.
- **Turn loss integral** This mode presents the turn-by-turn losses for a programmable number of turns.
- **Raw distribution** This is an expert mode used to analyse the correct behaviour of the system, in particular the noise and signal distribution levels. It presents a histogram of the measured ADC samples. Histogram counters are accumulated for a programmable number of turns.
- **Bunch integral distribution** Similarly to the previous mode, this mode displays the histogram of the bunch integral losses accumulated within 1 s.
- **Capture** This mode consists on writing continuously the digitised data to the DDR VFC-HD memories, until the reception of a freeze signal, which can be received through the Beam Synchronous Timing (BST), a front-panel connector, a VME command, or can be internally auto-generated based on different waveform recognition patterns. In addition, the data recording can be gated, using a selection of consecutive bunches or some internal counters.

FIRMWARE ARCHITECTURE

Figure 4 shows a simplified functional block with the most important components of the acquisition firmware. The mezzanine contains a two channel 14-bit ADC that streams the digitised data using 4 differential 6.5 Gbps lanes. The FPGA uses an Intel JESD204B receiver IP core to receive this data. The streamed data is decoded, and split in two independent channels, exposing 4 samples/channel at 162.5 MHz (frame clock). In order to relax the FPGA timing requirements, 2 consecutive frames are grouped in a 112-bit parallel bus per

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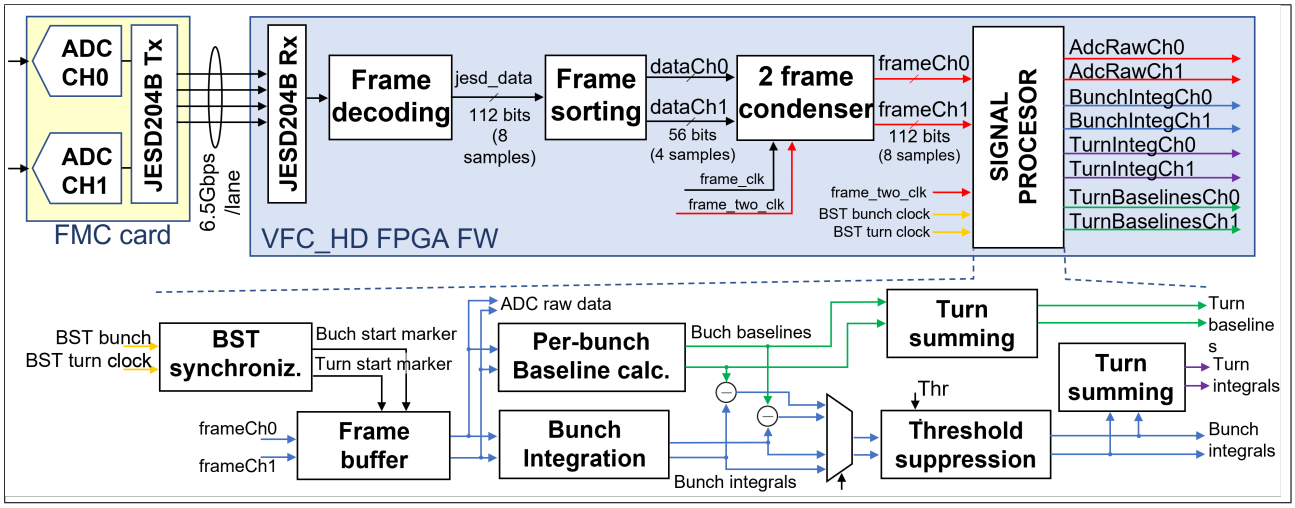

Figure 4: Simplified functional block diagram of the LHC and SPS diamond BLM firmware.

channel, which allows reducing the internal clock from this point to 81.25 MHz.

As mentioned earlier, one of the main functionalities required by the system is to accumulate the losses per bunch. For this, the system is connected to the LHC or SPS BST, which provides bunch and turn beam synchronous clocks. BST bunch and turn start flags are synchronized with the ADC samples by measuring the relative phase of those clocks with respect to the frame clock. A "Frame buffer" allows to manually apply thin delays to compensate for the cable lengths of each detector. After that, ADC samples between two consecutive bunch start flags are accumulated to get the bunch loss integrals on that turn. Unfortunately, the signals from LHC dBLM detectors show long decay tails (as it can be observed in Fig. 5), that overlap with the signals from the following bunches. This produces an error on the bunch-by-bunch loss calculation. In order to reduce this error, a module tries to estimate the baseline of each bunch, which can then be subtracted from the bunch loss integral. Finally, bunch loss integrals obtained between turn start flags are accumulated together to obtain the turn loss integrals. Optionally, one can enable a discriminator that will suppress the bunch loss integrals corresponding to values around the noise level. After this processing, bunch loss integrals are stored on buffers where each position corresponds to a particular bunch slot and are accumulated along consecutive turns for a programmable period of time. The per-bunch baseline interpolation algorithm is currently very basic. It calculates the average value using the first and last ADC samples of each bunch slot.

SYSTEM COMMISSIONING AFTER SECOND LHC LONG SHUTDOWN

The reduced input analogue range of the FMC-1000 card becomes a bottleneck at the LHC injection locations during parts of the commissioning phase, since the amount of losses change significantly between fills. This required the replacement of amplifiers and attenuators on several occasions and might require in the future an upgrade of the front-end acquisition chain to adjust the signal gains remotely.

As mentioned earlier, the calculation of the bunch loss integrals requires the beam loss data to be perfectly in phase with the bunch and turn flags. This required a commissioning step consisting in inducing losses on a particular bunch, and adjusting some fine delays, implemented in the firmware, until the signal appeared perfectly centred between the corresponding bunch flags. This can currently be done through a python application which can detect the beam populated bunch from the fast beam current transformer data and automatically calculate those delays.

Once this is done, the capture acquisition mode can optionally record data only from selected consecutive bunches, allowing longer capture windows with still very thin time resolution. This feature was tested injecting in the LHC a

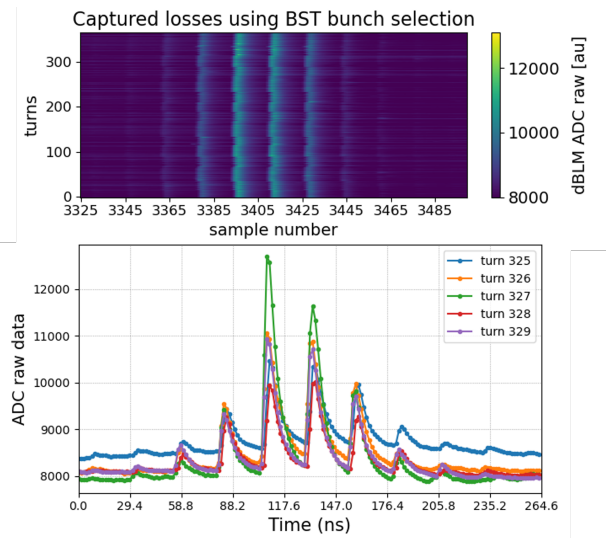

Figure 5: Capture data on selected bunches. Top: reconstruction with 365 turns. Bottom: Zoom on turns 325-329.

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train of 12 nominal bunches (3.3% of an LHC turn), and inducing transversal losses (horizontal or vertical) by adding white noise to the beam with the LHC Transverse damper (ADT) in some bunches at the center of the batch. Figure 5 shows on the top the captured data using this bunch selection feature. The bottom part shows an extraction of 5 turns from the previous figure. As it can be seen, the ADT excitation window length induced measurable losses in only 6 out of the 12 bunches of the train.

USE CASES

The time resolution of the diamond detectors opens the door to the use of loss signals in many use cases. Some examples are explained below.

LHC Injection Quality Checker (IQC)

The dBLM detectors installed at the end of the SPS to LHC transfer lines are one among the several beam instrumentation devices which are integrated into the controls application called Injection Quality Checker. This application is used to analyse the quality of each injection in terms of injection oscillations, losses, beam intensity, etc. Figure 6 shows the dBLM acquisitions from two consecutive injections on LHC B1 (top) and B2 (bottom). In the first injection, consisting of 3 batches of 36 bunches, similar losses were observed. While on the second injection, consisting of 5 batches of 36 bunches each, it can be clearly observed how the losses exponentially grow with each batch. The bottom red line represents the injection kicker strength, and it is used to examine the time relation between the losses and the kicker ramps. In the example shown, losses happened at the kicker flat top area, therefore the operators can clearly distinguish they were not due to a kicker timing misalignment.

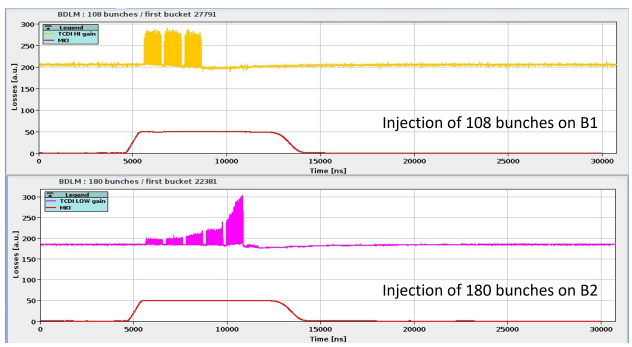

Figure 6: IQC screenshots showing injection data from the dBLM monitors in the LHC injection lines.

SPS North Area Slow Extraction

Two diamond BLM monitors are installed in the SPS extraction region towards a fixed target experimental facility, called SPS North Area. The beam is extracted via a slow extraction process (currently lasting 4.8 s), and it should be delivered to the users, unbunched and with uniform proton-on-target rates. The two detectors were recently tested to monitor the residual presence of the 200 MHz RF component along the extraction phase. Unfortunately, the diamond BLM signals in this case were very weak and polluted with some interference. In order to exploit the detectors signals it was necessary to make several 2 ms recordings using the capture mode on different extractions. These data were converted to frequency and the spectrum averaged. FFTs with and without beam were subtracted, removing thus all systematic interferences. Figure 7 shows the spectrum obtained. By triggering the capture on different moments during the slow extraction process, the evolution of the SPS RF component could be monitored and optimized [7].

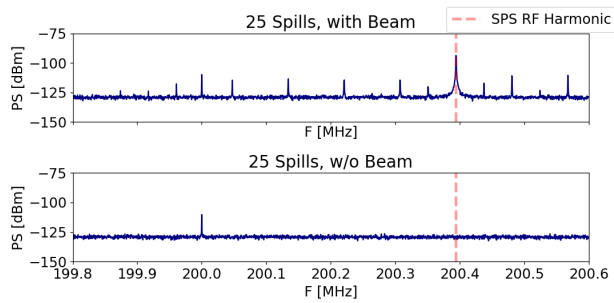

Figure 7: FFT data around the SPS RF nominal frequency as measured by diamond BLM detectors on the TT20 slow extraction line.

CONCLUSION

LHC and SPS have been equipped with BLM diamond detectors since several years. During the last LHC Long Shutdown, new acquisition systems were deployed using VFC-HD carrier modules and FMC digitiser mezzanines. It has allowed the implementation of several acquisition modes and triggering features, but its suffers from some constraints like its reduced input analogue range. The new functionalities, like the bunch-by-bunch integral and the advanced trigger mechanisms have rapidly become essential to monitor injection and extraction efficiency as well as bunch by bunch and turn by turn losses.

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