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Study on muon level-1 trigger scheme for TGC

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Abstract

In designing trigger electronics using TGCs, various choices were to be made among possible candidates of circuit designs. Synchronous and asynchronous trigger schemes were studied as part of preparation for designing Level 1 trigger for ATLAS muon TGC system. There are advantages and disadvantages for both system. Background immunity, bunch-ID efficiency and phase adjustment in clock distribution were the subjects of this study. Although we did not find large differences between these two schemes, we judged that the synchronous scheme has the edge for our TGC electronics.

1 Introduction

ATLAS experiment uses TGCs (Thin Gap Chamber) as its forward muon trigger. Forward-going muons are bent by a field generated by a toroidal coil and pass through the TGCs. There will be a triplet TGC wheel followed by two wheels of TGC doublet, totaling 7 layers of TGCs per side. Outer two wheels (four TGC layers altogether) are used for a low-Pt trigger in 3-out-of-4 majority coincidence. For high-Pt trigger, 2-out-of-3 majority coincidence from the triplets are combined with the low-Pt trigger from the doublets. We will be dealing with TGC signals totaling nearly half a million channels. Hence reliability, cost and bulk are of essential consideration in designing the electronics. One of the choice was when to do the bunch-ID. One can adjust

delays between the discriminator outputs and feed them into a coincidence. After the coincidence is taken, bunch-ID is done. We call this scheme as an "asynchronous" system. On the other hand, one can do the bunch-ID first, right after the discriminator output. Then the time-wisely-digitized signals are sent to a coincidence. We call this a "synchronous" system. These two schemes are shown in figure 1 and 2 respectively. We compared both schemes as this is the first step towards designing the muon trigger electronics system. (Please note that figs.1 and 2 show the two schemes in the simplest form to clarify the differences and real circuits when designed will be far more complex than these.)

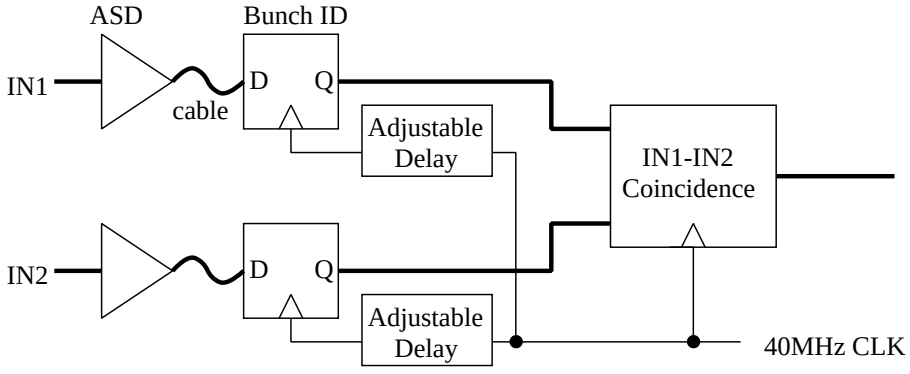

Figure 1: Conceptual description of the synchronous scheme. Bunch-ID is done right after the amplifier/discriminator circuit.

Main difference between the two is when the bunch-ID is done. In the synchronous scheme, bunch-ID is done right after the discriminator so that the signal is digitized time-wise (25 ns time block between beam crossing) at this stage. Hence the requirement for high bandwidth is on the delay adjustment circuits. From the coincidence circuit on, 40 MHz bandwidth is the requirement. In the asynchronous scheme, bunch-ID is done after the coincidence, so that high bandwidth is required to the coincidence circuit inclusively. This scheme will keep time-wise fine structure a bit. It is easy to talk about the simplicity of the two schemes, but simulation work is essential when performance on backgrounds etc. is compared. Characteristics of these two schemes will be discussed in the following sections.

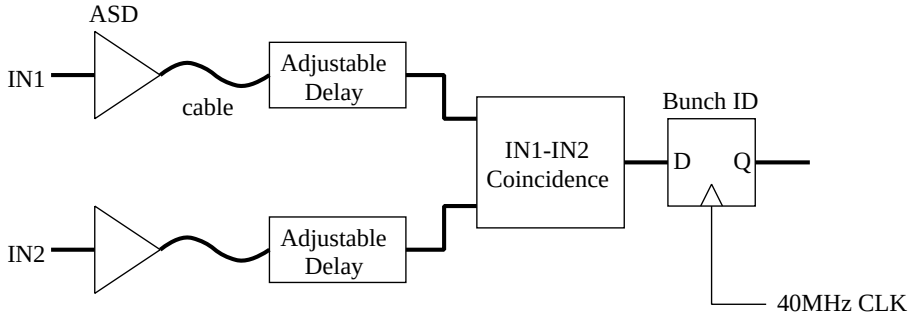

Figure 2: Conceptual description of the asynchronous scheme. Bunch-ID is done after the coincidence circuit.

2 Trigger conditions for both schemes

Figure 3 is for the synchronous scheme. In the figure, a signal will be assigned a bunch-ID number of N if the arrival time of the signal at the bunch-ID circuit, t, is

$$25ns \times N \leq t \leq 25ns \times N + GWs$$

$$25ns \leq GWs \leq 50ns$$

(GWs : gate width for the synchronous system)

Note: This is a condition for bunch-ID and not that for coincidence. The condition for the coincidence on inputs IN1 and IN2 is

$$25ns \times N \leq t_1 \leq 25ns \times N + GWs$$

$$25ns \times N \leq t_2 \leq 25ns \times N + GWs$$

t_1 and t_2 : arrival times for IN1 and IN2 respectively.
In the asynchronous scheme, the condition for two inputs, IN1 and IN2 is

$$|t_1 - t_2| \leq GWa$$

(GWa : gate width for the asynchronous system)

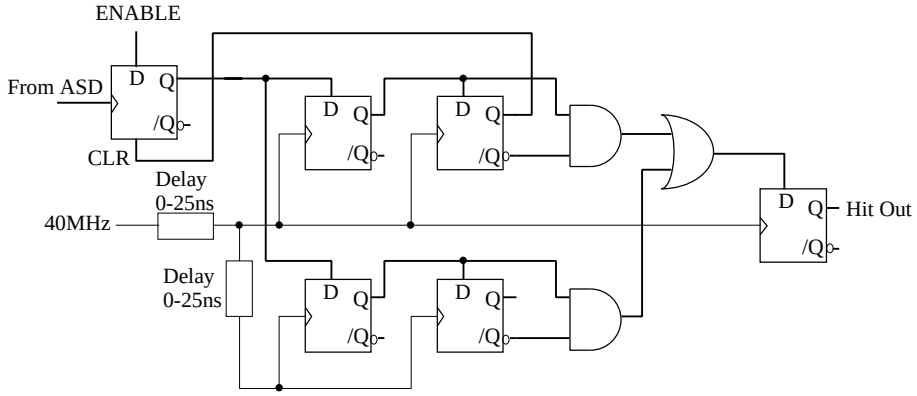

Figure 3: Conceptual design for the variable gate width for the synchronous system. First delay unit is to adjust for phase differences and the delay unit for lower-half section makes the gate width to be between 25 ns and up to 50 ns.

The gate width, GWa, is the signal width of the input (IN1/IN2), hence GWa can be varied by changing the input signal width. The output timing from the coincidence is normally the timing of coincidence condition being satisfied, ie., the last arrival timing of the input signal that establishes the coincidence condition. This output timing determines the bunch-ID timing for the coincidence.
The two different schemes result different time-window area on arrival times to the coincidence. This situation is shown in figure 4.
Background rate is, for the first approximation, proportional to the shadowed area in the figures. In the synchronous case when the gate width is larger than the time interval between beam crossings, there is an overlapped area in successive window areas. One way to deal with this situation is to select only the later entry when there are two consecutive entries. We will come back to this in later part of this section.

3 Time jitter distribution from TGC

The time jitter of a thin gap chamber (TGC) was calculated using a simulation program, "TARFIELD" [1] , using the parameters in ATLAS Technical

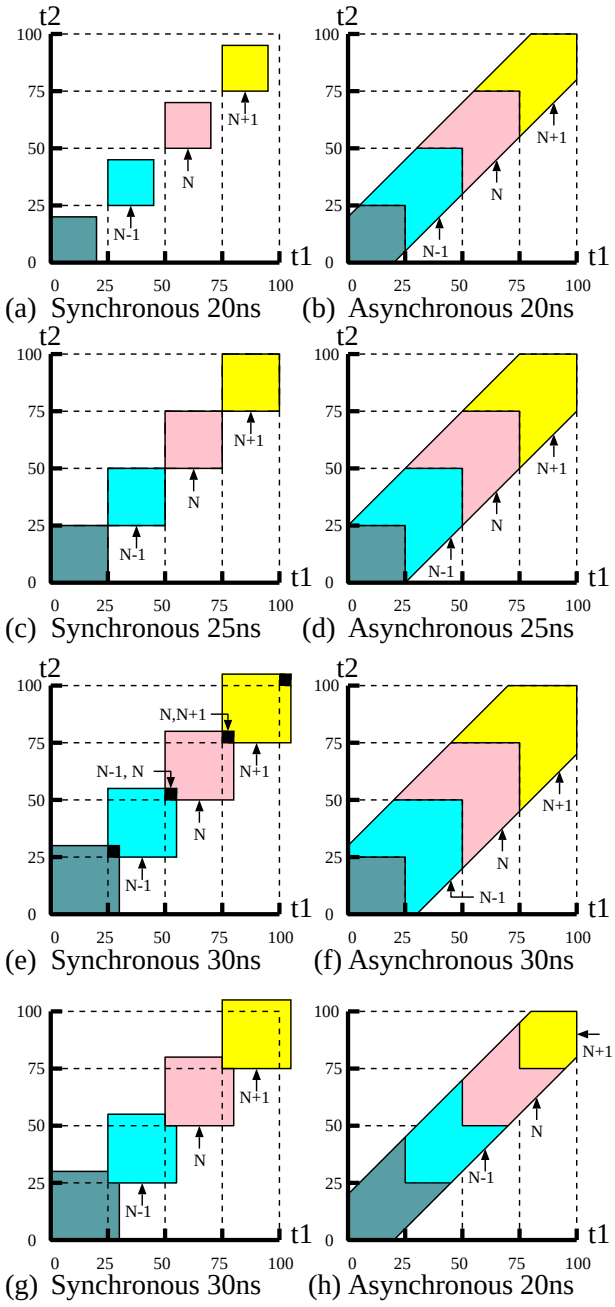

Figure 4: Time-windows for the coincidence are compared. Left-side figures are of the synchronous scheme and the right-side figures are of the asynchronous scheme both at different gate widths. Only two input signals to the coincidence is shown here. The t_1 and the t_2 corresponds to arrival times to the circuit. The figures 4-c and 4-d correspond to the gate width of 25 ns, exactly matching to the bunch crossing interval of 40 MHz. Figures 4-a and 4-b are for 20 ns gate width and figures 4-e and 4-f are for 30 ns gate width. In figure 4-e, darker-shadowed areas correspond to entries that would cause ambiguities. By taking only the last entry where there are more-than-one successive bunches that have hits, figure 4-g results. Figure 4-h results when special circuit is added to use the timing of the first arrival for bunch-ID. (see "Bunch-ID efficiency" section).

Proposal:

- ◇ distance between the anode wire and the cathode plane = 1.6 mm
- ◇ spacing between anode wires = 2.0 mm
- ◇ supplied high voltage = 3,100 volts
- ◇ anode wire radius = 25 μm
- ◇ chamber gas mixture = carbon dioxide + normal pentane

The TARFIELD program is known to work well since the program reproduced our beam test results very well. Figure 5 shows the time jitter of the TGC signal estimated by the TARFIELD program using above parameter set as well as the result from real beam test. Transmission delays through anode wires (or cathode readout strips) are taken into account. (note: Spacing between anode wires is changed to 1.8 mm which only improves the timing performance.)
At the present set up of end-cap TGCs in ATLAS experiment, most particles pass through a TGC plane at 10 - 30 degrees incident angle from vertical line to the TGC. As clearly shown in the figure 5, 30-degree incident angle case has less time jitter than that for 10-degree incidence. The tail of the time distribution reaches to the bunch crossing interval of the LHC experiment. Bottom two figures are the same as the middle ones except that 7ns transmission is included. The time-jitter distribution with 10 degree incident/7ns delay was used for all the simulation works shown below.

4 Background immunity

We used non-correlated 100 kHz random pulse inputs to the 3-out-of-4 coincidence and estimated accidental coincidence rate as a function of the gate width (GWs/GWa) for both schemes. The 100 kHz number came from the 10 cm x 1 m strip-size under 100 Hz/cm^2 rate. The result of this calculation is shown in figure 6 through figure 11. The difference in window area of figure 4 in these two schemes resulted difference in accidental rate for the same gate width (figures 6 through 11).
Figures 6 through 11 tell that background rate in the synchronous scheme

at a coincidence gate width (say GWs = 30 ns) is equivalent to that at 10 ns narrower gate width (say GWa = 20 ns) in the asynchronous scheme. In other words,

$$\text{background rate (GWs = W)} \approx \text{background rate (GWa = W} - 10 \text{ ns)}$$

5 Bunch-ID efficiency

We did simulations to find bunch-ID efficiency on 3-out-of-4 coincidence. In the following discussion, simulation is done assuming that the clock phase are matched to the optimum condition. Figure 6 corresponds to the figures 4-a,c,e case. We found that the accidental rate for one-crossing-earlier rises sharply on the synchronous case (figure 6) due to the overlap of two window areas with the (N-1)th beam-crossing window. By eliminating earlier-hits when there is a consecutive hit with a relatively simple additional circuit, the result will be an acceptable one as shown in figures 7 (which corresponds to figure 4-g case). Note that, as shown in figure 5, major part in time jitter distribution is between 0 and 10 ns. The overlap region is contains very small portion of events even for 10-degree incidence and negligible for 30-degree incidents. The result tells that less-than-30 ns gate width provides 100% efficiency with no mis-identification on bunch-ID in this case. Figure 8 shows the asynchronous case. (Corresponds to figures 4-b,d,f case). It tells that around 20 ns gate width will be adequate to establish a 100% 3-out-of-4 coincidence condition. However, it should be noted that further widening of the gate width will not improve the bunch-ID efficiency, because of a problem that some will get an incorrect assignment on bunch-ID as in figure8(d). This problem can be serious if intrinsic resolution of the TGC get much worse. This problem can be taken care if one could implement an extra circuit for each coincidence unit that uses the timing of the first arrival to assign a bunch-ID although the circuit would not be a simple one to implement. (This corresponds to figure 4-h.) However, if we could do this, the result will look like figure 9. When figure 8 and figure 9 is compared, the mis-identification problem is gone, but there is no other improvement in required gate width condition. Figures 10 and 11 show the same for the 30-degree incident angle for both synchronous and asynchronous schemes. The result clearly tells improvement in required gate width in both case as expected.

In summary, the synchronous scheme requires approximately 30 ns gate width while the asynchronous scheme requires approximately 20 ns gate width to get 100% bunch-ID efficiency. Both has the same background immunity under this condition.

6 Phase adjustment in clock distribution

It is obvious that clock phase has to be worried about in the synchronous scheme and in the asynchronous scheme although timing-adjustment circuits exists in both cases. To find out required precision we need to provide clock to bunch-ID circuits (in both schemes), we did a simulation study for both cases. Following argument assumes that there is no channel-to-channel transmission delay difference from a TGC ASD channel to the trigger circuit. We worry only about the required precision of relative clock phase to the bunch-ID circuits here. Figures 12 and 13 are the results of this simulation. (Figure 12 corresponds to figure 4-g. Figure 13 corresponds to figure 4-b.)
From the figures 12 and 13, the situation is basically the same between the two schemes and the required precision to align the clock phase will be around a few nanoseconds in both cases. Gate width does not play an important role here. However, intrinsic time jitter in TGCs does play an important role here.

7 Summary

Our study on trigger scheme made us to understand the problems we will face for the trigger circuit. As you can see from above, the synchronous scheme requires approximately 30 ns gate width while the asynchronous scheme requires approximately 20 ns gate width to get 100% bunch-ID efficiency. Both has the same background immunity under this condition. As for the phase adjustment in clock signal routing, the synchronous scheme seems to require a precision of several nanoseconds while the asynchronous system require slightly tighter adjustment for the same condition. There is no clear winner in the choice of a trigger scheme, we would prefer the synchronous scheme basically because it will be a bit more robust and simpler.

References

[1] This TARFIELD program is a simulation program for the TGCs which requires precision in estimating shower tail. It is more precise in estimating time jitter than standard GARFIELD program. (S.Tanaka : to be published.)

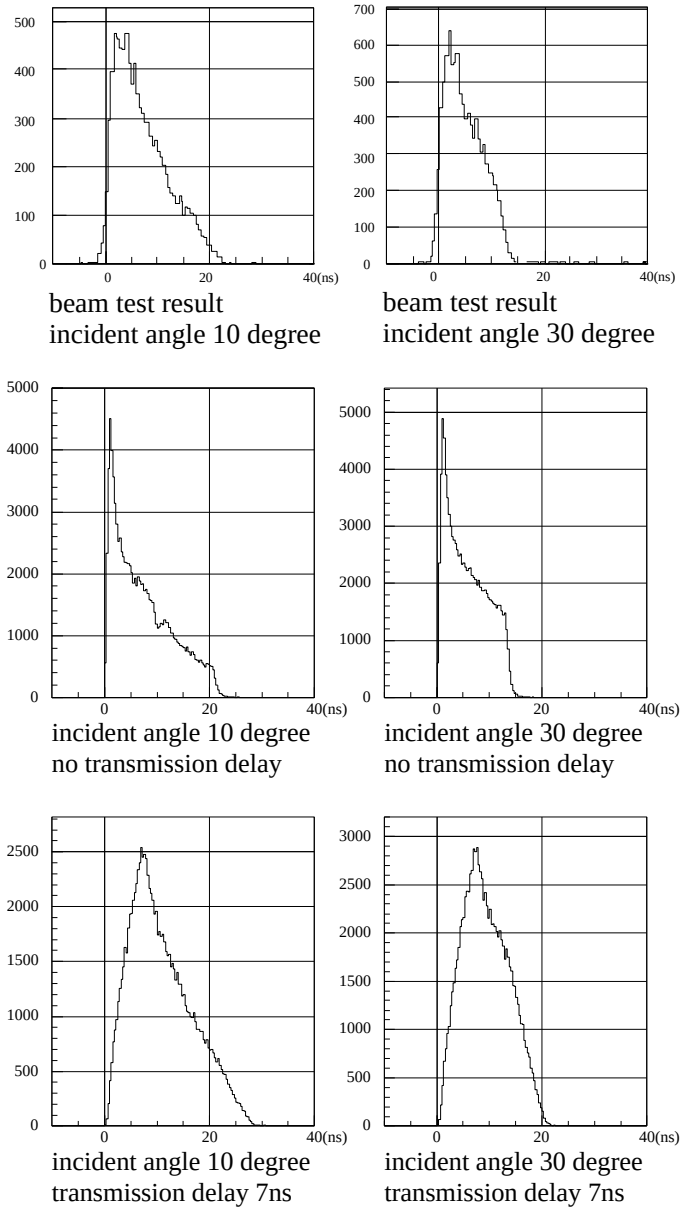

Figure 5: Time distributions of the TGC signal. The left-side figures are for 10-degree incident angle and the right-figures are for 30-degree incident angle. Top two figures are real data from experiments where beam was hitting a fixed spot. Rest of the figures were calculated from a simulation program TARFIELD. Middle figures are not counting transmission delays neither other factors which exists in reality, (time jitter of discriminator outputs, noise contribution and so forth), so that we could see raw data structure. Bottom two figures include a transmission delay of 7 ns through wires (or cathode readout strips).

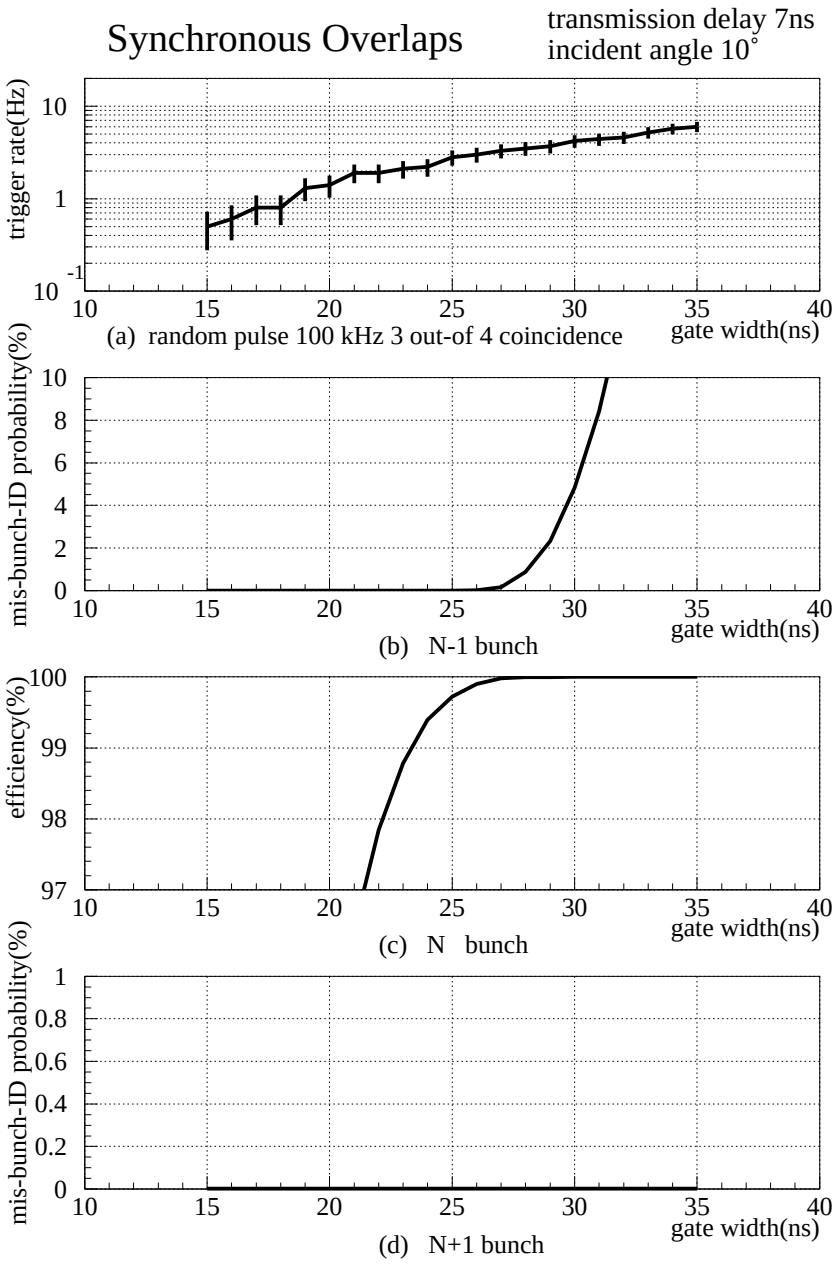

Figure 6: Synchronous scheme (corresponds to the case in figure 4-e. 10-degree incident angle case is considered.)
(6-a) The background rate from the random pulse of 100 kHz as a function of gate width.
(6-b,c,d) Calculation of the rate of coincidence for the background.
6-c is for the correct bunch-crossing time, 6-b for the bunch-crossing one prior to the correct one and 6-d the same for one after the correct one.

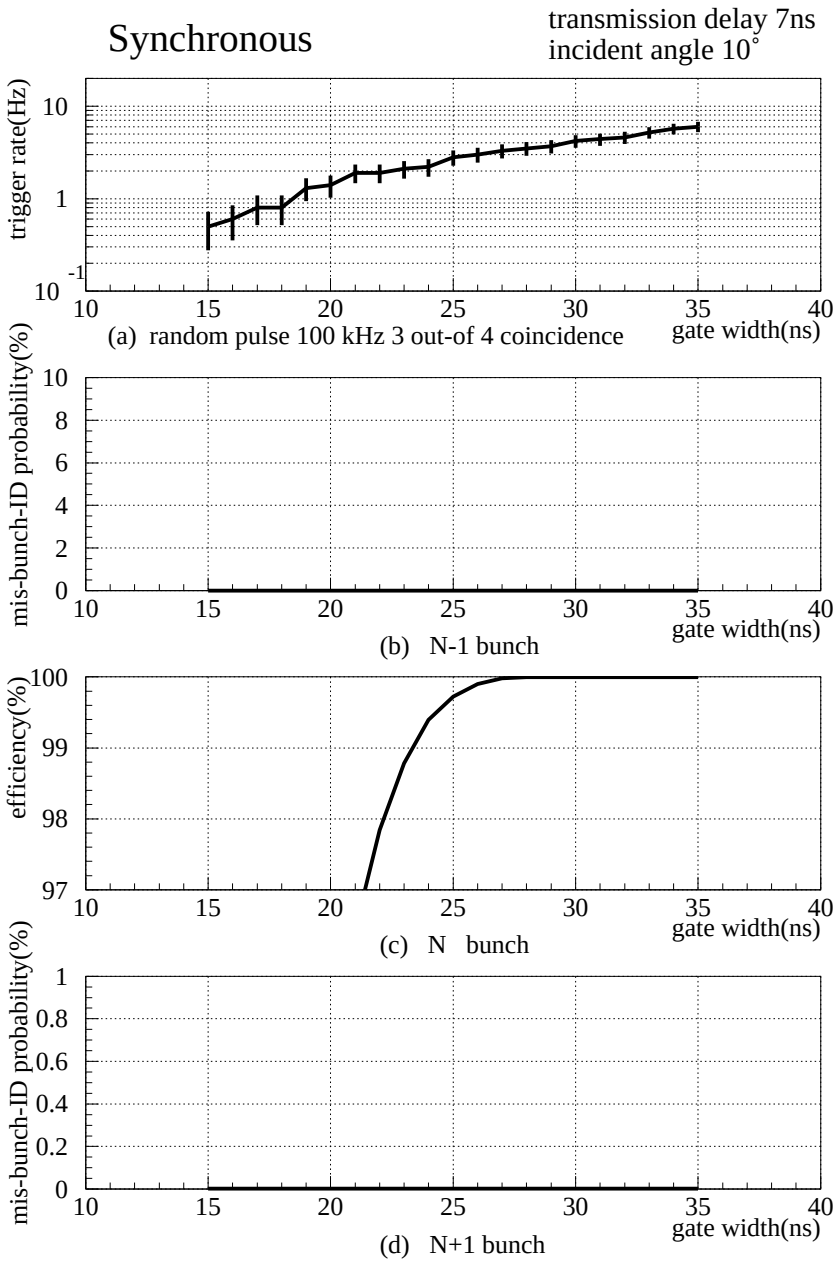

Figure 7: Synchronous scheme (corresponds to the case in figure 4-g. 10-degree incident angle case is considered here.)
(7-a) The background rate from the random pulse of 100 kHz as a function of gate width.
(7-b,c,d) Calculation of the rate of coincidence for the background.
7-c is for the correct bunch-crossing time, 7-b for the bunch-crossing one prior to the correct one and 7-d the same for one after the correct one.

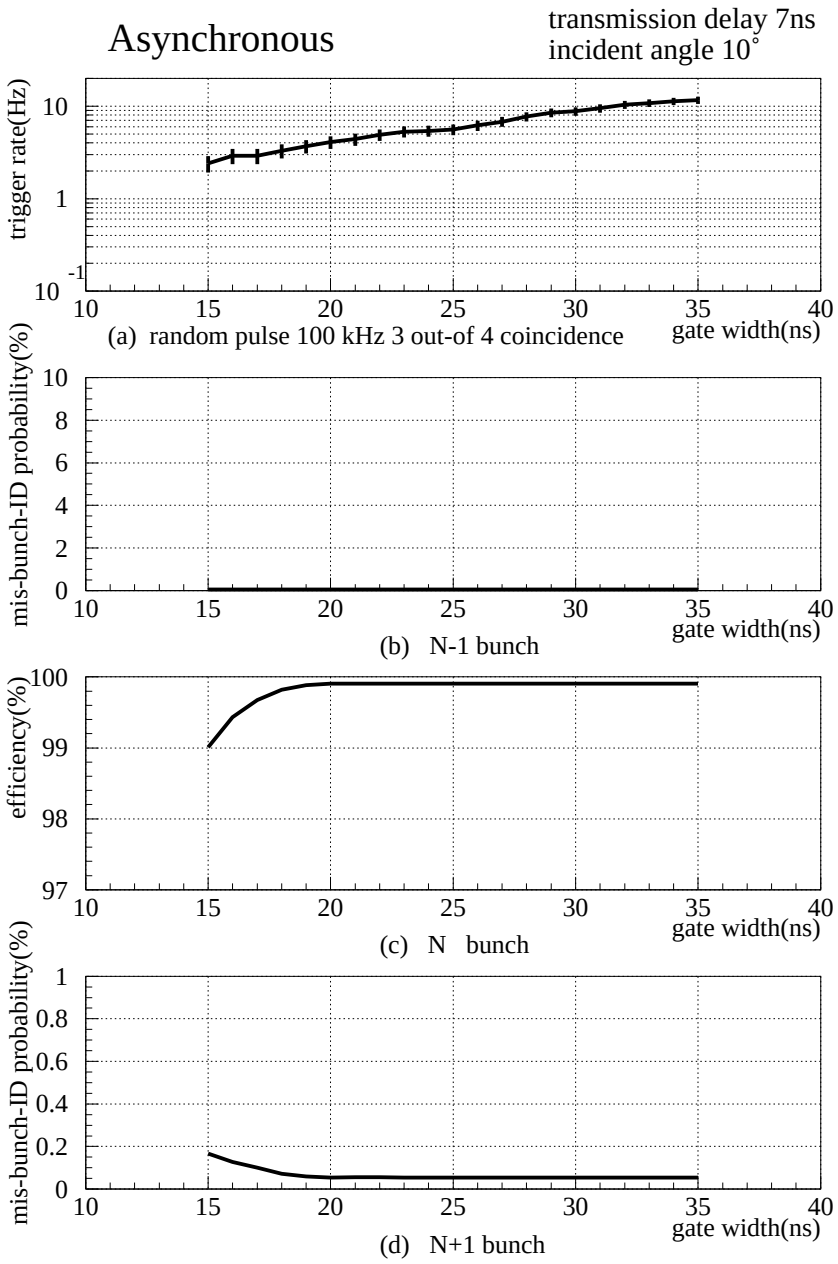

Figure 8: Asynchronous scheme (corresponds to the case in figure 4-f. 10-degree incident angle case is considered.)
(8-a) The background rate from the random pulse of 100 kHz as a function of gate width.
(8-b,c,d) Calculation of the rate of coincidence for the background.
8-c is for the correct bunch-crossing time, 8-b for the bunch-crossing one prior to the correct one and 8-d the same for one after the correct one.

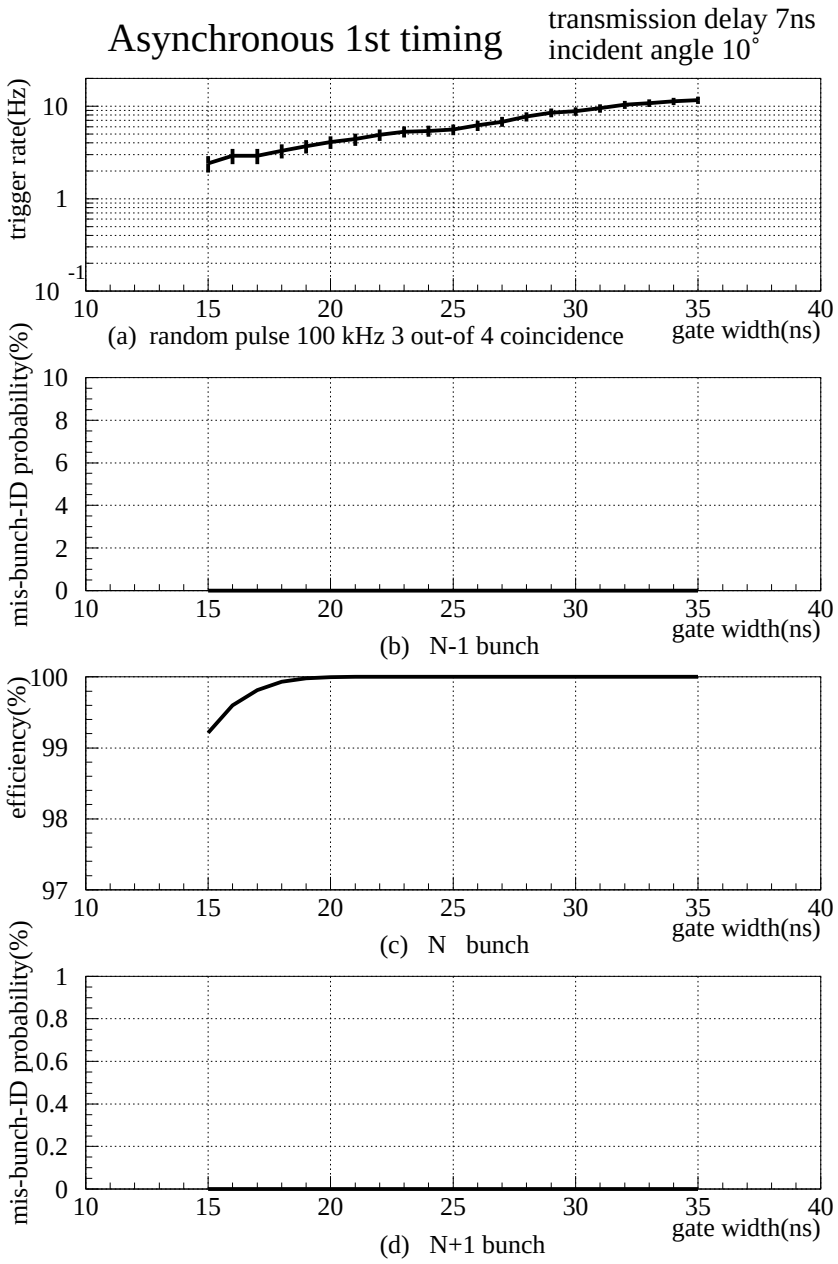

Figure 9: Asynchronous scheme (corresponds to the case in figure 4-h. 10-degree incident angle case is considered.)
(9-a) The background rate from the random pulse of 100 kHz as a function of gate width.
(9-b,c,d) Calculation of the rate of coincidence for the background.
9-c is for the correct bunch-crossing time, 9-b for the bunch-crossing one prior to the correct one and 9-d the same for one after the correct one.

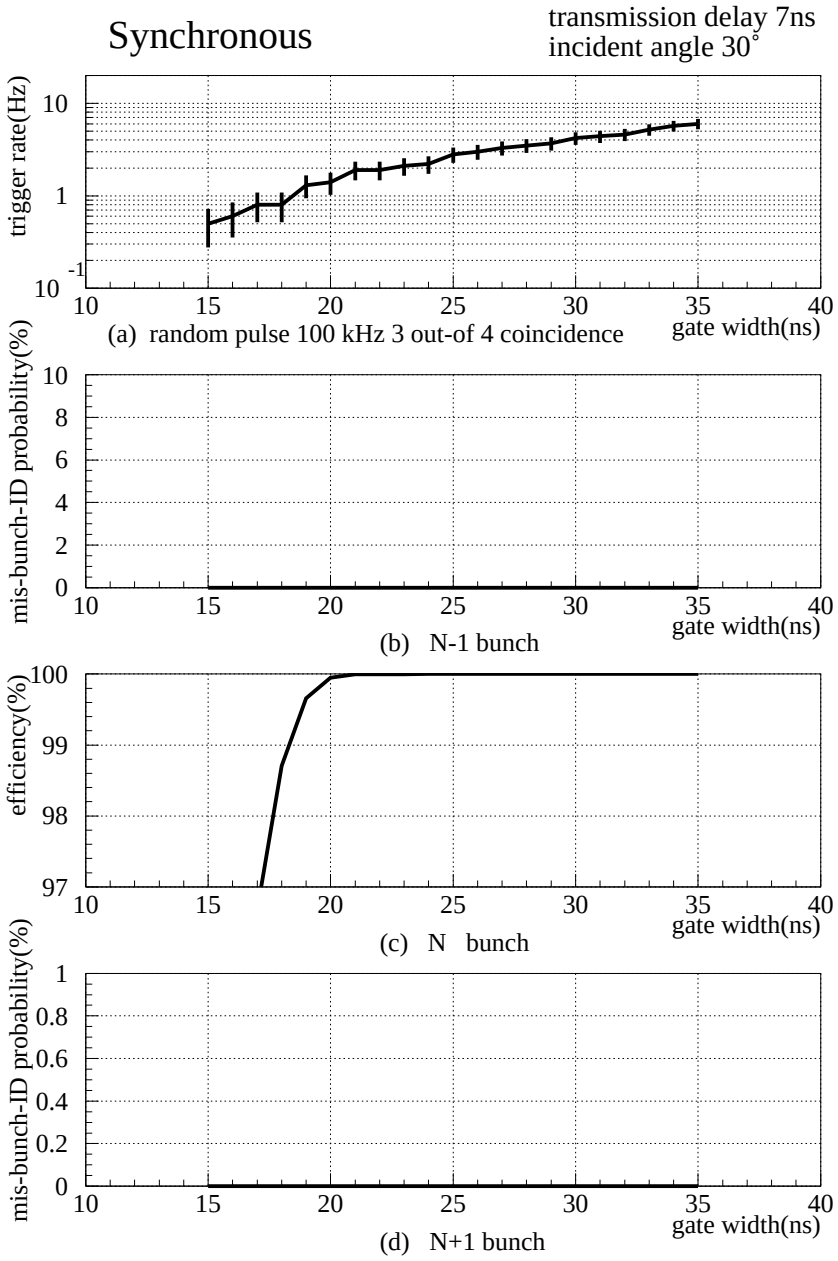

Figure 10: Synchronous scheme (corresponds to the case in figure 4-g. 30-degree incident angle case is considered.)
(10-a) The background rate from the random pulse of 100 kHz as a function of gate width.
(10-b,c,d) Calculation of the rate of coincidence for the background.
10-c is for the correct bunch-crossing time, 10-b for the bunch-crossing one prior to the correct one and 10-d the same for one after the correct one.

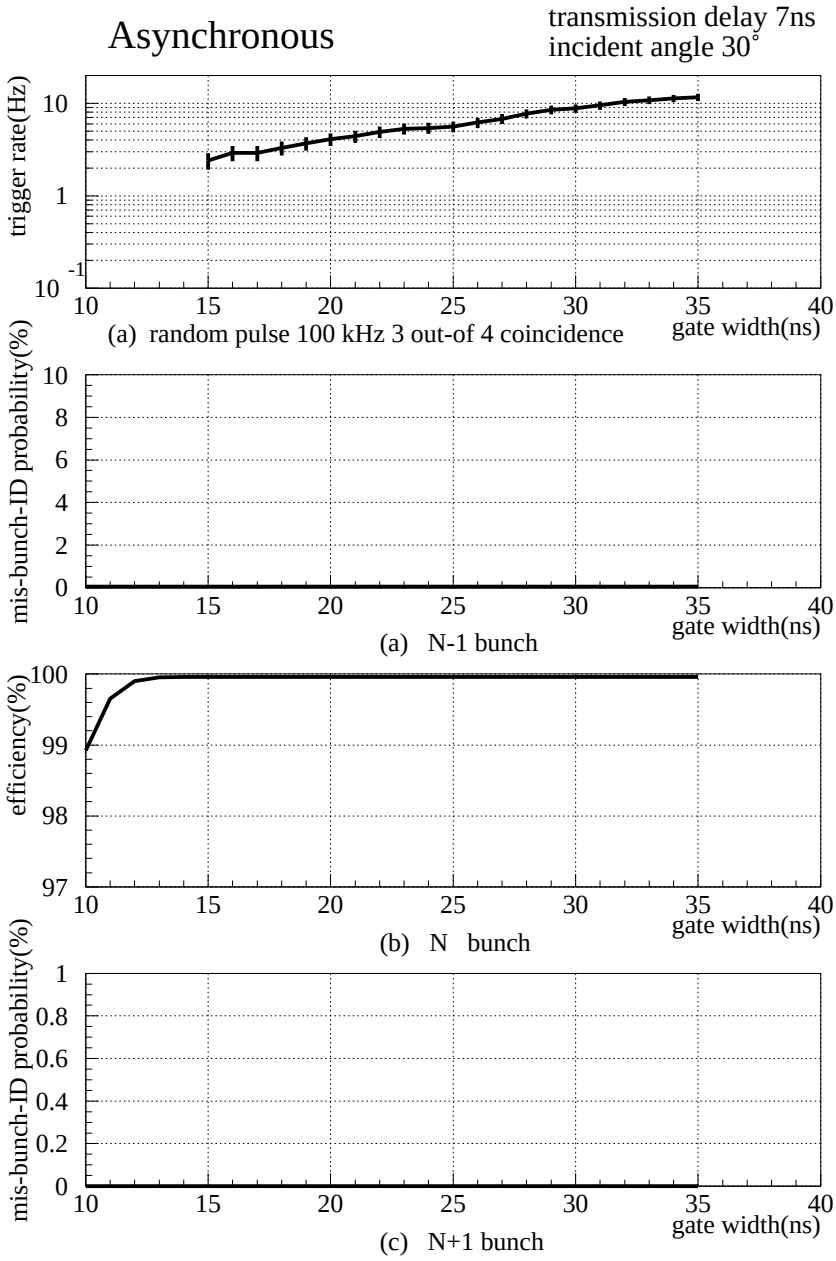

Figure 11: Asynchronous scheme (corresponds to the case in figure 4-h. 30-degree incident angle case is considered.)
(11-a) The background rate from the random pulse of 100 kHz as a function of gate width.
(11-b,c,d) Calculation of the rate of coincidence for the background.
11-c is for the correct bunch-crossing time, 11-b for the bunch-crossing one prior to the correct one and 11-d the same for one after the correct one.

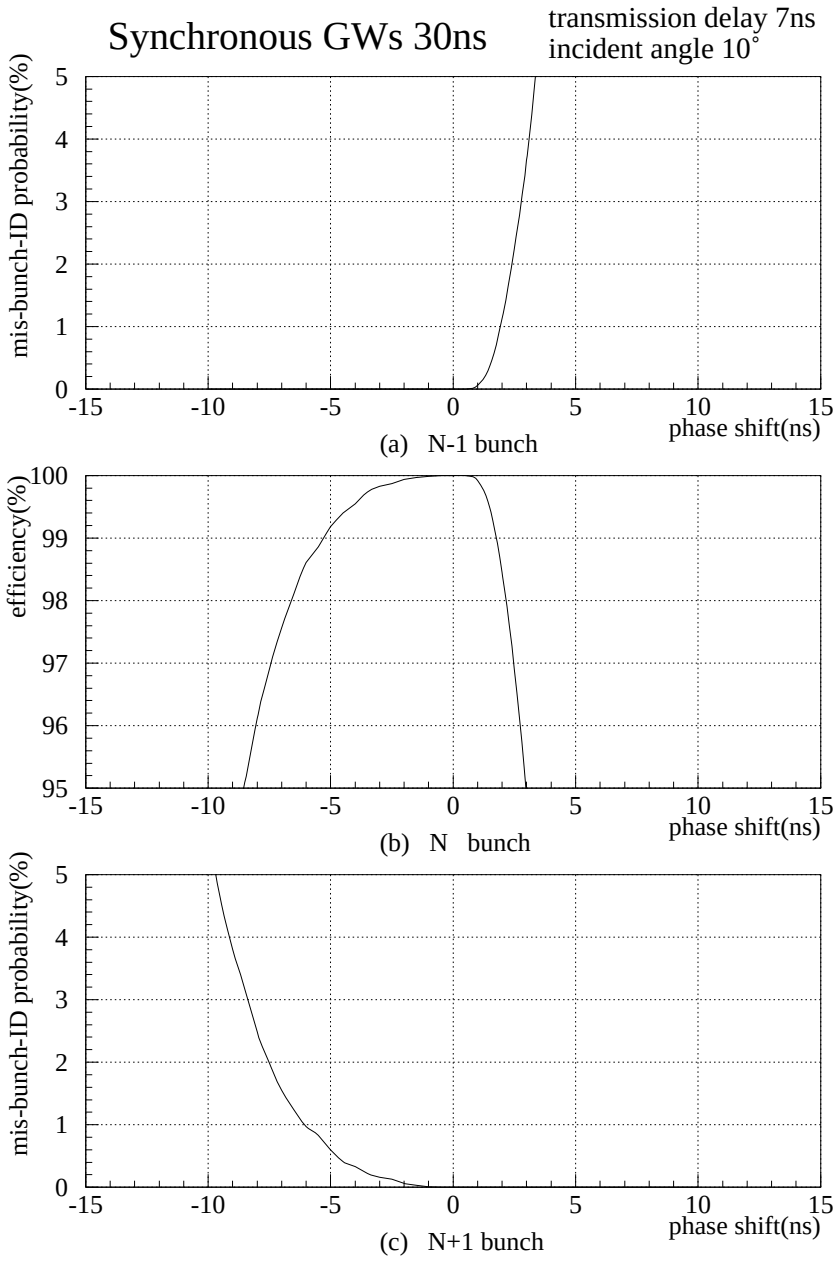

Figure 12: Phase-shift dependence for the synchronous scheme. Transmission delay of maximum 7 ns is taken into account as before. Gate width was fixed to 30 ns. Figure in the middle is the one for the correct (N)-th beam-crossing timing. Top figure is for the (N-1)-th beam crossing, bottom for the (N+1)-th beam crossing.

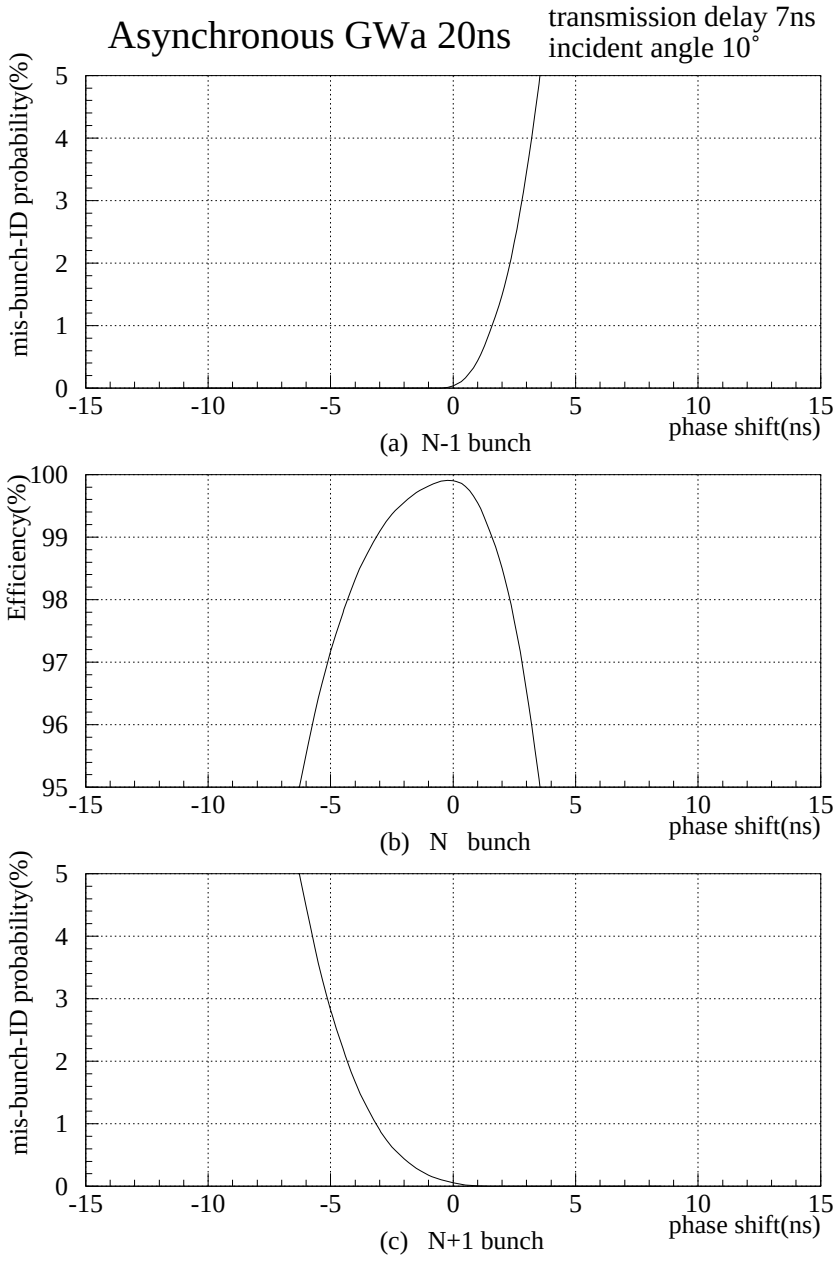

Figure 13: Phase-shift dependence for the asynchronous scheme. Transmission delay of maximum 7 ns is taken into account as before. Gate width was fixed to 20 ns. Figure in the middle is the one for the correct (N)-th beam-crossing timing. Top figure is for the (N-1)-th beam crossing, bottom for the (N+1)-th beam crossing.