Universität Bonn

Physikalisches Institut

Development of an FPGA-based FE-I3 pixel readout system and characterization of novel 3D and planar pixel detectors

Jens Janssen

USBpix is an FPGA-based test and readout system which was developed for the ATLAS FE-I3 pixel readout chip. The main part of this diploma thesis covers the code maintenance and further development of the USBpix test system. Particular attention will be given to the FPGA code which was redesigned during this work. In another step to become a fully integrated test system, USBpix was adapted to the requirements of the EUDET JRA1 beam telescope. In a second part, the USBpix test system was used for laboratory characterizations of pixel sensors bump bonded to FE-I3 pixel readout chips. All investigated sensor types, planar n-on-n and n-on-p, and 3D n-in-p, are candidates for future upgrades of the ATLAS pixel detector (IBL and HL-LHC). Detailed charge collection efficiency and noise studies were made on unirradiated as well as irradiated detectors.

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Contents

Chapter 1

Introduction

The ATLAS experiment is one out of four experiments at the Large Hadron Collider. The ATLAS detector is a multipurpose detector that covers a wide range of physics at high energy scale. That includes the search for the Higgs boson, extra dimensions and particles that does not belong to the Standard Model, such as supersymmetric particles and particles that make up dark matter.

The search for new physics relies on advanced technology and innovations in almost every aspect. More than a decade of research & development and construction involving thousands of people was needed to complete the work — for now? A new round of research & development has already begun. The aim is to improve the current detector. Two major upgrades are forthcoming in the next decade.

A major part of the ATLAS upgrade plan concerns the innermost detector, the pixel detector. The upgrade of the pixel detector is of great importance as it is closest to the interaction point. On the one hand, it delivers measurements with highest possible precision. On the other hand it has to be able to withstand the harsh environmental conditions close to the interaction point.

This work is produced within the IBL collaboration. The topic of this thesis is the development of a new test and readout system for the FE-I3 pixel readout chip. In a second step, the test system was used to study two novel sensor concepts, which are considered for future detector upgrades.

Chapter 2 gives a short introduction to the LHC and the ATLAS experiment. A closer view will be taken on the structure of the ATLAS detector.

Chapter 3 gives an introduction to the ATLAS the pixel detector. The ATLAS FE-I3 pixel readout chip is described in greater details and important functionality, which is used this thesis, is highlighted. A second part covers the principles of semiconductor detectors and gives a short introduction on sensor concepts.

Chapter 4 covers the development of the USBpix test system, a FPGA[1]-based readout system for the FE-I3 pixel readout chip. Software and hardware architecture of USBpix is described in greater details. The emphasis is on the development of Verilog[2] source code specifying the functionality implemented into the FPGA. The work on the FPGA source code is crucially responsible for the success of this work.

[1] FPGA stands for field-programmable gate array.
[2] Verilog is a hardware description language (HDL).

In Chapter 5, a detailed description of USBpix test setup and the equipment, which was used for the measurement, is given. This chapter can be read as a "manual labour" how to set up the USBpix test system.

In Chapter 6, the results of the laboratory measurements are presented and discussed.

Chapter 2

The LHC Experiment

2.1 The LHC Accelerator

The Large Hadron Collider (LHC, see figure 2.1) is the world's largest circular collider located at the international research facility CERN[1], the European Organization for Nuclear Research. The LHC was built into the tunnel of the former Large Electron-Positron Collider (LEP). The tunnel has a circumference of 27 km and is sited approximately 100 m beneath the surface and was extended to house new experiments at the LHC. The accelerator ring consists of large superconducting magnets and accelerator structures designed to boost proton pairs up to a center-of-mass energy of $\sqrt{s} = 14\,\text{TeV}$. Counter-rotating bunches of particles just mentioned are brought to collision at four distinct interaction points distributed along the accelerator ring. The particle bunches are colliding up to $40,000,000$ times per second, which corresponds to the bunch crossing frequency of 40 MHz. Four large detectors (ALICE, ATLAS, CMS and LHCb) are built around these collision points.

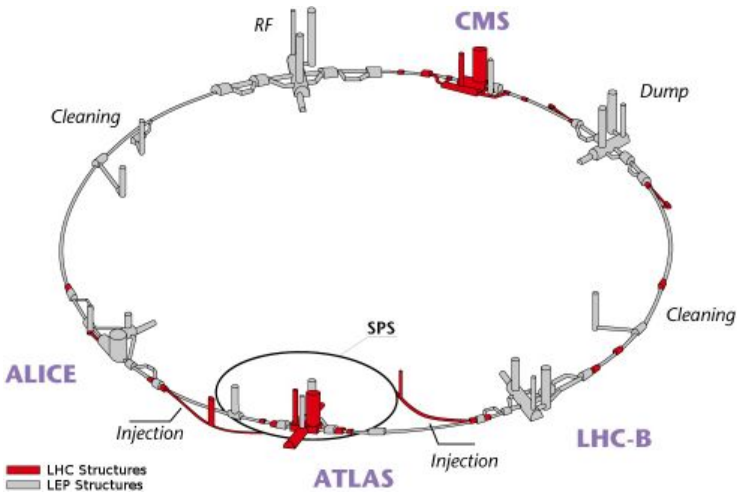


Figure 2.1: The Large Hadron Collider and its underground structures [1].

[1]European Organization for Nuclear Research CERN, CH-1211, Genève 23, Switzerland.

2.2 The ATLAS Detector

The ATLAS detector [2] (see figure 2.2) is one out of four detectors along the LHC accelerator ring, and is one out of two multipurpose collider detectors that covers a wide range of physics. It was designed to investigate proton-proton and ion-ion interactions at TeV energy scale. The detector is situated inside a cavern 80 m underground and has a diameter of 25 m and a length of 44 m. The particle collisions take place at the center of the detector. Due to the forward-backward symmetry of two colliding beams, the detector has a cylindrical shape along the beam axis.

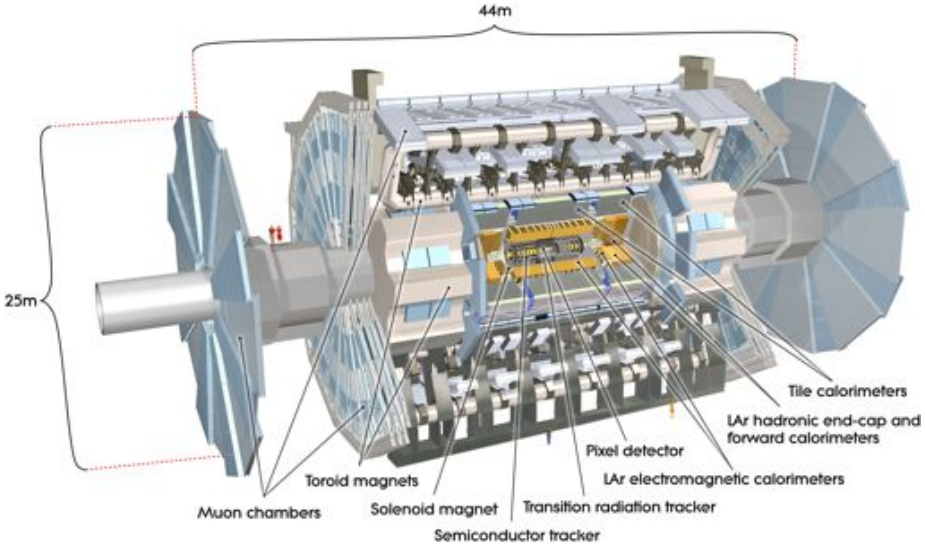


Figure 2.2: Cut-away view of the ATLAS detector. The LHC accelerator ring is extended in either horizontal direction.

The following points are crucial to meet the experimental challenges: a precise energy measurement, a precise momentum measurement, a possibility for particle identification and a hermetic design that covers a wide pseudorapidity[2] range to allow high particle detection efficiency. This is achieved by six different detector subsystems that identify particles and measure either their momentum or energy. To make the determination of the momentum possible, a solenoid, a barrel toroid and two end-cap toroids produce a magnetic field to bend the trajectory of charged particles. The measurement of the momentum is accompanied by precise track reconstruction.

A multi-stage trigger system reduces the event data recording rate to a level that does not exceed the limits of the data storage infrastructure. A proton-proton interaction rate of 1 GHz is expected at the design luminosity of $1\times10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. First, a fast trigger system that uses a small subset of available detector information (from calorimeter and muon detector) decides on whether or not to continue processing an event. The so-called Level-1 trigger system

[2]Pseudorapidity η is a coordinate to describe the angle θ of a particle trajectory with respect to the beam axis: $\eta = -\ln(\tan\frac{\theta}{2})$. The pseudorapidity is independent of Lorentz boost along the beam axis.

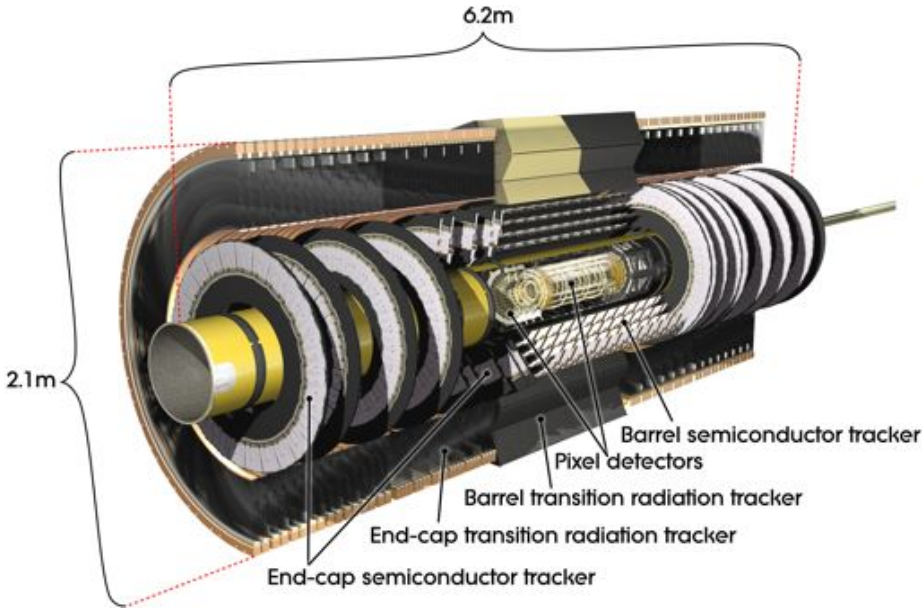


Figure 2.3: Cut-away view of the inner detector. The inner detector is composed of the following sub-detectors in successive order: the pixel detector close to the beam pipe, the silicon microstrip detector (SCT) and transition radiation detector (TRT). The inner detector is enclosed by a solenoid (not shown in the figure).

reduces the event data rate to approximately 100 kHz. Finally, two higher level triggers, the Level-2 trigger and the event filter, further reduce the data taking rate to approximately 200 Hz.

2.2.1 The Inner Detector

Figure 2.3 gives an overview about the structure of the inner detector. The multi-layered structure comprises, from the inside to the outside, the following three successive sub-detectors: the pixel detector close to the beryllium beam pipe, the silicon microstrip detector and the transition radiation detector. The inner detector is enclosed by a solenoid, which generates an axial magnetic field of approximately 2 T, to bend the trajectories of charged collision products and thus enable the measurement of their momentum.

The main purpose of the inner detector is the precise determination of the momentum of charged particles. It was also built to provide a hermetic pattern recognition and precise primary and secondary vertex measurements within a pseudorapidity range of $|\eta| = 2.5$ ($\theta = 9.4°$) and particle identification within $|\eta| = 2.0$ ($\theta = 15.4°$).

A particle has to interact with the detector material to determine its trajectory. This happens at discrete points within the detector at different distances from the place of origin e. g. the primary vertex of a collision inside the beam pipe. The pixels detector is placed closest to beam pipe. There, it can deliver the highest single point resolution (and thus very good pattern recognition) within

all sub-detectors. Such a high single point resolution is necessary to compete with the high particle occupancy due to the enormous particle flux close to the interaction point. To maintain the pixel detector operable at high radiation dose it must be kept at low temperature (approximately $-5°C$ to $-10°C$). The innermost layer (or b-layer[3]) has an expected lifetime of 3 years at LHC design luminosity. Beside the b-layer two other pixel layers and three end-cap disks on either side of the cylinder encloses the collision point. They are expected to withstand the particle flux over the operational lifetime of the experiment. More details on the pixel detector will be given in chapter 3.

A second sub-detector is built around pixel detector: the silicon microstrip detector (SCT). Its purpose is the same as that of the pixel detector: measurement of the momentum and pattern recognition. The SCT consists of four barrel layers and nine end-cap disks on either side. Each layer and disc is equipped with back-to-back sensors that have a stereo angle of 40 mrad to obtain two-dimensional spatial resolution. The strip pitch is 80 µm for the barrel sensors and for the disks between 57 µm and 90 µm due to the geometry. This results in an intrinsic resolution of 17 µm in R-ϕ-direction and 580 µm in z-direction (barrel) or R-direction (disks). To withstand the harsh environment the SCT is also kept at the same temperature as the pixel detector.

At larger radii, the transition radiation tracker (TRT) provides tracking information of particles that traverse many layers of close-packed drift straw tube elements of 4 mm in diameter. The straws (cathode) are filled with non-flammable gas mixture of 70% Xe, 27% CO_2 and 3% O_2. Each straw is equipped with an anode wire (the sense wire) that is placed in the center. Each tube provides a drift time measurement, giving a spatial resolution of 170 µm. Two independent thresholds are applied to every readout channel to discriminate between tracking hits, which pass the lower threshold, and transition radiation hits, which pass the higher one. The barrel is built up from axially oriented straws (approximately $50,000$) whereas both end-cap wheels contain radially oriented straws (approximately $320,000$). The entire sub-detector is designed to operate at room temperature and is surrounded by CO_2 to avoid pollution of the straws. With an average of 36 hits per crossing particle, it enhances the pattern recognition, improves the momentum resolution and provides electron/positron identification.

2.2.2 The Calorimeter System

An overview of the calorimeter system is given in figure 2.4. The calorimeter system can be classified into two sub-detectors: the inner electromagnetic calorimeter and the outer hadronic calorimeter. The electromagnetic calorimeter measures the energy of particles that primarily loses energy by electromagnetic interaction (e. g. electrons, photons) whereas the hadronic colorimeter measures the energy of the remaining particles, mainly those that are underlying strong interaction (i. e. hadrons). But in both cases the principle is the same: an incident particle of sufficient energy interacts with the absorber (or passive) material producing a particle shower. The constituents of the shower interact with the sensing (or active) material that is used for detecting the particles.

[3]The name can be derived from the fact that the innermost layer is designed to reconstruct the vertices of hadrons containing b-quarks and c-quarks (b-tagging).

The electromagnetic calorimeter uses lead as absorber material and liquid argon (LAr) as sensing material. Particles of the shower liberate electrons from the argon atoms. Liquid argon act as a conductor and therefore the electrons can be collected by electrodes and are read out.

The electromagnetic calorimeter has a particular geometry: the accordion-shaped (or folded) absorbers and electrodes allow having several active layers in depth. This is beneficial for the energy resolution which is in the order of $\sigma(E)/E = 10\%/\sqrt{E}$ [3]. A spatial resolution is obtained by segmenting the first layer.

The hadronic calorimeter is divided into three parts: the tile and tile extended barrel calorimeter, the LAr hadronic end-cap calorimeter (HEC) and the LAr forward calorimeter (FCAL). The both latter are using liquid argon as sensing material. The end-cap calorimeter uses copper (Cu) as passive material whereas the FCAL uses both, copper and tungsten (W). The tile barrel is made of steel with scintillating tiles in between. The light signals are read out by photomultiplier tubes.

Pion measurements show that the energy resolution $\sigma(E)/E$ is of approximately $50\%/\sqrt{E}$ for the tile barrel calorimeter, $90\%/\sqrt{E}$ for the HEC and $70\%/\sqrt{E}$ for the FCAL [3].

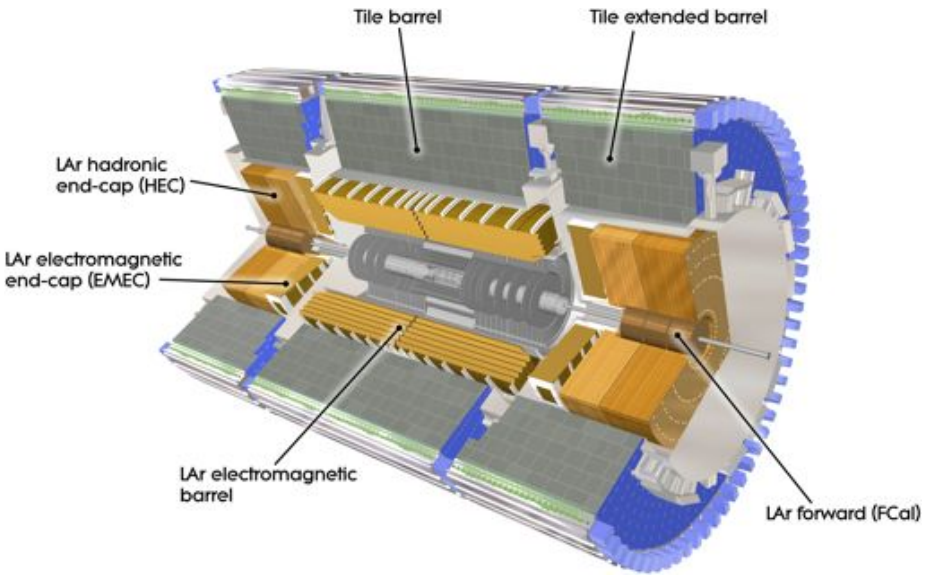


Figure 2.4: Cut-away view of the calorimeter system. The inner detector is indicated at the center and is enclosed by the electromagnetic calorimeter (liquid argon electromagnetic barrel and end-cap). The hadronic calorimeter (tile barrel, tile extended barrel, liquid argon hadronic end-cap and liquid-argon forward calorimeter) is built around the electromagnetic colorimeter. The part of liquid-argon forward calorimeter, which uses copper absorbers, is an electromagnetic calorimeter, while the part, which uses tungsten, is a hadronic calorimeter. A cryostat is required to keep the argon liquid.

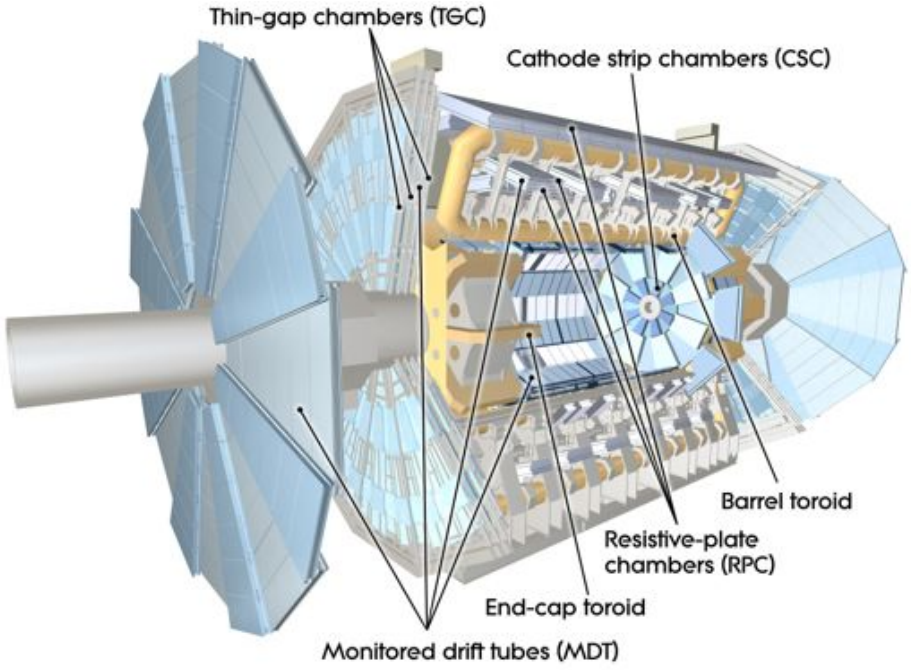


Figure 2.5: Cut-away view of the muon spectrometer. The nested structure of the tracking chambers minimizes the gaps in detector coverage.

2.2.3 The Muon Spectrometer

The muon spectrometer, as shown in figure 2.5, forms the outer part of the ATLAS detector and is the largest sub-detector in size. The tracking chambers of the muon sub-detector detect charged particles that exit the calorimeter. This are in most cases muons which live long enough to reach the outer regions of the detector. A barrel toroid and the two end-cap toroids generate a large-scale toroidal magnetic field of approximately 0.5 T and 1 T respectively. Thus makes it is possible to measure the momentum of charged particles in the pseudorapidity range of $|\eta| < 2.7$. The transverse momentum (p_T) resolution is of approximately 10% for 1 TeV particles.

In the barrel region, precision-tracking chambers are located on and between the eight coils of the barrel toroid. The nested chambers are arranged in three cylindrical layers at radii of approximately 5, 7.5 and 10 m. In the end-cap region, several muon chambers form large disks. The end-cap disks are located in front and behind each end-cap toroid at a distance of 7.4, 10.8, 14 and 21.5 m from the collision point.

The muon spectrometer is essential for the search of new physics. It is designed to deliver a fast trigger on particles in the pseudorapidity range of $|\eta| < 2.4$. The trigger occurs if a certain transverse momentum threshold is exceeded.

Chapter 3

Silicon Pixel Detectors

3.1 Introduction

This chapter will give an introduction on the ATLAS pixel vertex detector and the FE-I3 pixel readout chip (sections 3.2 and 3.3, respectively). The purpose of a vertex detector is to reconstruct the primary and secondary vertices of hadrons containing b- and c-quarks. The vertices are reconstructed by extrapolating the hit information measured by several detector layers around the interaction point. The high single point resolution and tracking efficiency of a pixel detector are required to obtain better tagging efficiency of the jet flavor. Also, in order to cope with the harsh environment close to the collision point, a pixel detector has an advantage of low per-pixel hit occupancy and per-pixel leakage current and thus noise.

In sum, the following criteria must be met by a modern pixel vertex detector:

- The innermost vertex layer should be as close to the collision point as possible to increase the accuracy of the vertex and impact parameter reconstruction.
- The detector and its components should be based on a radiation-hardened design.
- The material budget (in radiation length) of the detector and its supporting structures should be as low as possible to reduce the effect of multiple scattering. This is particularly important for the innermost detector layer.
- The pixel detector should have a high spatial resolution in order to provide a good hit resolution. Low noise and low hit occupancy are also important qualities for pattern recognition and for finding primary/secondary vertices [4] in a high multiplicity environment (e. g. nearby tracks in a jet).
- Hermetic coverage over a wide pseudorapidity range.

In a second part (section 3.4) and in a more general approach, the effect of radiation on silicon will be discussed. In section 3.4.1, the interaction of ionizing particles with the sensor material will be explained and thus the generation of charge that is detected as electrical signal. Section 3.4.2 will highlight another

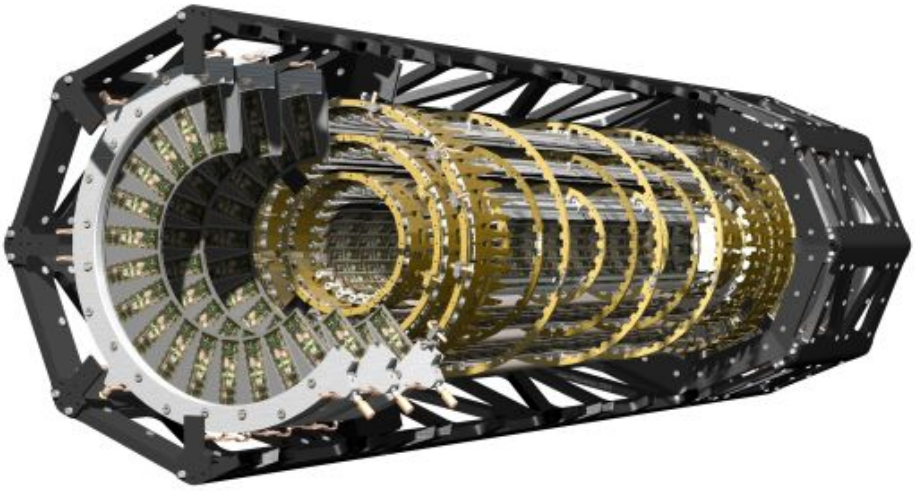


Figure 3.1: Cut-away view of the ATLAS pixel vertex detector. The mechanical support structure is built out of carbon composites which have a high stiffness, low mass and near-zero coefficient of thermal expansion. The global support frame (truss-like structure) holds three barrel layers and three end-cap disks on each side. The pixel modules (see figure 3.3) are mounted on local support structures (staves and sectors) with embedded cooling. The barrel layers and the end-cap disks are composed of several staves and sectors respectively.

effect of radiation on silicon: the damage to the silicon crystal lattice and its consequences will be discussed. In the last section (3.4.3), different sensor concepts will be presented and their advantages and disadvantages will be explored.

3.2 The ATLAS Pixel Detector

The ATLAS pixel detector [5] (see figure 3.1) is the smallest sub-detector in size (length of 1.4 m, with a radius of 0.2 m) but has the vast majority of readout channels. More than 80 million readout channels are distributed over a sensitive area of about 1.7 m^2. The pixel detector consists of three cylindrical barrel layers at a radius of 5, 9 and 12 cm and three end-cap disks on each side at a distance of 50, 58 and 65 cm from the interaction point. Such a hermetic design allows to have at least three pixel hits in the pseudorapidity range of $|\eta| < 2.5$. The entire sub-detector is immersed in a solenoidal magnetic field of approximately 2 T to enable momentum measurement of charged particles.

The smallest unit of the pixel detector is the hybrid[1] pixel module (see figure 3.3). It consists of a flex-hybrid holding the module readout electronics and a bare module. The bare module is made of a single sensor bump bonded to 16 FE-I3 chips (2 columns of 8 chips). The entire pixel module has an active area of approximately 6 cm $\times$ 2 cm containing 46080 readout channels. To allow a contiguous sensitive area between the FE-I3 readout chip boundaries, some of the readout channels are connected to two sensor pixel cells and/or to sensor

[1] Sensor and readout chip are separate entities are attached to each other.

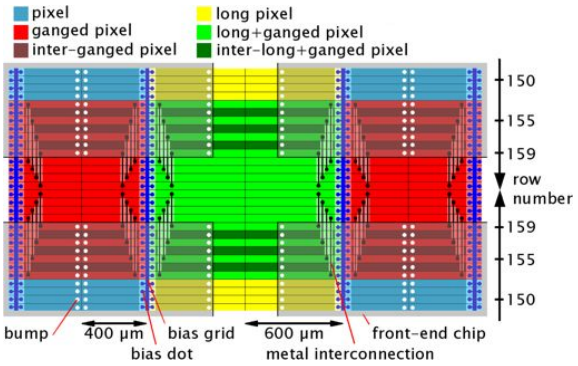


Figure 3.2: Layout and interconnection of FE-I3 pixel types in the interchip region. The FE-I3 pixel readout chip is indicated by light grey shading, whereas all four sensors meet in the middle. Normal pixels (red and blue): $50 \times 400\,\mu\text{m}^2$. Long pixels (green and yellow): $50 \times 600\,\mu\text{m}^2$. [7]

pixel cells of slightly larger dimension (see figure 3.2). In total, this leads to 47232 pixel cells on the sensor. The sensor is connected to the FE-I3 chips using the flip chip technology to minimize the signal path length between sensor pixel and readout electronics. Two different bump bond techniques are used to attach the sensor: electroplated-PbSn and evaporative-indium bumping [6].

The nominal pixel size is $50\,\mu\text{m}$ in ϕ-direction and $400\,\mu\text{m}$ in z-direction (barrel) or R-direction (disk). Under the assumption that only one pixel per particle track fires and binary readout, the spatial resolution is given by

$$\sigma_{\text{position}} = \frac{p}{\sqrt{12}}\,, \tag{3.1}$$

where p is the pixel pitch [8]. The alignment of the pixel cells leads to a resolution of $14\,\mu\text{m}$ in R-ϕ-direction and $115\,\mu\text{m}$ in z-direction or R-direction. However it is possible that the signal charge is shared between pixel cells. A group of pixels triggered by a single incident particle further improves the resolution. Having a readout that delivers the collected charge, the spatial resolution can be further improved by using a charge weighted clustering algorithm. The charge sharing and thus also the cluster size is affected by several parameters [8, 6]: the average cluster size is determined by the position and the incident angle of a particle track with respect to the sensor surface (the latter can be adjusted by tilting the modules), by intrinsic sensor properties (e. g. inter-pixel capacitance and pixel capacitance to the backplane), by operational parameters (e. g. reverse bias voltage and radiation damage) and by parameters related to electronic readout (e. g. threshold, crosstalk, charge resolution). Also the presence of the solenoidal magnetic field has an impact on charge sharing and thus cluster size. This is due to the fact that the signal charge inside the sensor is deflected by the Lorentz angle. The results of resolution studies are summarized in [6].

The hybrid pixel modules are mounted on so-called local support structures (glued on the surface with the FE-I3 side). The local support structures, which also carry Al-tubes to provide cooling (evaporative C_3F_8-cooling), are made of thermally conductive carbon composites. The cooling is needed to reduce the leakage current and therefore noise and to control beneficial/reverse annealing

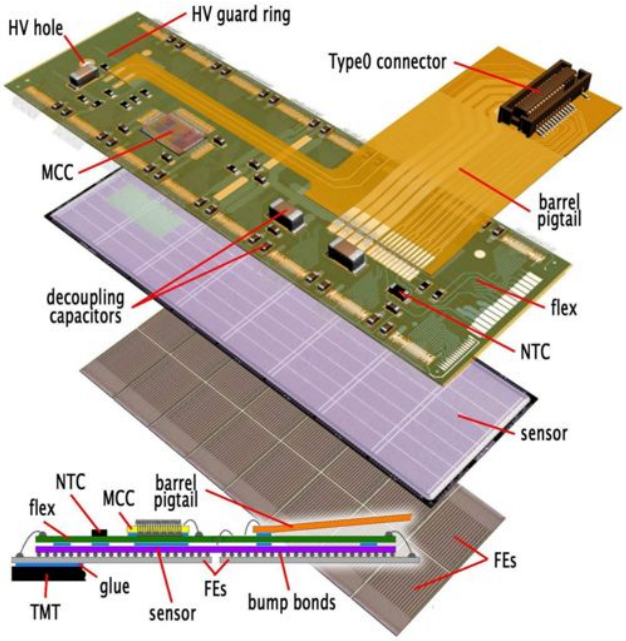


Figure 3.3: The ATLAS hybrid pixel module. The module readout electronics is mounted on a polyimide printed circuit board (flex-hybrid). The flex-hybrid is attached with an adhesive to the bare module (sensor bump bonded to 16 FE-I3 chips). The flex-hybrid also provides high-voltage and low-voltage to the attached components. The sensor is wire bonded through a hole in the flex-hybrid exposing the sensor backplane (p-side). Wire bonds are also used to electrically interconnect the FE-I3 readout chip to the flex-hybrid.

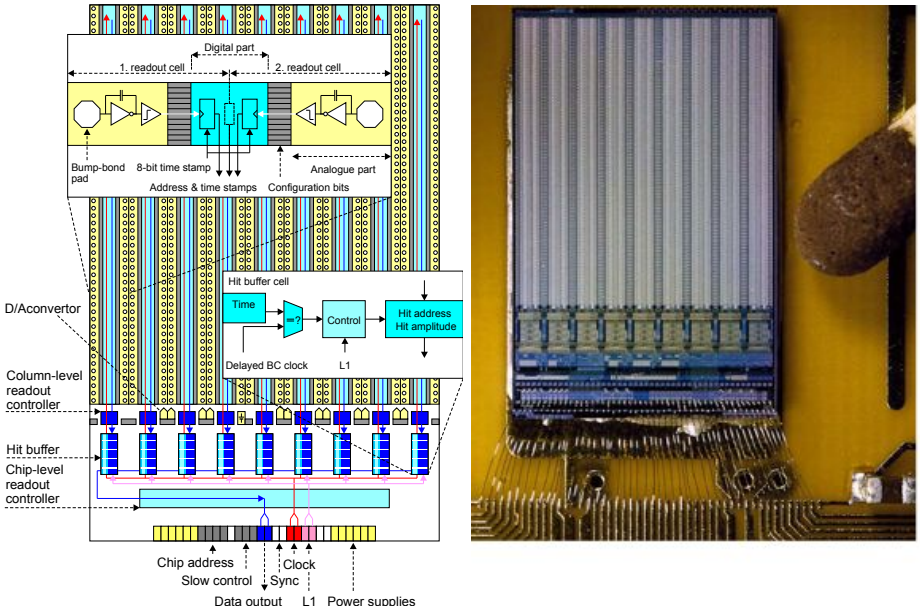
of irradiated sensor material (see section 3.4.2). The use of lightweight materials is crucial to reduce multiple scattering. The contribution of the pixel detector to the total inner detector material budged is of the order of $10\%\, X_0$ (radiation length) and $0.05\%\, \lambda$ (interaction length) at $\eta = 0$ [6].

There are two types of local support structures: staves and sectors. A stave holds 13 pixel modules while a sector holds eight pixel modules. Each barrel layer consists of different numbers of staves (22 staves for the b-layer, 38 for the second and 52 for the third layer) and each end-cap disc is made of eight sectors. This leads to a total number of 1744 pixel modules for the entire pixel detector.

3.3 FE-I3 Pixel Readout Chip

The ATLAS FE-I3 pixel readout chip is implemented in a 0.25 µm CMOS fabrication process. The die has a size of 5.4 mm × 11 mm. 3.5 million transistors are fabricated on silicon using radiation tolerant design rules[2] to withstand the

[2]On transistor level: the NMOS transistors are separated by p^+ guard rings. Also a deep sub-micron technology is beneficial for radiation hardening. Due to the small MOS gate oxide thickness the upcharge is reduced significantly. On design level: single event upset (SEU) tolerant redundant structures/blocks/registers and parity checking. For more information see



(a) (b)

Figure 3.4: On top view of the FE-I3 readout chip. (a) Overview of the most important logic blocks of the FE-I3. (b) Size of the readout chip compared to a match. Clearly visible are the double column structure and the chip periphery at the bottom containing the readout logic and buffers.

required radiation tolerance up to a total dose of 50 Mrad. The chip contains 2880 readout channels arranged in matrix of 160 rows × 18 columns. The size of each readout cell is 50 µm × 400 µm (row-to-row pitch × column-to-column pitch). The power consumption should be less than 40 µW per readout channel to fulfill the design requirements [11]. However, the chip typically draws 40 mA of current from a 2 V (digital supply voltage) supply and 80 mA of current from a 1.6 V (analog supply voltage) supply (see also [12]), which is 30 µW above design requirements per readout channel.

Figure 3.4 shows the most important logic blocks of the FE-I3. Each pixel consists of an analog and a digital block. The task of the analog pixel block is to amplify and shape the input signal charge which is generated by particles hitting the sensor. The digital block comprises all digital elements beginning from the digital pixel block and ending at the readout controller in the chip periphery. The digital pixel block communicates with the logic located in the chip periphery and transmits the hit data. The 18 pixel columns are aligned to 9 double columns. The double column comprises 320 readout channels, each sharing the same column bus, column arbitration unit (CAU, also referred to as column readout controller) and end-of-column (EoC) buffer. Beside the double column readout logic (CAU and EoC buffer), also the chip level readout controller (ROC) is located in the chip periphery. The ROC collects the hit data and sends them out serially. The following sections will give a more detailed description about the analog and digital design.

3.3.1 Chip Configuration

The FE-I3 readout chip has a 14-bit local configuration register which is located in each of the 2880 pixel readout blocks. Also 231-bit long global configuration register exists. Parts of the global configuration register are located underneath the pixel matrix and in the chip periphery in vicinity of the corresponding logic blocks. All configuration bits are stored in single event upset (SEU) tolerant latches/RAM cells.

The latches can be accessed by using two long shift register. One 231-bit long shit register for the global register and one 2880-bit long shift register for accessing the pixel register bits.

An additional 29-bit long command register controls the shifting of the bit pattern and the latching of the bits into the corresponding RAM cells. The command register determines into which shift register the received bit pattern is shifted. It also determines into which local register the pixel shift register is latched.

Three input signals are needed: command clock (CCK), data input (DI) and a load signal (LD). The clock is sent in parallel with data: DI must be synchronous to the CCK and the CCK is enabled only during shifting the data.

The procedure is as follows: first, the 29-bit command has to be written to the command register to get access the intended configuration register (clock command). When LD is low the command data can be shifted into the command register (CCK enabled for 29 clock cycles). To latch the command data, LD must be asserted. Immediately, the command becomes active. Second, the configuration data is shifted to the shift register. The LD stays asserted and

[8, 9, 10, 11].

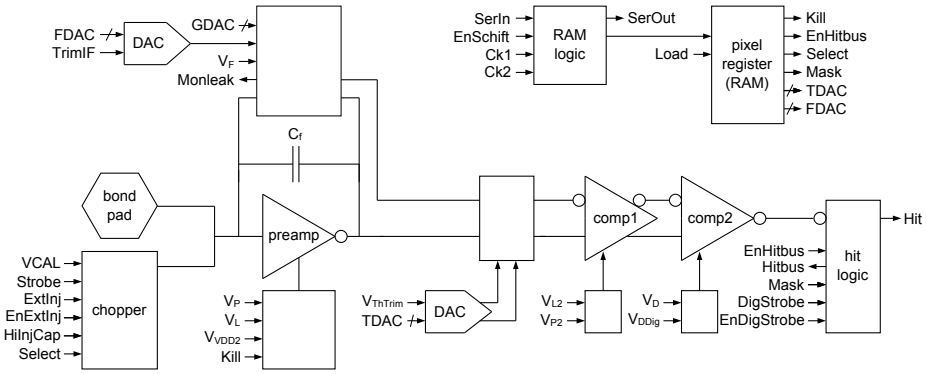


Figure 3.5: The analog pixel block and the associated pixel register of a single readout channel [11]. For a detailed view of the chopper see figure 5.2 and for the hit logic see figure 3.7.

the CCK is enabled for 231 or 2880 clock cycles corresponding to length of the shift register. Now, LD must be de-asserted. Third, to latch the data from the shift register into the RAM cells another command is needed (write command).

A detailed description is given in [12, 11].

3.3.2 Analog Pixel Block

The analog pixel block (figure 3.5) consists of various stages, beginning with the bond pad, which is connected to the sensor, and ending with the hit signal output of the hit logic. The analog readout electronic collects the charge that is generated by radiation hitting the sensor. The so-called signal charge is induced by electrons and holes drifting towards the sensor electrodes. The signal charge flows through the bond pad into the charge sensitive amplifier[3] (CSA, also referred to as preamplifier). The current pulse, which arises at the CSA input is integrated on the feedback capacitor C_f and forms a positive voltage step at the CSA output. To decrease the output voltage and to return again to base level, the CSA is realized with a feedback circuit (continuous reset), which consists of an adjustable resistor (implemented by using only PMOS transistors) in parallel to the capacitor C_f . In addition, a leakage current compensation circuit prevents the leakage current of the sensor to be integrated over time.

To sum up, the output of the CSA is a unipolar triangular signal whose time over a certain threshold is proportional to the collected charge (see figure 3.6). The rise time is limited by the stringent constraints on the power consumption of the FE-I3 readout electronics and is of approximately 15 ns [6]. In contrary, the fall time of the preamplifier signal is primarily determined by the feedback current and can be adjusted. The feedback current can be tuned locally by the FDAC pixel register (fine tuning) whose step size can be adjusted by the TrimIF global register. The feedback current of every readout channel is pre-biased and is adjusted by the IFDAC global register (coarse tuning).

The output signal of the CSA is DC-coupled to a comparator. The comparator consists of two amplifiers arranged in series: the first stage is a fully

[3]The amplifier uses a single-ended folded-cascode topology with PMOS input transistor, which is a common choice for low-voltage and high-gain amplifiers [13].

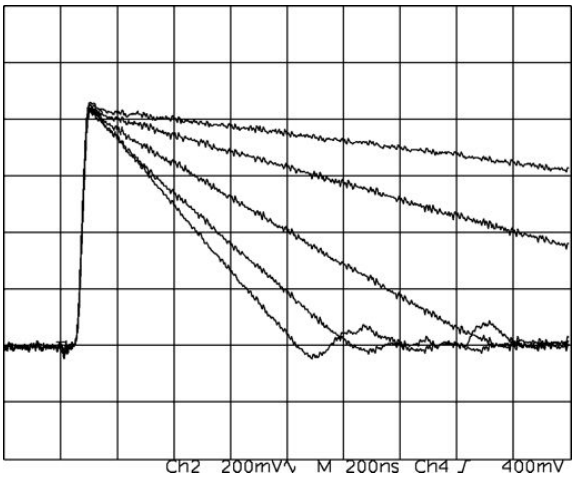


Figure 3.6: Output of the charge sensitive amplifier (CSA). The unipolar triangular signal, whose time over a certain threshold is proportional to the collected charge, is DC-coupled to the comparator.

differential low-gain amplifier and the second stage is a classical two-stage differential amplifier [13]. The comparator compares the output signal of the CSA to a well-defined threshold potential. The reason for this is as follows: the base line potential of the CSA output depends on VDD_{ref}[4]. VDD_{ref} is also used to generate the threshold potential (often referred to as V_{replica}). Then, the threshold is defined as the difference between the threshold potential and base line potential. The threshold potential is generated locally to avoid variations in threshold across the chip. Again, the threshold potential can be adjusted locally by setting the TDAC pixel register (fine tuning) and globally by setting the GDAC global register (coarse tuning). The step size of the TDAC is adjusted by the TrimTh global register.

In the moment when the output signal of the CSA exceeds the threshold potential, the comparator asserts the binary hit signal. The hit signal is de-asserted when output signal falls below the threshold. Consequently, the length of the hit signal depends on the feedback current and threshold and is proportional to the collected charge. The time the signal is asserted is called Time-over-Threshold (ToT).

The hit signal is received to the hit logic (see figure 3.7). The hit signal is sent to the hitbus if the WriteHitbus pixel register is set. The hitbus can be asserted by any of the 2880 readout channels (OR'ed). The hitbus signal can be used internally for self-triggering or can be read out from a pad on the FE-I3 readout chip. A second output (indicated as "Hit") is connected to the digital pixel block. The transmission of the hit signal to the digital block can be disabled by setting the WriteMask pixel register bit to 1.

In addition, each readout channel has a separate charge injection mechanism (indicated as "chopper" in figure 3.5), which is used to adjust the feedback current of the CSA and the threshold of the comparator. The charge injection circuit is topic of section 5.4.

[4] As well as on the bias current of the amplifier.

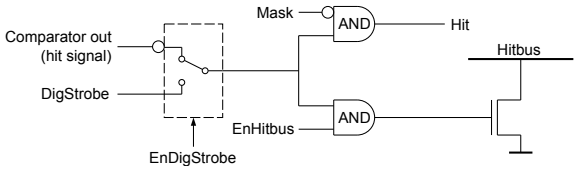


Figure 3.7: The hit logic is part of the analog pixel block [11]. The hit signal can be sent through the global hitbus (OR'ed with all other readout channels) and is available on an output pad of the FE-I3. The hitbus signal can be used for internal self-triggering (see section 4.6). A specific circuit is implemented to test the digital functionality of the FE-I3 (DigStrobe).

3.3.3 Digital Pixel Block

The digital pixel block generates the hit information and preserves the data until transmitted to the CAU in the chip periphery.

A block diagram of the digital pixel block is shown in figure 3.8. The binary hit signal is received by a circuit denoted as differentiator. The differentiator generates two short signals at the leading edge (LE) and trailing edge (TE) of the hit signal. Each signal causes that the current 8-bit Gray-coded time stamp is saved to either the LE RAM or TE RAM, respectively. The time stamp (TSI) is received via the timing bus and is increased by one every 25 ns according to the bunch crossing frequency of 40 MHz. The signal in coincidence with the TE also asserts a read request that is sent to the CAU. Then the CAU starts the readout of the hit information. The hit information (or data) comprises the LE and TE time stamps and the row address[5]. If more than one pixel saw a hit, the CAU starts a readout sequence determined by priority logic. As long as the hit information has not been read out, the digital pixel block is not able to process any other hit signal. A freeze signal prevents sending out of hit data of a pixel cell with higher priority that just received a hit while a pixel cell with lower priority communicates with the CAU. After finishing the readout of a pixel cell (read signal is de-asserted), the readout of a pixel cell with highest priority, which contains hit data, begins.

3.3.4 Chip Periphery

The chip periphery contains the CAU, the ROC and a EOC buffer for each column pair. The following paragraphs will only give a brief description of the functionality implemented in the periphery. An introduction into the functionality is needed to understand how the data, which is sent out to the readout system, is generated. More detailed information can be found in [11, 13].

The task of the CAU is to receive the Gray-coded hit information. In second step, the Gray-coded hit information is converted to the binary format and the ToT information is calculated by subtracting the TE time stamp from the LE time stamp. The ToT information is associated to the LE time stamp.

Hits that are affected by a timewalk effect can be discarded or doubled by the CAU. More details can be found in section 5.9.2.

[5]The column address is determined by the CAU.

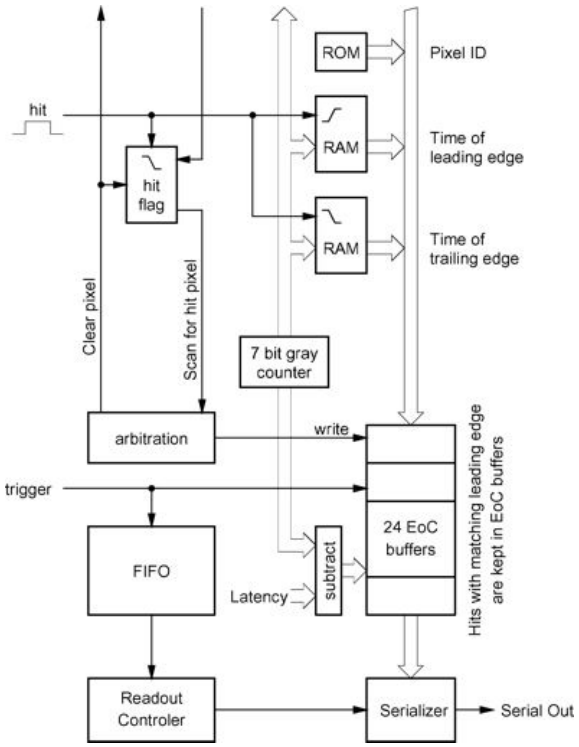


Figure 3.8: The digital block of the FE-I3.

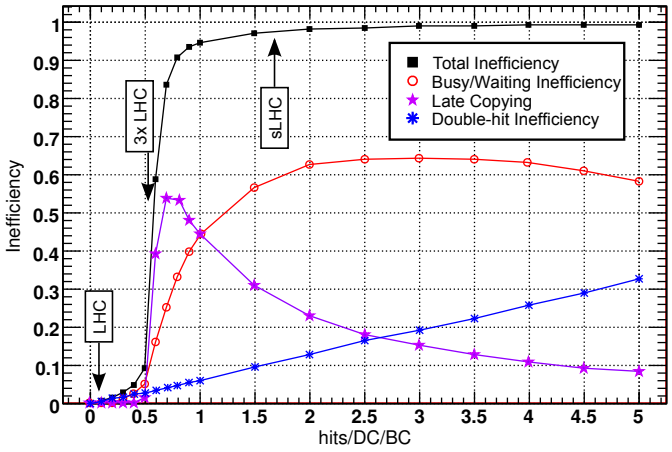


Figure 3.9: Inefficiencies in the current b-layer as function of hit rate per double column (DC) and bunch crossing (BC, equivalent to 25 ns) [14]. Note that the hit rate is even greater at smaller radius as foreseen for the ATLAS detector upgrades, which translates in even more challenging requirements for the IBL.

The LE time stamp and the associated ToT information generated by the CAU are stored in the EOC buffer. The EOC comprises 64 memory block and is associated to a single double column. The LE time stamp stored in each memory block is then compared with a bunch crossing clock. The bunch crossing clock (TSC) is a time stamp, which is offset from the original time stamp (TSI) by an adjustable delay (global register [1:8]). A read out of a buffer cell is initiated by the ROC if the bunch crossing clock coincides with the LE time stamp and if the external initiated LV1 trigger arrives in-time. Otherwise, if no LV1 trigger is asserted, the buffer cell is marked empty and the containing data is lost. The ROC is able to handle 16 consecutive LV1 trigger.

The ROC receives the data stored in a buffer cell, converts it and sends it out serially (hit word). If there is no (more) hit data that correspond to a LV1 trigger, the ROC generates the end of event data and send it out serially (EoE word).

The hit word contains column, row and ToT information and the corresponding bunch crossing time of the LV1 trigger (BCID). The EoE word also contains the BCID, error bits and the LV1 identification number. The LV1 number is increased by one every LV1 trigger. Table 4.1 gives a brief summary of the hit and EoE word data format. More detailed information about the data output format is given in [12].

3.3.5 Future Detector Upgrade Plans

The innermost pixel layer, which is built around the beam pipe, has a minimum distance from the interaction point of $\sim 5\,\mathrm{cm}$. It has an expected lifetime of three years at design luminosity of $1 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and thus has to be functionally replaced before failure due to radiation damage. In addition, not only the pixel b-layer, but the entire pixel detector faces another problem that will be discussed in the next paragraphs: the pixel cells generate more data than

the digital readout of the chip can cope with.

The LHC is planned to be upgraded to higher luminosity. This happens in two steps: with a first upgrade estimated in 2016, it is planned to reach peak luminosity 2 to 3 times higher than the current design luminosity. In a second step, the luminosity will be increased to approximately 10 times the initial luminosity in a more ambitious upgrade. This upgrade is commonly referred to as HL-LHC[6] (or sLHC) and is currently scheduled for completion at the beginning of the next decade.

This higher luminosity leads to new problems that arise from the fact that the double column inefficiency of the ATLAS FE-I3 pixel readout chips increases drastically with the hit occupancy [14]. Figure 3.9 shows the progression of the inefficiency and points out why FE-I3 pixel readout chip cannot cope with higher luminosity as it is foreseen. The following points contribute to the inefficiency:

Double-hit inefficiency Two temporally close hits to a given pixel cannot be resolved. After a hit, the pixel is busy for a certain amount of time until the data transfer is finished. A second hit can also results in a pile-up of the first hit.

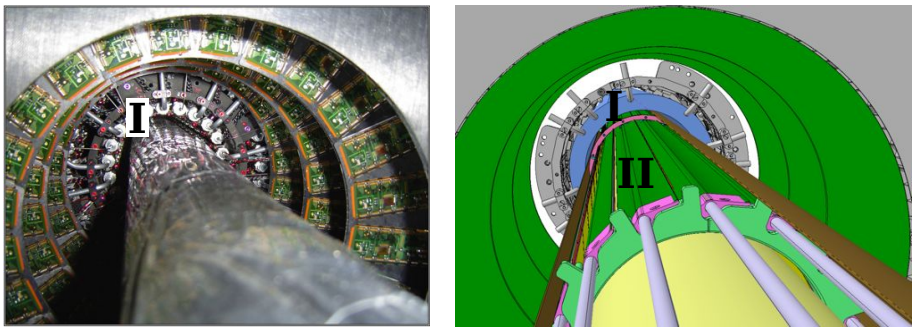
Busy/Waiting inefficiency At high luminosity the double column bus becomes saturated. This increases the time it takes for a pixel to start copying data to the double column buffer. While waiting for double column bus to become free, the pixel gets a second hit that cannot be stored.

Late copying inefficiency At high luminosity the double column bus becomes saturated. The increase in time it takes for a pixel to copy data to the double column buffer results in the loss of hit information. The hit information has not arrived at the double column buffer in time to be read out synchronous to the Level-1 trigger.

One possible solution is the reduction of the pixel size. A smaller pixel cell size can cope with a higher luminosity due to lower per-pixel occupancy and will also have a benefit on tracking resolution. The inefficiency related to the data transfer in the double-columns can be overcome by a new digital design of the readout chip. The effort of a new ATLAS readout chip (FE-I4A) has started in 2008 [15] and a full-sized prototype is currently under investigation.

During the first LHC upgrade phase it is planned to insert a new b-layer inside the current pixel detector together with a smaller radius beam pipe (without replacing the former b-layer). This project is referred to as insertable b-layer (IBL). The new b-layer is within a radius of 3 cm away from the interaction point (see figure 3.10). Great efforts must still be made, especially in order to deal with the high radiation dose and to keep the material budget as low as possible, e. g. new powering scheme, thin chips and new types of sensors. The latter is topic of this thesis. In contrast, the HL-LHC upgrade makes it necessary to replace the entire pixel detector.

[6] HL stands for high luminosity.



(a) (b)

Figure 3.10: a) The ATLAS pixel detector before the IBL upgrade. (I) denotes the current b-layer. b) The ATLAS pixel detector after insertion of the new b-layer which is based on the FE-I4 readout chip (II). The former b-layer stays inside the detector.

3.4 Semiconductor Pixel Sensors in HEP Experiments

Semiconductor detectors are widely used in high energy physics (HEP) experiments to detect ionizing radiation. Semiconductor detectors use a semiconductor sensor material to detect ionizing radiation (i.e. charged particles and photons). They are using a broad spectrum of different sensor materials, e.g. silicon (Si), gallium arsenide (GaAs) and Diamond[7], which have one thing in common: a band gap. Charged particles, which interact with the sensor material, generate free charge carriers. The energy needed to create electron-hole pairs varies with the sensitive material being used but is still low compared to the energy required for production electron-ion pairs in a gaseous detector (even for Diamond[8]). Hence, in semiconductor detectors the statistical fluctuations of the deposited energy are smaller and thus the spread of the signal pulse height. This leads to a better energy resolution compared to a gaseous detector. Also the time resolution is better for the following reasons: free charge carriers, especially electrons, have a high mobility and thus a high drift velocity for a given electric field strength: $v_d = \mu E$, where v_d denotes drift velocity, μ mobility, and E the magnitude of the electric field. Fast charge carriers travelling towards their readout electrode, decrease the rise time of the induced signal (Ramo theorem, see following section).

The simplest semiconductor detector imaginable is a single PIN diode. However, todays detectors consist of thousands of individual readout channels which are densely packed on a chip of a few cm^2 in size. Such detectors have a high tracking resolution compared to other technologies such as wire chambers. The disadvantages of semiconductor detectors are the high costs for large-volume tracker detectors and the requirement of sophisticated cooling technology to reduce leakage currents and thus noise. In addition, in semiconductor detectors,

[7]Normally considered as an insulator.

[8]Mean ionization energy [16]: 3.62 eV for silicon, 13.1 eV for diamond and 20...30 eV for a gaseous detector.

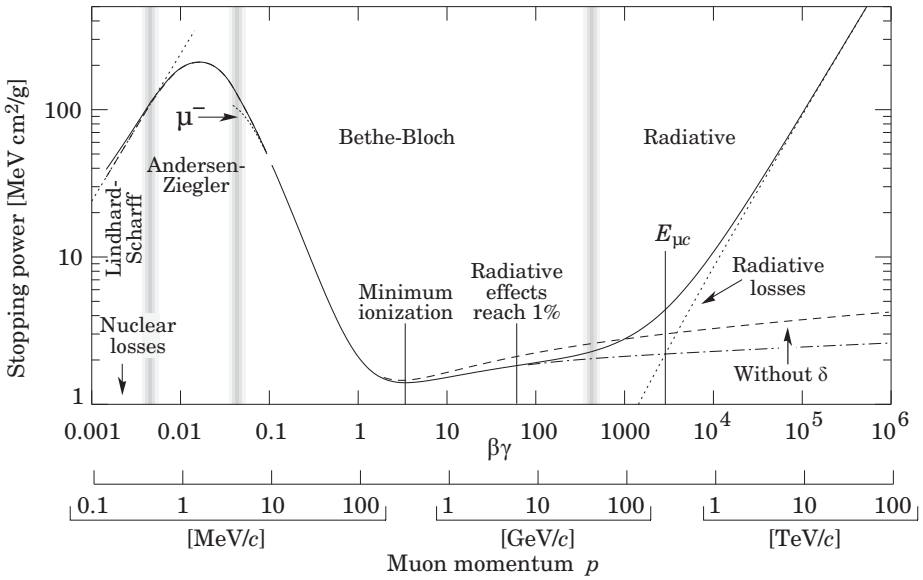


Figure 3.11: Stopping power $-\langle dE/dx \rangle$ for positive muons in copper as a function of momentum $p = M\beta\gamma c$ [19].

the sensor material suffers from radiation damage, which leads to a degradation of the signal-to-noise ratio (S/N).

The following sections will focus on silicon hybrid pixel detectors but most topics are also true for semiconductor detectors in general.

3.4.1 Energy Loss of Charged Particles and Signal Formation

Charged particles traversing matter lose energy along their path. In case of heavy charged particles, the energy is transferred to the absorbing material through many inelastic scattering processes (e. g. ionization, excitation etc.). The energy loss per length (often referred to as stopping power) at intermediate energy is described by the Bethe formula [17, 8]:

$$-\left\langle \frac{dE}{dx} \right\rangle = Kz^2 \frac{Z}{A} \frac{1}{\beta} \left[\frac{1}{2} \ln \frac{2m_e c^2 \beta^2 \gamma^2 T_{\max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2} \right], \qquad (3.2)$$

where $-\langle dE/dx \rangle$ is the stopping power (see figure 3.11). Particles at the minimum of formula 3.2 (corresponds to a value of 3 on the $\beta\gamma$ scale) are denoted as minimum ionizing particles (MIPs). But due to the flatness of the curve the notion applies to all particles with $\beta > 0.96$ ($\beta\gamma > 3$) [8].

It is important to mention that the result given by formula 3.2 is only a mean value which is independent of the thickness of the absorber. Formula 3.2 is not adequate for describing the energy loss for a single particle for the following reasons [17, 18]: for absorbers of moderate thickness statistical fluctuations have to take into account. There the number of collisions and the amount of energy transferred at each collision fluctuates.

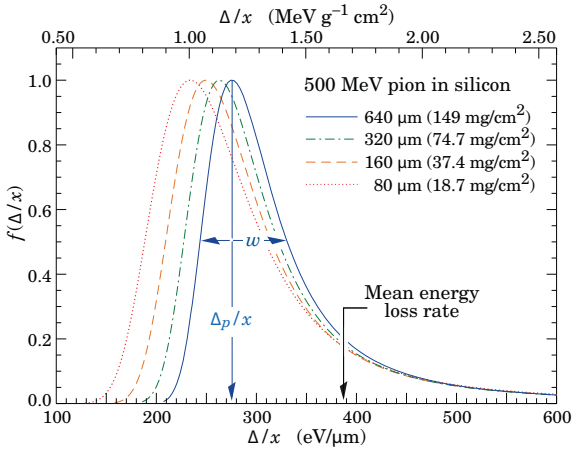


Figure 3.12: Landau distribution in silicon for 500 MeV pions, normalized to unity at the most probable value $\delta p/x$. The width w is the full width at half maximum (FWHM) [17].

The first energy loss probability distribution for a thin detector was carried out by Landau [20]. The skewed Landau distribution shows a high-energy tail (Landau tail, see figure 3.12). The reason for this tail is a rare occurrence of knock-on electrons (also δ rays or δ electrons) which are generated by large single-collision energy transfers. The knock-on electrons are emitted most likely at approximately 90° angle with respect to the incident particle path. The emitted electrons travel only short distances and deposit their energy into the absorber material. Due to this high energy tail, the most probable energy loss Δ_p is always lower than the average energy loss [8]. For thick absorbers the Landau becomes more Gaussian-shaped distribution but a tail still persists.

The energy loss of electrons (and positrons) is different to that of heavy charged particles. This is because of the kinematics of the electron and its collision partners are, in case of shell electrons, of the same identity. At low energies the electrons lose energy by ionization. At high energy, losses by bremsstrahlung are dominant. For that reason formula 3.2 cannot be applied to electrons. But for absorbers of moderate thickness, the Landau shape of the energy loss probability distribution remains valid. For an electron, the most probable energy loss Δ_p can be calculated by the following equation [21]:

$$\Delta_p\,[\mathrm{keV}] = d(0.1791 + 0.01782 \ln d)\,, \tag{3.3}$$

where d denotes the thickness of the absorber in µm.

The energy deposited in the absorber material generates electron-hole pairs. For silicon, the minimum energy required is 1.1 eV[9] (at 300 K) which corresponds to the band gap. The mean excitation energy to generate electron-hole pairs is larger than the band gap and is 3.62 eV[10] (at 300 K) for silicon, whereas the excess energy excites phonons. The most probable numbers of electron-hole pairs is given by dividing formula 3.3 by the mean excitation energy.

[9] By neglecting momentum conservation. A phonon is needed for excitation due to the fact that silicon has an indirect band gap.

[10] This is true if the energy of the incident particle is large with respect to the band gap.

The free charge carriers need to be detected by the readout electronics. The movement of the newly generated charge carriers induces a signal which can be detected by the readout electronics. Because of an electric field, which is applied to the detector by an external voltage supply, the electrons and holes start drifting in opposite directions. Without field, the electrons and holes would recombine after a short time without being recognized. The electronic properties and conductivity of a semiconductor are decidedly determined by the concentration of dopant atoms.

The equilibrium concentration of free charge carriers in a semiconductor can be calculated by using the Fermi-Dirac statistics. The result of the calculation is independent of the doping concentration and is known as mass-action law[8]:

$$np = n_i^2 \tag{3.4a}$$
$$= N_\mathrm{C} N_\mathrm{V} \mathrm{e}^{-E_g/kT} \tag{3.4b}$$

In an intrinsic (undoped or pure) semiconductor in equilibrium the free charge carriers are thermally generated. The number of free electrons is equal to the number of free holes and therefore the concentration n_i of free charge carriers can be calculated. The thermal excitation and recombination is supported by imperfections within the crystal lattice and by impurities. It is extremely difficult to reach purity so that the lifetime of the free charge carriers is long enough so that an intrinsic semiconductor can be used for detecting ionizing radiation.

By adding a small fraction of dopant atoms new energy states are added within the band gap. Donor states are close to the conduction band (e. g. 0.054 eV for arsenic atoms in silicon) and acceptor states are close to the valence band (e. g. 0.045 eV for boron atoms in silicon). At room temperature ($k_\mathrm{B}T \approx 0.025\,\mathrm{eV}$) most of the donor and acceptor states are ionized. Material with more donor atoms than acceptor atoms is called n-material and the majority charge carriers are electrons according to the mass-action law. In p-type material the majority charge carriers are holes.

If p-doped and n-doped material forms a junction, free charge carriers will diffuse according to the concentration gradient of free electron and holes. An electrical field is generated by the diffusion and counter-acts the diffusion. A fraction of the free charge carriers drift back towards their majority carries side. In equilibrium, the counter-acting voltage, which causes the drift, is called built-in voltage V_bi and is in the order of 0.5 V. By applying a voltage (reverse bias), which has the same direction as V_bi, the recombination region can be extended even more. Around the junction, electrons and holes recombine. The recombination region is free of charge carriers and has a high resistivity. This region is called depletion zone (or space charge region). The width W of the depletion zone is given by following equation [8]:

$$W = \sqrt{\frac{2\varepsilon_0 \varepsilon_\mathrm{Si}}{e} \left(\frac{1}{N_\mathrm{A}} + \frac{1}{N_D} \right) (V + V_\mathrm{bi})}\,. \tag{3.5}$$

By assuming a p-n junction of a highly doped and lowly doped material (e. g. for an unirradiated ATLAS sensor is $N_\mathrm{A} \gg N_\mathrm{D}$), and by neglecting the built-in voltage V_bi one can derive the following relationship:

$$W = \sqrt{\frac{2\varepsilon_0 \varepsilon_\mathrm{Si}}{e N_\mathrm{D}} V}\,. \tag{3.6}$$

In this case the depletion zone extends widely into the lowly doped region (in our example the n-type bulk). The voltage needed for full depletion is called depletion voltage V_{depl}. Ideally, the depletion zone is extended over the complete thickness of the sensor. But this is not always possible due to limitations on the height of the supply voltage or early breakdown, to name a few. The size of the depleted volume, and the geometry and strength of the electric field within the depletion zone are important parameters which determines the efficiency of the detector. To receive maximum signal charge, a fully depleted sensor is essential.

Another important aspect is the detector capacitance which contributes to the pre-amplifier input capacitance. The capacitance of the signal source should be low in order to reduce the noise of the detector and to achieve a better overall S/N ratio [22, 18]. In case of planar sensor, the capacitance is influenced by the size of the depleted region whose capacitance C can be approximated by following formula [8]:

$$C(V) = \begin{cases} A\frac{\varepsilon_0\varepsilon_{\text{Si}}}{W(V)} & V < V_{\text{depl}} \\ A\frac{\varepsilon_0\varepsilon_{\text{Si}}}{d} & V > V_{\text{depl}} \end{cases}, \tag{3.7}$$

where A is the size of the p-n junction and d the thickness of the sensor. Increasing the reverse bias voltage V leads to a lower sensor capacitance but increases in revers the leakage current. The statistical fluctuations of the leakage current can be understood as noise current source feeding into the amplifier input (shot noise) [22]. However, for a pixel detector, the pixel to pixel capacitance dominates by far [18].

If an ionizing particle generates free charge carriers within the depletion zone, the charge carriers starts drifting along the electric field gradient to the corresponding electrodes. The movement of the free charge carriers induce a current at the collecting electrodes and hence in the input of the readout amplifier. The instantaneous current in the amplifier can be calculated by using Ramo's Theorem [23]:

$$i = e\boldsymbol{E}_{\text{W}}\boldsymbol{\nu}\,, \tag{3.8}$$

where $\boldsymbol{v}$ denotes the drift velocity of the charge carriers and is equal to $\mu\boldsymbol{E}$. $\boldsymbol{E}_{\text{W}}$ is the weighting field, which is given by $-\nabla\phi_{\text{W}}$, where ϕ_{W} is the weighting potential. The weighting potential can be calculated by applying a unit potential ($= 1$) to the readout electrode and a zero potential to all the others. The injected charge is given by integrating over time:

$$Q = \int_{t_1}^{t_2} i(t)\mathrm{d}t\,. \tag{3.9}$$

In case of a pixel detector two conclusions can be drawn. They are denoted under small pixel effect [8]:

- Most of the signal charge is induced by the charge carrier drift close to the electrodes.
- Charge carriers drifting towards the backplane do not contribute significantly to the signal.

The first point particularly concerns irradiated sensors: the mobility μ and the lifetime τ[11] of free charge carriers is reduced and the result is a smaller signal charge.

3.4.2 Radiation Damage in Silicon

High energy particles, which traverse the sensor material, not only transfer energy to the valence electrons crystal lattice atoms, but also to the crystal lattice itself. The impact can be severe, so that atoms are displaced from their lattice sites. The displacement leads to point defects such as interstitials (atoms in between lattice sites) or vacancies (empty lattice sites). If the impact is strong enough, defect clusters (conglomerates) may occur. Also possible are direct nuclear interactions, which lead to nuclear transmutation, and thus possibly to activation.

Such externally generated defects disturb the thermodynamic equilibrium. Most of these defects are mobile and attempt to attain thermodynamic equilibrium, e. g. point defects can annihilate or diffuse out of the surface. But it can be shown that also stable defects are formed: defects interact with each other and form new type of defects which can become immobile. Some of the defects are intentional such as dopants and oxygen but they can form a complex with unwanted defects, thereby losing their former functionality. This will result in a change of macroscopic (i. e. electrical) properties of the crystal. Especially the capturing dopants, e. g. phosphorus and boron for silicon, lead to the so-called effect of type inversion[12]: Initially n-typed silicon becomes effectively[13] intrinsic after a fluence of a few times[14] $10^{12}\,\mathrm{n_{eq}/cm^2}$ (NIEL[15]) [22]. Above this point, it becomes effectively p-type (see figure 3.13).

Many defects in the crystal, as stated above, diminish over time and hence all negative effects, which affects the sensor characteristics, will degrade in time. The speed of this process, which is called beneficial annealing, depends strongly on the temperature. In case of silicon, this process slows down in time. At some point it reverses and a increase of the effective doping change take place. The reason are former inactive defects which after a time become electrically active. This disadvantageous effect is called reverse annealing. The whole process can be slowed down by cooling down the sensor material.

The annealing and the following degradation of the detector can be controlled by the temperature at which the detector is kept during the maintenance periods.

Oxygen is used to radiation-harden silicon (oxygenated silicon). Oxygen has been found capturing silicon vacancies which leads to a decreased post-radiation depletion voltage [26].

To conclude, defects will have the following main consequences [22]:

[11] The charge collection distance (CCD) is the product of μ and τ and is commonly used to characterize detector materials.

[12] Applies to low-doped bulk silicon as the doping concentration is several orders of magnitude less than in the electrodes.

[13] The difference in the concentration of donors and acceptors determines the type.

[14] Depends on the doping concentration.

[15] NIEL stand for non-ionizing energy loss and is a quantity which describes the incident particle dependent rate of energy loss due to atomic displacements. The product of the NIEL and the particle fluence (time integrated flux) gives the displacement damage energy deposition per unit mass of material [24].

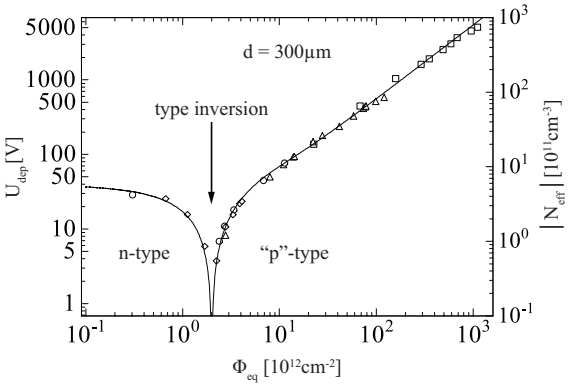


Figure 3.13: Absolute value of the effective doping concentration $|N_{\text{eff}}|$ depending on the fluence Φ_{eq} (neutrons, 1 MeV neutron equivalent) [25].

- They act as recombination–generation centers (recombination and generation of electron-hole pairs); in the depletion zone this leads to an increased reverse-bias (or leakage) current (shot noise, thermal runaway).

- They act as trapping centers; this leads to a reduced charge collection distance and hence smaller signal charge (loss of charge).

- They can change the charge density in the space-charge region; higher depletion (or bias) voltage is needed or under depletion may occur.

The first two points have consequences for the S/N ratio. The increase of the reverse-bias current is the most noticeable change. The volume-generated leakage current I_{vol} increases linearly[16] with the fluence ϕ [22]:

$$\triangle I_{\text{vol}} = \alpha V \phi \,, \tag{3.10}$$

where V denotes the detector volume and α has to be determined. If the fluence is scaled by the non-ionizing energy loss, then the increase of the leakage current is independent of the particle type.

3.4.3 Sensor Types and Technologies

For a detector, an efficient charge collection is necessary to meet the requirements of space, time and energy resolution and overall efficiency. All of these points depend largely on the properties of the sensor. In addition the sensor has to meet geometrical constraints on size and thickness while sustaining a massive amount of radiation damage. Concerning the IBL upgrade, there are three sensor technologies which may fulfill the requirements [27]: planar, 3D and diamond sensors. Each technology is demanding for different operating and environmental variables such as reverse-bias voltage and operating temperature. The first two sensor concepts (see figure 3.14) will be explained in the following.

[16] Above type inversion, the rise is stronger (see figure 3.13).

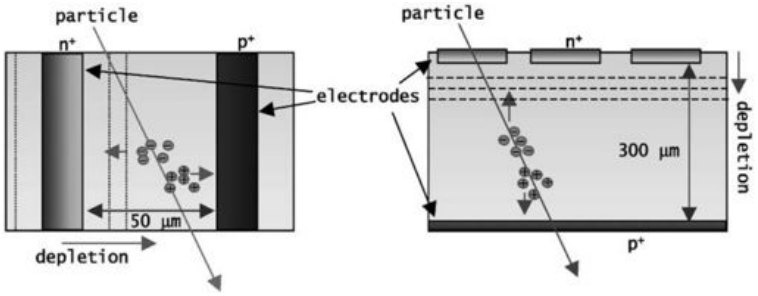


Figure 3.14: A 3D n-in-p sensor (left) in comparison to a planar n-on-n sensor (right) after type inversion. In case of a 3D sensor, the charge, which is generated by a traversing ionizing particle, is collected by a much shorter length. The result is a faster signals and a much lower depletion voltage. The dashed lines show how the depletion region grows from the n^+-implants, when a reverse bias voltage is applied [28].

Planar Sensors The planar technology is the most commonly used and preferred technology for vertex and tracking detectors. The electrical and mechanical properties of planar sensors are very well understood and the manufacturing is relatively low cost and has high yield. Compared to the other sensor technologies, planar sensors require the lowest operating temperature and a high bias voltage. This is because of its geometry: The electrodes are located on top and bottom of the bulk. For full charge collection, the depletion zone has to be extended throughout the whole bulk ($\approx 250\,\mu m$). According to formula 3.6 and Ramo's Theorem (formula 3.8) a high voltage has to be applied and charge carriers have to travel long distances to generate an adequate signal.

If one assumes negative charge collection at the readout electrode (due to limitations of the CSA), two different approaches for the sensor design are possible (see also figure 3.15):

n-on-n This type is used in the current Atlas pixel detector. Before type inversion the depletion region starts growing from the high voltage backside electrode (p^+-type) into the n-bulk. The potential drop towards the cutting edge is ensured by a multi guard ring[17] structure. For full charge collection, unirradiated n-on-n sensors have to be operated fully depleted or over-depleted. P-stop or p-spray implant are needed to isolate the n^+-pixel implants from each other due to electron accumulation beneath the Si-SiO_2 junction. After type inversion (now "p"-bulk) the depletion zone starts growing from the n-pixel implants. To be able to collect charge negative carriers the detector does not need to be operated fully depleted after type inversion.

n-on-p In contrast to the n-on-n type sensors, the p-bulk of the n-on-p type sensors does not change its type. Independent of the fluence, the depletion zone always starts to grow from the pixel side. Therefore n-on-p-type sensors suffice to having only a homogeneous p^+-implant on the high voltage

[17] Guard rings are biased by a punchthrough mechanism. A punchthrough current flows through the high field region at the cutting edge of the sensor, and creates a potential drop through the different guard rings [30].

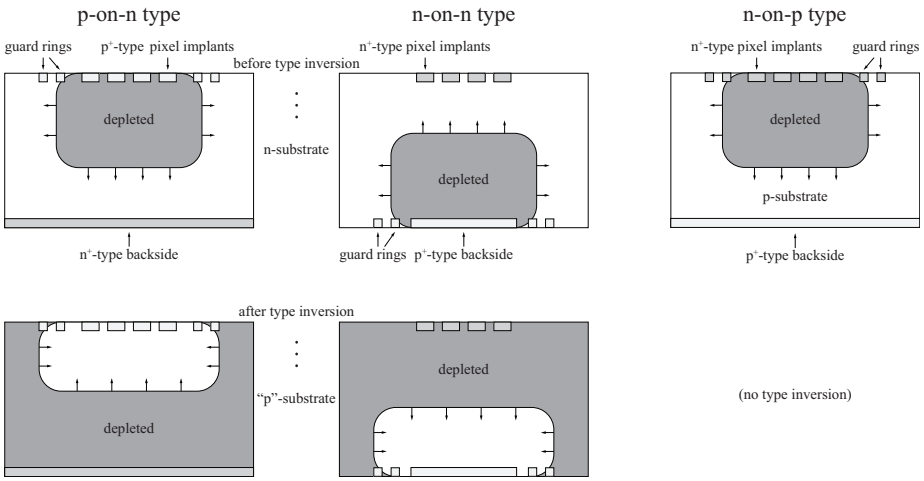


Figure 3.15: Comparison between basic planar sensor concepts: p-on-n, n-on-n and n-on-p type from left to right, respectively. Both, the p-on-n and the n-on-n type, have initially an n-bulk. After a certain fluence (several times $10^{12}\,\mathrm{n_{eq}/cm^{-2}}$), the bulk becomes p-like. The p-on-n type sensor is the only sensor collecting holes at the pixel implants. It is mentioned for the sake of completeness and will not be addressed any further [29].

backside. Having structured implants (namely n^+-pixel and p-stop/spray implants) only on one side makes this sensor cost-effective [31]. In addition, the sensor can easily be thinned down. This reduces the material budget and improves tracking performance. A major drawback are possible discharges at the cutting edge of the sensor into the readout chip [32]. Although the sensor is biased from the back side the potential drop happens at the front side. A multi guard ring structure on the pixel side ensures the potential drop towards the pixel implants.

3D Sensors 3D sensors are the most advanced technology concerning radiation hard silicon detectors. It also requires most advanced process technology which is responsible for the higher costs compared to planar sensors. Cylindrical electrodes are implemented perpendicular to the sensor surface. Implanting the electrodes makes this sensor cost-intensive. 3D sensors require the lowest bias voltage by preserving the full bulk thickness and are operable at intermediate temperatures. This is because of the short distance between the electrodes ($\leq 100\,\mu\mathrm{m}$). Due to the geometry of electrodes, the major drawback is the higher detector capacitance which leads to a higher noise and thus reduces S/N ratio. Another drawback is the reduced hit detection probability and charge collection efficiency for normal incidence. This only affects ionizing particles traversing the sensor electrodes. The detector recover full efficiency under a certain incident angle. Another possibility is the implementation of the electrodes under a certain angle into the bulk.

Two different design concepts are proposed for the IBL upgrade [27]: Single-sided ("full-3D") with active edges and double-sided 3D sensors. The active edge technology allows a minimum of dead area at the edge of the sensor (a

few µm compared to a few 100 µm). Active edges becomes an important feature regarding IBL since overlapping (shingling) of modules in direction of the beam pipe is not possible.

Chapter 4

The USBpix Test System

4.1 Introduction

USBpix was developed as a small and light weighting test system for ATLAS FE-I3 pixel readout chips. As successor to TurboDAQ, which is rather big in size and consists of many expensive hardware components, it provides the functionality which is needed for a full characterization of pixel sensors attached to the FE-I3 pixel readout chip.

The development of the USBpix readout system started in the late 2008. The hardware design and basic software parts (USB driver, microcontroller code, hardware interface libraries, and basic FPGA code) were developed at SiLAB[1][33, 34]. Other parts of the software (STcontrol and PixLib) were contributed by the ATLAS Pixel Collaboration and were adapted to the USBpix test system with support of University of Göttingen[2].

A main part of this diploma thesis covers the code maintenance and further development of the USBpix test system for the FE-I3 readout chip. In the beginning of this work, source code refactoring was the main task to ensure extensibility and maintainability of the test system. During this work many parts of the source code were rewritten and new functionality was added. Changes were made to all system levels, i.e. driver, microcontroller code, libraries, user interface and in particular to the FPGA code. Continuous testing and the characterization of sensors (see section 6) during the development cycles helped to improve the overall quality of the software.

Furthermore, USBpix is capable to fulfill the needs for an ATLAS FE-I4 test system, of which development started in the late 2009. The FE-I3 test system's source code was ported to support the future ATLAS FE-I4 readout chip which is foreseen for a future IBL upgrade of the ATLAS pixel detector.

4.2 Requirements

The USBpix test system main purpose is the characterization of new generation of sensor material intended for being used for IBL and HL-LHC detector

[1]Silizium Labor der Univerität Bonn, Nussallee 12, D-53115 Bonn, Germany.

[2]Georg-August-Universität Göttingen, II. Physikalisches Institut, Friedrich-Hund-Platz 1, D-37077 Göttingen, Germany.

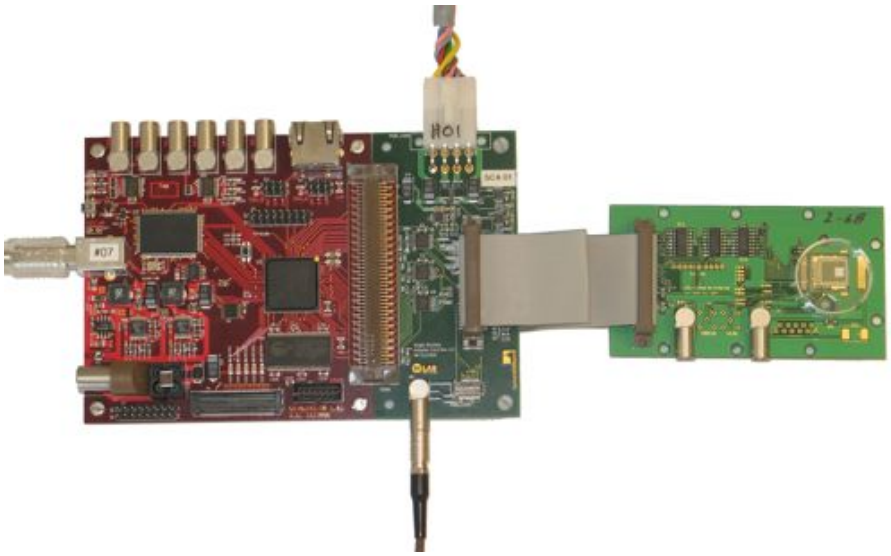


Figure 4.1: The USBpix test system (from left to right): the S3Multi-IO-Board, the Single Module Adapter Card (SMAC), and the Single Chip Card (SCC).

upgrades. Besides that, the USBpix test system has to provide most of the functionality as its predecessor TurboDAQ. The functionality of USBpix includes the following scan types (to name the most important ones):

Analog Test Test of the analog pixel block

Crosstalk Scan Measurement of the electronic crosstalk between adjacent pixels

Digital Test Test of the digital pixel block and digital readout chain

Monleak Scan Measurement of the leakage current

Source Scan Data taking with radioactive source and external trigger

Threshold Scan Measurement of the S-curve

GDAC and TDAC Tuning Coarse and fine tuning of the threshold

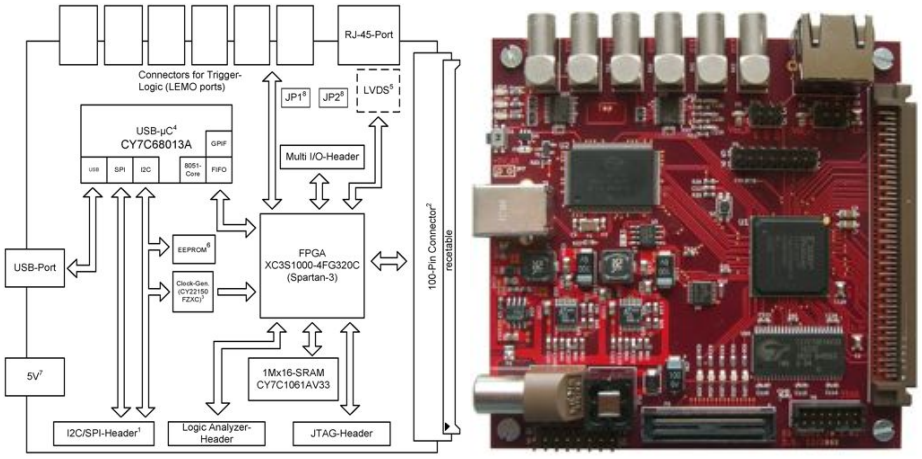
FDAC Tuning Tuning of the Time-over-Threshold (ToT)

ToT Calibration Measurement of the relationship between collected charge and ToT

Additionally, the integration of the USBpix test system into the framework of the EUDET beam telescope is one of the major tasks.

4.3 Hardware Parts of USBpix

The USBpix hardware is built up in a modular way (see figure 4.1). It consists of three different PCB boards which are connected over flat ribbon cable and



(a) (b)

Figure 4.2: (a) Block diagram of the S3Multi-IO-Board. (b) Picture of the S3Multi-IO-Board [35].

on-board connectors. The entire hardware of the test system is connected via a USB 2.0 Hi-Speed interface (480 Mbps raw data speed) to a host computer (or DAQ computer) which is running the control software (STcontrol).

4.3.1 S3Multi-IO-Board

The S3Multi-IO-Board is a multi-purpose I/O board (Rev. 1.03, see figure 4.2). It is the central control unit of the test system containing all of the programmable hardware parts. The communication between the host computer and the S3Multi-IO-Board is implemented in an 8051-based USB-capable microcontroller (Cypress CY7C68013A). The 8051-microcontroller steers the communication between hardware parts on the S3Multi-IO-Board (FPGA, EEPROM, programmable clock generator, ADC; for more details see following sections) and the software running on the host computer. To set the programmable clock generator (Cypress CY22150FZXI) or to read out the analog-to-digital converters (Maxim MAX1238, located on the Adapter Card) the microcontroller uses a 2-wire I²C serial interface. The EEPROM (Microchip 24LC128), which contains the firmware of the microcontroller, is serially connected to the 8051-microcontroller. Registers and Block RAM inside the FPGA (Xilinx Spartan-3 XC3S1000-FGG320) can be accessed by using the Slow Interface. The Slow Interface[3] is a 8-bit wide parallel data bus with a 48 MHz clock (UCLK, internal clock of the microcontroller). The address space is 16-bit wide. The microcontroller and the FPGA have access to 16 Mbit asynchronous SRAM. The SRAM (Cypress CY7C1061AV33) is connected to a 16-bit wide data bus[4]. The clock speed depends on whether the microcontroller or the FPGA is accessing the SRAM and is 48 MHz or 40 MHz, respectively. The memory can

[3]The name derives from the fact that the internal clock was initially running on 24 MHz. The speed of the internal clock was changed during this thesis.

[4]A 16-bit wide parallel interface is available in hardware but not implemented in software. Currently, only a 8-bit wide data bus is used.

be accessed through a 20-bit wide address bus. The overall maximum readout speed reaches 1/4 of the raw data speed of the USB 2.0 Hi-Speed interface (approximately 15 MB/s).

Various input/output (I/O) connectors can be accessed by the FPGA. The main I/O connector (100-pin connector) is placed on the edge of the S3Multi-IO-Board and can hold different types of adapter cards. In addition, there are various other multi-purpose I/O ports available. Six LEMO connectors, an 8P8C[5] jack, a 100-pin Samtec connector and a 16 pin header are placed on the S3Multi-IO-Board.

4.3.2 Single Module Adapter Card

The Single Module Adapter Card (SMAC, Rev. 1.2) holds low-voltage differential signaling (LVDS) transceiver to enable high-speed data transmission over standard flat ribbon cable. The flat ribbon cable connects the SMAC to the Single Chip Card (see next section). Additionally, analog voltage (AVDD), digital voltage (DVDD) and low voltage (LVDD), which are needed for the Single Chip Card (see section 4.3.3), are transmitted over the flat ribbon cable. The supply voltages are received from external power supplies which are connected to the 8-pin Molex power connector. The SMAC also holds an analog-to-digital converter (ADC) which is connected to the microcontroller over the I²C bus. The ADC reads out AVDD and DVDD, and a negative temperature coefficient (NTC) thermistor which can be soldered to the Single Chip Card.

4.3.3 Single Chip Card

The Single Chip Card (SCC) holds the FE-I3 chip which receives AVDD and DVDD from the SMAC. LVDS transceivers are placed on the SCC to convert incoming LVDS signals to single-ended CMOS and vice versa. The transceivers can either be powered by using LVDD (2.8 V) from the SMAC or externally by connecting a power supply to a LEMO connector. Another LEMO connector can be connected to a high voltage power supply and receives bias voltage for biasing the sensor. Two more LEMO connectors are available which provides access to the MonAmp and VCal pad on the FE-I3 chip.

Several test pads are available for testing and measuring signal integrity of the FE-I3 readout chip. Some of them are needed during chip/sensor characterization (see section 5.4).

4.4 Software Framework of USBpix

The software framework of USBpix has a multi-layer structure which reflects the hardware structure of the test system. It encapsulates functionality within useable objects which creates function modules. In the following sections, a closer look will be given on the USBpix framework. The focus is on changes which have made during this thesis.

[5] 8P8C jacks are often referred to as “RJ-45” jacks.

4.4.1 USB Driver

The USB driver controls the data transfer between the host computer (USB master) and the peripheral device (USB slave), which is built into the USB-capable 8051-microcontroller. A driver for Microsoft Windows[6] is available as well as a Linux kernel mode driver.

During this thesis it turned out that the Linux driver has compatibility issues with recent Linux kernels (2.6.24 and upwards). Efforts were undertaken to solve these issues but without success.

A possible solution for that issue is to use the open source libusb[7] driver for both Microsoft Windows and Linux-based systems.

4.4.2 SiUSBLib Library

The SiUSBLib library is a collection of classes and functions providing rudimentary access to the USBpix hardware. SiUSBLib is implemented as a dynamically linked library[8] (DLL), namely `SiUSBLib.dll`. To give access to the USBpix hardware other objects and libraries can be built against[9] SiUSBLib library.

The functionality of SiUSBLib library is closely related to the USBpix hardware. It provides functionality which gives access to the hardware such as programming the microcontroller and FPGA, flashing the EEPROM, and writing and reading SRAM and registers.

Under Microsoft Windows and Linux-based systems the USB device handling is controlled by the SiUSBLib library. Due to historical reasons the maximum number of USBpix boards, which can be attached to a single host computer, is limited to 8 peripheral devices (mainly due to limitations of the USB driver). During this thesis it shows up that this limitation leads to erroneous multi-device handling so that the host computer can securely handle only one USB device at the same time. Changes in the USB driver and the SiUSBLib library are needed to overcome this limitation.

Another possible solution to overcome this limitation, it is suitable to use the libusb driver (see section 4.4.1). In either case, the SiUSBLib library needs to be adapted.

During this thesis only slight changes were made to the SiUSBLib library. Only the `ReadInterrupt(...)` and `WriteInterrupt(...)` functions were changed to support new functionality in the USBpixdll library (see section 4.4.3), and microcontroller firmware (see section 4.5).

4.4.3 USBpixdll Library

The USBpixdll library consists of classes providing access to the functionality which is built into the FPGA and microcontroller. To get access to the USBpix

[6] The USB driver supports Microsoft Windows XP/Vista/7 (32-bit).

[7] Libusb is a library which gives user level applications uniform access to USB devices across many different operating systems. Libusb is an open source project licensed under the GNU Lesser General Public License version 2.1 (LGPLv2.1). `http://www.libusb.org`

[8] A dynamic link library is executable code which is loaded and linked during load time or runtime. Only a minimum amount of work is done during link time.

[9] This process is also called linking. After compilation, the linker links all of the specified object and library files to create executable files.

hardware, USBpixdll library uses functionality provided by the SiUSBLib library (USBpixdll library is built against the SiUSBLib library). USBpixdll library is implemented as a DLL (`usbpixdll.dll`).

During this thesis, most parts of USBpixdll library were rewritten. In the following paragraphs a closer look will be given to particular changes to the classes.

The ConfigRegister class was completely rewritten and new functionality was implemented. This class provides access to the register inside the FPGA (see section 4.6) as well as to the SRAM on the S3Multi-IO-Board. It makes functionality available, which is implemented in the FPGA, to other classes or applications, but protect it against improper operation. This class is also responsible for data related tasks. It reads out and processes the data produced during every scan, so that higher-level applications have easy access to histogrammed data. Most of the changes were made due to the implementation of the Source-Scan (see section 5.8). Functions for controlling the Source-Scan and reading out the status of the Source-Scan were implemented. To give existing data analysis software access to the raw data, which is generated during the Source Scan (see section 5.8), it is possible to write TurboDAQ-compatible output files. Additionally several histogram functions were added to ConfigRegister. They were used to introduce new types of histograms to STcontrol/PixLib. Among these histogram functions two different cluster algorithms and a seed finding algorithm were implemented (see section 5.9.2).

The ConfigFEMemory class provides functionality to configure the FE-I3 readout chip. It has access to the Block RAM[10] to store and modify FE-I3 global and pixel register data. During this thesis mainly source code maintenance was performed.

4.4.4 USBpixController Class

The USBpixController class is the interface class between the STcontrol/PixLib DAQ and the classes belonging to the USBpixdll library (see previous section). The goal of the USBpixController class is to hide implementation details of USBpix from STcontrol/PixLib DAQ.

During this thesis many changes were made to the USBpixController class, in particular code maintenance and implementation of new functionality (e.g. Source Scan), which have implemented into USBpix.

4.5 Microcontroller Firmware

Most parts of the microcontroller source code are provided “as is”. The core functionality (access to the hardware components on the S3Multi-IO-Board as described in section 4.3.1) relies on functionality implemented in the SiUSBLib library (see section 4.4.2).

Functionality was implemented to run a full scan (e. g. Threshold Scan, ToT Scan) on the 8051-microcontroller without any interaction between the host computer and the microcontroller [34]. For that purpose, the microcontroller has access to the registers and Block RAM inside the FPGA to control the FSMs and to change the global and pixel register data of the FE-I3. During

[10] Block RAM is a dedicated dual-port memory placed on the FPGA.

the scan, histogrammed data is stored in the SRAM for later readout (for more details, see following section).

During this thesis, parts of microcontroller source code, in particular those concerning the automatic scans loop, were rewritten to ensure stability and data integrity. The ability to apply all possible FE-I3 masks was added. In addition to that, the mask shifting problem with two applied masks (e. g. SEL-ENA, SEL-PRE) was solved. During this thesis it turned out that simultaneous shifting of two pixel masks at the same time results in "missing hits". It turned out that this only affects the first charge injection[11] immediately after the mask shift. This means, that the strobe signal was applied to a pixel but no hit was seen. To come over this problem, a "fake injection"[12] is applied to every pixel before the regular injection starts. In other words, after every mask shifting an additional charge injection is applied (strobe signal) but the data received from the FE-I3 associated with this injection is not saved. The reason for this behavior is not understood but is most likely a feature of the FE-I3 readout chip. This behavior will not affect the operation of the test systems, nor regular detector operation. Similar problems while shifting of three masks (SEL-ENA-PRE) at the same time is also not understood and left unresolved.

During the work on the microcontroller firmware, a severe bug, which results in a measured threshold discrepancy between TurboDAQ and USBpix, was fixed. The threshold discrepancy between TurboDAQ and USBpix was observed for the first time in [34] and then verified in [36]. The threshold discrepancy was due to a programming error in the microcontroller source code which put the histogrammed data into the wrong memory location. This was fixed as of release 1.4 of USBpix. For a threshold comparison between USBpix and TurboDAQ see figure 4.3.

4.6 FPGA Firmware

Many affords were undertaken to redesign the source code of the FPGA firmware. This was done in a two stage process. The first step was refactoring of the source code. During this process the existing source code was replaced without modifying the external functionality and behavior. In a second step, new functionality was added and the source code was further developed. The next paragraphs will highlight the functionality and the changes made during this work.

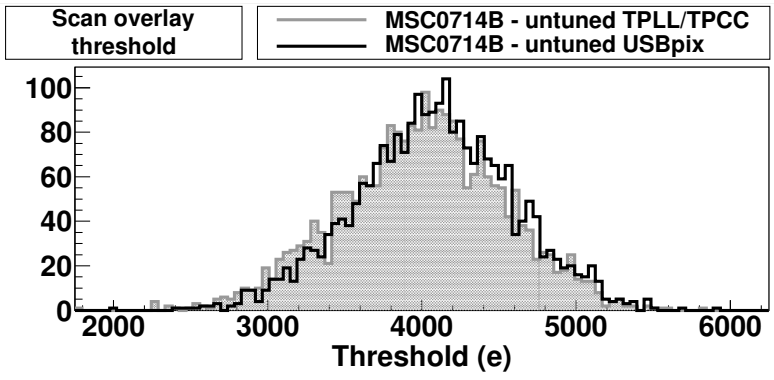
To define the behavior of the FPGA, the Verilog[13] programming language was used. Verilog is hardware description language (HDL) which is most commonly used to describe and simulate digital designs. The syntax of Verilog is similar to C programming language (e. g. bitwise operators, statements). In addition to being able to process sequential/synchronous logic, which is supported by most of today's programming languages, Verilog also incorporates syntax to describe combinatorial/asynchronous logic.

Figure 4.4 gives an overview of the modular structure of the USBpix HDL design. A Verilog design consists of a hierarchy of modules, starting with the

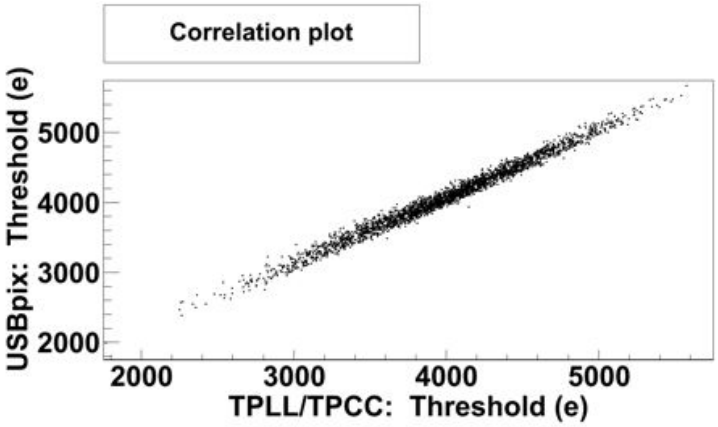
[11] On the rising edge of the strobe signal negative charge is injected into the preamplifier (see section 5.4).

[12] The FPGA has to be set to "fake injection mode" (see section 4.6). Set to this mode, the FPGA receives raw data but doesn't save histogrammed data to the SRAM.

[13] IEEE 1364-2001, known as Verilog-2001.



(a)



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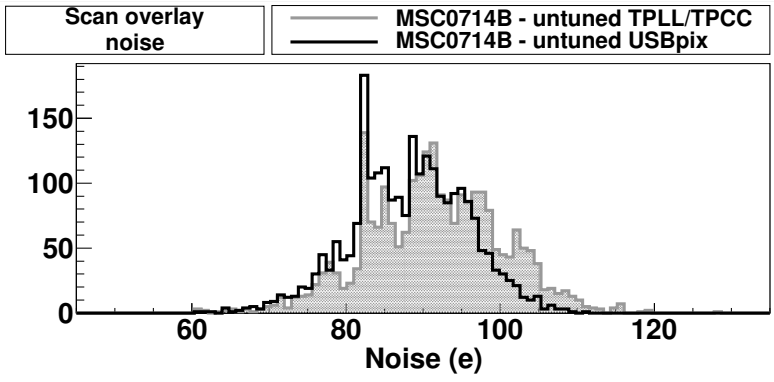


(c)

Figure 4.3: Comparison between USBpix and TurboDAQ (in the figures referred to as TPLL/TPCC) [37]. The FE-I3 readout chip (7-14B) was not connected to a sensor (measured noise of approximately 90 electrons). It was left untuned to not bias the results by using different tuning algorithms on each readout system. Instead, the standard configuration was used (see [34]). (a) Overlay plot of the threshold distribution. (b) Pixel-by-pixel comparison of the threshold. (c) Overlay plot of the noise distribution.

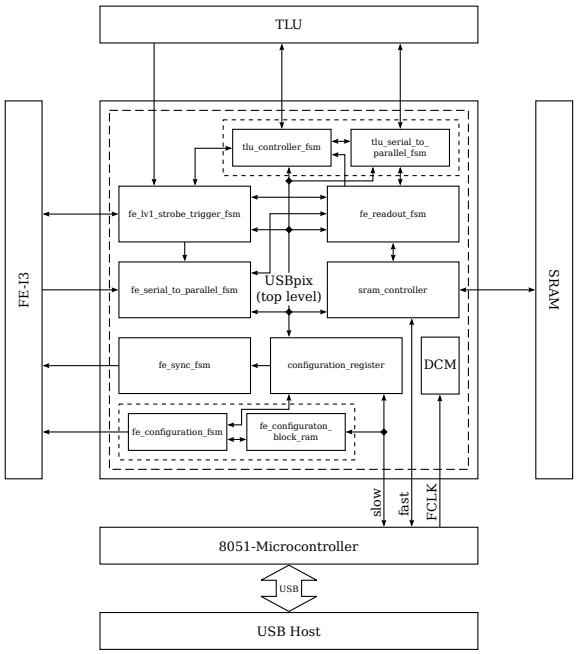


Figure 4.4: USBpix HDL design.

top-level module. All I/O ports of the top-level module are expected to be realized in hardware (I/O ports of the FPGA) as described in the user constraints file (UCF). All remaining modules communicate with other modules through a set of I/O ports. Internally, every module uses sequential and combinatorial logic which is connected to I/O ports, internal wires or internal registers. The functionality of every module is as follows: the top-level module is called `USBpix.v`. Every I/O port of USBpix.v is assigned to an I/O pin on the FPGA chip as described in the user constraints file `USBpix_S3MultiIO_V103.ucf`. Internally, USBpix.v is connected to instances of other modules which form a sub-hierarchy. Every logic element, which is instantiated by synthesis tool[14], belongs to a clock domain. A clock domain determines the signal frequency[15] of a section of logic. Inside this section all synchronous logic (e.g. flip-flops) is clocked by the same net (e.g. clock net with a clock of a certain frequency and phase). The clock domain also determines the length of signal paths between logic elements to satisfy constraints as defined in the UCF file. The calculation of signal path is integral part of the process of placing and routing[16].

The FPGA receives the FCLK (see section 4.5) from the microcontroller. The digital clock manager (DCM), which is instantiated inside the module `clock_generator.v`, generates the crossing clock (XCK, 40 MHz) and com-

[14]Synthesis is a process by which an abstract form of desired circuit behavior (e.g. as defined by HDL) is turned into a design implementation in terms of logic elements (e.g netlist).

[15]All signals in a clock domain are synchronized to a fixed clock. Signals which are crossing from one clock domain into another have to be synchronized. Even input signals of the FPGA which have the same frequency must be synchronized (phase alignment). To avoid metastable events, two stage synchronizer are used to synchronize all input signals into the FPGA.

[16]Place and route (P&R) describes a processes where the netlist is mapped to the FPGA physical resources.

mand clock (CCK, 4 MHz[17]) by multiplying or dividing the incoming FCLK. The FCLK is used in the `sram_controller.v` module for reading out the SRAM (fast interface). Additionally, the FCLK is used for writing data, which is received from the microcontroller via the slow interface, to the registers inside the FPGA. Those registers are placed in the `configuration_register.v` module.

The XCK and the CCK are mainly used to drive the flip-flops which are placed inside the FPGA. Both clocks are getting forwarded to an attached FE-I3 readout chip using a double-data rate flip-flop (OFDDRRSE) to deskew data to clock phase alignment.

The behavior of combinatorial logic and finite state machines[18] (FSM), which are instantiated inside the FPGA, can be controlled by setting registers values. The corresponding registers placed inside the `configuration_register.v` module. The FSM coding style is using the three always block coding style (two sequential always blocks and one combinatorial always block) with registered outputs. This coding style was chosen because it is easily modifiable and extendable and is readable by every HDL design tool (e. g. Aldec Active-HDL, Mentor Graphics Precision Synthesis). Following FSM were developed during this thesis:

`fe_lv1_strobe_trigger_fsm.v` This module contains a FSM, which controls the length, delay and the number of repetitions of the strobe and LV1 signal, which are sent to the FE-I3. In source scan mode, this FSM also receives the external trigger signal. The external trigger signal causes the generation of the LV1 trigger signal. This process is repeated until the desired number of triggers signals, hit words or EoE words is received. Two trigger input ports are available on the USBpix board: A LEMO RX0 jack[19] and the RJ45 jack (intended to be used by the trigger logic unit (TLU), see next section for more details). Different sources of a trigger signal can be used to trigger the readout, e. g. the FE-I3 hitbus signal (self-triggering[20]), an amplifier/discriminator board or the TLU.

`fe_serial_to_parallel_sr_fsm.v` This module contains a 26-bit shift register which is receiving the serial raw data from the FE-I3 readout chip. The FSM reads out the shift register data and makes it available to other FSMs on a 26-bit wide internal bus. The FSM also checks the received data: it recognizes whether the data is an EoE word or hit word and checks for errors and invalid data and sets an appropriate flag inside the trigger word (see table 4.1).

[17] The CCK operates at 5 MHz. In order to reuse the CCK for reading out the Trigger Logic Unit (see section 4.7) the frequency was lowered to 4 MHz. This saves the use of another DCM and low skew clock net inside the FPGA. The change of the frequency of the configuration clock has no influence on the behaviour of the FE-I3 readout chip.

[18] A finite state machine consists of sequential and combinatorial logic. It is a model of behavior composed of a finite number of states. The output values of a FSM are determined by its current state and by the input values (Mealy machine). The transition between those states depends on the current state and is also influenced by the input values.

[19] LVTTL/LVCMOS, unipolar, 0... + 3.3 V.

[20] The LEMO TX2 jack has to be connected to the LEMO RX0 jack. The MonHit MUX has to be set up so that the hitbus signal is available on the MonHit output pin of the FE-I3 (global register [23:26]). This self-trigger mode should not be confused with the internal self-trigger as described in [12], whereas in both cases the hitbus signal is used to generate the LV1 trigger.

`fe_readout_fsm.v` This FSM is reading out the parallel data on the 26-bit wide internal bus and controls the data writing to the SRAM. Depending on the readout mode ("fake injection mode", "ToT mode", "calibration mode", "source scan mode") different data is written to the SRAM. The "fake injection mode", "ToT mode" and "calibration mode" are set by the microcontroller depending on the scan type (e. g. ToT Scan, Threshold Scan). If the FSM is set to "fake injection mode", no data is written to the SRAM (see section 4.5). If set to "ToT mode", only histogrammed ToT data is written to the SRAM to save memory. The data is stored at predetermined addresses within the SRAM, depending on the pixel address (column/row) and the scan loop number. The same is true for the "calibration mode", but in this mode only hit information is saved (hit word counter). In source scan mode all hit words and EoE words received from the readout chip are written to the SRAM. Also a 32-bit trigger word is stored to the SRAM to identify the BCID windows[21]. The trigger word is stored behind the last received EoE word which belongs to a BCID window. The trigger word consists of a 1-bit header and 31-bit trigger data. Depending on the trigger mode, the trigger number is generated internally (trigger counter, only in no-handshake and simple handshake mode) or is received from the TLU (TLU trigger number, only in trigger data handshake mode). If enabled, additional status data can be added to every trigger word by means of cutting off 8 most significant bits (MSB) of the trigger number. The status data includes 6 error bits and 2 bits for the trigger mode (see table 4.1). The status data can be used by external analysis software to detect if the BCID window is incomplete or defect.

`fe_configuration_fsm.v` This FSM writes to the configuration registers of the FE-I3 readout chip. It controls the CCK and the LD signal and has access to two dual-port Block RAMs (RAMB16_S1_S9), which contain the configuration data. Two sets of each global register data (231 bit) and pixel register data (2880 bit) can be stored at the same time inside the Block RAMs. One Block RAM holds the configuration data for writing to the FE-I3, and the other one holds configuration data that is read back from the FE-I3 readout chip. This allows the verification of the configuration data which is stored inside the FE-I3 registers. The Block RAMs are instantiated inside the `fe_configuration_block_ram.v` module. Both modules, in turn, are instantiated inside the higher-level `fe_configuration.v` module.

The next section will cover the EUDET telescope integration and will highlight functionality implemented in the FPGA design.

[21] A BCID window is a series of EoE words and hit words which belong to a sequence of consecutive LV1 triggers (maximum of 16 consecutive LV1 trigger à 25 ns). The number of EoE words corresponds to the total length of the LV1 trigger in units of bunch crossings (a bunch crossing is equivalent to 25 ns).

raw data word bit	[31:0]							
hit word w/o parity	6'b0	1'b1	BCID [3:0]	row [7:0]	column [4:0]		ToT [7:0]	
EoE word w/o parity	6'b0	1'b1	BCID [3:0]	flag [7:0]	1'b0	L1ID [3:0]	BCID [7:4]	warn [3:0]

(a)

trigger word bit	[31:0]		
trigger word w/o status data	1'b1	trigger number [30:0]	
trigger word with status data	1'b1	trigger number [22:0]	status data [7:0]

(b)

status data bit	[7:0]						
status data	EoE word error	EoE word warning	unknown word	wrong number of EoE	EoE/hit word timeout	BCID window timeout	trigger mode [1:0]

(c)

Table 4.1: Data alignment and structure: (a) Hit word and EoE word. (b) Trigger word. The MSB is always equal to 1 to easily identify the trigger word. (c) Status data. The status date is part of the trigger word and includes additional error/waring flags and 2-bit trigger mode.

4.7 Integration of USBpix into the Framework of EUDET Telescope

Within the research and development towards the International Linear Collider[22] (ILC) the EUDET[23] JRA1[24] project has developed a high resolution telescope (hereinafter referred to as "EUDET telescope" or simply telescope). The EUDET project is an EU-funded infrastructure project which comes to a close at the end of the year 2010. A follow-up project for advanced detector research and development, AIDA[25], has already started.

The EUDET telescope is available for detector tests at beam tests at DESY and CERN. The telescope package comprises the telescope itself, trigger hardware, data acquisition software and analysis software.

The EUDET telescope is shown in figure 4.5 . It consists of two arms, each holding a maximum of 3 layers of MIMOSA 26[26] pixel detector. The device under test (DUT) is placed in between these two arms. On each outside of the telescope arms, plastic scintillators can be attached to provide fast trigger signals. A maximum of 4 planes of plastic scintillators can be attached to the trigger logic unit (TLU, see figure 4.6) to generate a beam trigger signal (coincidence of the trigger input signals) which is distributed to the MIMOSA DAQ and the DUT DAQ. The TLU is the interface between the beam trigger scintillators, the MIMOSA DAQ (EUDRB, the EUDET data reduction board, see figure 4.7) and the DUT DAQ. Every DAQ is running a "producer" process[27]

[22] `http://www.linearcollider.org`
[23] `http://www.eudet.org`
[24] `http://www.eudet.org/e13/e21`
[25] `http://cern.ch/aida`
[26] MIMOSA 26 is a monolithic pixel detector using CMOS technology [39].
[27] The USBpix producer is inherited from the producer base class provided by the EUDAQ software framework. The USBpix producer runs as a separate thread inside STcontrol.

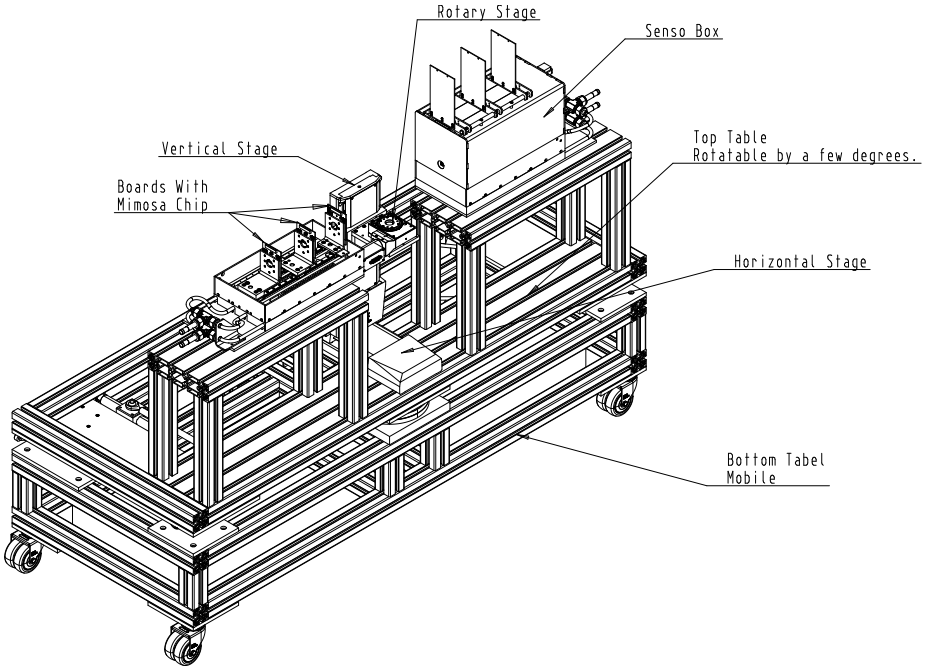


Figure 4.5: The EUDET telescope [38].

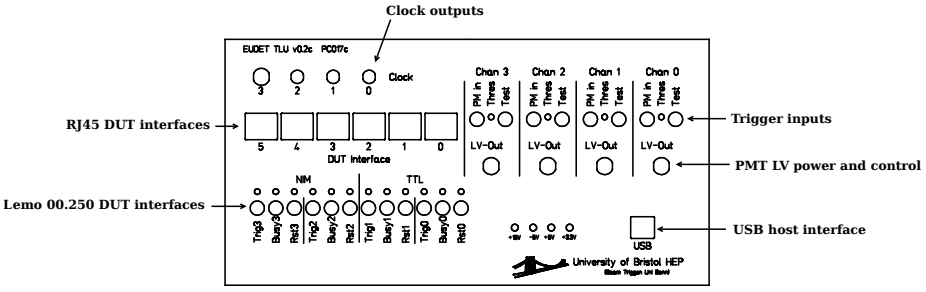


Figure 4.6: The trigger logic unit (TLU) [40].

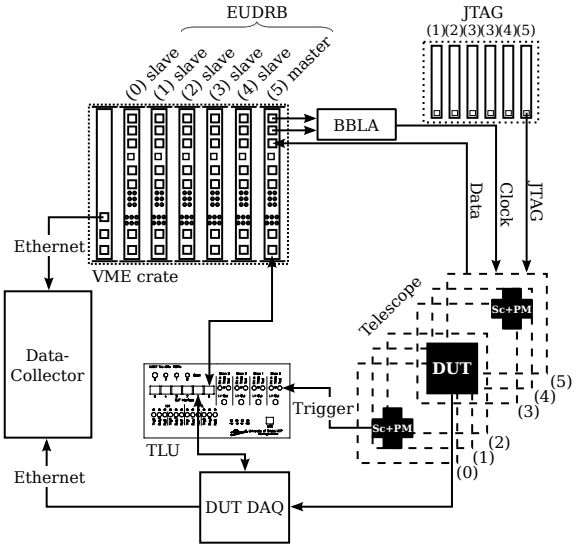


Figure 4.7: Overview of interconnections between the trigger logic unit (TLU), the MIMOSA DAQ (EUDRB), and the DUT DAQ. The MIMOSA DAQ and the DUT DAQ are handled equally by the TLU. The MIMOSA 26 pixel detectors are configured over a JTAG interface controlled by a dedicated computer.

that converts the raw data received from every detector into EUDAQ readable format. Then, after the conversion, the data is sent to the EUDAQ data collector via Ethernet.

The EUDET-ATLAS producer was developed in cooperation with DESY[28] [41]. The TLU integration into the FPGA design and USBpix classes is topic of this work. The next paragraphs will give an overview about the functionality implemented in the FPGA design.

The communication protocol (also referred to as "handshake") between TLU and the USBpix test system is implemented in the FPGA. All 3 handshake modes are supported: "no-handshake" mode, "simple handshake" mode and "trigger data handshake" mode (see figure 4.8). Only in trigger data handshake mode, a TLU trigger number (15-bit or 31-bit) is sent to the DUT. This mode is intended to be used for beam tests: each DUT receives the same trigger number. This enables the identification and association of events to a beam particle. The no-handshake mode and the simple handshake mode are intended for use in laboratory tests using a radioactive source. Then, 31-bit trigger number is generated inside the FPGA. Any trigger signal can be received on the RX0 input by setting USBpix to the no-handshake mode. This is the only trigger mode where no TLU is required (see previous section for details about the trigger mode).

Following FSM were developed to support the TLU:

`tlu_controller_fsm.v` If a trigger is received and accepted by the `fe_lv1_strobe_trigger_fsm.v` FSM, the `tlu_controller_fsm.v` FSM controls the communication between the TLU and the USBpix test system.

[28] Deutsches Elektronen-Synchrotron, Notkestrasse 85, D-22603 Hamburg, Germany.

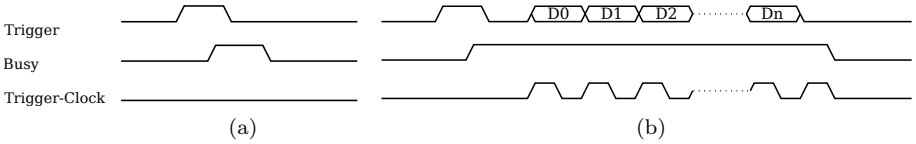
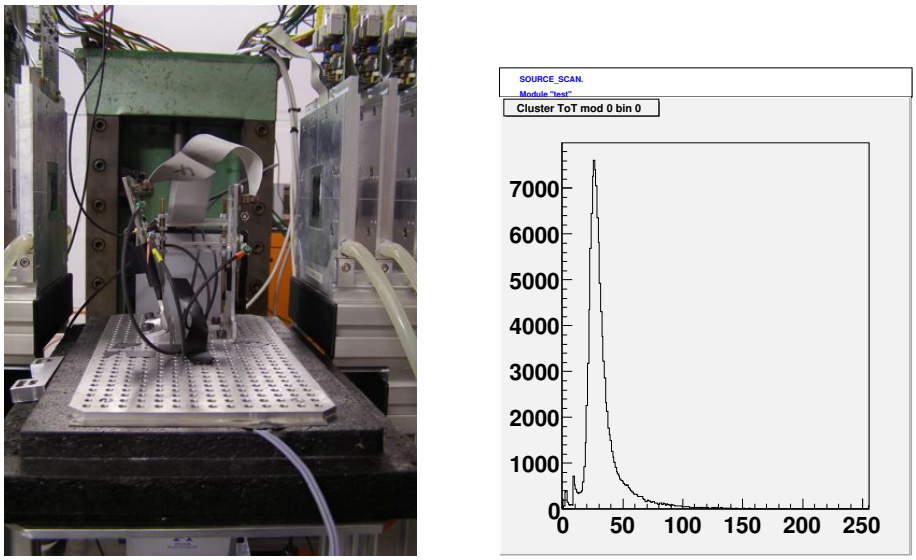


Figure 4.8: Comparison between TLU handshake modes [40]. The TLU asserts the trigger signal and receives the busy signal and the trigger clock. In no-handshake mode only the trigger signal is asserted. (a) Simple handshake mode. (b) Trigger data handshake mode.

`tlu_serial_to_parallel_sr_fsm.v` This FSM sends the trigger clock to the TLU and receives the trigger data. After deserialization of the trigger data, the `fe_readout_fsm.v` FSM saves the trigger data at the end of the raw data received from the FE-I3 readout chip.

In addition to that, several registers were implemented to control the source scan, the communication between TLU and the FPGA, the readout of raw data and trigger data (see Appendix B).

The communication between TLU and USBpix test system was first tested in laboratory at the SiLAB. The entire system (incl. telescope and data collector) was successfully tested during the IBL test beam at CERN in October 2010 (see figure 4.9).



(a) (b)

Figure 4.9: (a) Two FE-I3 DUTs mounted on a X-Y table between the telescope planes (on the left and right side of the picture). The table allows a precise alignment of the DUTs with respect to the beam axis and the telescope. (b) First test beam data with USBpix and EUDET telescope at CERN SPS, North Area, in October 2010. The plot shows the Time-over-Threshold distribution of 180 GeV pions.

Chapter 5

USBpix Test Setup

5.1 Introduction

Testing new sensor structures and materials is one of the major goals toward IBL. The sensors are attached to the well-known and extensively tested ATLAS FE-I3 readout chip. This helps to make sure that the whole test system, including the readout chip, behaves predictably.

The test setup was built up in a climate controlled laboratory at the SiLAB. Three independent measuring stations were built up and are available for characterization and testing. A climate chamber is available to guarantee a constant operating environment of the detectors.

USBpix release 1.5 was used as basis for the measurements. This release adds fully functional support for the trigger logic unit (see section 4.7) which was used as a trigger generator in the source scan setup (see section 5.8).

5.2 Aim of Measurements

Aim of the measurements is a comparison between different sensor technologies. For that purpose, an attempt was made to apply a constant experimental environment and to develop a standard test procedure. The results of the lab measurements done in this thesis should be comparable with each other and also comparable to lab measurements done by other members of the ATLAS IBL collaboration.

5.3 The Test Setup

Figure 5.1 provides an overview about the test setup. To guarantee a constant operating environment, an climate chamber (Binder MK 53) was used. The Single Chip Cards holding the detector are screw mounted on an acrylic glass board which is placed on a rack in the middle of the chamber. The wires and cables to connect the detectors are introduced through an access port on top of the chamber. This access port is also used to convey dried nitrogen gas (N_2) into the chamber to control the humidity of the air inside the chamber (controlled by an additional humidity sensor).

Figure 5.1: The USBpix test setup: the S3-Multi-IO-Board (DAQ computer not shown), LV power supplies (HV power supplies not shown), and the climate chamber.

Unirradiated detectors are operated at room temperature (nominally at 20°C) inside the climate chamber. Unirradiated detectors don't need to be cooled down, because unirradiated sensors have a significantly lower leakage current than irradiated sensors. To operate the chip with the sensor and to avoid problems, which results of high leakage current such as thermal runawy and additional noise, irradiated detectors are cooled down below 0°C. Before cooling down the detectors the climate chamber is purged with nitrogen gas until a humidity level of less than 5 % is reached. During the cooling down and during the measurements at low temperatures a constant flow of dry nitrogen gas of less than 2 l/min is introduced to the climate chamber. This keeps the humidity out.

The heat transport away from the detector is dominated by convection and conduction. The detector is supported by two ceramic strips (Al_2O_3, insulator with a thermal conductivity comparable to metals). The printed circuit board (PCB), the ceramic strips and the detector are glued together using a removable silicone adhesive with a high thermal conductivity to ensure efficient heat transport. During the measurements, the chip protection cap was removed to take advantage of the air flow inside the chamber.

Keithley 2400/2410 power supplies were used for reverse-biasing the sensors and for measuring the leakage current. The Keithley power supplies are connected to the dedicated high voltage connector on the SCC (Lemo connector). The Keithley power supplies were controlled via GPIB[1], which is implemented into STcontrol.

A TTi QL355TP power supply was used for digital and analog powering of the FE-I3 readout chip. The TTi power supplies are connected to the 8-pin power connector on the SMAC. The USBpix board and the LVDS transceiver chips on the Single Chip Card were powered externally also using the TTi power supply (5.0 V and 2.8 V respectively).

[1] General Purpose Interface Bus (IEEE-488) is a bus specification for digital communication between instruments.

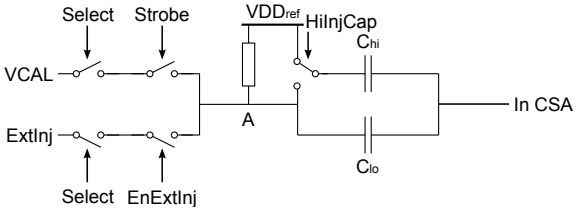


Figure 5.2: The charge injection circuit (chopper) is part of the analog pixel block [11]. The output is connected to the charge sensitive preamplifier (CSA). The charge is injected by applying a voltage step to the node A. The VCAL input is connected to an internal DAC that generates a well-defined potential. The ExtInj input is connected to a FE-I3 pin to allow applying an externally generated pulse. In combination with the VCAL DAC, the chopper is also used to test the analog functionality of the FE-I3 (Analog Test).

The digital power (hereinafter referred to as VDD or VDDD) has standard operating value of 2.0 V and is referred to digital ground (DGND). The analog power (hereinafter referred to as VDDA) has a standard operating value of 1.6 V and is referred to analogue ground (AGND) [12]. In this test setup, both, VDD and VDDA, were set to the nominal operating value of 2.1 V and 1.7 V respectively. This is due to the fact that earlier measurements with TurboDAQ used these settings and to overcome the voltage drop on the supply lines.

5.4 The Charge Injection Circuit

The determination of the properties (V_{cal}, C_{hi} and C_{lo}) of the charge injection circuit is of fundamental importance for a proper calibration of the FE-I3 readout chip (see section 5.5). Each preamplifier input is connected to a separate charge injection circuitry (often referred to as chopper).

The adjustable injection potential V_{cal} is used to pull down a reference potential VDD_{ref} (equal to VDDA, see [12]). The voltage drop is applied to the capacitance C_{hi} or C_{lo} in order to inject negative charge into the charge-sensitive amplifier. The amount of injected charge is calculated by

$$Q_{\mathrm{inj}} = C_{\mathrm{inj}}(VDD_{\mathrm{ref}} - V_{\mathrm{cal}})\,, \tag{5.1}$$

where C_{inj} is either $C_{\mathrm{hi}} + C_{\mathrm{lo}}$ or C_{lo} depending on whether high injection capacitance (global register [156]) is selected or not[2]. The potential V_{cal} is determined by a 10-bit digital-to-analog converter (DAC) inside the FE-I3 readout chip. The injection is initiated by the Strobe signal if the pixel is selected by the WriteSelect pixel register (see figure 5.2).

Due to the dependence of V_{cal}, C_{hi} and C_{lo} on wafer-to-waver (inter-process) and die-to-die (intra-process) process variation, the determination of these parameters for every single FE-I3 readout chip is essential. Wafer-to-wafer process variation is the natural occurring of variation of parameters during the processing of wafers. Die-to-die process variation is the variation on wafer level.

[2]During the measurements only C_{lo} is used as this is the standard injection capacitance for the FE-I3.

Not only the wafer processing affects all three parameters. Even though, the FE-I3 is designed to be radiation hard, damage received from irradiation with ionizing and none-ionizing particles can have a small influence on V_{cal}, C_{hi} and C_{lo}.

5.4.1 Measurement of V_{cal}

The injection potential V_{cal} is generated by a 10-bit current DAC (referred to as VCAL DAC, global register [144:153]). The output current of the DAC (approximately 0.5 µA/DAC) is converted to a potential using a resistor and a cascoded current mirror to keep the output current constant independent of the load. At the MonVCal pad (diodes to AGND and VDDA) it is possible to directly measure the voltage step V_{cal} at the resistor mentioned above. For that purpose, global register [74] has to be enabled to redirect the output voltage V_{cal} to the MonVCal pad of the FE-I3 (instead to the VCAL input in figure 5.2). To obtain the characteristic curve of the VCAL DAC, the measured potential V_{cal} has to be plotted against the 10-bit VCAL DAC value:

$$V_{\mathrm{cal}} = a\,\mathrm{DAC}_{\mathrm{VCAL}}\,, \tag{5.2}$$

where the slope a (in mV/DAC) of the characteristic curve is now used to calculate the chare which is injected into the preamplifier. To calculate the number of electrons N_{e}, following formula holds:

$$\begin{aligned} N_{\mathrm{e}} &= (C_{\mathrm{inj}}\,V_{\mathrm{cal}})/\mathrm{e}\,, & (5.3)\\ &= (C_{\mathrm{inj}}\,a\,\mathrm{DAC}_{\mathrm{VCAL}})/\mathrm{e}\,, & (5.4) \end{aligned}$$

where C_{inj} is the injection capacitance, $\mathrm{DAC}_{\mathrm{VCAL}}$ is the VCAL DAC setting, e the elementary charge, and a is the slope of the characteristic curve of the VCAL DAC.

A comparison with an external injection circuit was performed (TurboDAQ) to determine the characteristic of the VCAL DAC, but without clear results. In general, the error on the injected charge can be estimated to be about 10% [42, 18, 32]. This error seems to be reasonable due to the error on the injection capacitance and the error on the measured parameter a [43].

5.4.2 Measurement of C_{hi} and C_{lo}

To measure the injection capacitance C_{hi} and C_{lo}, the FE-I3 has a dedicated on-die capacitance measurement structure. The measurement circuit makes use of the charge-pump capacitor measurement technique as described in [12] and [44]. This test structure consists of 16 different test capacitors, whereas eight of them are used to measure C_{hi} and C_{lo}. In particular, the test capacitors are a multiplicity $n = 0$, 1, 2 and 4 of either the high injection capacitance ($C_{\mathrm{hi}} + C_{\mathrm{lo}}$) or the low injection capacitance (C_{lo}). The charge-pump capacitor measurement technique makes also use of different clock periods $1/f$, in which the capacitor is once charged and then discharged. Possible frequencies are $f = 10\,\mathrm{MHz}$, 5 MHz, 2.5 MHz and 1.25 MHz. The injection capacitance is calculated by

$$C_{\mathrm{test}} = \frac{I_{\mathrm{CapMeas}}}{V_{\mathrm{CapMeas}} \cdot f}\,, \tag{5.5}$$

where C_{test} is the capacitance equal to $n \cdot (C_{\text{hi}} + C_{\text{lo}})$ or $n \cdot C_{\text{lo}}$, f is the frequency of the charging/discharging circuit, V_{CapMeas} is the potential applied to the CapMeas pad (usually 2 V, diodes to DGND[3] and VDD) and I_{CapMeas} is the measured mean current. The multiplicity n and the charge/discharge frequency f can be set by global register [67:64] and [69:67], respectively. The nominal value for the low injection capacitance C_{lo} is 8 fF and for high injection capacitance $(C_{\text{hi}} + C_{\text{lo}})$ is 40 fF.

The measurement results of the test capacitor deviates by about 10% each successive measurement. Also an error in the capacitance over the entire FE-I3 readout chip has to be considered, though it is not possible to measure the absolute values for each pixel.

5.5 Tuning of the FE-I3

Tuning of the FE-I3 means the calibration of the analog part of every readout channel on the FE-I3 readout chip. In other words, registers need to be adjusted in such a way that the preamplifier and discriminator of each pixel on the FE-I3 readout chip operate in a limited range.

The tuning starts with a standard setup as given in Appendix A. The standard tuning has a typical target threshold of 4000 e^- and aims for a gain of 60 bunch crossings[4] (BC) Time-over-Threshold[5] (ToT) at charge collection of 20,000 e^- (colloquially referred to as "60 ToT at 20,000 e^-"). The charge of 20,000 e^- is to be expected for a minimum ionizing particle (MIP) passing through bulk silicon of 250 µm thickness.

The standard tuning as described above is not sufficient for lab characterization. The following points were changed compared to the standard tuning:

1. The threshold was lowered to 3200 e^-. Apart from the fact that this threshold was chosen for former laboratory measurements and was used during test beam, there are several reasons for choosing a lower threshold: first, the threshold can be lowered to that value because there is no influence of large detector system on the electronics of the device under test (this includes effects on noise and threshold dispersion). Second, for sensor characterization it is necessary to measure as much generated charge as possible. The lower the threshold, the more pixels see a hit (increased hit probability). In case of charge sharing between adjacent pixels the additional measured charge can be assigned to the seed pixel (higher charge collecting efficiency). Third, the threshold of 3200 e^- is a compromise between charge collection efficiency and noise occupancy (also referred to as noise hit rate, see [8]). As shown in [34], in case of unirradiated 3D sensors, noise occupancy starts rising significantly from a threshold of approximately 3200 e^- and lower on.

[3] DGND is connected to AGND if jumper SJ16 of the Single Chip Card is closed.

[4] The bunch crossing (BC) rate at LHC is 40 MHz and corresponds to a time of 25 ns.

[5] The discriminator asserts a hit signal if the signal from the second amplifier is over a certain threshold. The length of the hit signal is proportional to the amount of collected charge. The digital readout electronics generates a leading edge (LE) and trailing edge (TE) flag out of the hit signal. LE and TE are sent to the column arbitration unit (CAU) where the time between LE and TE is calculate by a 8-bit counter which is incremented every 25 ns (40 MHz). This time is called Time-over-Threshold (ToT) and is proportional to the collected charge.

2. The tuning was changed to a gain of 30 ToT at a collected charge of $10,000\,e^-$. This tuning is comparable to the standard tuning (60 ToT at $20,000\,e^-$) but for the ToT distribution a higher precision[6] can be achieved for shorter ToT which is the case for irradiated detectors. The generated charge for a MIP passing through a highly irradiated sensor material is expected to be between $15\,ke^-$ and $19\,ke^-$ (250 µm bulk silicon, 1 MeV neutron equivalent fluence of $1 \times 10^{15} cm^{-2}$) caused by charge trapping [6]. The charge seen per pixel is reduced even more due to charge sharing between adjacent pixels n[8]. Setting the tuning values of the ToT Calibration close to the expected charge is important to achieve high precision measurement results (see also section 5.9.1 and 5.9.3).

During the tuning process the threshold of the discriminator and the feedback current of the preamplifier of each pixel get adjusted. The threshold is controlled by the GDAC global register and the TDAC pixel register. For tuning the ToT response, the feedback current of the preamplifier can be adjusted by changing the IFDAC global register, the FDAC pixel register and the TrimIF global register. Changing the global register has an influence on the entire FE-I3 readout chip (coarse tuning), while the pixel register determines the behavior of a single pixel (fine tuning).

GDAC The GDAC is a 5-bit global DAC (global register [227:223], often referred to as GlobalTDAC) controlling the threshold of the discriminator for every pixel (coarse tuning of the threshold). It covers a threshold range of 0–$5000\,e^-$. The standard value for GDAC is 16 and targets a mean threshold of $4000\,e^-$ if all TDAC pixel registers are set to 64. To reflect the lower target threshold of $3200\,e^-$, which is used during characterization, the GDAC was manually set to 13. This will result in a TDAC mean value close to 64 (in the middle of the TDAC range, see figure 5.3).

TDAC The TDAC is a 7-bit pixel register that determines the threshold of each pixel (fine tuning of the threshold). Within the range of 40 to 100, the TDAC DAC is linear and thus the threshold which depends on it [45]. The GDAC must be set manually to a reasonable value, so that the TDAC mean value (after tuning) is in the middle of its range (see figure 5.3). The TDAC tuning works as follows: for each pixel, a Threshold Scans is performed at different TDAC settings. The appropriate TDAC value is derived from the measured thresholds (linear regression).

IFDAC The IFDAC is an 8-bit global DAC (global register [132:125]) controlling the feedback current of the preamplifier of every pixel (coarse tuning of the feedback current). Changing the IFDAC changes the collected ToT-to-charge calibration. The standard value is 32 and targets a charge of approximately $20,000\,e^-$ that is expected for a MIP (TrimIF is set to 16). To obtain a gain of 30 ToT at a collected charge of $10,000\,e^-$ the IFDAC must be manually set to a value equal or below 16. Setting the IFDAC to an appropriate value is of great importance for the FDAC tuning because of the limited range that is covered by the FDAC.

[6] This is due to the fact that the ToT-to-charge calibration is only linear in the first order (see section 5.9.1).

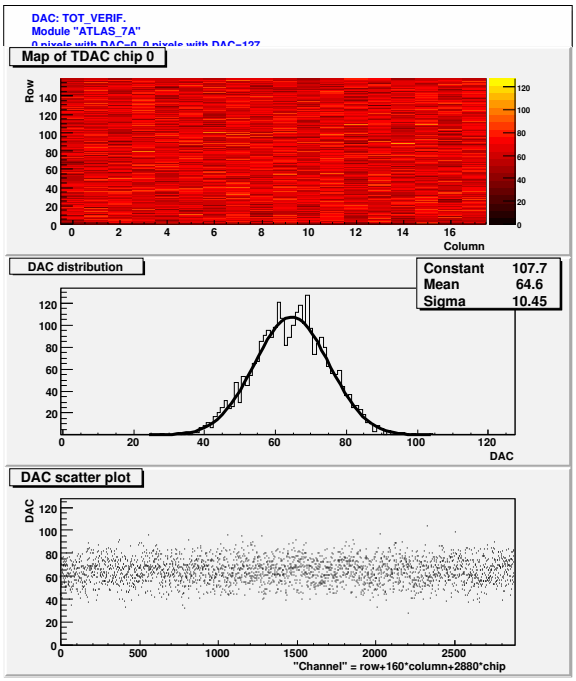


Figure 5.3: TDAC distribution after fine tuning.

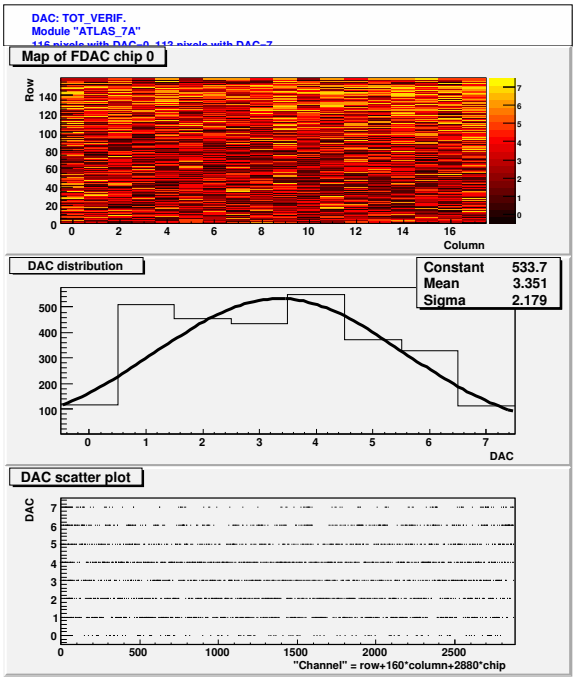


Figure 5.4: FDAC distribution after fine tuning.

FDAC The FDAC is a 3-bit pixel register that configures the feedback current of the preamplifier of each pixel (fine tuning of the feedback current). IFDAC and TrimIF must be set in that way that the FDAC mean value is in the middle of the FDAC range and that the minimum possible value (0) and the maximum possible value (7) is applied to a limited amount of pixels (approximately 50). Changing the FDAC also results in a change of the threshold. As it is the case with the TDAC tuning, the FDAC tuning is done by an automatic tuning algorithm.

TrimIF The TrimIF is a global 8-bit DAC (global register [143:136], often referred to as ITrimIf) that changes the step size of the FDAC, measured in mA/DAC. TrimIF must be manually configured in that way, that the limited range of the FDAC is fully covered (see figure 5.4). Changing the TrimIF involves a change of the IFDAC.

The entire tuning process is an iterational process that comprises several manual steps to find appropriate values for the IFDAC and TrimIF. The last step is always a combination of a TDAC tuning, FDAC tuning and TDAC tuning. This is because of the influence of the feedback current on the threshold.

After finishing the tuning, the threshold of each pixel is verified by running a Threshold Scan (see next section). The threshold and noise are calculated for every single pixel. Also the mean value of the threshold distribution and the width of the threshold distribution (σ_{thr}) of all pixels are calculated. A successful tuning results in a mean value only a few electrons away from the target threshold and has a σ_{thr} below $40\,\mathrm{e}^{-}$. The ToT-to-charge calibration of each pixel is verified using a ToT Verification Scan that measures the ToT distribution for a given amount of charge. For that purpose, the ToT Verification Scan injects a constant amount of charge into every preamplifier. The amount of charge is determined by the tuning parameters, e. g. 30 ToT at a collected charge of $10,000\,\mathrm{e}^{-}$. Knowing the characteristic of the VCAL DAC (mV/DAC), a VCAL DAC value is calculated (mV/DAC) according to formula 5.1. The injection is repeated 200 times for every pixel to get the ToT distribution with high statistics. Also here, the mean value of the ToT distribution and the width of the ToT distribution (σ_{ToT}) of the entire pixel matrix are calculated. Typical values for the mean value are less than 0.5 ToT away from the target ToT and σ_{ToT} is equal or less than 1 ToT. The accuracy of the ToT response is limited by the accuracy of the DACs (e. g. VCAL DAC) and is caused by variation of the injection capacitance over the pixel matrix. The uniformity of the ToT response can only be achieved for a fixed amount of charge which is determined by the tuning parameters. See section 5.8 for more details.

5.6 Threshold Scan and Noise Measurements

The Threshold Scan plays an important role, first, to verify the threshold tuning of each pixel, and second, to measure the noise of every readout channel. Additionally, for the entire pixel matrix, a histogram of threshold distribution is generated to calculate the mean threshold and the width of the threshold distribution. Both values are used to verify the overall performance of the tuning and the detector in general.

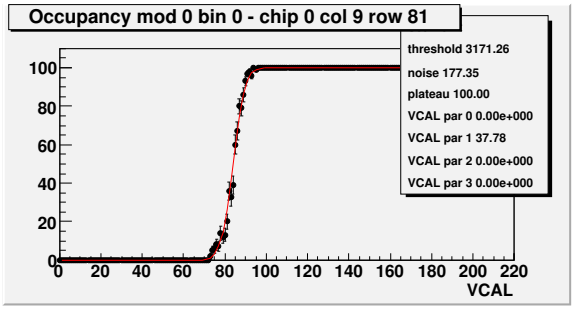


Figure 5.5: The S-curve of a single pixel. Increasing the VCAL DAC lead to a decreased threshold and thus higher hit probability.

The standard Threshold Tuning works as follow: a specified amount of charge, corresponding to the VCAL DAC setting, is injected into the preamplifier (as described in section 5.4). The charge injection is repeated 100 times for each scan step and each pixel to gain high statistics. The hit information (hit counter, which is increased by one if the discriminator asserts the hit signal) is stored in the SRAM. The next scan step, the VCAL DAC value is increased by one, which decreases the threshold, and the process is repeated. By plotting the hit counter versus the VCAL DAC value an S-curve (see figure 5.5) is obtained for reasons described in the next paragraph.

The Threshold is defined as the number of collected electrons that are needed to make the signal of the preamplifier high enough, so that the discriminator asserts the hit signal. Ideally, a Heaviside step function Θ can be used to describe this behavior:

$$P_{\text{hit}}(Q_{\text{inj}}) = \Theta_{\text{hit}}(Q_{\text{inj}} - Q_{\text{thr}}) \tag{5.6a}$$

$$= \begin{cases} 0 & Q_{\text{inj}} < Q_{\text{thr}} \\ 1 & Q_{\text{inj}} \geq Q_{\text{thr}} \end{cases}, \tag{5.6b}$$

where P_{hit} is the probability to see a hit, Q_{thr} the charge that is needed to reach the threshold and Q_{inj} the collected charge by the preamplifier.

But in reality, noise effects have to take into account. Three main sources of noise contributes to overall noise, wherein the ratio depends on the operating conditions:

1. Thermal and flicker (1/f) noise from the preamplifier input transistor (PMOS).
2. Thermal noise from the preamplifier feedback transistor.
3. Shot noise from the sensor leakage current.

The latter noise source is of grater interest because it depends on the sensor type and the reverse-biasing voltage of the sensor. Altogether, the noise leads to a smearing-out effect of the step function and we obtain an S-curve as mentioned above.

It is possible that collected charge slightly below the threshold can trigger a hit and slightly above can trigger no hit. Therefore, to overcome this uncertainty, the threshold is defined as the amount of charge that leads to a hit

probability of 50%. Mathematically, the probability P_{hit} is given by convoluting the Heaviside step function Θ with a normal (or Gaussian) distribution:

$$P_{\mathrm{hit}}(Q_{\mathrm{inj}}) = \Theta_{\mathrm{hit}}(Q_{\mathrm{inj}} - Q_{\mathrm{thr}}) \otimes \exp\left(-\frac{Q_{\mathrm{inj}}^2}{2\sigma_{\mathrm{noise}}^2}\right) \tag{5.7a}$$

$$= \frac{1}{2}\mathrm{erfc}\left(\frac{Q_{\mathrm{thr}} - Q_{\mathrm{inj}}}{\sqrt{2}\sigma_{\mathrm{noise}}}\right). \tag{5.7b}$$

The solution of the convolution is a complementary error function $\mathrm{erfc}(x) = (2/\sqrt{\pi})\int_x^\infty \exp(-t^2)dt$, where σ_{noise} is the equivalent noise charge[7] [46]. σ_{noise} is proportional to the slope of the S-curve at $P_{\mathrm{hit}} = 50\%$ and is typically in the order of $160\,\mathrm{e}^-$ (for planar sensors and for a pixel size of $50 \times 400\,\mu\mathrm{m}^2$). The threshold setting should be well above the overall noise to avoid fake hits due to noise.

By plotting the threshold histogram, the mean threshold and threshold dispersion σ_{thr} (root mean square, RMS) can be obtained assuming a normal distribution. The threshold dispersion of an untuned FE-I3 readout chip is about $600\,\mathrm{e}^-$ and for a tuned chip it is less than $40\,\mathrm{e}^-$. The dispersion of the pixel-to-pixel threshold has a similar effect as noise, but it can be treated as a time-independent noise source [11]. The contribution to overall noise can be neglected in the case of a tuned chip.

Neither the threshold dispersion nor the noise depends on the target threshold [6]. But both are characteristic for the sensor type attached to the FE-I3 readout chip. In case of the noise there is also dependence on the reverse-biasing of the sensor (see next chapter).

5.7 Bias Scan Setup

The purpose of the bias scan is to measure the leakage current of the entire pixel matrix and pixel-wise (MONLEAK), noise, threshold, threshold dispersion and crosstalk depending on the reverse-biasing voltage applied to the sensor.

The measurement was done using the Primitive List (often referred to as Prim List) functionality that is implemented in STcontrol. A Primitive List is a list of scans (e. g. Threshold Scan) and actions (e. g. setting the voltage, waiting for a given amount of time) that defines the procedure of the scan. Items in the Primitive List are processed in a sequence. The Primitive List used for the bias scan contains following steps:

1. Setting the reverse-biasing voltage
2. Waiting 5 (30) minutes
3. MONLEAK Scan
4. Configuring the readout chip
5. Waiting 1 minute

[7] In High Energy Physics applications, the equivalent noise charge (ENC) is a convenient way to express the noise-to-signal ratio of a charge sensitive amplifier and is given by the ratio of root mean square (RMS) noise voltage V_{RMS} to the signal pulse height $V_{\mathrm{max}}(q_{\mathrm{e}})$ for a charge signal of a single electron: $\mathrm{ENC} = V_{\mathrm{RMS}}/V_{\mathrm{max}}(q_{\mathrm{e}})$.

Figure 5.6: Source scan setup: The Single Chip Card (SCC) is mounted on an acrylic board. Above the SCC is the metal collimator with acrylic core, below the plastic scintillator. The signal output of the scintillator is connected to the trigger logic unit (TLU, not shown).

6. Measuring the leakage current
7. Threshold Scan
8. Crosstalk Scan

All steps listed above are repeated every bias voltage step. After setting the reverse-biasing voltage, a waiting time of 5 minutes was added to stabilize the leakage current. In case of irradiated sensors, the waiting time was increased to 30 minutes. The waiting time before measuring the leakage current is to dissipate heat from the sensor that was accumulated by the MONLEAK Scan. Before reading out the leakage current the readout chip is configured (writing pixel and global register data as stored in the tuning file). Global and pixel register (especially pixel masks), which were changed by previous scans, can have an influence on the leakage current.

5.8 Source Scan Setup

The aim of the Source Scan is the characterization of the sensor using high-energy particles. The Source Scan in the laboratory provides a first impression of the overall performance of the sensor. Of greater interest is the charge collection efficiency (charge collecting distance) and the amount of charge sharing between adjacent pixels.

High energy β^--particles can penetrate the entire thickness of the detector. By placing the β^--source on the one side and a scintillation detector on the other side of the detector, β^--particles can be used to generate a trigger signal. Assuming MIPs, a homogeneous charge distribution throughout the entire thickness of the sensor can be achieved. By using the Landau theory (see section 3.4.1), it is possible to calculate the amount of deposited charge.

The beam of β^--particles, which is coming from a ^{90}Sr source (12 MBq flood source), is perpendicular to the detector surface. The detector is placed so

that the particles first impinge the sensor. The particle beam is collimated to a beam diameter of 1 mm. The collimator was placed so that the beam spot is in the middle of the pixel matrix. A plastic scintillator (Sc) attached to a photomultiplier tube (PMT) is placed on the side faced away from the source. The PMT output is connected to the TLU (see section 4.7) which processes the trigger signal and communicates with the USBpix board (trigger data handshake).

Also for this scan a Primitive List was set up:

1. Setting the reverse-biasing voltage
2. Waiting 5 (30) minutes
3. Source Scan
4. Configuring the readout chip
5. Waiting 1 minute
6. Measuring the leakage current
7. Threshold Scan

The same principles apply as described in the former section. The measurement of the leakage current and the Threshold Scan are for verification purposes. The Source Scan was set up to take 500,000 external triggers. The raw data was stored to TurboDAQ-compatible output files (as described in section 4.4.3). The threshold of the discriminator, which is built into the trigger logic unit, was set to 150 mV, so that almost all noise hits coming from the PMT are suppressed. This results in an effective trigger rate[8] of approximately 500 Hz (limited by the TLU[9]). The total length of LV1 trigger was set to 16 bunch crossings (16 consecutive triggers à 25 ns) and the delay of the LV1 trigger is set so that first hit data approximately belongs to the third consecutive LV1 trigger (see figure 5.7). Several pixel rows and columns were disabled during the Source Scan: column 0 and 17 (long pixels), row 153 to 159 (ganged and inter-ganged pixels), row 152 (also shows a higher noise induced by its neighbours) and row 0 to 7 (in case of 3D sensors they show unpredictable behavior) were always disabled. In addition to that, any pixel with high noise or high hit occupancy was disabled.

5.9 Analysis of the Raw Data

The analysis of the raw data taken during the Source Scan (see former section) is important for the characterization of the sensor. During the analysis, the raw data undergoes several steps:

1. Clustering of hits[10] from the same particle.

[8] Effective trigger rate means accepted and processed triggers. This includes receiving raw data from FE-I3 and writing the raw data to the SRAM.

[9] An upper limit for the effective trigger rate of USBpix can be calculated: $40\,\mathrm{Mbit/s}/(255\,\mathrm{bit} + 17 \cdot 26\,\mathrm{bit}) \approx 57\,\mathrm{kHz}$

[10] A hit is understood as any kind of single pixel hit, so that the collected charge is over the threshold. An event comprises all single pixel hits that are triggered by the same incident particle. In this case the charge is shared between the pixels.

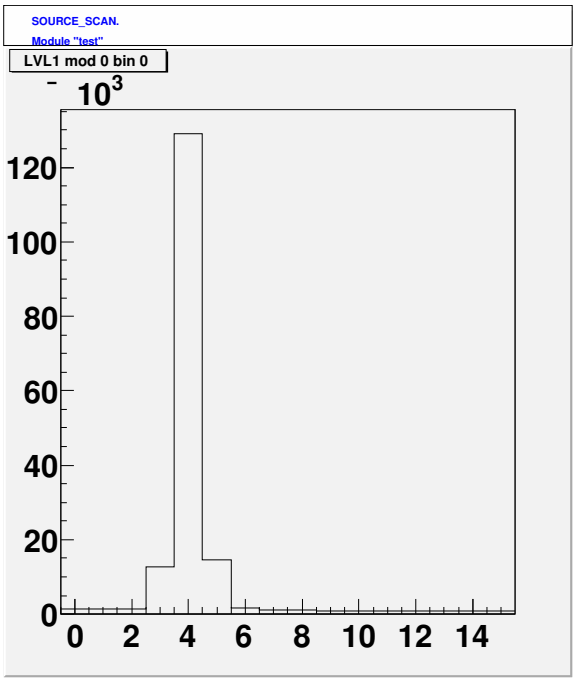


Figure 5.7: LV1 histogram: hit counter plotted against bunch crossing number. Increasing the LV1 delay would move the peak to the left. Care has to be taken that the peak is inside readout time frame. Otherwise the hit data, which corresponds to the trigger signal, would not be read out. Noise hits show up outside the peak.

2. Conversion of (clustered) Time-over-Threshold to charge (ToT-to-charge conversion).

3. Analysis of the clustered hit data and generation of the histograms.

The analysis software[11] was developed in cooperation with CERN[12]. It is written in C++ and is using ROOT macros which are executed in the ROOT C interpreter (CINT). The analysis software splits into two parts: first, a ROOT macro analyzes the raw data file and saves the clustered hit information to a ROOT container file (first step, see section 5.9.2). A second ROOT macro that reads in the clustered hit data and the ToT calibration data converts ToT into charge and generates the histograms (latter two steps, see section 5.9.3).

5.9.1 ToT Calibration

After the tuning of the pixel mask and before starting the Source Scans, a ToT Calibration Scan was performed. The ToT Calibration measures the ToT response of each pixel to a wide range of electric charge injected into the preamplifier. This is in contrast to the ToT Verification Scan, where only a fixed amount of charge, given by the tuning parameters, is injected (see section 5.5). Even though the ToT response for a given charge has been adjusted by the FDAC tuning and is uniform over the entire pixel matrix (e. g. 30 ToT at a collected charge of $10,000\,\mathrm{e^-}$), there are still differences in the ToT response. The pixel-to-pixel differences in ToT increases the more the charge deviates from the value determined by the tuning parameter. Therefore, it is sufficient to measure over a wide range the relationship between injected charge and the correlating ToT response for each pixel.

The empirical [42] ToT calibration function[13] is

$$\mathrm{ToT}(N_\mathrm{e}) = A\left(\frac{N_\mathrm{e}+B}{N_\mathrm{e}+C}\right), \tag{5.8}$$

where ToT is the response in units of bunch crossings, N_e the number of injected electrons. The parameters A, B and C are fit parameters and are unique for each pixel. The fit parameters are strongly correlated [43]. For each fit parameter A, B or C, the data for the entire pixel matrix is stored in a ROOT macro and is later used for the ToT-to-charge calibration (see section 5.9.3).

5.9.2 Charge Sharing and Clustering

A particle, which passes the sensor, generates charge along its path. The charge can be shared between neighboring pixel cells (so called charge sharing) for the following reasons:

1. The point of impact is located at the border between two or more pixel cells.

2. A δ-electron deposit energy along its path inside the sensor.

[11] Source code as of December 8, 2010.
[12] Christian Gallrapp, CERN, PH & DT Department, CH-1211, Genève 23, Switzerland.
[13] Also used in the current ATLAS DAQ firmware.

3. The incident angle of the particle is not perpendicular to the sensor surface so that the particle passes several pixel cells.

The latter can be excluded due to the construction of the source scan setup. In case of charge sharing between adjacent pixel cells, the resulting cluster is most likely composed of a high-charge hit (seed pixel) and one or more low-charge hits. But it cannot be precluded that the collected charge in the low-charge hits is below the threshold and therefore is not recognized at all.

Another effect, which has influence on the clustering, is the timewalk effect. The timewalk effect is related to the rise time of the preamplifier. The timewalk effect is the dependence of the time, that the preamplifier output signal needs to cross the discriminator threshold, on the maximum pulse height of the preamplifier output signal. In other words, the recognition time of a hit and the assignment to a bunch crossing interval depends on the collected charge of the preamplifier. To assign as many hits that were induced by the same particle as possible to the corresponding bunch crossing interval, it is necessary to adjust the phase of the 40 MHz clock (XCK) with respect to the bunch crossing. This is of great importance for the operation at the LHC, where only hits associated to a single LV1 trigger (within 25 ns) are read out. The loss of the low-charge hits, which are affected by the timewalk effect if the clock phase is adjusted correctly, prevents the usage of charge interpolation to improve the single point resolution [47]. To recover these hits, a timewalk correction is implemented in the FE-I3 electronics (global register [219:220]). For hits with a ToT less than or equal to a certain threshold (ThrDub, global register [211:218]), the hit is sent twice to the end of column (EOC) buffer: one with the original LE time stamp information and another assigned to the previous bunch crossing (LE time stamp subtracted by one). Another mode allows the rejection of all hits with a ToT below a certain threshold (ThrMin, global register [203:210]). It is possible to operate both modes at the same time.

However, the automatic correction is inappropriate for laboratory characterization (and in most cases for beam tests) where particles crossing the sensor have a random phase with respect to the XCK. The timewalk effect therefore is not limited to a certain input signal charge.

The task of the clustering algorithm is to cluster hit information, which is distributed in space and *time*, to restore the total charge that was generated by a crossing particle. It has to be emphasized that for a laboratory characterization, the total amount of charge is of interest, whereas in HEP experiments the single point resolution is of greater interest (which also takes advantage of the ToT).

5.9.3 Analysis and Histogramming

According to formula 5.8, the collected charge that corresponds to a distinct ToT is

$$N_{\mathrm{e}}(\mathrm{ToT}) = \frac{AB - C\,\mathrm{ToT}}{\mathrm{ToT} - A}\,. \tag{5.9}$$

By definition, a ToT of 1 corresponds to threshold charge defined by the tuning parameter, i. e. $N_{\mathrm{e}} = 3200\,\mathrm{e}^{-}$. By entering the parameters A, B, and C for every single pixel into equation 5.9, one can calculate the collected charge. By entering ToT = 1 in the formula, the calculated result deviates by about 30 % of the expected charge of $3200\,\mathrm{e}^{-}$. At a ToT of 30 the results deviate by about 1 %

from the expected charge of 10000 e^-. Especially for a small amount of charge, the empirical calibration function (equation 5.8) does not reflect the reality very well (e. g. non-linearities of the DACs and amplifiers).

After the ToT-to-charge conversion, the analysis of the clustered hit data is proceeded. The analysis includes the generation of hit maps, hit histograms, cluster size distributions and ToT distributions of different cluster sizes. The most important aspect is the calculation of the most probable value (MPV). The MPV is calculated by fitting a Landau distribution to the ToT distribution. To take noise effects (e.g. electronic noise) into account the Landau distribution is convoluted with a Gaussian ("Langau").

Chapter 6

Sensor Characterization

6.1 Introduction

The different sensor types used for laboratory characterization are listed in table 6.1. The first sensor (3631-303, hereinafter referred to as "ATLAS") is of n^+-on-n-type and is used as a reference sensor. This sensor is taken from the same batch of wafers that was previously used to assemble the ATLAS pixel detector. Two other planar sensors (WR13 and W11) were fabricated by CiS[1]. Both sensors are of n^+-on-p-type. All planar sensors are solder bump bonded to the FE-I3 by IZM[2]. The W11 sensor is mistakenly mounted rotated by 180°. Two more sensors (2EM6 and 4EM9) were contributed by FBK[3]. The sensors make use of 3D technology with n^+-electrodes in p-bulk (2 and 4 electrodes per pixel cell, respectively), and are indium bump bonded to the FE-I3 pixel readout chip by SELEX[4]. They were irradiated with 25 MeV protons to a calculated fluence of $1 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ at the Karlsruhe Irradiation Center[5] in April 2009. Only a limited amount of data is available that was taken before the irradiation so that it could not be used for data analysis.

Company/Institute	Sensor	Technology	Type	FE-I3	Thickness	Fluence
CiS	3631-303 "ATLAS"	planar	n^+-on-n	5-7A	$256 \pm 10\,\mu m$	unirradiated
CiS	W11 19GR-2	planar	n^+-on-p	8-13B	$300 \pm 10\,\mu m$	unirradiated
CiS	WR13 19GR-NM2	planar	n^+-on-p	8-10A	$300 \pm 10\,\mu m$	unirradiated
FBK	2EM6	3D, 2 electrodes	n^+-in-p	n/a	$200 \pm 10\,\mu m$	$1 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$
FBK	4EM9	3D, 4 electrodes	n^+-in-p	n/a	$200 \pm 10\,\mu m$	$1 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$

Table 6.1: Comparison between the different sensor types that were investigated during the laboratory characterization. All sensors types are, among types from other companies, candidates for the ATLAS IBL pixel detector upgrade.

[1]Forschungsinstitut für Mikrosensorik und Photovoltaik GmbH, Konrad-Zuse-Straße 14, D-99099 Erfurt, Germany.

[2]Fraunhofer-Institut für Zuverlässigkeit und Mikrointegration, Gustav-Meyer-Allee 25, D-13355 Berlin, Germany.

[3]Fondazione Bruno Kessler, Via Santa Croce 77, I-38122 Trento, Italy.

[4]Sistemi Integrati S.p.A., Via Tiburtina 12, I-00131 Rome, Italy.

[5]Karlsruher Institut für Technologie, Institut für Experimentelle Kernphysik, Campus Nord, PO Box 36 40, D-76021 Karlsruhe, Germany.

6.2 Unirradiated Planar Sensors

The ATLAS sensor consists of a 256 µm thick oxygenated n-bulk. On the readout side, there are n^+-type pixel implants separated by moderated p-sprays. A p^+-type implant covers almost the entire backside forms a p-n junction. The depletion starts to grow from the backside before type inversion. After irradiation induced type inversion of the bulk the depletion starts to grow from the segmented (or pixel) side and the behavior is similar to unirradiated n^+-on-p detectors. To protect the pixels side of high voltage 16 guard rings are located on the back side [30].

Figure 6.1 shows the layout of a single pixel cell of the WR13 and W11 sensor. The oxygenated substrate is of 300 µm thickness. The sensors are of n^+-on-p-type and the n^+-type pixel implants are separated by p-sprays. The WR13 has moderated and the W11 has homogeneous p-spays. In contrast to the ATLAS sensor the 19 guard rings are on the readout side. To reduce the risk of a spark between sensor and readout chip, the surface is coated by a thin layer of Benzocyclobutene (BCB).

All three sensors are tuned at 20°C and at a reverse bias voltage of 150 V. The results of the tuning process and the tuning parameters are listed in Appendix 5.5.

Due to the mistakenly rotated sensor, not all bump bonds are connected properly. Therefore the W11 detector shows a higher noise in rows 0–3. The pixel of the uppermost two rows (158–159, ganged and inter-ganged pixels) are not connected properly. The pixel 10/112[6] shows a higher threshold but this does not affect the measurements so it stays unmasked.

All three detectors show a comparable tuning performance. A threshold dispersion of approximately 22 e^- was measure for every device. The noise for normal pixels is in case of the n-on-p devices of approximately 190 e^- and for the ATLAS device 180 e^-. The results of the ToT Verification Scans show also comparable performance. A ToT dispersion of about 0.6 ToT was possible (at an injected charge of 20,000 e^-) with all three detectors. The ToT dispersion strongly depends on the preamplifier feedback current. The IFDAC and TrimIF tuning parameters were set manually to find the optimum value.

The ATLAS n-on-n device needs a minimum reverse-bias voltage of 60 V to work properly. The depletion zone grows from the backside and below that voltage the pixels cells are shorted (ohmic n^+-n contact). The pixel cells become isolated once the depletion voltage is exceeded (depletion zone reached the pixel side).

Figure 6.1: Structure of a pixel cell of a CiS n-on-p sensor. The metal layer is shown in pink, the n-type implantation in green, the opening in the nitride and oxide in blue and the opening in the passivation layer in red. The bulk is of p-type [32].

[6] In the following column and row are denoted as column/row.

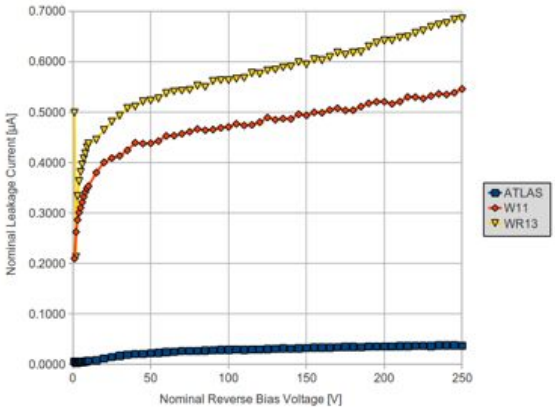


Figure 6.2: Leakage currents of the planar devices at 20°C.

6.2.1 Results of the Bias Scan

Leakage Current Figure 6.2 shows the leakage current of the planar pixel sensors. At 250 V the leakage current is below 0.04 µA for the ATLAS device. At the same bias voltage, the W11 and WR13 devices have a 15 (0.55 µA) and 18 (0.69 µA) times higher leakage current.

Threshold and Noise Figure 6.3 shows the mean noise for the normal, long, ganged and interganged pixels depending on the reverse bias voltage. In case of the W11 device the ganged and interganged cannot be plotted due to the reasons stated above. The noise drops constantly with increasing the reverse bias voltage. For voltages below the depletion voltage the noise increases rapidly due to the increased detector capacitance. At 250 V the mean noise for normal pixels is 167 e^- for the ATLAS device, 186 e^- for the W11 device and 183 e^- for the W11 device. Both n-on-p devices behave very much the same. Clearly visible is a step in the noise for the long pixels for both n-on-p devices which is most likely a geometric effect of the electric field in this region of the sensor.

6.2.2 Results of the Source Scan

Figure 6.4 shows the most probable value (MPV) for different pixel cluster sizes depending on the reverse-bias voltage. The ATLAS device almost reaches maximum charge collection close to the depletion voltage (60 V). Both n-on-p devices are fully depleted at approximately 50 V. Below depletion voltage the charge collection decreases rapidly. Above depletion voltage the charge collection stays almost constant.

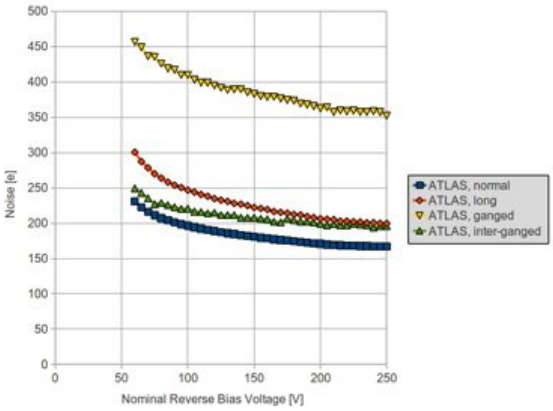
Table 6.2 summarizes the results of the Source Scans. The maximum possible overall charge collection efficiency is between 76% and 81% whereas the CiS n-on-p devices show a slightly better performance.

For the MPV an error of 10% is estimated (not drawn), due to the uncertainties of the ToT Calibration (see section 5.9.3). Another source of uncertainty arises from the fact the charge below the threshold of pixels in a cluster cannot be detected. In case of charge sharing between adjacent pixel cells it can happen

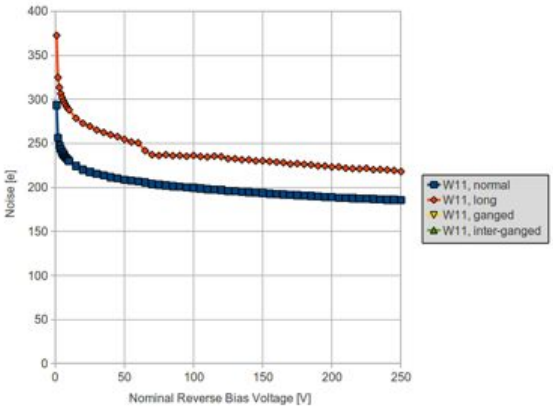
Sensor	3631-303 “ATLAS	W11 19GR-2	WR13 19GR-NM2
Calculated MPV [e^-]	19654 ± 817	23266 ± 825	23266 ± 825
Measured MPV [e^-]	14980	18940	18160
$\sum$ Efficiency	76.2%	81.4%	78.1%
1 Pixel Efficiency	74.0%	78.7%	76.0%
2 Pixel Efficiency	79.1%	82.7%	79.4%
3 Pixel Efficiency	88.0%	88.8%	84.8%

Table 6.2: Average charge collection efficiency and cluster size dependent charge collection efficiency of planar devices at 250 V. The most probable value of electron-hole pairs is calculated according to equation 3.3. The error on the calculated MPV is calculated by assuming an error of 10 µm on the bulk thickness. The measured most probable value includes all cluster sizes.

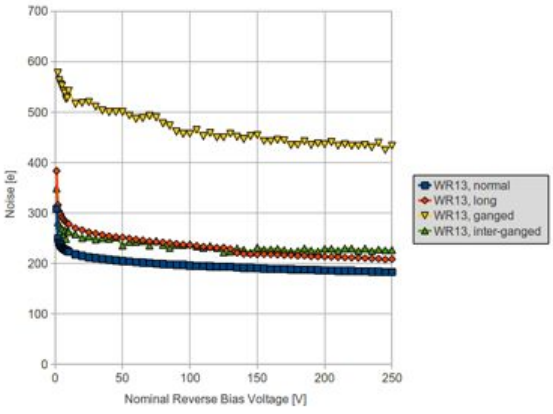
that the charge in one or more pixel cells stays below the threshold and thus is lost. This theory is supported by the fact that the higher the pixel cluster size the higher the charge collection efficiency. The reason for that is the decreased probability of losing charge due to the threshold in bigger pixel cluster sizes. This becomes clearly visible in figure 6.4 where bigger pixel cluster sizes leads to higher efficiency. Almost full charge collection is achieved for 3-pixel cluster as stated in table 6.2.



(a)

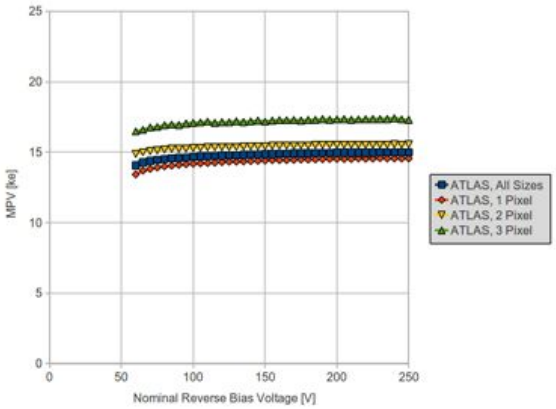


(b)

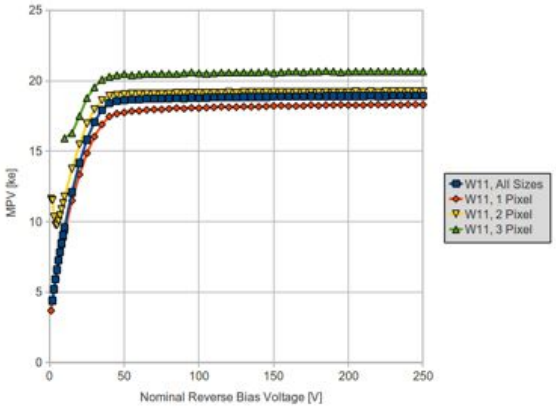


(c)

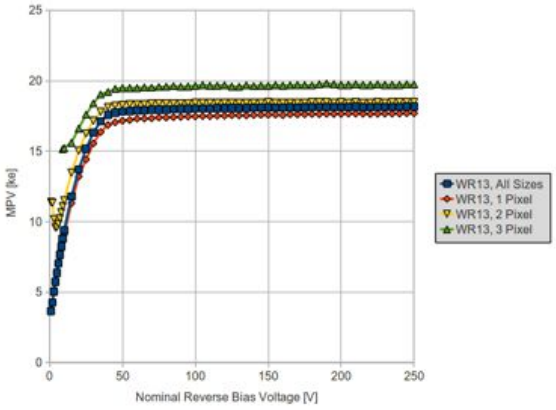
Figure 6.3: Mean noise of the planar devices at 20°C. (a) ATLAS (b) W11 (c) WR13



(a)



(b)



(c)

Figure 6.4: Planar devices: most probable value depending on reverse bias voltage at 20°C. (a) ATLAS (b) W11 (c) WR13

6.3 Irradiated 3D Sensors

The structure of the 3D sensors is shown in 6.5. Both FBK sensors are of double-side double type column (3D-DDTC).

The tuned thresholds have been observed to disperse the faster the higher the temperature. This results also in a shift of the mean threshold to higher values. A periodic retuning is needed. At low temperature, the tuning stays stable during the measurement period (2 days per measurement). A retuning was made after every cooling down. In case of the Source Scan, and to avoid additional heating and cooling cycles, the ^{90}Sr source was placed over the sensors during the tuning. However, the tuning quality is not affected by the radiation of the source.

The results of the tuning for the FBK sensors are listed in Appendix 5.5. Both detectors show a comparable tuning performance. A threshold dispersion of approximately $30\,e^-$ and $27\,e^-$ is measured for the 2EM6 and 4EM9 respectively. The noise for normal pixels is in case of the 2EM6 devices of approximately $233\,e^-$ and for the 4EM9 device $257\,e^-$. A minimal ToT dispersion of about 1 ToT was possible (at charge injection of $20,000\,e^-$). Again, the ToT dispersion strongly depends on the IFDAC and TrimIF setting that were manually tuned.

Once the bias voltage is applied, the highly irradiated detectors show a decrease of the leakage current in time. That is particularly relevant at higher bias voltages. To avoid any instability, the measurement is paused for 30 minutes after each time the bias voltage was increased.

All 3D modules suffer from disconnected bump bonds in the corners. Especially the 4EM9 module is affected. Indium bump bonds are known to become brittle at temperatures of approximately $-50°C$. However, repeated temperature cycling can lead to failure.

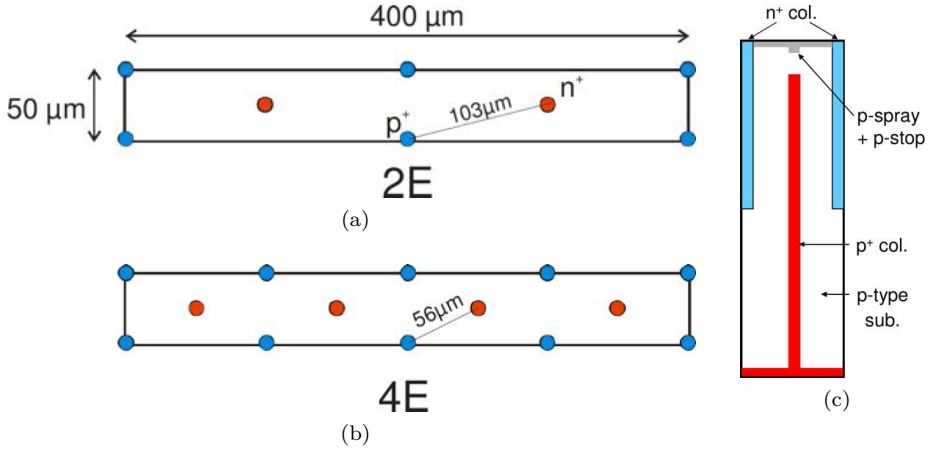


Figure 6.5: Sketch of the electrodes: (a) 2E type and (b) 4E type. (c) Schematic of a 3D device along a plane intersection crossing both types of columns. [48]

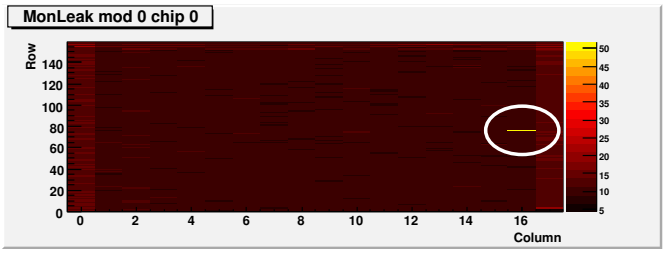
6.3.1 Results of the Bias Scan

Leakage Current Figure 6.7 shows the result of the leakage current measurements for both FBK devices. The leakage current is measured at three different temperatures: −10°C, −20°C and −30°C. The current limit is set to 100 µA to protect the sensors from damage.

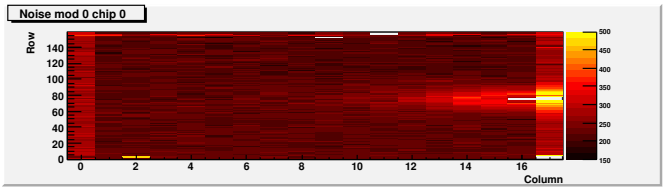
The 2EM6 detector shows an early single-pixel breakdown (see figure 6.6). This pixel suffers from higher leakage current and increased noise. Pixels in the vicinity of that pixel are also affected by the breakdown and show an also increased noise .

Single-pixel breakdowns have also been observed on other 3D devices but is not yet understood [49].

Noise Figure 6.8 shows the mean noise for the normal, long, ganged and interganged pixels depending on the reverse bias voltage. The noise was measured at −10°C. In case of the 2EM6, a step in the noisecurve at 60 V was measured. The step has also been observed on other FBK 3D devices but is not yet understood.



(a)



(b)

Figure 6.6: Single-pixel breakdown of the 2EM6 detector at 106 V. (a) Monleak Scan: The circle denoted the point of origin of the breakdown. (b) The pixels in the vicinity are also affected. They suffer from increased noise.

Sensor	2EM6	4EM9
Calculated MPV [e^-]	15111 ± 805	15111 ± 805
Measured MPV [e^-]	10070	10540
$\sum$ Efficiency	66.6%	69.8%
1 Pixel Efficiency	64.2%	67.4%
2 Pixel Efficiency	73.9%	77.0%
3 Pixel Efficiency	88.4%	99.8%

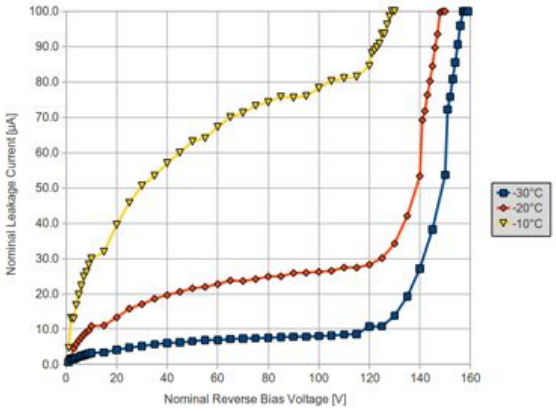
Table 6.3: Average charge collection efficiency and cluster size dependent charge collection efficiency of 3D devices: 2EM6 at 105 V and 4EM9 at65 V. The most probable value of electron-hole pairs is calculated according to equation 3.3. The error on the calculated MPV is calculated by assuming an error of 10 µm on the bulk thickness. The measured most probable value includes all cluster sizes.

6.3.2 Results of the Source Scan

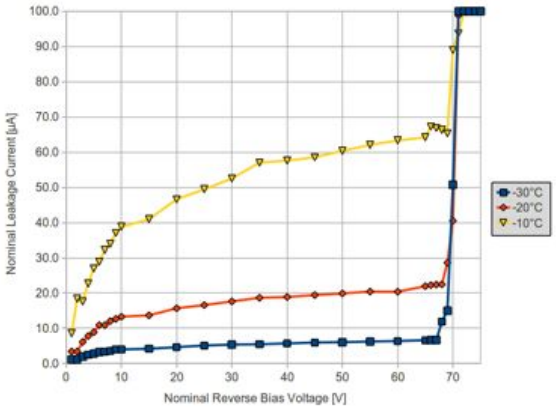
Figure 6.9 shows the results of the Source Scan for the FBK 3D devices at −30°C. This temperature was chosen to reduce disturbing effects of the leakage current (fluctuations at higher temperatures). It is evident that the MPV strongly depends on reverse bias voltage and pixel cluster size. Even at higher voltages the MPV is not constant and still tends to increase for higher voltages. The upper voltage is limited by the breakdown of the sensors which appears at lower bias voltages than suggested in figure 6.7. The breakdown (2EM6 at 106 V, 4EM9 at 66 V) is characterized by an abrupt increase of noise hit rate that is distributed over the whole pixel matrix. The noise hits tend to have a lower ToT (below MPV) but the large amount of noise hits make the analysis impossible.

The unexpected shape of the 3-pixel and 2-pixel at lower bias voltages is an effect of low statistics. There the MPV of the "Langau" distribution tends to shift to higher values.

Table 6.3 shows the charge collection efficiency of the irradiated FBK 3D devices. The overall charge collection efficiency is 67% and 70% for the 2EM6 and 3EM9 device respectively. Again, a bigger pixel cluster size leads to higher charge collection efficiency as stated in section 6.2.2 for planar devices. But the difference between 3-pixel cluster size and all other cluster sizes is more evident: in case of the 4EM9 almost full charge collection efficiency can be achieved. But one has to take into account that the 3D modules were annealed after irradiation. The annealing time can be approximated from 5 to 7 days at room temperature. The modules take advantage of the decreased charge trapping.

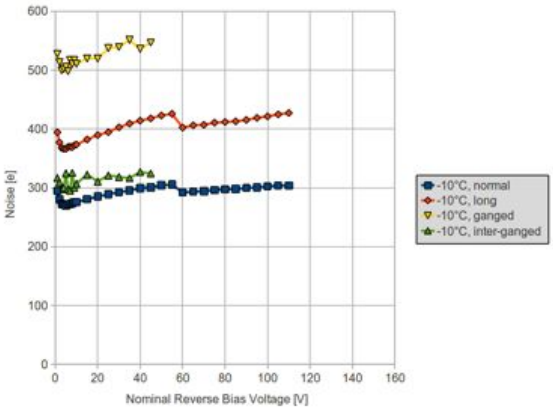


(a)

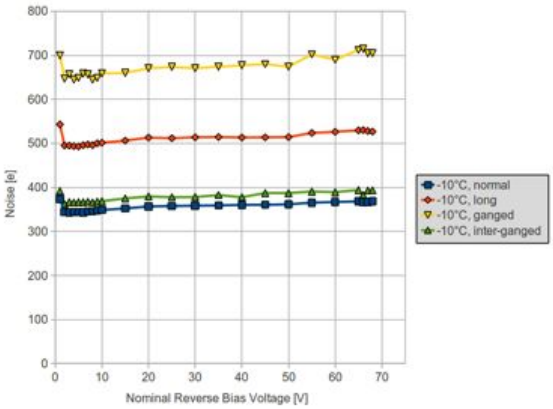


(b)

Figure 6.7: Leakage current of the 3D devices at −10°C, −20°C and −30°C. (a) FBK 2EM6. (b) FBK 4EM9.

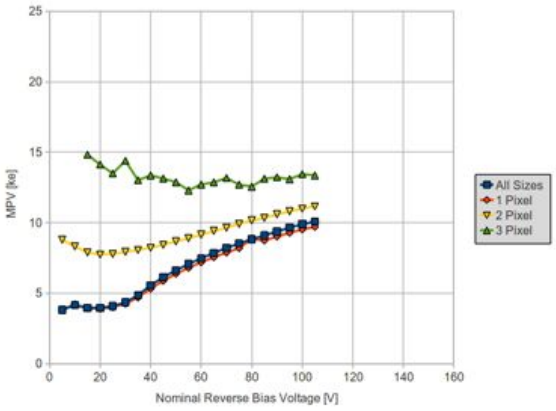


(a)

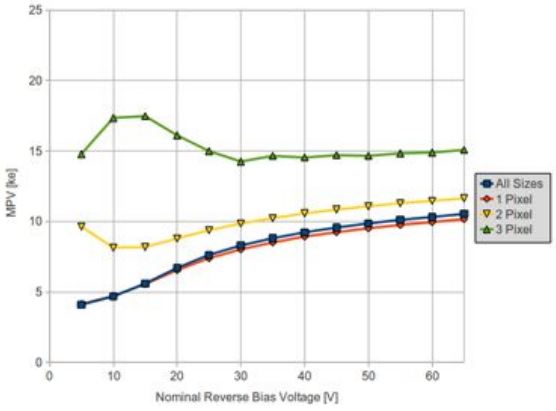


(b)

Figure 6.8: Noise of the 3D devices at −10°C. (a) FBK 2EM6. (b) FBK 4EM9.



(a)



(b)

Figure 6.9: FBK 3D devices: most probable value depending on reverse bias voltage at −30°C. (a) FBK 2EM6. (b) FBK 4EM9.

Chapter 7

Summary and Outlook

A small and lightweight test and readout system was developed for the ATLAS FE-I3 pixel readout chip. In addition, measurements were performed on a new generation of pixel sensors, which are possible candidates for the ATLAS IBL upgrade. High-statistics laboratory characterizations with β radiation and noise studies of the pixel sensors delivered valuable information about charge collection efficiency and noise performance.

USBpix has proved its functionality in laboratory characterizations as well as at beam test at CERN. The integration of USBpix into the JRA1 EUDET beam telescope was a big step closer to a fully integrated test system. Especially data taking at high trigger rates has proved to work reliably so that USBpix will become the successor of TurboDAQ.

Beside the changes that have made to the USBpix test system during this thesis, there is still room left for further improvements. As mentioned earlier, the USB driver needs to be reworked to work with modern Linux-based systems. The seamless integration of USBpix into the EUDET framework is a major milestone in the near future.

Appendix A

FE-I3 Standard Configuration

Name	Value
TDAC	64
FDAC	4
ENHITBUS	off
MASK	off
KILL	off
SELECT	off

Figure A.1: FE-I3 standard pixel configuration.

Name	Value	Name	Value
LATENCY	255	ENABLECOL6	1
SELFTRGDELAY	0	TESTDACITRIMTH	0
SELFTRGWIDTH	0	ITRIMTHDAC	64
ENABLESELFTRG	0	IFDAC	32
ENABLEHITPARITY	0	TESTDACIF	0
SELECTDO	8	ENABLECOL5	1
SELECTMONHIT	1	TESTDACITRIMIF	0
TSITSCENABLE	1	ITRIMIFDAC	16
SELECTDATAPHASE	0	VCALDAC	0
ENABLEEOEPARITY	0	TESTDACVCAL	1
HITBUSSCALER	0	ENABLECOL4	0
MONLEAKADC	0	HITINJECTCAPSEL	0
AREGTRIM	0	ENABLEEXTINJ	0
ENABLEAREGMEAS	0	TESTANALOGREF	0
AREGMEAS	0	EOCMUXCONTROL	0
ENABLEAREG	0	CEUCLOCKCONTROL	3
ENABLELVDSREFMEAS	0	ENABLEDIGITALINJ	0
DREGTRIM	0	ENABLECOL3	1
ENABLEDREGMEAS	0	TESTDACITH1	0
DREGMEAS	0	ITH1DAC	0
CAPMEASCIRCUIT	0	ITH2DAC	0
ENABLECAPTEST	0	TESTDACITH2	0
ENABLEANALOGOUT	0	ENABLECOL2	1
TESTPIXELMUX	2	TESTDACIL	0
ENABLEVCALMEAS	0	ILDAC	64
ENABLELEAKMEAS	0	IL2DAC	64
ENABLEBUFFERBOOST	0	TESTDACIL2	0
ENABLECOL8	1	ENABLECOL1	1
TESTDACIVDD2	0	THRMIN	0
IVDD2DAC	64	THRDUB	0
IDDAC	64	READMODE	0
TESTDACID	0	ENABLECOL0	1
ENABLECOL7	1	HITBUSENABLE	1
TESTDACIP2	0	GLOBALTDAC	14
IP2DAC	64	ENABLETUNE	0
IPDAC	64	ENABLEBIASCOMP	1
TESTDACIP	0	ENABLEIPMONITOR	0

Table A.1: FE-I3 standard global configuration.

Appendix B

FPGA Configuration Registers for Source Scan/EUDET

`CS_READOUT_MODE` 2-bit register. 2'b11: source scan mode.

`CS_TRIGGER_MODE` 2-bit register. 2'b01: no-handshake mode; 2'b10: simple handshake mode; 2'b11: trigger data handshake mode.

`CS_COUNTER_MODE` 2-bit register. 2'b00: triggers; 2'b01: hit words; 2'b10: EoE words.

`CS_NUMBER_OF_EVENTS` 32-bit register. Set up the maximum number of events (triggers, hit words or EoE words). After the desired number of events is reached, the measurement stops automatically.

`CS_MEASUREMENT_START_STOP` 1-bit register. If asserted, the measurement starts. If de-asserted, the measurement stops.

`CS_MEASUREMENT_PAUSE_RESUME` 1-bit register. If asserted, the measurement stops without resetting the counters. If de-asserted, the measurement continues.

`CS_ENABLE_RJ45` 1-bit register. If enabled, the RJ45 port must be used to connect the S3Multi-IO-Board to the TLU.

`CS_XCK_PHASE` 1-bit register. If enabled, the XCK phase is shifted by 180°.

`CS_DISABLE_EOE_WORD_COUNTER` 1-bit register. If enabled, directly accept new trigger after all EoE words arrived. If disabled, wait for data as in `CS_LENGTH_TOTAL` specified.

`CS_LENGTH_TOTAL` 16-bit register. Maximum waiting time (in units of bunch crossings) to receive all data words from the FE-I3 readout chip that belongs to a trigger. If the timeout is reached, EoE/hit word timeout is asserted (see figure 4.1). 0 means disabled (standard).

`CS_EOE_HIT_WORD_TIME_OUT` 8-bit register. Timeout (in units of bunch crossings) for for receiving data words (hit/EoE word) from the FE-I3 readout chip. If the timeout is reached, BCID window timeout is asserted (see figure 4.1). 0 means disabled (standard).

`CS_SAVE_UNKNOWN_WORD` 1-bit register. If disabled, data received from FE-I3 readout chip that is no hit word or EoE is ignored (standard). If enabled, all data gets saved.

`CS_MINIMUM_TRIGGER_LENGTH` 8-bit register. Set up the minimum length (in units of bunch crossings) of the trigger signal to be accepted. If set to 0 every trigger is accepted (standard).

`CS_SAVE_COMPLETE_TRIGGER_NUMBER` 1-bit register. If disabled, trigger word with status data is saved (standard). If enabled, the full trigger word gets saved (see figure 4.1).

`CS_TLU_TRIGGER_DATA_LENGTH` 8-bit register. Set up the length of the trigger number in bits (standard value is 32).

`CS_TLU_TRIGGER_DATA_DELAY` 8-bit register. Set up additional delay to the trigger data shift register (standard value is 0).

`CS_TLU_TRIGGER_DATA_MSB_FIRST` 1-bit register. If disabled, the LSB is clocked first (standard). If enabled, the MSB is clocked first.

`CS_TLU_TRIGGER_LOW_TIME_OUT` 8-bit register. Timeout for the trigger signal to be de-asserted. If the timeout is reached, the source scan will be stopped. 0 means disabled (standard).

Appendix C

Tuning Results

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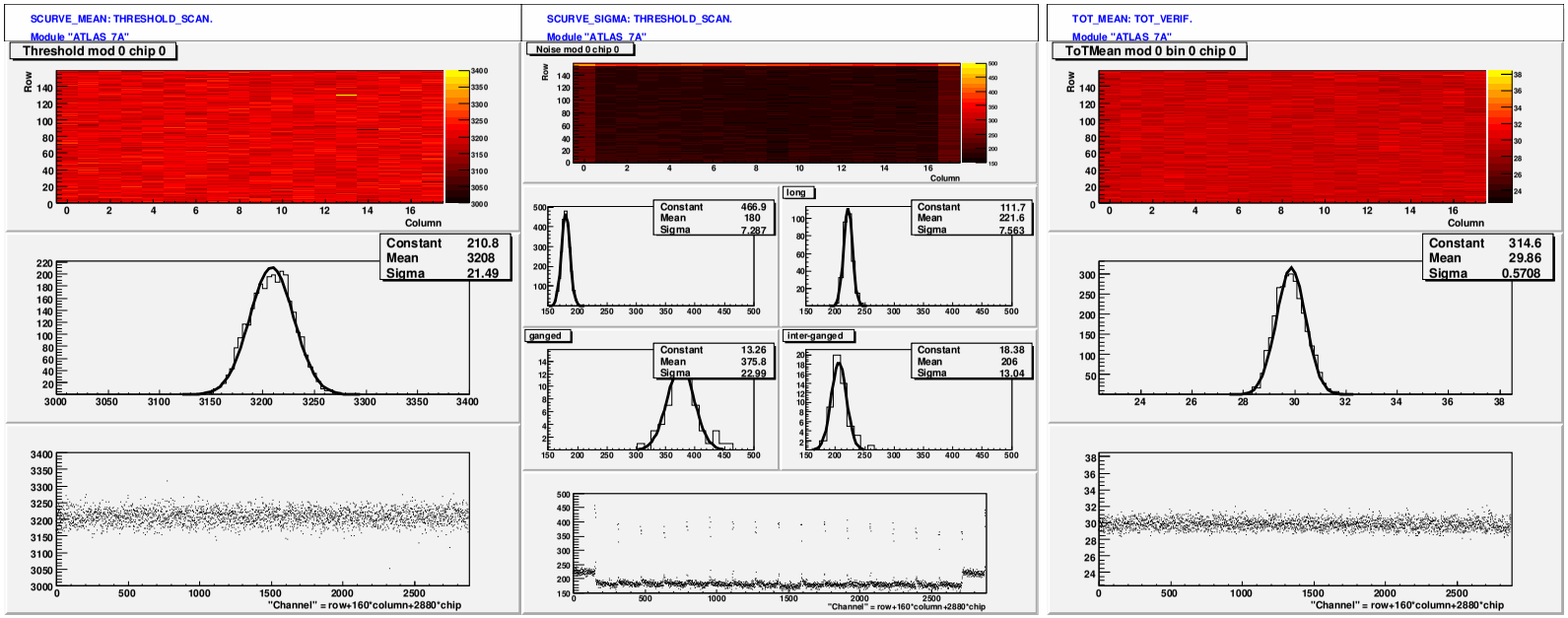
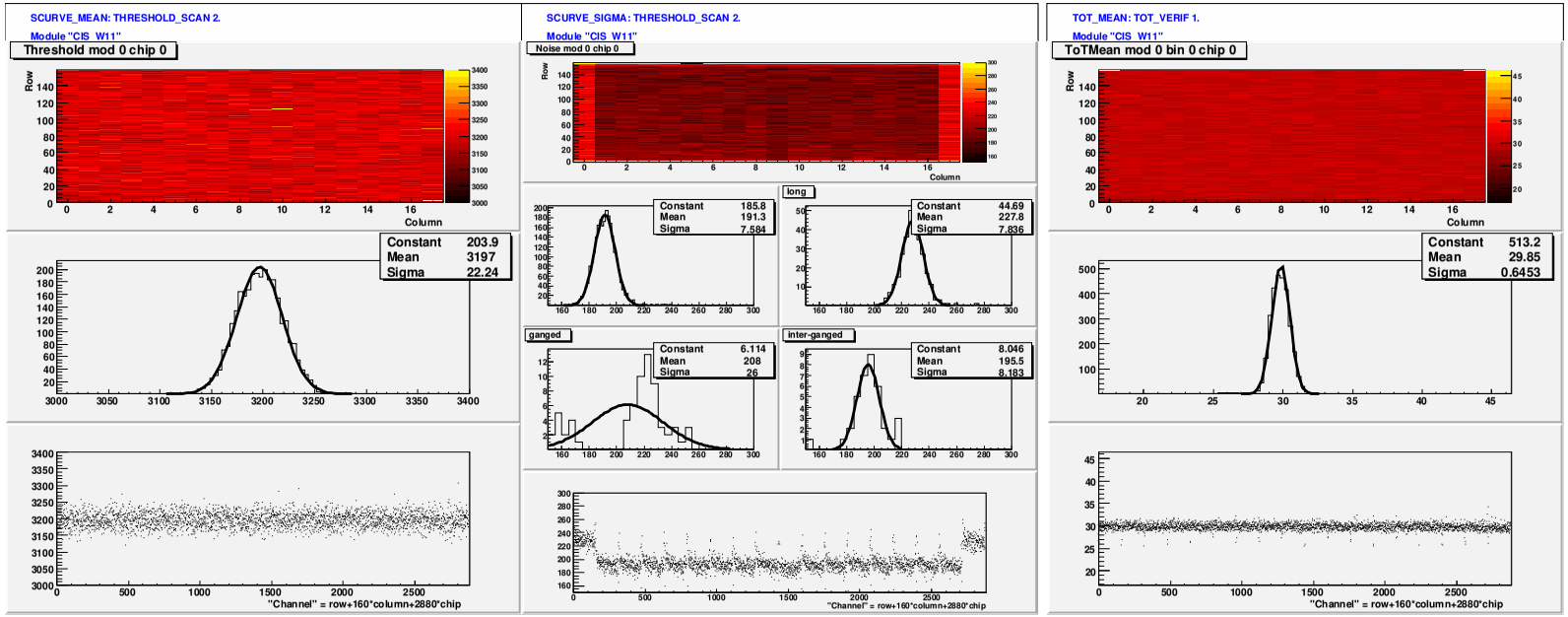
Sensor	GDAC	IFDAC	TrimIF	a [mV/DAC]	C_{lo} [fF]	C_{hi} [fF]
3631-303 “ATLAS”	13	16	8	0.7883	7.679	34.024
W11 19GR-2	13	15	7	0.8594	7.833	36.009
WR13 19GR-NM2	13	15	7	0.7541	8175	36.617
2EM6	13	10	9	1.0562	7.912	40.134
4EM9	13	11	9	1.0135	8.034	41.499

Table C.1: Tuning parameters. Planar sensors tuned at 20°C. Irradiated 3D sensors tuned at −30°C.



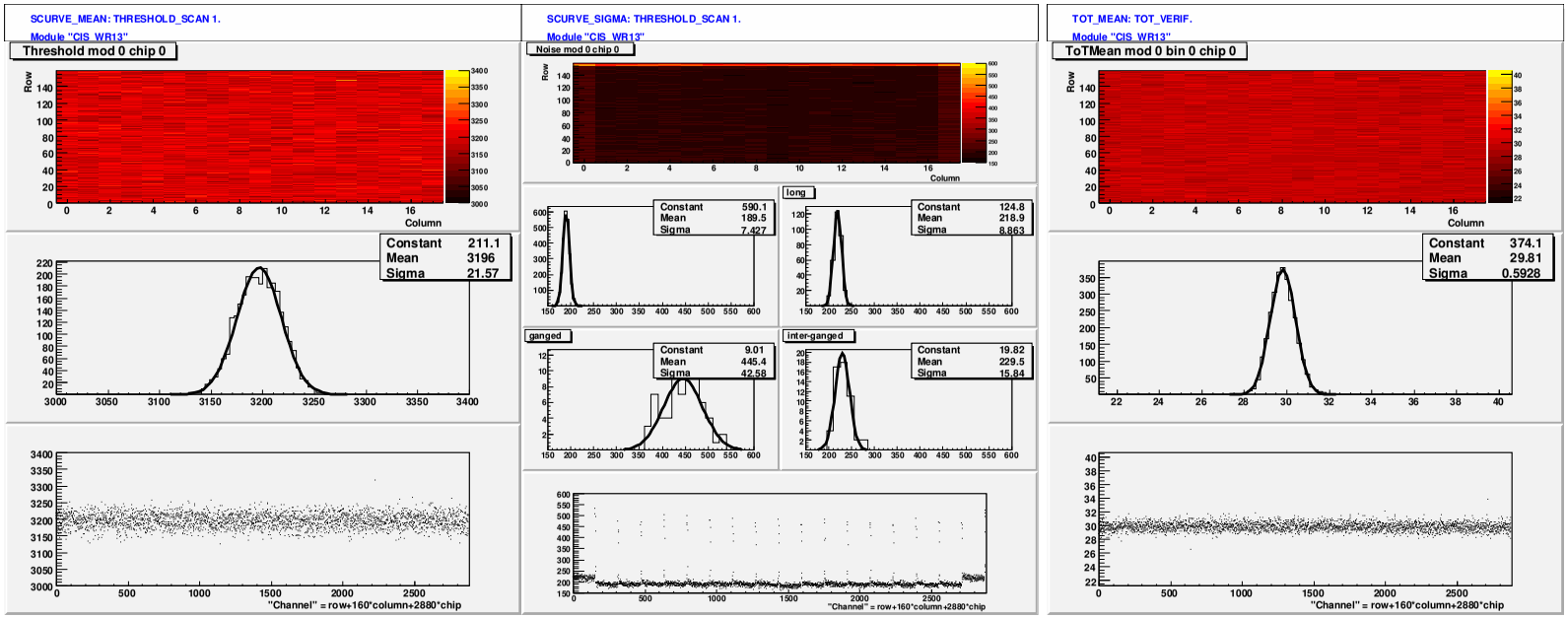
(a) (b) (c)

Figure C.1: Tuning of the 3631-303 "ATLAS" detector. (a) Threshold Scan: Mean threshold and threshold distribution. (b) Threshold Scan: Mean noise and noise distribution. (c) ToT Verification Scan: Mean ToT and ToT distribution at $20,000\,e^-$.



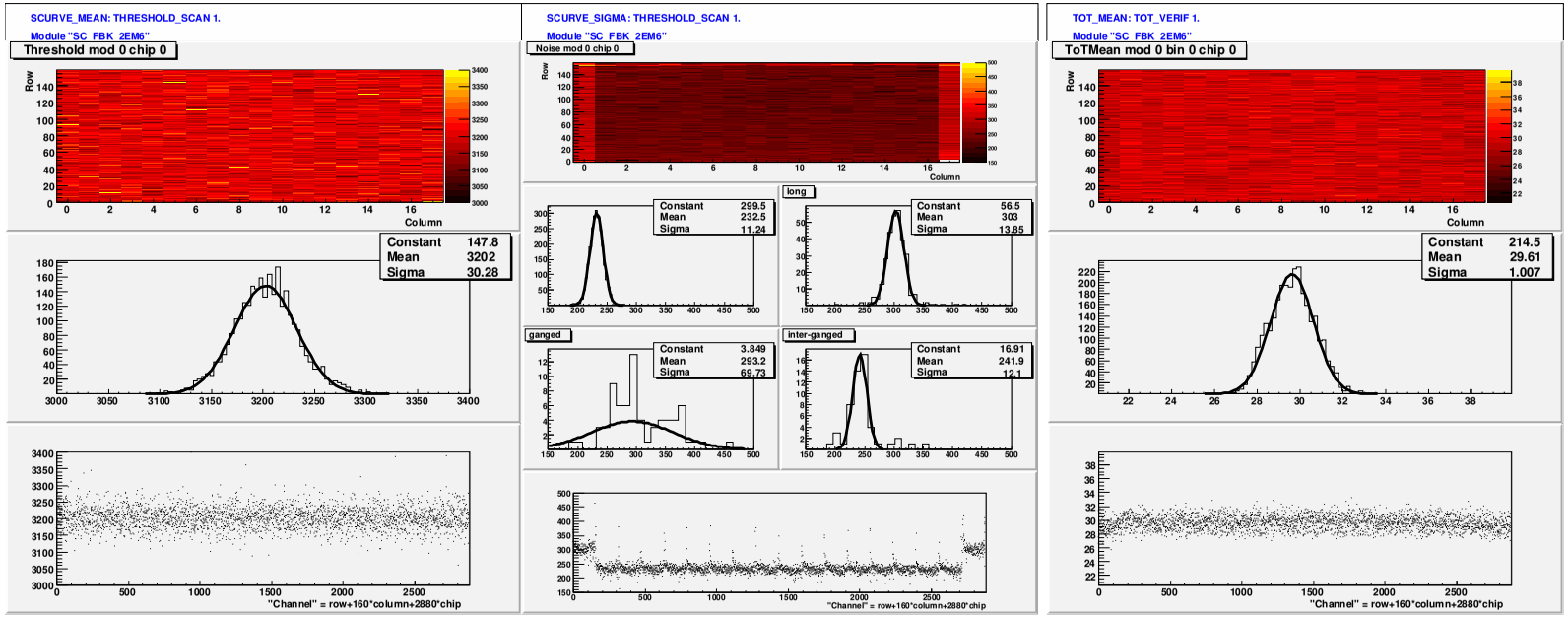
(a) (b) (c)

Figure C.2: Tuning of the W11 19GR-2 detector. (a) Threshold Scan: Mean threshold and threshold distribution. (b) Threshold Scan: Mean noise and noise distribution. (c) ToT Verification Scan: Mean ToT and ToT distribution at $20,000\,e^-$.



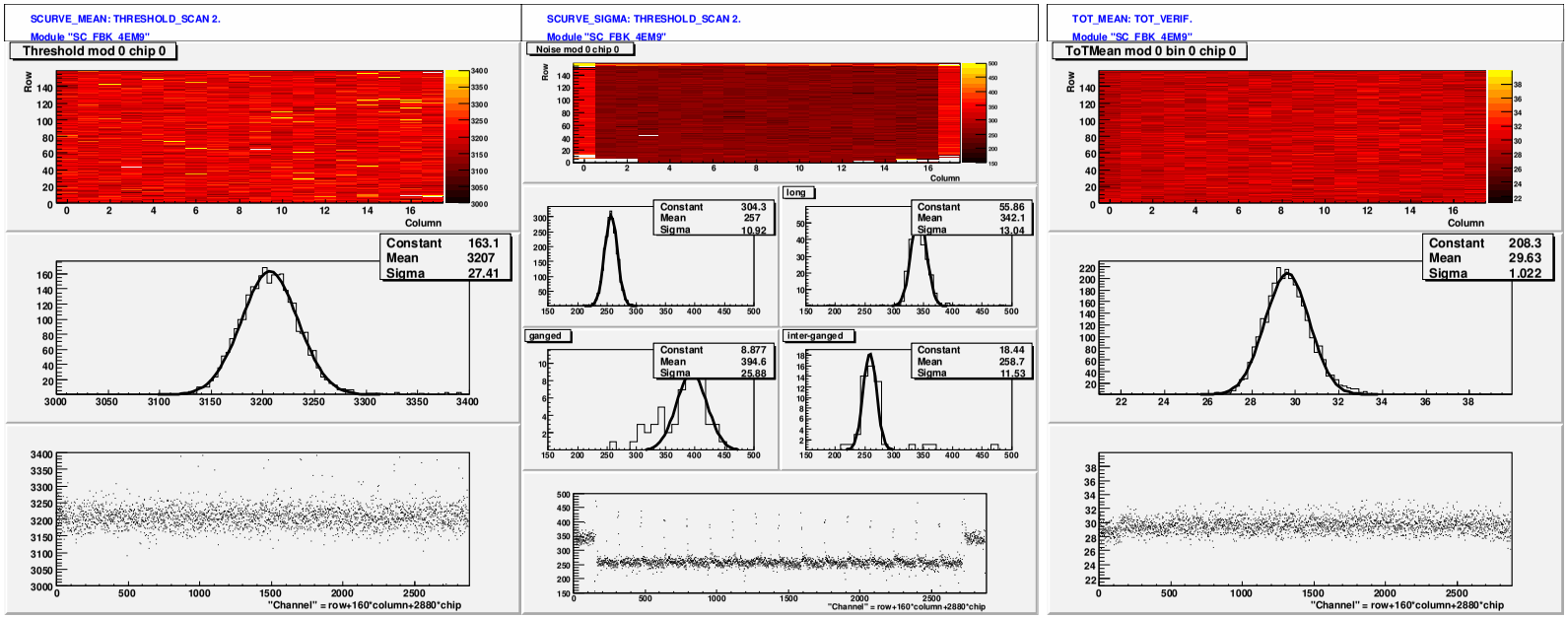
(a) (b) (c)

Figure C.3: Tuning of the WR13 19GR-NM2 detector. (a) Threshold Scan: Mean threshold and threshold distribution. (b) Threshold Scan: Mean noise and noise distribution. (c) ToT Verification Scan: Mean ToT and ToT distribution at $20,000\,e^-$.



(a) (b) (c)

Figure C.4: Tuning of the 2EM6 detector. (a) Threshold Scan: Mean threshold and threshold distribution. (b) Threshold Scan: Mean noise and noise distribution. (c) ToT Verification Scan: Mean ToT and ToT distribution at $20,000\,\mathrm{e}^-$.



(a) (b) (c)

Figure C.5: Tuning of the 4EM9 detector. (a) Threshold Scan: Mean threshold and threshold distribution. (b) Threshold Scan: Mean noise and noise distribution. (c) ToT Verification Scan: Mean ToT and ToT distribution at $20,000\,e^-$.

Bibliography

[1] Brüning, O.S. *et al.*: *LHC Design Report Volume II — The LHC Infrastructure and General Services*. CERN, Geneva, 2004.

[2] The ATLAS Collaboration: *ATLAS detector and physics performance: Technical Design Report, Volume 1*. 1999. CERN-LHCC-99-14.

[3] Aad, G. *et al.*: *The ATLAS experiment at the CERN large hadron collider*. Journal of Instrumentation, 3:S08003, 2008.

[4] Strandberg, S.: *Results from the commissioning of the ATLAS Pixel detector*. Journal of Instrumentation, 4(03):P03020, 2009. `http://stacks.iop.org/1748-0221/4/i=03/a=P03020`.

[5] The ATLAS Collaboration: *ATLAS Pixel Detector: Technical Design Report*. 1998. CERN-LHCC-98-13.

[6] Aad, G. *et al.*: *ATLAS pixel detector electronics and sensors*. Journal of Instrumentation, 3(07):P07007, 2008. `http://stacks.iop.org/1748-0221/3/i=07/a=P07007`.

[7] Dobos, D.: *Commissioning Perspectives for the ATLAS Pixel Detector*. PhD Thesis, University of Dortmund, Dortmund, Sept. 2007.

[8] Rossi, L. *et al.* (eds.): *Pixel Detectors — From Fundamentals to Applications*. Springer-Verlag, Heidelberg, 2006, ISBN 3-540-28332-3.

[9] Szczygiel, R.: *A state of the art rad-hard digital ASIC design for high energy physics experiments*. Measurement Science and Technology, 18(8):2413, 2007. `http://stacks.iop.org/0957-0233/18/i=8/a=016`.

[10] Anelli, G. *et al.*: *Radiation Tolerant VLSI Circuits in Standard Deep Submicron CMOS Technologies for the LHC Experiments: Practical Design Aspects*. Nuclear Science, IEEE Transactions on, 46(6):1690–1696, Dec. 1999, ISSN 0018-9499. DOI 10.1109/23.819140.

[11] Perić, I.: *Design and Realisation of Integrated Circuits for the Readout of Pixel Sensors in High-Energy Physics and Biomedical Imaging*. PhD Thesis, University of Bonn, Bonn, Aug. 2004.

[12] Einsweiler, K.: *ATLAS Pixel FE Chip: Description and Failure Summary*, Dec. 2003. `http://pixdata.lbl.gov/html/docs/ATLASPixelFEChip_v3_0.pdf`, visited on 14 Oct. 2010.

[13] Peric, I. *et al.*: *The FEI3 readout chip for the ATLAS pixel detector*. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 565(1):178–187, 2006, ISSN 0168-9002. http://www.sciencedirect.com/science/article/B6TJM-4K3CY3J-5/2/bc39d9782e35df5fb1076dc06584c623, Proceedings of the International Workshop on Semiconductor Pixel Detectors for Particles and Imaging - PIXEL 2005.

[14] Arutinov, D. *et al.*: *Digital architecture and interface of the new ATLAS Pixel Front-End IC for upgraded LHC luminosity*. In *Nuclear Science Symposium Conference Record, 2008. NSS '08. IEEE*, pp. 1923–1928, Oct. 2008. DOI 10.1109/NSSMIC.2008.4774765.

[15] Karagounis, M. *et al.*: *Development of the ATLAS FE-I4 pixel readout IC for b-layer Upgrade and Super-LHC*. 2008. http://cdsweb.cern.ch/record/1158505, visited on 15 Dec. 2010.

[16] Mathes, M. *et al.*: *Characterization of a single crystal diamond pixel detector in a high energy particle beam*. Journal of Instrumentation, 3(12):P12002, 2008. http://stacks.iop.org/1748-0221/3/i=12/a=P12002.

[17] Nakamura, K. *et al.*: *Review of Particle Physics, 2010–2011. Review of Particle Properties*. J. Phys. G, 37(7A):075021, 2010. http://pdg.lbl.gov.

[18] Mathes, M.: *Development and Characterization of Diamond and 3D-Silicon Pixel Detectors with ATLAS-Pixel Readout Electronics*. PhD Thesis, University of Bonn, Bonn, Dec. 2008.

[19] Groom, D.E., Mokhov, N.V., and Striganov, S.I.: *Muon Stopping Power and Range Tables 10MeV–100TeV*. Atomic Data and Nuclear Data Tables, 78(2):183–356, 2001, ISSN 0092-640X. http://www.sciencedirect.com/science/article/pii/S0092640X01908617.

[20] Landau, L.D.: *On the energy loss of particles by ionization*. J. Exp. Phys.(USSR), 8:201–205, 1944.

[21] Bichsel, H.: *Straggling in thin silicon detectors*. Rev. Mod. Phys., 60(3):663–699, Jul 1988. DOI 10.1103/RevModPhys.60.663.

[22] Lutz, G. (ed.): *Semiconductors Radiation Detectors*. Springer-Verlag, Heidelberg, 2007, ISBN 978-3-540-71678-5.

[23] Ramo, S.: *Currents Induced by Electron Motion*. Proceedings of the IRE, 27(9):584–585, 1939, ISSN 0096-8390. DOI 10.1109/JRPROC.1939.228757.

[24] Jun, I. *et al.*: *Proton nonionizing energy loss (NIEL) for device applications*. IEEE Transactions on Nuclear Science, 50(6):1924–1928, Dec. 2003, ISSN 0018-9499. DOI 10.1109/TNS.2003.820760.

[25] Wunstorf, R.: *Systematische Untersuchungen zur Strahlenresistenz von Silizium-Detektoren für die Verwendung in Hochenergiephysik-Experimenten*. PhD thesis, University of Hamburg, Hamburg, 1992. http://books.google.de/books?id=XmTlSgAACAAJ.

[26] Lindström, G. *et al.*: *Radiation hard silicon detectors–developments by the RD48 (ROSE) collaboration.* Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 466(2):308–326, 2001, ISSN 0168-9002. http://www.sciencedirect.com/science/article/B6TJM-43CK059-F/2/0380b762a87258cfe9e69c45098e53ca, DOI 10.1016/S0168-9002(01)00560-5.

[27] Capeans, M. *et al.*: *Atlas insertable b-layer technical design report.* Tech. Rep. CERN-LHCC-2010-013. ATLAS-TDR-019, CERN, Geneva, Sept. 2010.

[28] Da Via, C. *et al.*: *Advances in silicon detectors for particle tracking in extreme radiation environments.* Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 509(1–3):86–91, 2003, ISSN 0168-9002. http://www.sciencedirect.com/science/article/B6TJM-48R1NFT-9/2/e861edbfa4bcd1cee9a87375cc819433, DOI 10.1016/S0168-9002(03)01554-7".

[29] Hügging, F.G.: *Der ATLAS Pixelsensor: Der state-of-the-art Pixelsensor für teilchenphysikalische Anwendungen mit extrem hohen Strahlungsfeldern.* PhD Thesis, University of Dortmund, Dortmund, June 2001.

[30] Benoit, M., Lounis, A., and Dinu, N.: *Simulation of Radiation Damage Effects on Planar Pixel Guard Ring Structure for ATLAS Inner Detector Upgrade.* Nuclear Science, IEEE Transactions on, 56(6):3236–3243, Dec. 2009, ISSN 0018-9499. DOI 10.1109/TNS.2009.2034002.

[31] Beimforde, M.: *The ATLAS Planar Pixel Sensor R&D project.* Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 2010, ISSN 0168-9002. http://www.sciencedirect.com/science/article/B6TJM-4YYGGSV-7/2/69a1b88494d7445642f1e59a59590708, DOI 10.1016/j.nima.2010.04.078.

[32] Weigell, P. *et al.*: *Characterization and Performance of Silicon n-in-p Pixel Detectors for the ATLAS Upgrades.* Arxiv preprint arXiv:1012.3595, 2010.

[33] Krüger, H.: *Test Systems for ATLAS Pixel Detector Upgrade Activities*, Jan. 2008. http://icwiki.physik.uni-bonn.de/twiki/pub/Systems/WebHome/ATLAS_Pixel_Chip_Test_Systems.pdf, visited on 30 Dec. 2010.

[34] Backhaus, M.: *Development of an USB-based test system for the FE-I3 readout chips of the ATLAS pixel detector and Noise Occupancy Studies.* Diploma Thesis, University of Bonn, Bonn, Dec. 2009.

[35] Schneider, J. and Krüger, H.: *S3 Multi IO System*, Jan. 2010. http://icwiki.physik.uni-bonn.de/svn/USBpixI4/doc/MultiIOboard_V1.03_Manual.pdf, visited on 18 Nov. 2010.

[36] Köhler, F.: *Threshold difference USBpix – TurboDAQ*, Jan. 2010. http://indico.cern.ch/event/80615, visited on 14 Oct. 2010.

[37] Backhaus, M. *et al.*: *Development of a versatile and modular test system for ATLAS hybrid pixel detectors.* Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 2010. DOI 10.1016/j.nima.2010.12.087.

[38] EUDET JRA1 Group: *Mechanics of the EUDET JRA1 telescope.* `http://www.desy.de/~gregor/EUDET/Mechanics/CERN_Aufbau2.pdf`, visited on 16 Oct. 2010.

[39] Baudot, J. *et al.*: *First test results of MIMOSA-26, a fast CMOS sensor with integrated zero suppression and digitized output.* Nuclear Science Symposium Conference Record (NSS/MIC), 2009 IEEE, pp. 1169–1173, Oct. 2009, ISSN 1082-3654. DOI 10.1109/NSSMIC.2009.5402399.

[40] Cussans, D.: *Description of the JRA1 Trigger Logic Unit (TLU), v0.2c*, Sept. 2009. `http://www.eudet.org/e26/e28/e42441/e57298/EUDET-MEMO-2009-04.pdf`, visited on 14 Oct. 2010.

[41] Schultes, S.: *Entwicklung eines Strahl-Teleskops mit ATLAS-Pixeldetektoren.* Diploma Thesis, University of Bonn, Bonn, July 2011.

[42] Hügging, F. Private communication, Dec. 2010.

[43] Köhler, M.: *Studies of the Timing Behaviour of the ATLAS Pixel Detector.* Master Thesis, University of of Siegen, Siegen, Aug. 2008.

[44] Chen, J., Sylvester, D., and Hu, C.: *An on-chip, interconnect capacitance characterization method with sub-femto-farad resolution.* IEEE Transactions on Semiconductor Manufacturing, 11(2):204–210, May 1998, ISSN 0894-6507. DOI 10.1109/66.670160.

[45] Behara, P. *et al.*: *Threshold Tuning of the ATLAS Pixel Detector.* Tech. Rep. ATL-INDET-PUB-2010-001, CERN, Geneva, Aug. 2010. `http://cdsweb.cern.ch/record/1283928`, visited on 18 Nov. 2010.

[46] Große-Knetter, J.: *Vertex Measurements at a Hadron Collider — The ATLAS Pixel Detector.* Habilitation Thesis, University of Bonn, Bonn, Mar. 2008.

[47] Andreazza, A.: *Test beam performance of the ATLAS Pixel Detector modules.* Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 565(1):23–29, 2006, ISSN 0168-9002. `http://www.sciencedirect.com/science/article/B6TJM-4K5J9HH-3/2/a3ecf43b5e5811b4926f14638fcaa99f`, DOI 10.1016/j.nima.2006.04.095.

[48] Dalla Betta, G.F. *et al.*: *Development of 3D-DDTC pixel detectors for the ATLAS upgrade.* Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 2010, ISSN 70168-9002. `http://www.sciencedirect.com/science/article/B6TJM-4YYGGSV-8/2/ea5307c6c1b214b9835d1aa11cd068fc`, DOI 10.1016/j.nima.2010.04.079.

[49] La Rosa, A.: *Measurements of 3D/FBK sensors*, Nov. 2009. `http://indico.cern.ch/event/65918`, visited on 25 Dec. 2010, RD50 Workshop.