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Z80 Based Voltage and Temperature Monitor for the Main Ring Control Crate: The CC48 Card

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Figure Captions

1. Introduction

Several years ago, there seemed to be a need to monitor the power supply voltages and temperatures in the three bay racks of the Main Ring service buildings. A few years ago, another engineer seemed to have done a preliminary design using analog voltage comparators.

In late 1979, it was proposed to use a microprocessor instead of analog voltage comparators. It was dramatic that all the people at a meeting were excited about the idea and unanimously approved the project. The author can remember some of the reasons why they were so enthusiastic about the idea at the time, i.e., (1) It was new to have microprocessor based cards on the Main Ring control system, (2) programmable alarm limits were preferred to resistor dividers or potentiometers with analog voltage comparators, (3) it was the first to try the communication between a host computer and distributed intelligent cards.

The author started the design on the CC48 in January, 1980 and completed in April, 1980. We had the prototype card working in July, 1980 and tested the card on the system in September, 1980. Seven CC48s of the pilot production were installed in July, 1981. We mass-produced 35 more cards and finished installing them around the Main Ring in May, 1982.

In the following sections, the author will talk about the hardware, software and operation on the CC48 card, and he will make some remarks on his experience on the project.

2. Hardware

2.1 Block Diagram

The CC48 card has a Z80-CPU, 2K bytes of PROM, 2K bytes of RAM, 3PIOs, a PCI and so forth as shown in Fig. 1. The CC48 communicates with the MAC computer via the Main Ring Utility Link. The MAC is always the master and tells the CC48 what to do. The MAC sends a WRITE-B command to the CC48, where the WRITE-B PIO receives the command and generates an interrupt. The Z80 acknowledges the interrupt, executes the task that the MAC has specified and deposits data in the READ-A PIO, if the MAC has asked data. The MAC reads the data from the PIO with a READ-A command in a proper timing.

The Z80 scans through all the 32 analog channels in approximately 10 m sec, digitizing, comparing each with limits and setting an alarm if it is out of tolerance. The ADC PIO has Port A and Port B. The digitized data consist of one sign bit and 10 data bits, and are read through Port A (which has 8 bits) and Port B (three high order bits used for the purpose). The Port B of the ADC PIO is operated in 'CONTROL MODE', in which the three high order bits are used for inputting and the five low order bits are used for outputting. The five low order bits are used to select one of 32 analog channels. When the PIO is operated in Control Mode, handshake signals are not available, and therefore we had to generate the ADC trigger pulse by ANDing few signals. The trigger pulse is delayed approximately 20 µsec before it is applied to the ADC, allowing the analog signal to settle through the multiplexers and the amplifier.

The CC48 has a RS 232-port on the front panel. When the CC48 is tested in the lab, a CRT terminal is connected to this port. With a monitor program, one can perform basic tests on the micro-computer, i.e., (1) Substitute and/or examine memory, (2) non-destructive memory test, (3) input and output from / to PIOs, (4) go-to and execute a short test program and so forth. Now, the CC48 is once installed in the field, this port provides a remote terminal access to the Main Ring control system. Although not yet implemented in software, it is envisioned that one can monitor some Main Ring control parameters in the service building with a portable terminal.

The MAC periodically (approximately once every 16 seconds) checks the status on the CC48. The status latch on the CC48 holds several status bits, i.e., (1) Alive (If the CC48 functions normally, this bit is held true), (2) Reboot (When the CC48 is powered up or reset, this bit is set true. The MAC sends alarm parameters over and clears it.), (3) Alarm (If any one of 32 voltage values is out of tolerance and if it is not bypassed, this bit is true.), (4) Local (If the sense switch on the CC48 is turned on, this bit is true.), and (5) Terminal data (If the remote terminal which is connected to the CC48 has a character to send, this bit is true.).

The CC48 card is plugged into Slot F of the Main Ring Control crate, and allows the MAC to address the F subslots. When the MAC sends a WRITE-A command to talk to a F subslot, the CC48 decodes the command and generates a proper F subslot strobe.

2.2 Memory Map

The CC48 has sockets for 2K bytes of RAM and 2K bytes of PROM. The RAM and PROM can be relocated by manipulating jumper wires around base address generators (U25 and U26 in the schematic). The first address of the RAM can be located at 0000H, 1000H, 2000H, ----- or F000H. The first address of the PROM can be located at 0000H, 2000H, 4000H, ----- or E000H. The CC48 memory map is shown in Fig. 2.

2.3 I/O Ports

The CC48 has three PIOs (Zilog Z80-PIO), one PCI (Signetics PCI 2651) and one status latch (74LS273). The Z80 CPU communicates with these devices or ports at the address locations shown in Fig. 3.

2.4 Analog Input Grouping

The 'HI' connections of the 32 analog channels are multiplexed by two CMOS multiplexers (Harris HI 506A, 16 single channels) and one CMOS switch (Harris HI 5043, dual SPDT). Differential connections are ideal for measuring analog signals coming from outside the card. However, because a limited space is available on the card and because a limited number of contacts available in the I/O connector, the analog channels are divided into eight groups of four as shown in Fig. 4. Each group has basically one common 'LO' connection. One CMOS multiplexer (Harris HI 508A, 8 single channels) selects a proper common connection for a group which is selected at a given time. This quasi-differential arrangement seems to be well suited to the Main Ring three bay racks where all the power supplies have three or four output voltages and where they need only one common connection.

2.5 Interesting Points

The CC48 has three PIOs, and there were some possibilities that it would have four of them instead of three. In order to multiplex 32 analog channels and read back 12 bits of data from the ADC, it seemed that one would need two PIOs just for the purpose. The author felt that the scheme was wasteful, and proposed to use one PIO and operate one of its ports in Control Mode (or Mode 3). The Port A is operated in Input Mode, and handles a sign bit and 7 data bits. The Port B is operated in Control Mode with 3 high order bits set for inputting and 5 low order bits set for outputting. The three bits, combined with the eight bits of the Port A, provide 11 bit accuracy reading from the ADC. The five bits are used to select one of 32 analog

channels. The output bits are properly latched in the PIO, when the Z80 writes. Accurate sets of input data are read back via the PIO, when the Z80 reads. It works very well except the fact that handshake signals are not available in this mode and that the I/O address has to be detected with a few extra gates to generate a trigger for the ADC. A sketch is drawn for the arrangement as shown in Fig. 5.

When the first CC48 was constructed on a p c board, we had an unexpectedly high noise level, even though we had given a special consideration to isolate analog circuits from digital circuits in laying out the p c board. The ultimate solution was to suspend Z80 activities during the ADC conversion. The scheme is illustrated in Fig. 5. As soon as the I/O address is detected, a D type flip-flop is set, and it is reset at the end of ADC conversion. The $\overline{Q}$ output of the flip-flop drives the Bus Request input of the Z80. As soon as the current machine cycle is terminated, Z80 goes into a suspended state and resumes activities after the end of conversion.

In abnormal situations, the CC48 goes out of program control. One can put it back in order by resetting it. However, it is located at a remote place, and therefore one needs an auto reset circuit on the card. Under a program control, the Z80 scans through all the 32 analog channels and updates the status latch in approximately 10m sec. We trigger a one-shot with the update pulse for the status latch. As long as the Z80 is normally functioning, the one-shot is kept triggered and nothing happens. Should the Z80 become out of control, the one-shot loses the trigger pulse and its output changes from true to false. We trigger the reset circuit with the output from the one-shot.

The input of Channel 3 is tied to the ground. The supervisory program, which resides in the PROM, reads Channel 3 and compensates zero offsets on other channels.

The input of Channel 4 is tied to a temperature compensated zener diode (1N936A, 9.0V, 50 ppm/^{o}C). We just monitor the voltage on this channel as a reference, and we do not compensate the full scale gain with this.

The input of Channel 6 is tied to a temperature sensor (National LM335A, 2.98V at 25^{o}C, 10mV/^{o}C). The sensor is located at the top rear corner of the CC48 to measure the crate temperature. The device is linear over a 0^{o}C to 100^{o}C temperature range and has a large gain of 10mV/^{o}C. We found this device to be accurate, reliable and easy to use.

We use an instrumentation amplifier (Analog Devices AD521k, 10V/sec, 150μV/^{o}C) as a buffer. Some of 521Ks were temperature sensitive, and they just ran away with a small amount of heat applied. We feel unhappy that a company like Analog Devices does not have a good quality control over their products.

When we installed CC48 cards in the F sector, we observed strange phenomena. Channel 6 read the crate temperature and was behaving strangely with readings jumping from 75°F to 230°F. We once questioned whether the MAC had brought error-free data back or not. It took for a while before we came to realize that the performance of the CMOS multiplexers would heavily rely on the supply voltage. We use Harris Semiconductor's HI-506As, HI-508s and a HI-5043. According to their data sheets, the digital inputs require 4.0V min. when they are high. The solution was to install 4.7K ohm pull-up resistors on the multiplexer address lines. With these pull-up resistors, we can lower the Vcc down to 4.5V. Without them, we can hardly come down to 4.75V.

3. Software

A supervisory program resides in the 2K byte PROM with memory addresses extending from 0000H to 07FFH. It uses 1K bytes of RAM as buffers with memory addresses extending from 1000H to 13FFH.

The primary function of the program is to scan 32 ADC channel voltages periodically and signals to the MAC computer when any one of them has gone out of tolerance.

The CC48 card communicates over the Main Ring Utility Link with the MAC computer. The Z80 on the CC48 updates status register during the alarm scan in the program. The MAC periodically polls it with a READ-B command. If there is an alarm, the MAC knows it by checking the alarm bit in the status word.

A flow chart on the supervisory program is shown in Fig. 6. On power-on or on reset, the program counter of the Z80 is forced to be zero, and the Z80 executes a jump instruction, which is stored at Location 0 in the PROM, and jumps to the start of the supervisory program. The program first does a general initialization, verifies the RAM, sets the 'Alive" and "Reboot" bits, enables interrupts and starts scanning.

At the start of the scan, the program checks all the alarm latches, and sets the alarm status bit if any one of them is true. It checks on the terminal status and does terminal input/output. If the terminal has a character, the program inputs it, queues it up and sets the 'Character available' status bit for the MAC. After all the status bits being updated, it outputs the status byte to the READ-B status latch so the MAC can read it.

The program then initializes a 32 channel scan. It digitizes and reads a channel, adjusts the reading with the zero offset, and stores it. The zero offset is obtained from readings on Channel 3 whose input is tied to the ground. The program checks the alarm bypass bit for the channel just read. If bypassed, it goes to the next channel. If not bypassed, it compares the reading against the upper and lower limits. If the reading is in tolerance, it records another OK reading for the channel and

goes to the next channel. If the reading is out of tolerance, it de-glitches it and sets an alarm latch bit. De-glitching is accomplished by requiring out of tolerance readings to occur twice within a certain number of scans before an alarm latch bit is set for the channel in question.

The program goes to the next channel, digitizes and reads it and compares it against the limits. The program does the same things for 32 channels. After having done with the 32 channels, the program goes back to the start of the scan and repeats the same process over and over again.

While the CC48 is doing scanning, the MAC sends inquiries and alarm parameters to the CC48 with WRITE-B commands. These are accepted by the WRITE-B PIO, which interrupts the Z80. The interrupt service program extracts a type code from three low order bits of the 16 bit WRITE-B command and executes a routine specified in the type code. There are 8 type code routines, i.e., (0) Data mirror, (1) set new voltage limits, (2) read voltage limits, (3) toggle latch or bypass bit, (4) miscellaneous control functions, (5) read back voltage from last scan, (6) terminal (PCI chip) I/O and (7) data mirror. If the CC48 is expected to respond back, it writes 16 bits of data to the READ-A PIO, which the MAC then reads with a READ-A command. It is MAC's responsibility to properly time the delay between WRITE-B and READ-A.

Eight typecodes and their command formats are summarized in Table 1.

4. Operation

When a CC48 card is installed, one person goes out to a service building and installs the card in Slot F of the Main Ring Utility crate, and another person sits at a console in the control room and waits for the first person to call. As soon as the second person receives a call that the installation is complete, he can go to Page 26.20 on the console. On Page 26.20, he sees a display like the one shown in Fig. 7. On the page, he interrupts under 'Equipped', and the MAC then sends all the alarm parameters to the CC48 for the house in question and resets the 'Reboot' indicator on the CC48. During the rebooting process, one can observe 'RELOAD' indication under the column of the house in question.

The MAC does diagnostic tests, i.e., data mirror and memory verification. In the data mirror test, the MAC periodically sneds a command of all Os or 1s, which the CC48 complements and sends back. If the received data are verified with the sent data without any error, we have a good communication link between the MAC and the CC48. In the memory verification, the MAC sends a command requesting the Z80 to do a non-destructive test on the

on-board RAM. If there is any failure in these tests, 'DATA MIR' and/or 'MEM VER' indications appear under the column of the house in question.

If any one of 32 voltage channels is out of tolerance, 'ALARM' indication appears. If the local sense switch on the CC48 is on, 'LOCAL' indication appears. If the MAC does not receive a proper response to its commands, 'I/O ERR' indication appears.

If one interrupts right under the building name, that takes him to the subpage for the building. A subpage example is shown in Fig. 8. If any of these 32 voltage readings are out of tolerance, they are displayed in red. These can be cleared by interrupting right under the reading in red or under 'RESET' on the page. If one wants to bypass a voltage channel, he can do that by interrupting right in front of the voltage value displayed and putting a red asterisk there. To clear this, he simply interrupts there one more time.

To enter new upper and lower limit values, one uses Sense Switches 1 and 2 respectively at the console. One can also copy from another building by simply using 'GET LIMITS FROM ( )', which is located at the bottom of the subpage.

5. CC48 Specifications

Analog channels: 32, quasi-differential

Analog input grouping:

External: 6 groups each with 4 voltages and a common for each set of 4

Internal: 2 groups each with 4 voltages, and 3 commons tied together

Analog input impedance: $\geq$10M ohms

Analog voltage range: -10.24 to +10.23V

Analog voltages should be properly divided to meet the said voltage range with a voltage divider external to the card. Temperature voltages generated from a thermistor should be properly amplified to meet the said voltage range with an amplifier external to the card.

Temperature monitor: 1 crate temperature, others from users' equipment.

A/D converter: 1 sign bit and 10 data bits

Alarm limit setting: Adjustable at console, down to $\pm$2.5%

Alarm reset: Individual and aggregate

Sample rate: All 32 channels sampled every 10m sec, asynchronously with 60 Hz

De-glitching: De-glitch parameter can be set at console from 0 to 31. (31 means 2 out of 31 x 4 + 2 consecutive scans need to be bad to cause an alarm.)

Data Mirror: MAC periodically sends command of all 0s or 1s which CC48 complements and sends back. (Link diagnosis)

Memory verification: RAM on CC48 can be verified from console.

Local indications and controls:

Alive: Z80 is active under program control.

Reboot: Tells MAC to send new alarm parameters.

Alarm: Analog voltage is out of tolerance.

Sense: When this switch is on, 'LOCAL' is displayed at console.

Reset: Manual reset switch on front panel.

Auto Reset: When Z80 goes out of program control, this circuit automatically resets it.

RS232 Port: Allows portable terminal access to Main Ring control system in service building.

Subslot access: Subslots F0, F1, F2 and F3 are accessed via CC48 which resides in Slot F.

Operating ambient temperature range: 0 to 50^{o}c.

6. Remarks

The CC48 was the first card that had a microprocessor on board throughout the Main Ring control system. We learned something from this experience. A project like this demands persons of versatile knowledge, who know (1) analog and digital circuits, (2) how to isolate the two, (3) the microprocessor and peripheral ICs, (4) how to write programs, (5) how to troubleshoot microprocessor based circuits, (6) environmental tests and so forth. If one lacks knowledge in some area, he should be self-motivated and work hard to gain it.

7. Acknowledgement

The author would like to thank colleagues, Loren Anderson, Norm Brown, Rick Divelbiss and Mike Glass. Loren Anderson worked on the prototype card and the 10 unit pilot production. Loren Anderson and Norm Brown were responsible for assembling, testing and installing approximately 35 cards. Rick Divelbiss laid out the p c board. Mike Glass wrote the PROM resident supervisory program and implemented software on the MAC computer.

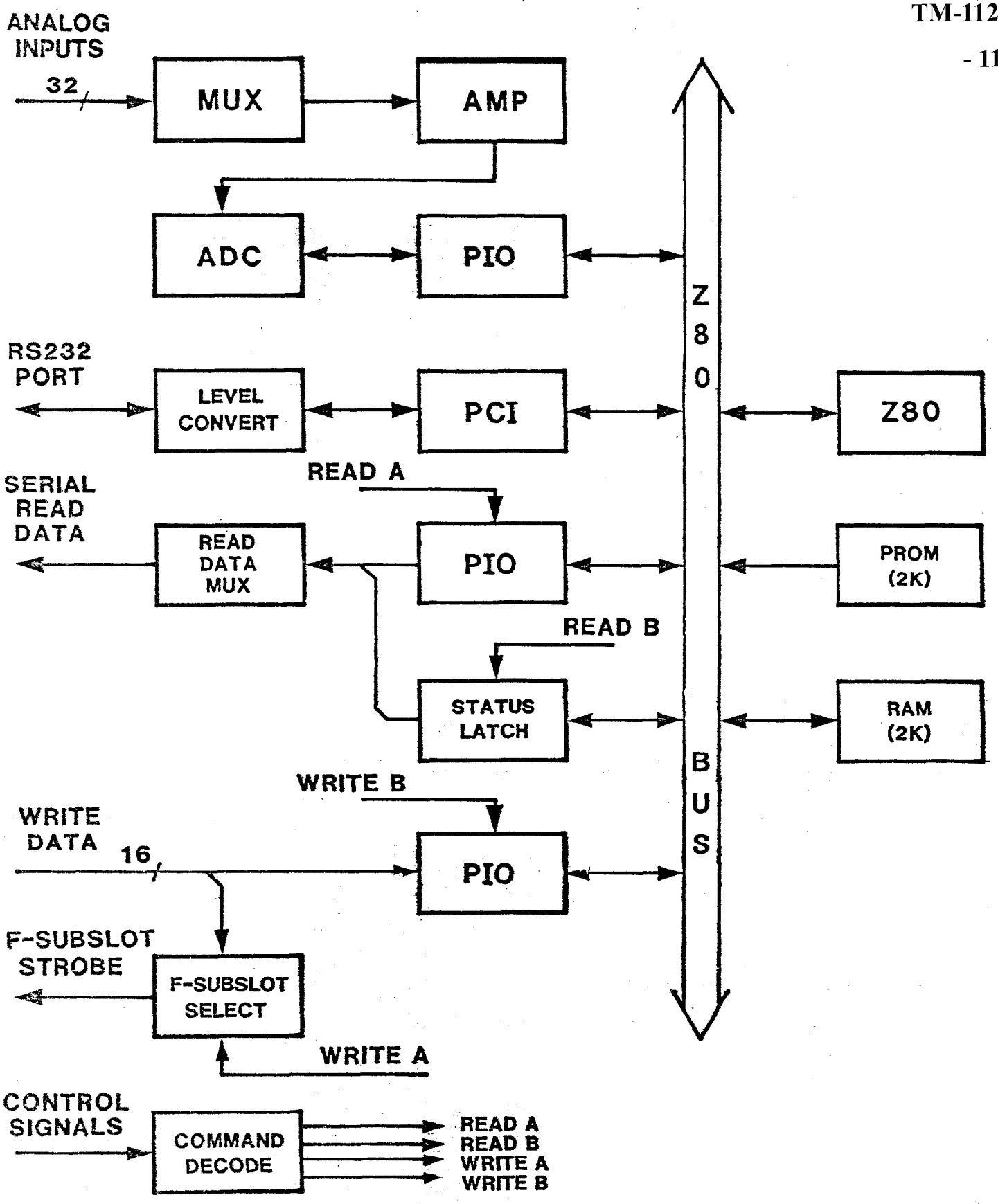
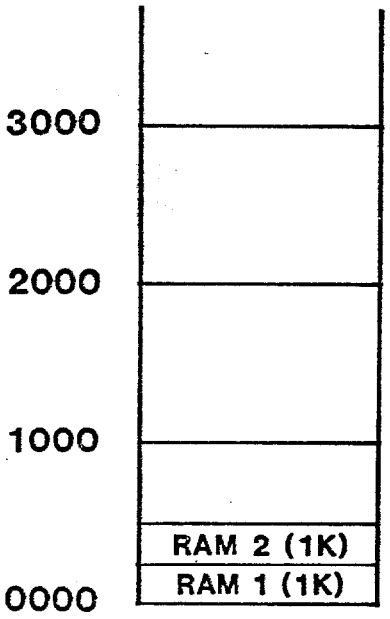
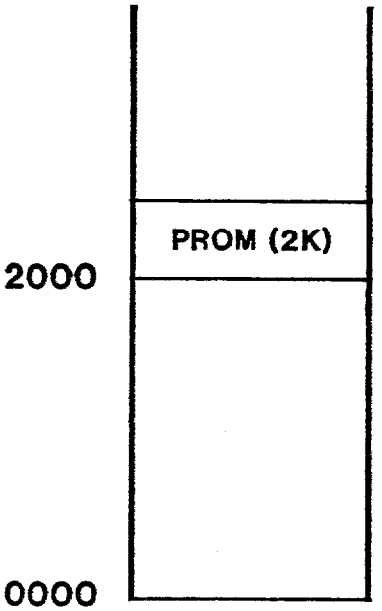


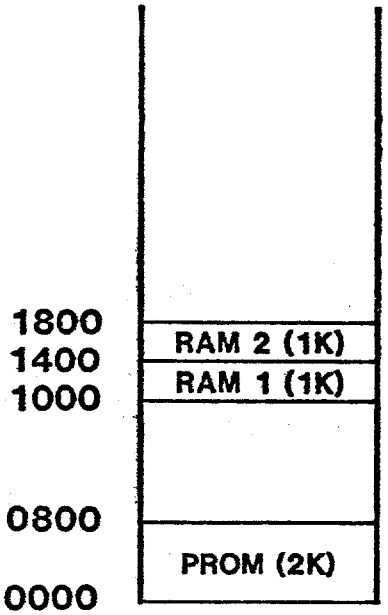
FIG. 1 CC48 BLOCK DIAGRAM



(a) RAM LOCATIONS



(b) PROM LOCATIONS



(c) TYPICAL MAP

FIG. 2 CC48 MEMORY MAP

	FUNCTION	ADDRESS
WRITE B PIO	INPUT PORT A	00H
	INPUT PORT B	01H
	SET PORT A MODE	02H
	SET PORT B MODE	03H
	SET PORT B FOR INTR	03H
	LOAD INTR VEC TO PORT B	03H
ADC PIO	INPUT PORT A	04H
	INPUT PORT B	05H
	OUTPUT PORT B	05H
	SET PORT A MODE	06H
	SET PORT B MODE	07H
PCI	INPUT RECEIVE REGISTER	08H
	LOAD TRANSMIT REG.	08H
	INPUT STATUS REGISTER	09H
	SET MODE REGISTER 1	0AH
	SET MODE REGISTER 2	0AH
	SET COMMAND REGISTER	0BH
READ A PIO	LOAD PORT A FOR OUTPUT	0CH
	LOAD PORT B FOR OUTPUT	0DH
	SET PORT A MODE	0EH
	SET PORT B MODE	0FH
READ B LATCH	LOAD STATUS LATCH	10H

Fig. 3 CC48 I/O Ports

CHANNEL NO.	PIN NUMBER	
	HI	LO
0	--	33, 35, 36
1	--	33, 35, 36
2	--	33, 35, 36
3	--	33, 35, 36
4	--	33, 35, 36
5	--	33, 35, 36
6	--	33, 35, 36
7	31	33, 35, 36
8	30	26
9	29	26
10	28	26
11	27	26
12	24	25
13	23	25
14	22	25
15	21	25
16	20	16
17	19	16
18	18	16
19	17	16
20	14	15
21	13	15
22	12	15
23	11	15
24	10	6
25	9	6
26	8	6
27	7	6
28	4	5
29	3	5
30	2	5
31	1	5

Fig. 4 CC48 I/O Connector Pin Grouping for Analog Inputs

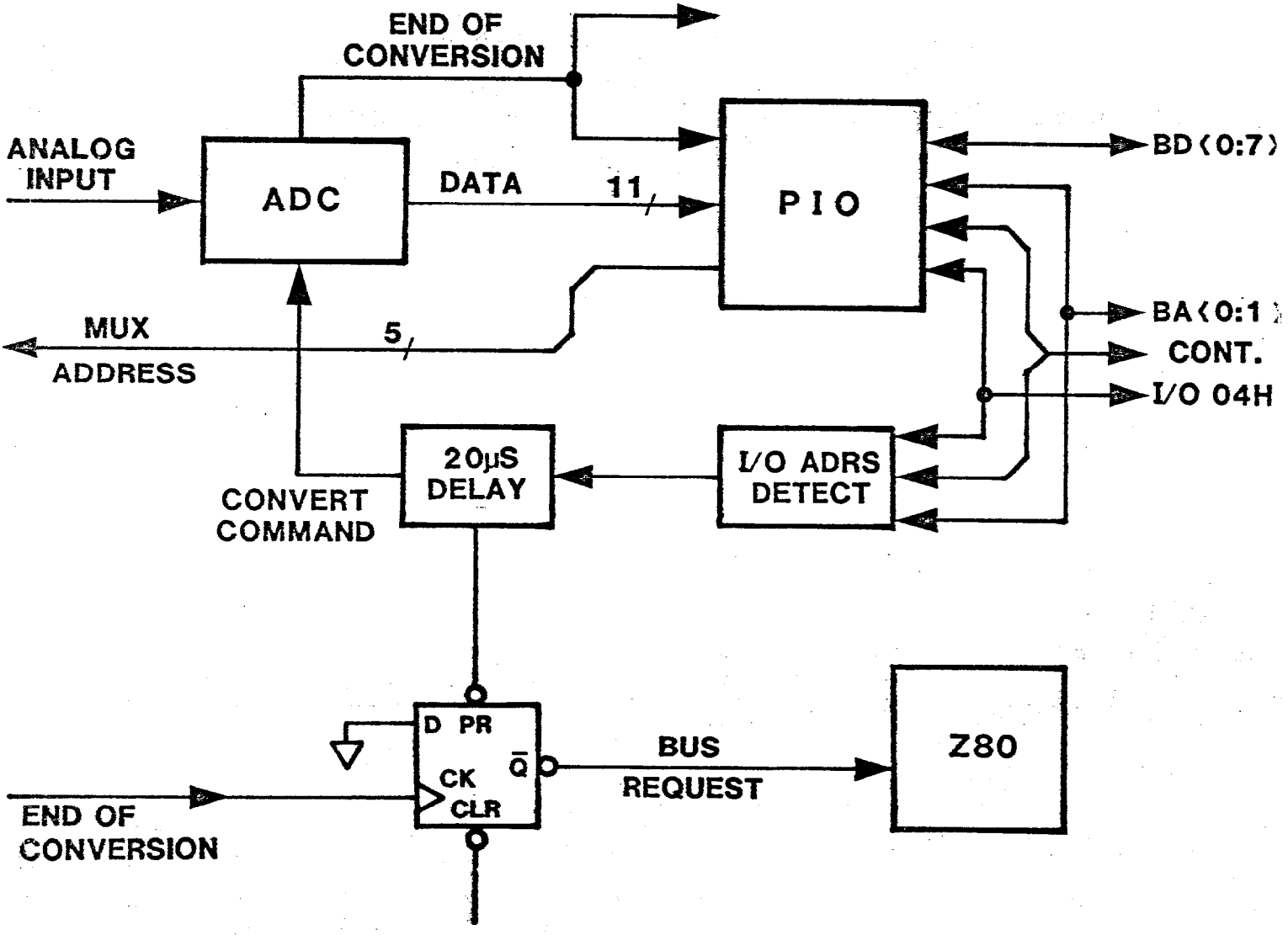


FIG. 5

CC48 - PORT B OF ADC PIO IS OPERATED IN MODE 3, AND Z80 OPERATION IS SUSPENDED DURING ADC CONVERSION

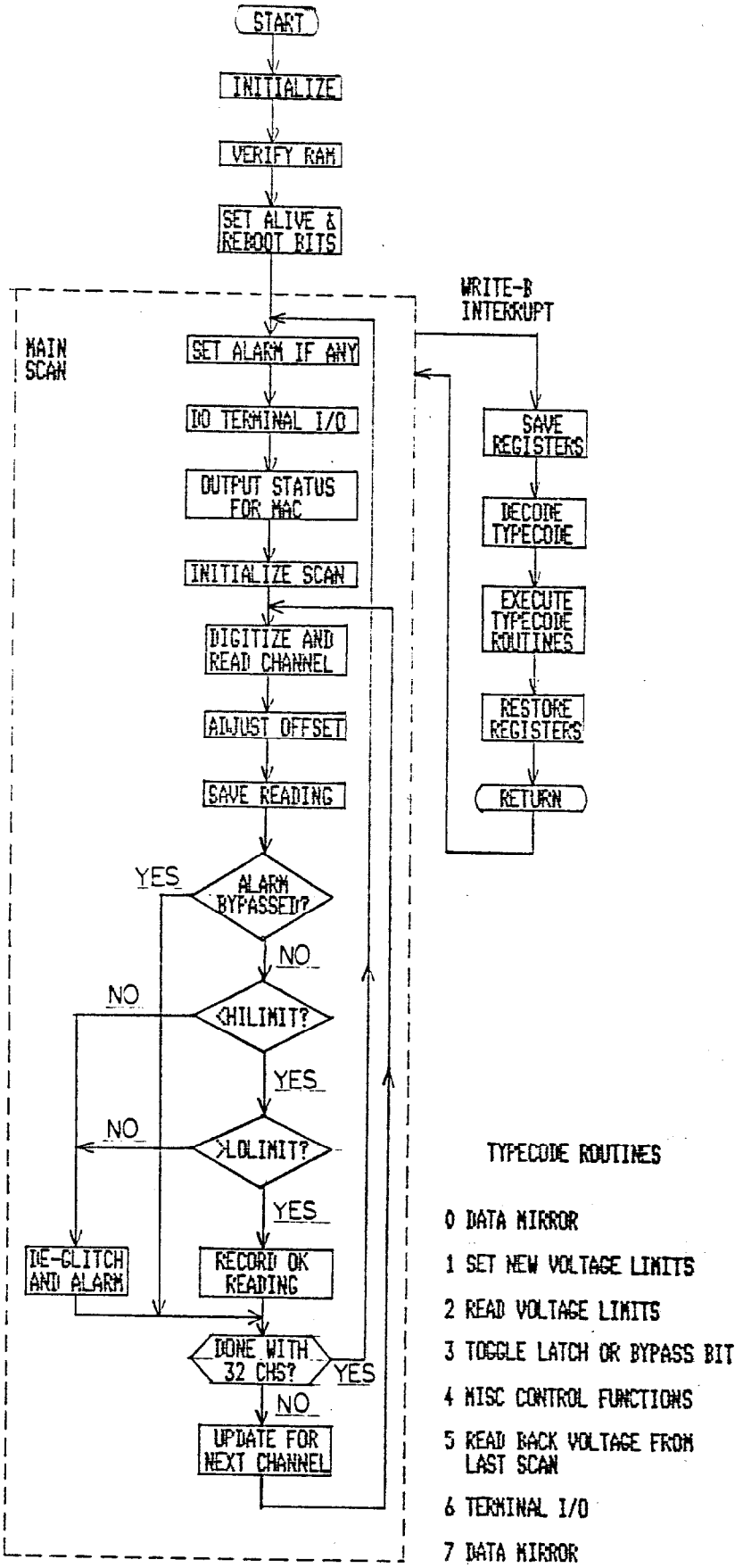


FIG. 6 CC48 SUPERVISORY PROGRAM FLOW CHART

```
                                                    06/17/82   1234
   CC48  VOLTAGE  /  TEMPERATURE  MONITOR
*INDEX                                  *DISPLAY+<20>-
*CVT  (BYPASS/ENABLE)
            AAAAAM00BBBBB111CCCCCC22222222233
            01234R67012343450123452345678901
ALARM         .....     .....       ....
DATA MIR      .....     .....       ....
I/O ERR       .....     .....       ....
LOCAL         .....     .....       ....
MEM VER       .....     .....       ....
RELOAD        .....     .....       ....
EQUIPPED      .....     .....       ....

            DDDDD333EEEEE444FFFFF555CCG5666A
            01234789012345670123434 5UR1901 2G
ALARM         .....     .....       ....
DATA MIR      .....     .....       ....
I/O ERR       .....     .....       ....
LOCAL         .....     .....       ....
MEM VER       .....     .....       ....
RELOAD        .....     .....       ....
EQUIPPED      .....     .....       ....

*EDIT  (0-15/16-31)
```

Fig. 7 Console Display on CC48 - Page 26.20

```
                                                    06/17/82  1239
   CC48  VOLTAGE / TEMPERATURE MONITOR
*INDEX                          *DISPLAY+<20>-
            CRATE -<E3>+
*EXIT   *RESET   *GLITCH SENSITIVITY ( 1)


CRATE     + 5      4.9        CVT  P.S.  +15*   0
CRATE     +15      15          PS  RK       -15   -15.11
CRATE     -15    -15.12        PS  RK       +15    15.15
GRND  REF   0    -.02          PS  RK        -  5   -5.06
SPARE       0     2            PS  RK        +  5    5.17
SPARE             1.66         PS  RK  SPARE        0
CRATE  TEMP.      105.6        PS  RK  SPARE        0
SPARE             2.78         PS  RK  SPARE        0
NIM  BIN  -24    -24.12        AUX  PS       -15    0
NIM  BIN  +24     24.03        AUX  PS       +15    0
NIM  BIN  -12    -12.03        AUX  PS        -  5   0
NIM  BIN  +12     12.03        AUX  PS        +  5   0
NIM  BIN  -6     -6.02         PS  RK     TEMP*   177.6
NIM  BIN  +6      6.02         CTLS  RK   TEMP*   177.6
NIM  SPARE        0            AUX  PS    TEMP*   177.6
NIM  SPARE        0            SPARE               0

*EDIT (0-15/16-31) *GET LIMITS FROM (   )
```

Fig. 8 Console Display on CC48 - Subpage Example

Table 1 CC48 Typecodes and Command Formats

Data Mirror
XXXX/XXXX/XXXX/XTTT
T = 000 (Typecode)
X = All 0's

Set a New Voltage Tolerance
DDDD/DDHW/CCCC/CTTT
T = 001 (Typecode)
C = Channel on the A/D Mux (0-31)
W = Which Voltage Limit (0-Low Limit, 1 - High Limit)
H = Which Half (0-Leftmost 6 Bits, 1-Rightmost 5 Bits)
D = Data (The 6 or 5 Bits, Left Justified)

Retrieve One Voltage Limit
0000/000W/CCCC/CTTT
T = 010 (Typecode)
C = Channel (0-31)
W = Which Voltage Limit (0-Low Limit, 1-High Limit)

Toggle Alarm Latch of Bypass Bits
0000/000B/CCCC/CTTT
T = 011 (Typecode)
C = Channel (0-31)
B = Bit Table (0-Latch Bits, 1-Bypass Bits)

Miscellaneous Control Functions
LVIF/GRSB/PPPP/PTTT
T = 100 (Typecode)
P = New De-Glitch Parameter (If G=1)
B = Bit Table (0-Latch Bits, 1-Bypass Bits) (If R=1)
S = Set of Bits (0-Channels 0-15, 1-Channels 16-31) (If R=1)
R = Read 16 Bits from Bit Table (If R=1)
G = Load New De-Glitch Parameter (If G=1)
F = Clear 'Reboot Me' Flag (If F=1)
I = Initialize the Program
V = Verify the RAM (If V=1)
L = Clear All Latch Bits (If L=1)

Read Back Voltage from Last Scan
0000/0000/CCCC/CTTT
T = 101 (Typecode)
C = Channel (0-31)

Read and Write from to Terminal
BBBB/BBBB/000S/STTT
T = 110 (Typecode)
S = Subtype 0-Read Character from Terminal
1-Transmit Character to Terminal
2-Send PCI Command
3-Set PCI Mode
B = Byte (Character to output, PCI Mode, or PCI Command)

Data Mirror
XXXX/XXXX/XXXX/XTTT
T = 111 (Typecode)
X = All 1's