ISBN: 978-3-95450-231-8 ISSN: 2673-5490 doi: 10.18429/JACoW-IPAC2023-THPA163

ULTRA-FAST GENERATOR FOR IMPACT IONIZATION TRIGGERING*

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Abstract

In recent years, it has been discovered that thyristors triggered in impact ionization mode find their dI/dt capability boosted by up to three orders of magnitude. This innovative triggering requires applying an important overvoltage on the anode-cathode of the thyristor with a slew rate > 1 kV/ns. Compact pulse generators based on commercial off the shelf components (COTS) would allow the spread of this technology into numerous applications, including fast kicker generators for particle accelerators.

Our approach for such a compact pulse generator begins with a HV SiC MOS with an ultra-fast super-boosting gate driver. Super boosting in the gate of a 1.7 kV rated SiC MOS allows to reduce its rise time by a factor of ≈30 (datasheet tr = 20 ns vs. measured tr < 680 ps), resulting in an output voltage slew rate > 1 kV/ns and an amplitude > 1 kV.

Next, additional boosting is obtained by a Marx generator with D2PAK thyristors, reaching an output voltage slew rate > 16 kV/ns. Finally, creating sufficient current necessary for the triggering of a big thyristor presents a new challenge. In this paper, we present an upgraded board design with a higher current output capacity.

INTRODUCTION

The transfer of particle beams in accelerator facilities often requires magnets that use pulse generators capable of producing high voltage and current levels in the multi kV/kA range. Thyratrons are currently used for this purpose, but they have various drawbacks such as risk of erratic firing, complex triggering and biasing electronics, high cost, rarity, and approaching obsolescence. Therefore, there is a need for an alternative, and semiconductor switches are being considered as a replacement.

Recent studies have shown that thyristors switched in impact ionization mode could replace thyratrons [1]. This technique achieves ultra-fast switching through the creation of an ionization wavefront in the semiconductor structure when subjected to high dU/dt and a sufficient overvoltage. Thyristors are cheaper than thyratrons and offer higher current density, making them an attractive alternative.

In previous works [2] authors used drift step recovery diodes (DSRD) and semiconductor opening switch (SOS) diodes as triggering generators for impact ionization, but these are not commercially available, require bulky designs, and have relatively long pre-charging phases. To address these issues, a new approach is proposed using COTS components in a compact topology that requires no pre-charging.

Our previous publication [3] provides details on the conditions required to achieve impact ionization on a thyristor. The triggering circuit needs to apply a voltage on the anode-cathode of the thyristor that exceeds twice its static breakdown voltage. To achieve the necessary conditions in the semiconductor structure, a slew rate of over 1 kV/ns is required for the triggering voltage. Additionally, the triggering circuit must supply sufficient current to charge the parasitic capacitance of the thyristor with the required dU/dt.

Our current focus is on enhancing the output voltage, slew rate, and current of the super-boosting driver to accelerate the commutation time of the SiC MOS and prepare the driver for higher MOS gate loads.

METHODOLOGY

The first stage of our thyristor triggering has been described in our previous works [4, 5]: we have enhanced the gate boosting technology initially developed at KIT [6], resulting in a gate driver that can deliver higher maximum output voltage (≈ 300 V), as well as a faster output voltage slew rate. The concept of gate boosting involves applying a significant overvoltage to the MOS gate to offset the impact of its leads inductance and internal parasitic capacitance. This overvoltage is only applied during the commutation time, which is less than 1 ns, and after the process is complete, the gate voltage adheres to the manufacturer's recommended specifications.

Our work shows that by applying an aggressive gate-boosting approach to our SiC MOSFETs, it results in a remarkable acceleration of their rise time (calculated as 10-90% for all of our results) by a factor of ≈30, which varies depending on the device, as presented in [7].

To achieve a more aggressive MOS device boosting, as demonstrated in the method depicted in [5], we have designed a specialized driver capable of delivering 430 V/ns to a 50 Ω load, with a maximum output voltage exceeding 300 V. The resulting output voltage was presented in [3].

Based on our tests, we found that driver's output current limitation can present a bottleneck when driving one or multiple parallel SiC MOS with high gate charge.

Therefore, we propose a driver upgrade: a GaN FET current boosting stage in source follower configuration (Fig. 1), amplifying the output current and reducing the output stage's output impedance and loop surface (therefore reducing its stray inductance).

The key element of the GaN FET driver is the super boosted Si PMOS (PM) triggering a two stage Marx generator with two avalanche transistors as switches (Fig. 1). The

* This work has been sponsored by the Wolfgang Gentner Programme of the German Federal Ministry of Education and Research
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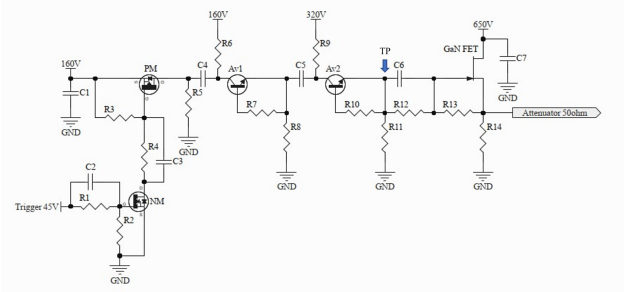

Figure 1: Schematic of the GaN FET driver.

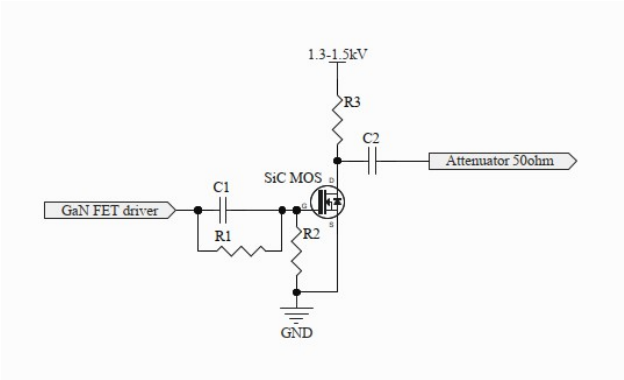

Figure 2: Schematic of the SiC MOS driving and output signals.

fast rising pulse of the PMOS drain (voltage on C1 = 160 V) is added to the collector-emitter voltage of Av1 (biased to 160V = voltage on its energy storage capacitor C4) and triggers an avalanche phenomenon on it. The sum of voltages of C1 and C4 is then added to the collector-emitter voltage of Av2 (biased to 320 V) and triggers subsequently an avalanche breakdown on it. At the end, the sum of the voltages on C1, C4 and C5 appears on the Av2 emitter (minus the voltage drops on PM, Av1, Av2 and the series resistances of the energy storage capacitors C1, C4 and C5), which makes it ready to drive the 650 V rated GaN FET (with the decoupling capacitor C7 ground close to the source of the SiC MOS that it is intended to drive) via its coupling capacitor C6.

This GaN FET in turn drives the gate of a 1.7 kV SiC MOS, as per Fig. 2. The advantage of adding this step in the driver after the avalanche transistors is that the GaN FET in the source follower configuration acts as an impedance transformer that reduces the load on the Marx generator. This results in a lower voltage drop on all transistors and energy storage capacitors in series, while also ensuring low output impedance and a significantly reduced output loop surface (reducing inductance). This greatly improves the output voltage swing, slew rate, and the maximum available current. This will guarantee that the voltage triggering the gate of the SiC MOS is not only sharpened, but the lower output impedance will also provide a higher current pulse.

All of these results are presented in the following section of this paper.

RESULTS

The driving circuit shown in Fig. 1 starts with a pulse trigger of 45 V, rise time 425 ps and slew rate ≈ 80 V/ns, as seen on Fig. 3. This is the result of boosting the 10 V, 2 ns output signal from a Philips PM5786B [8] pulse generator.

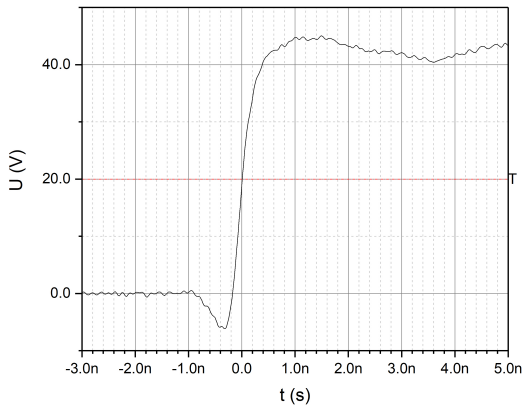

Figure 3: Triggering pulse on a 50 Ω load.

As it is, this first triggering signal needs improvement to deliver a voltage pulse with an ultra-fast rising edge. This is why we developed the first design for the SiC MOS driving described in our previous publications [3–5, 7], with an avalanche transistor that improved this signal.

However, the hereby presented driver design results in a much improved signal. The output at the second avalanche transistor level is a pulse of 520 V in amplitude and a rise time of 1.4 ns (Fig. 4). This measurement is taken at the test point marked ”TP” in Fig. 1 with a 50 Ω attenuator. Since this pulse is still not rising fast enough for our purposes, as we can see that after the first very sharp edge, the pulse loses its kick.

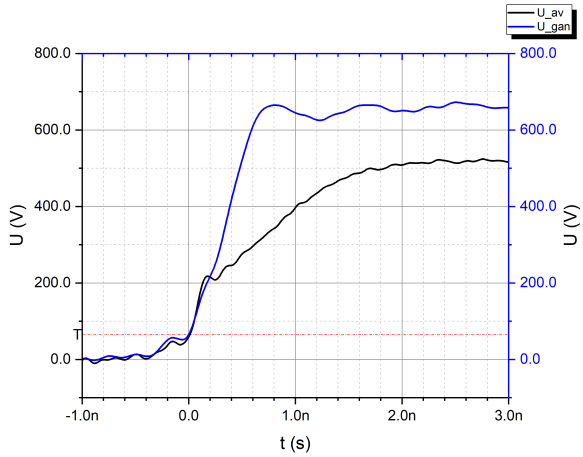

Figure 4: Output voltage of the second avalanche transistor (black) and the GaN FET (blue), respectively on a 50 Ω load.

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After the two avalanche transistors, the addition of a GaN FET operated at 690 V makes the driver able to deliver >670 V onto a 50 Ω load (Fig. 4) at ≈1.1 kV/ns in its fastest section. These are excellent conditions to trigger a MOS component in ultra-boosted mode.

In an attempt to find the limit of our approach we operated our setup above the maximum rating voltage. Operating a 650 V rated GaN FET at 690 V is safe since these devices only have a hard breakdown at 30% above their rated voltage, as stated in its datasheet [9].

Finally, the GaN FET triggers a 1.7 kV SiC MOS [10] working at 1.3 kV and this SiC MOS accomplishes an output pulse of 1.3 kV amplitude, a ≈ 550 ps rise time and a maximum slew rate of ≈ 2 kV/ns, as per Fig. 5.

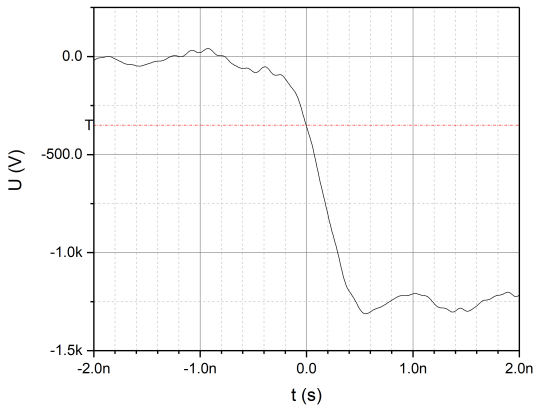

Figure 5: Output voltage of the 1.7 kV SiC MOS on a 50 Ω load.

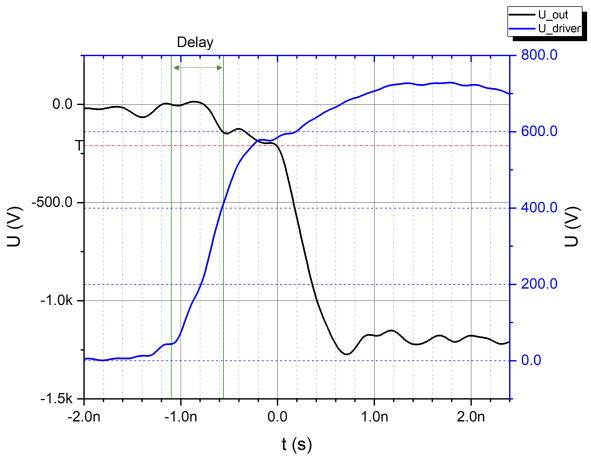

Figure 6: Output voltage of the 1.7 kV SiC MOS (black) and 650 V GaN FET (blue) on a 50 Ω load.

It is worth mentioning that the turn-on delay of the output signal is <450 ps (green lines in Fig. 6), which is significantly shorter (≈ 60x reduction) than the 27 ns reported on the datasheet [10] for the transistor, a significant advantage of this triggering method. Figure 6 shows both the driving (U_driver) and the output (U_out) signals, whose length mismatch of 140 ps has been corrected. The 50 Ω from the GaN output test point induces a loss in slew rate at the SiC output due to the added load at its gate.

Summing up, the use of two avalanche transistors and a GaN FET in series as the driving section allows for an extremely sharpened rising edge, which results in slew rates that can reach values higher than 1 kV/ns for the driving pulse. This is essential in order to subsequently trigger high voltage MOS components in ultra-boosted mode. Indeed, we have shown that a 1.7 kV rated SiC MOS can achieve an output pulse of 1.45 kV and a maximum slew rate of ≈ 2.5 kV/ns. The rise time is accelerated by a 36x factor.

CONCLUSION

In conclusion, we have presented a new method for increasing the current output of our driver circuit, with a highly performant outcome.

These ultra-boosted components will be utilized to trigger an ultra-fast Marx generator capable of generating higher output voltage and current than the one previously described in [3], in view of triggering a high voltage, 5 cm diameter puck thyristor.

Our ultimate goal is to trigger a larger stack of thyristors, reaching higher output voltage and current. This advancement has the potential to replace thyratrons in beam transfer facilities for particle accelerators, offering a more reliable and cost-effective alternative to traditional thyratron-based systems.

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