A low jitter all - digital phase - locked loop in 180 nm CMOS technology

2016 J. Phys.: Conf. Ser. 675 042042

(http://iopscience.iop.org/1742-6596/675/4/042042)

A low jitter all – digital phase – locked loop in 180 nm CMOS technology

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Abstract. An all-digital phase locked loop (ADPLL) was implemented in 180 nm CMOS technology. The proposed ADPLL uses a digitally controlled oscillator to achieve 3 ps resolution. The pure digital phase locked loop is attractive because it is less sensitive to noise and operating conditions than its analog counterpart. The proposed ADPLL can be easily applied to different process as a soft IP block, making it very suitable for system-on-chip applications.

1. Introduction

The PLL is a self-correcting control system in which one signal chases another signal. PLLs can be classified into the four categories shown in Table 1. ADPLL receives only digital signals. The phase and frequency information can be more accurately stored using digital techniques. Digital PLLs allow a faster lock time to be achieved and are attractive for clock generation on high performance microprocessors.

Table 1. Types of PPL.

Types of PPL	Comparison	Evaluation	Storage	Oscillator
Linear PLL (LPLL)	Analog multiplier	LPF	Analog voltage on filter capacitor	VCO
Digital PLL (DPLL)	EXOR PD or JKPD	LPF	Analog voltage on filter capacitor	VCO
Charge-pump PLL (CPPLL)	PFD	Charge pump and LPF	Analog voltage on filter capacitor	VCO
All-digital PLL (ADPLL)	EXOR PD or JKPD or PFD	Digital LPF	Digital word	Digitally controlled oscillator (DCO)

A diagram of an ADPLL is shown in figure 1. An ADPLL consists of the following represented blocks: Phase Frequency Detector Controller (PFD_CTRL), digitally controlled oscillator (DCO) and Frequency Divider (FD). The DCO is the most critical component in ADPLL design.

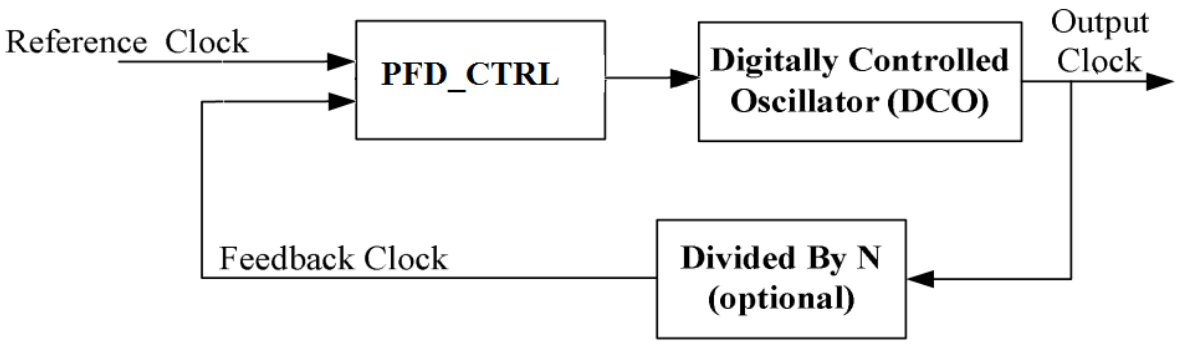

Figure 1. A typical ADPLL Block diagram.

The components of ADPLL are similar to the analog PLL, but the implementation consists of digital components. A voltage controlled oscillator was utilized instead of a digitally controlled oscillator. The PFD_CTRL detects the phase and frequency mismatch of the reference clock and divided DCO clock. Phase Frequency Detector compares the frequency and outputs a signal delay, advance or equivalence. The ADPLL is locked when the PFD_CTRL detects, that the phase and frequency of the two clock inputs match. The output signal of DCO, becomes close to the reference frequency.

The different applications of ADPLL are discussed [1-5]. All the components are created in Verilog, except DCO. DCO contains schematically based components.

2. ADPLL design

2.1. Phase Frequency Detector Controller

A diagram of PFD_CTRL is shown in figure 2. Waveforms of Phase Frequency Detector is shown in figure 3. The phase detector compares the reference frequency (FREF) with a frequency of divider (DCO_CLK). To begin the comparison unit should get a signal started (START). The signal sampling

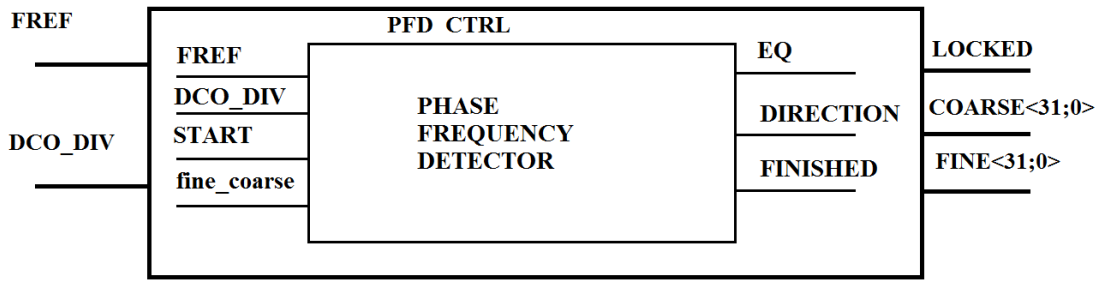

Figure 2. PFD_CTRL diagram.

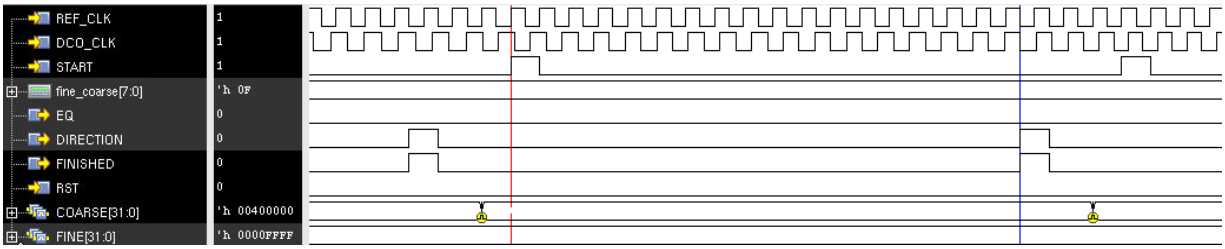

Figure 3. Waveforms of Phase Frequency Detector.

mode comparisons COARSE or FINE (fine_coarse). At the end of phase comparison of the two signals at the end of the iteration signal is generated (FINISHED), the direction (DIREKTION) and equivalence (EQ). FINISHED marks the end of the iteration, the direction indicates that the signal is late or ahead of the reference frequency. The signal EQ marks equity compared frequencies. The length of the account, which can be customized, determines resolution of the phase detector.

A novel frequency detector with variable resolution is used. PFD consists of two counters, which counts clock edges of divided DCO output signal and reference clock signal. When number of reference clock edges achieves maximum, PFD stops and DCO control code changes according to the frequency comparison result. FD accuracy is specified by the maximum counter value, which is different for coarse and fine tuning.

2.2. Digitally Controlled Oscillator

This article describes a digital controlled oscillator for use in an all-digital phase-locked loop. The whole ring contains 32 buffers, which outputs are combined together through three-state invertors and connected to the input of the ring. RST forms the initial step. It also defines the generator is turned on or not: logical 0 – on, 1 – off. The DCO used a two-stage frequency setting – hard tuning (coarse) consisting of the delay circuit and the third state inverters, and fine tuning (fine), constructed from AND-NO elements. The actual ring length is determined by the coarse control one-hot code. In this way, coarse frequency tuning is carried out. To perform fine frequency tuning 32 NAND gates are connected in parallel to the DCO ring. Effective loading capacitance of the NAND gates is determined by the fine control temperature code. The frequency range of the DCO from 170 – 670 MHz With the step of coarse tuning to 15 MHz and 0.5 MHz is fine.

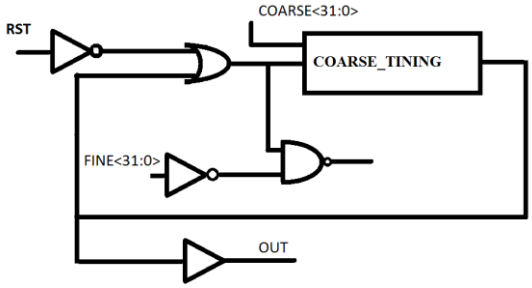

Figure 4. Digitally Controlled Oscillator diagram.

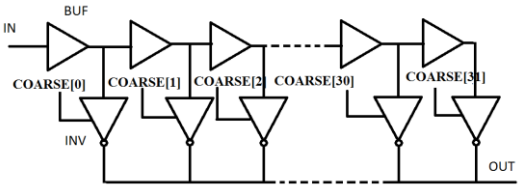

Figure 5. COARSE_TINING of DCO.

2.3 Frequency Divider

The output of the DCO needs to be divided to match the reference frequency. The implementation contains a divide by four frequency state, enabling the ADPLL to have a multiplication factor of 8, 16, 32, 64. The divider is implemented by using two series D Flip-flops by four times. In divider use a multiplexer for selection divider state.

3. Results and comparisons

The ADPLL was found to lock time at 2 μs. The reference frequency was at 80 MHz. For one iteration COARSE setting mode requires 21 clock. For FINE iteration must be 133 cycles. The power of used by the ADPLL system is 6.34 mW. The frequency range of the DCO from 170 - 670 MHz. When the voltage of 0.1 V, the frequency reference DCO falls to 60 MHz. By increasing the temperature by 1 ºC rate falls to 1.2 MHz The supply voltage of the system is 1.8 V.

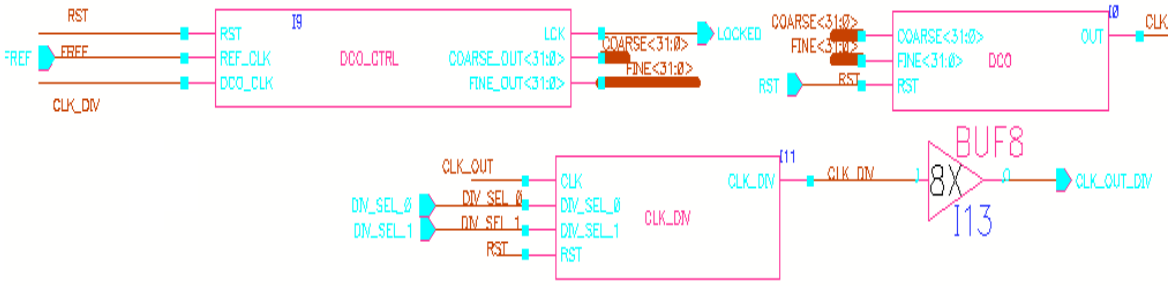

Figure 6. The final system of ADPLL.

4. Conclusion

The paper describes the concept and ADPLL behavioral model of each block. The results can be considered successful - the simulation results are quite good compared to other similar models ADPLL. A good lock time was achieved of 175 cycles and considerations for power were implemented in this project. The work was performed at UMC 180nm technology with a supply voltage 1.8 V. The implementation of the presented ADPLL block focused on the area minimization and design efficiency. The block utilizes only standard digital cells. This significantly reduces design time. The designed ADPLL may be used as IP-block of application-specific SoCs in particular intended for experimental physics' apparatus.

Acknowledgements

This work was supported by Grant No. 14.A12.31.0002, issued by the Russian Federation Ministry of Education and Science according to the RF Governmental resolution No 220. This work was partially supported by MEPhI Academic Excellence Project (contract № 02.a03.21.0005, 27.08.2013).

References

[1] Khalil A H, Ibrahim K T and Salama A E 2002 Digital of ADPLL for good phase and frequency tracking performance *Proc. of the Nineteenth National Radio Science Conf. (Alexandria)* pp 284-90

[2] Olsson T and Nilsson P 2004 A digitally controlled PLL for SoC applications *IEEE J. of Solid-State Circuits* **39** 751-60

[3] Yang S-Y *et al.* 2009 A 7.1 mW 10 GHz all-digital frequency synthesizer with dynamically reconfigurable digital loop filter in 90 nm CMOS *IEEE Int. Solid-State Circuits Conf. - Digest of Technical Papers* pp 90–1

[4] Kumn M and Klingbeil H 2010 An FPGA-Based Linear All- Digital Phase-Locked Loop *IEEE Trans. on circuit and systems* **57**(9)

[5] Yau T Y and Caohuu T 2011 An Efficient All-Digital Phase-Locked Loop with Input Fault Detection *Proc. of IEEE Conference, Information Science and Applications* pp 103-10