Fermi National Accelerator Laboratory

FERMILAB-Conf-99/319

The Design and PCB Layout of the CDF Run 2 Calorimetry Readout Module

Theresa Shaw, Charles Nelson and Thomas Wesson

Fermi National Accelerator Laboratory
P.O. Box 500, Batavia, Illinois 60510

November 1999

Published Proceedings of the *1999 IEEE Nuclear Science Symposium and Medical Imaging Conference*, Seattle, Washington, October 24-30, 1999

Operated by Universities Research Association Inc. under Contract No. DE-AC02-76CH03000 with the United States Department of Energy

The Design and PCB Layout of the CDF Run 2 Calorimetry Readout Module

Theresa Shaw, Charles Nelson and Thomas Wesson
Fermilab, P.O. Box 500, Batavia, Illinois 60510

Abstract

The CDF Calorimetry Readout module, called the ADMEM, has been designed to contain both the analog circuitry which digitizes the phototube charge pulses, and the digital logic which supports the readout of the results through the CDF Run 2 DAQ system. The ADMEM module is a 9Ux400mm VMEbus module, which is housed in a CDF VMEbus VIPA crate. The ADMEM must support near deadtimeless operation, with data being digititized and stored for possible readout every 132ns or 7.6 Mhz. This paper will discuss the implementation of the analog and digital portions of the ADMEM module, and how the board was laid out to avoid the coupling of digital noise into the analog circuitry.

I. INTRODUCTION

The upgraded CDF data acquisition (DAQ) system[1], see figure 1, will be capable of running at a rate of up to 1000 Hz into a Level 3 processing farm and will approach a deadtimeless system. To accomplish this goal it becomes necessary to digitize the detector data at every beam crossing (132 ns).

The analog data from the calorimeter is received by the **AD**C/**MEM**ory (ADMEM)[2] modules. The function of the ADMEM module will be to receive the analog information (current pulses from the phototube bases), digitize it at a rate of 7.6 MHz, store the result in a pipeline, and move the data that passes the Level 1 trigger decision into one of four L2 Decision buffers. The L2 Decision buffers will be accessible as slave memory through VMEbus. Figure 2 provides a functional block diagram of the module.

The ADMEM board also provides phototube tower sums[3] to the L1 Trigger. Channel values from the ADCs will be digitally summed together across up to four channels. Pedestal subtraction will be done prior to tube summing. Sine theta weighting of the trigger sum will be done by running the digital sum through a lookup table.

The data in the L2 Decision buffers will be read out via a VMEbus Readout Controller (VRC) and sent upstream on serial lines to VMEbus Readout Buffer[4] (VRB) modules. These VRB modules will serve to concentrate the data for readout by the Scanner CPU (SCPU) over VMEbus. The SCPU will service the movement of the data onto the data switch, through which it is routed into the Level 3 processing farm.

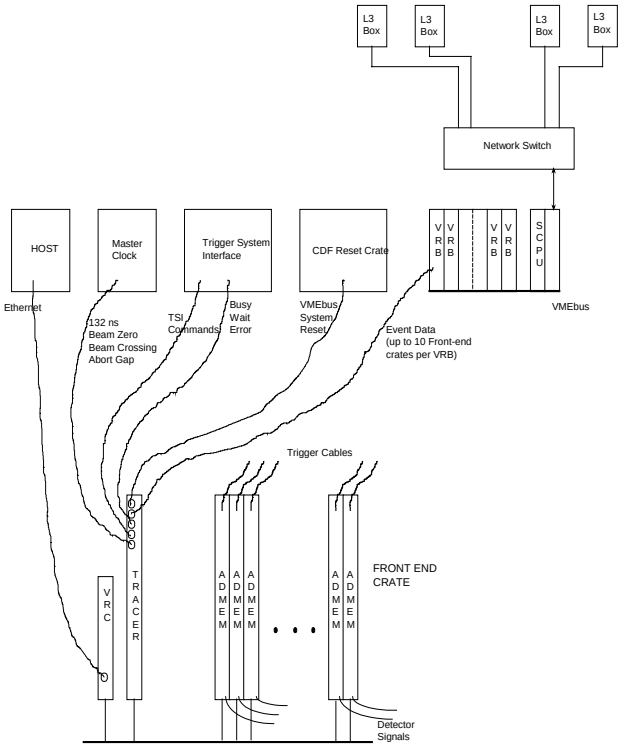

Figure 1: CDF Run 2 DAQ Architecture

II. ANALOG SECTION

The Analog Front-end portion of the ADMEM board will be implemented on removable CAFÉ modules. The CAFÉ modules populate up to twenty 72-pin SIMM sockets, with each CAFÉ module servicing a single channel.

Each CAFÉ module receives current pulses from a calorimetry photomultiplier tube. A functional block diagram of the Café module can be seen in figure 3.

The input section of the CAFÉ Module consists of a current buffer which will receive these pulses and drive the signal to a QIE[5] chip. The Input Section also provides the logic to do a DC current calibration and a source calibration. Analog switches are used to select among the different input functions.

The QIE Section makes use of a custom ASIC designed at Fermilab. The QIE uses a current splitter and integrates charge on eight non-overlapping binary scales. It then selects the correct range, and puts out a two bit capacitor ID (identifying one of four sets of internal capacitors used), a three bit exponent

[1]Work supported by the U.S. Department of Energy under contract No. DE-AC02-76CH03000.

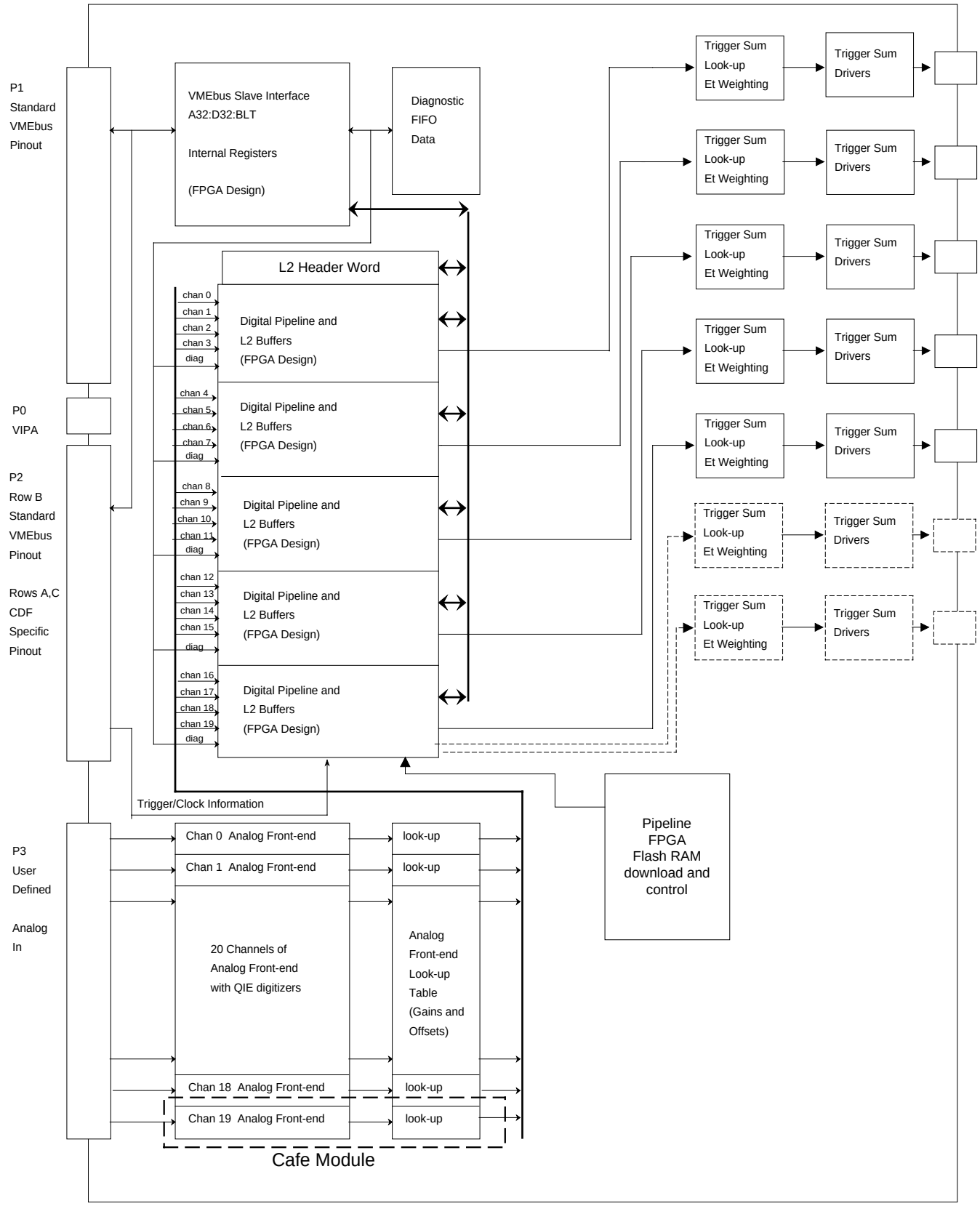

Figure 2: Block Diagram of ADMEM

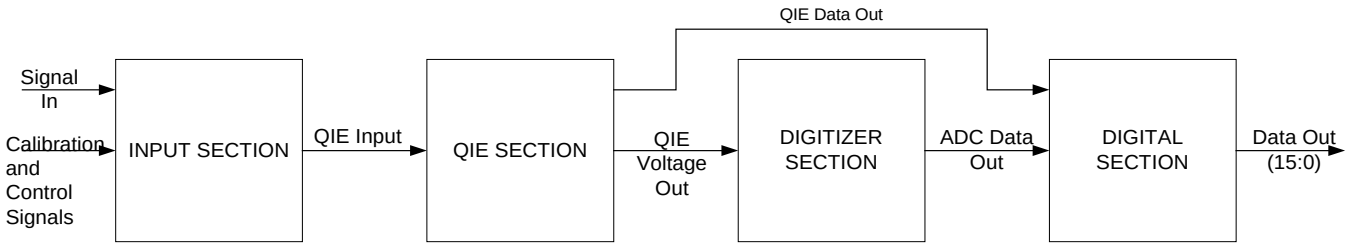

Figure 3: Block Diagram of CAFÉ Module

(identifying which of eight scales the current pulse falls in) and which of eight scales the current pulse falls in) and an analog output which is fed into a 10 bit Flash ADC.

The Digitizer Section consists of a 10 bit Flash ADC which is operating at the crossing rate of 7.6 Mhz.

The digital data coming from the QIE and the result of the Digitizer Section are fed into the Digital Section. The Digital Section consists logic to synchronize the Flash ADC data and the QIE digital data, as well as a 1Mb Flash RAM. The Flash RAM is used as a look-up table to linearize the results. The look-up table allows the user to subtract pedestals, adjust for offsets and gains.

The data from the CAFÉ module is then passed to the digital pipeline FPGAs is in the form of 15 data bits with a x8 range bit.

III. DIGITAL SECTION

The Digital sections of the ADMEM have been primarily designed by using Xilinx FPGAs[6]. The L1 decision pipeline, trigger sum logic, L2 buffers and VMEbus slave are all designed with Xilinx devices. Flash RAM has been used to implement look-up tables to supply sine theta weighting to trigger sums.

A. Digital Pipeline and Level 2 Buffers

The ADCs on the ADMEM module are required to digitize analog detector information every beam crossing (132 ns). This digitized data must be stored in a digital pipeline for a maximum period of 5+ us or 42 crossings. This is the period of time it takes the Level 1 trigger decision to reach the front-end crates. A Level 1 Accept causes the data to be written into one of four L2 Decision buffers, based upon the buffer address supplied by the Trigger System Interface (TSI)[7]. A Level 1 Reject will cause the data at the end of the storage pipeline to be lost.

The TSI will keep track of all Level 2 Decision buffer status. Buffers will be overwritten with new Level 1 Accept data if a Level 2 Reject has occurred on a given buffered event.

A Level 2 Accept will cause the VMEbus Readout Controller (VRC) to address each ADMEM card within the crate and do a block read of all channel data for a particular buffer address.

The digital pipeline and Level 2 buffers will be implemented with Xilinx FPGAs, see Figure 4. The Xilinx XC4013EPQ240-3 FPGA is the targeted device. The FPGA design takes in four channels worth of data from the Café Modules.

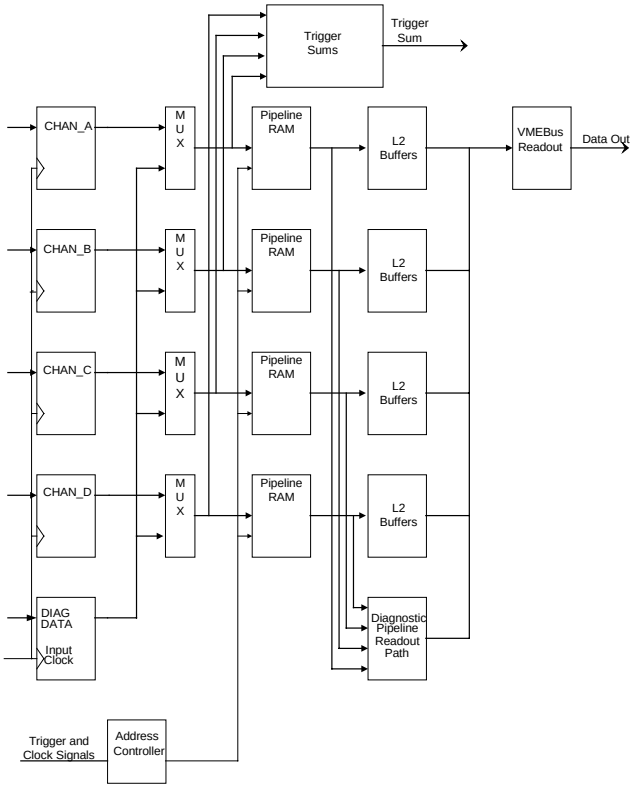

Figure 4: Block Diagram of Pipeline FPGA Design

A separate diagnostic path allows the user to send a pre-determined set of diagnostic data through the pipeline chip. The diagnostic data can be directed through a single channel or a

mask set of channels and comes from the Diagnostic FIFO, as shown in the ADMEM block diagram (Fig. 2). The FIFO data is 8k deep and will loop back on itself when the FIFO empties, presenting a steady stream of user supplied data.

A multiplexing stage allows the user to select between the diagnostic data path or the default Café module data. At the output of the multiplex stage, data is moved into both the pipeline stage (implemented as a circular buffer) and the Trigger Sum logic.

At the end of the pipeline stage, four L2 Decision buffers have been implemented. A L1 Accept will move the data at the end of the pipeline into a L2 Decision buffer, a L1 Reject will cause the data to be thrown away.

Trigger Sums are formed by adding up to four channels worth of data. The Trigger Sum data is then sent out of the FPGA, to the Trigger Sum look-up tables.

B. Phototube Tower Sums

ADMEM boards must provide phototube channel sums to the Trigger. Values from one to four channels will be summed together digitally. The pipeline chip will provide up to 15 trigger sum bits. The bits will the be fed into the lookup memories where they are mapped into ten trigger sum output bits. Et weighting will be done through the lookup memories.

The Flash RAM used for the Trigger Sum look up tables are identical to those used by the Café Modules.

To form a trigger sum, the following logic is applied

- Read in the 16 bits of data coming from the Café module.
- Subtract an 8 bit pedestal (programmed by user).
- If the MSB is set, multiply the number by 8 - all numbers are now 18 bits.
- Add 1, 2, or 4 (depending on the type of trigger sum) of these numbers together to get the raw Trigger Sum.
- Select 15 bits of the Trigger Sum which will be presented to the Look-up Table.
- Data which has been sine theta weighted comes out of the Trigger Sum Look-up Tables.
- The sums will be transmitted to the trigger system on parallel copper cable, using LVDS drivers, through connectors on the front panel at a rate of one sum per crossing (where a crossing is assumed to be 132 ns).

C. The L2 Header Word

The L2 Header word[8] is defined by the CDF Run 2 experiment to contain a Bunch ID, and board identification information. It is the first word which is to be read out of a L2 buffer Space. This word is used to verify synchronization of modules across the experiment. The ADMEM implements this header word in a Xilinx FPGA.

D. VMEbus Slave Interface

The ADMEM will implement the CDF Run 2 specified version of a VMEbus slave interface. Only 32 bit aligned data transfers will be supported; these may be either single word transfers or block transfers. Only extended (32-bit) addressing modes will be supported. All boards will be assigned a unique geographical address through use of backplane pins on the VIPA[9] J1 backplane. ADMEM modules will respond to the following address modifier codes: 09, and 0B.

E. Configuration of the Module

The Xilinx FPGAs which are used for the Pipeline, L2 Header, and the CAFÉ Timing on the ADMEM board are downloaded from Flash RAM.

This makes it fairly easy to implement design changes or implement special functionality. For example, already two flavors of ADMEM are planned to deal with the Central and Plug Calorimeters. Separate trigger algorithms are required by the two calorimeters.

Special ADMEM boards will also be used to implement CDF's lumonosity monitor (LUMON) and Time Of Flight (TOF) systems.

IV. PCB LAYOUT

Initial prototyping of the ADMEM revealed definite signs that digital noise was coupling into Analog sections of the board. Our second attempt at producing a printed circuit board made use of some special layout techniques and components, which allowed the analog section to exist with the digital section on the ADMEM and to reside within a primarily digital crate. When producing the production layout of the ADMEM printed circuit module, we took special efforts to keep high frequency digital noise from coupling into the Analog power supplies and returns. The analog power, by definition of the VIPA crate, comes in on the P0 connector which is located in the middle of the side of the board plugging into the backplane. There is a lot of potential digital activity in this area.

We bring analog powers and returns into the board through a EMI Suppression Filter produced by Murata Electronics, part number BNX002-01[10]. The analog power returns are not connected to the digital returns until they reach the CAFÉ modules.

After the EMI supression filter, the analog powers and returns are bussed above the PCB by using custom laminated

copper bus bars. This allows us to move the analog power path away from possible digital noise sources.

The analog power is brought down to large copper planes which roughly cover the bottom fifth of the ADMEM module. The CAFÉ modules, which populate the bottom quarter of the ADMEM, have been designed such that the top half contains all digital functionality and the bottom half contains the analog circuitry. The analog planes lie under the analog half of the CAFÉ modules. Digital power planes lie under the top half, or digital section, of the CAFÉ cards. There is no overlapping of digital and analog power planes. We carefully control signal routing so that no "analog" signal passes over a "digital" power plane, and vice versa. All power planes have a large number of bulk capacitors placed near the CAFÉ module sockets.

Finally, before any power is supplied to the CAFÉ card, it must pass through a ferrite bead which will look like a high impedance path to any high frequency noise. These layout changes reduced board level noise by more than a factor of ten.

V. CONCLUSION

The ADMEM board is now in use for vertical slice testing at CDF. The board is meeting all specifications.

VI. ACKNOWLEDGMENTS

We wish to thank Fermilab physicists Mike Lindgren, Steve Hahn, Hao Wei, Howard Budd, Willis Sakumoto and many others for the work they did to verify the ADMEM design.

VII. REFERENCES

[1] The CDF Collaboration, *Proposal for an Upgraded CDF Detector* , CDF/DOC/PUBLIC/1172, 1990.

[2] T. Shaw, Specification for ADC/Memory Module (ADMEM), December 15, 1998.

[3] P. Wilson, Specification for Trigger Tower Summing an ET Weighting CDF/DOC/TRIGGER/PUBLIC/ 4781, 1998.

[4] M. Bowden, et. al., VRB Readout Buffer/Fanout, Document # ESE-SVX-950719.

[5] R. Yarema, et al., A Pipelined Multiranging Integrator and Encoder ASIC for Fast Digitization of Photomultiplier Tube Signal, Fermilab-Conf-92/148.

T. Zimmerman and M. Sarraj, A second Generation Charge Integrator and Encoder ASIC, IEEE NS V43#3, June 1996.

[6] Xilinx FPGAs are manufactured by Xilinx, Inc. 2100 Logic Drive, San Jose, CA 95124.

[7] The Front-End/Trigger/DAQ upgrade group, The Clock for the CDF Upgrade CDF/DOC/PUBLIC/xxxx, 1993.

[8] K. Ohl, Specification of DAQ/Trigger Synchronization Checking Protocol and VME Board Header Word CDF/DOC/TRIGGER/CDFR/3145, May 10, 1995.

[9] E. Barsotti, et al., Specification for: VME64 Extensions 10U & 7U Subracks for Physics, Document # ESE-SVX-960305.

[10] The BNX002-01 is manufactured by Murata, Inc. 2200 Lake Park Drive, Smyrna, GA 30080.