Si/SiGe spin qubit device building blocks for scalable architectures

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1 Introduction

In 2025, the centenary of quantum mechanics marks a milestone in the history of a theory that has fundamentally transformed the understanding of the physical world. After experimental observations provided the first hints of quantum nature, 1925 marked the birth of quantum mechanics [1–4]. This fundamental change in the perception of the world through quantum physics not only had a tremendous impact on science but also paved the way for groundbreaking technological advancements, such as clean energy solutions like photovoltaics, precise time measurement with atomic clocks, semiconductor technology as the core of modern smart technologies, and magnetic resonance imaging as a key tool in medical diagnostics. Just as classical physics reached its limits in fully describing quantum nature, R. Feynman stated in 1981 [5] that classical computation faced fundamental constraints in simulating it and that computation itself should follow the rules of quantum mechanics to overcome these limitations. This realization sparked the idea of quantum computing, which has since become a major research field. The unique strength of quantum computing lies in encoding information in quantum mechanical states, enabling it to utilize quantum superposition and entanglement for computation. This fundamental distinction from classical computers makes quantum computing a promising counterpart for applications that can benefit from this unique form of computation. Beginning with the quantum algorithms of Deutsch-Jozsa [6], Grover [7], and Shor [8], the field has since seen a growing number of proposed applications, ranging from materials science and chemistry to logistics and optimization, encryption, machine learning and artificial intelligence. However, the full spectrum of potential applications has likely not yet been imagined. At this stage, the transformative impact of quantum computing can only be speculated, including the groundbreaking insights and technologies that may arise from it.

Since the first theoretical proposals, various approaches and physical systems have been competing in the ongoing race to realize a quantum computer. The fundamental requirements that a candidate for the physical implementation of a quantum computer has

to meet were formulated by D. DiVincenzo [9] in 2000, as follows:

- A scalable physical system with well-characterized qubits.
- The ability to initialize the state of the qubits to a simple fiducial state.
- A universal set of quantum gates.
- Long relevant decoherence times (longer than gate operation times).
- A qubit specific measurement capability (readout).

The qubit represents the quantum mechanical counterpart of a bit in a classical computer. While a classical bit, encoding either a 0 or 1, is commonly implemented in transistor-based circuits, a qubit can be any physical system that realizes a well-defined quantum mechanical two-level system with states $|0\rangle$ and $|1\rangle$. For computation with this system, the criteria state that it is necessary to initialize a well-defined state, perform computational operations before the information is lost, and read out the final computed state. As quantum mechanics manifests in nearly all physical systems, the possible implementations of quantum computers are equally diverse. The approaches span photonic qubits, trapped ion qubits, neutral atoms, nuclear spins in a liquid, semiconductor quantum dots, impurities in silicon or diamond, superconducting qubits, and Majorana qubits [10–12]. Each qubit platform comes with its own strengths and challenges, and it remains unclear which one will take the lead, while further advancements may still bring new platforms into consideration. Across all considered platforms the primary challenge toward realizing universal quantum computing nowadays is scalability, requiring a transition from proof-of-principle systems to millions of qubits estimated to be required for fault-tolerant computing [13].
A promising candidate for quantum computing, particularly in terms of scalability, are spin qubits in Si/SiGe quantum well semiconductor heterostructures. First proposed by D. Loss and D. DiVincenzo in 1998 [14], the use of single-electron spin states confined in quantum dots exploits their natural two-level system in a magnetic field for encoding qubit information. Choosing Si/SiGe as a material platform offers the advantage of low spin-orbit coupling and the availability of nuclear-spin-free isotopes. Naturally occurring silicon consists of only 4.7 % ^{29}Si, the only stable isotope carrying a nuclear spin. Additionally, it can be grown in an isotopically purified form (^{28}Si with < 60 ppm in our group). Compared to other material systems, such as GaAs, this results in long coherence times, with typical spin relaxation times T_1 on the order of seconds [15, 16] and decoherence times T_2^* reaching up to 20 µs [17, 18]. Furthermore, this qubit implementation has already shown all required qubit operations with sufficient fidelities in few-qubit systems. Initialization and readout have been achieved with a fidelity over 97 % [19]. Single-qubit operations have been demonstrated with gate times on the order of 100 ns [17], while two-qubit gate times range from tenths to hundreds of nanoseconds [20]. Single-qubit operation fidelities exceed 99.9 % [17], while two-qubit operation fidelities surpass 99 % [19, 21, 22]. So far, only few-qubit devices with up to 12 qubits have

been demonstrated [23, 24], yet the intrinsic properties of this platform make it a strong contender for rapid scaling. Its small physical footprint of only a few 100 nm per qubit enables high qubit densities, while its compatibility with industrial large-scale silicon semiconductor fabrication could allow fast scaling to system sizes capable of fault-tolerant operation. As pathways to scaling up, two fundamental architectural blueprints have been proposed for this platform. The first approach is a dense qubit architecture [25–27], featuring a tightly packed grid of qubits. However, an inherent challenge of this design is the inevitable crowding of gate electrodes and their wiring as the qubit count grows, commonly referred to as the fan-out problem. To address this, several strategies have been proposed, including multiplexing techniques, cross-bar arrays, and floating memory gates. Nonetheless, this design typically imposes strong requirements on the homogeneity of the quantum-dot potentials across the array, and many operations can only be executed sequentially. The second approach is a sparse qubit architecture [25, 28, 29], where intentionally more space is left between qubits to incorporate classical electronics on-chip. For qubit operations, transport links connect qubits, such as electron shuttling [30–32]. This design helps alleviate the fan-out problem and enables the on-chip integration of classical electronics for qubit operations.
Within this thesis, we address building blocks for scalable Si/SiGe spin qubit device architectures, beginning with gate-controlled undoped semiconductor field-effect stacks (FESs) as the basis of these qubit systems and the correlation of their stack details to their transport properties. It then explores the biased cooling effect on FES, which is closely linked to a precise understanding of electrostatics and device tuning. Furthermore, the thesis introduces a new sensor design for qubit readout with an enhanced output signal and concludes with the investigation of one of the first devices fabricated on an industrial fabrication line within the national research consortium QUASAR. These topics are covered in this thesis as follows:

- Chapter 2 introduces the fundamental concepts providing the framework for the research findings presented in this thesis.

- Chapter 3 examines five state-of-the-art FES, establishing correlations between their layer stack properties, fabrication details, and transport characteristics extracted from Hall-bar geometry magneto-transport measurements. This analysis, which provides direct access to the properties of the two-dimensional electron gas forming the basis for qubits, is vital as it yields insights that cannot be obtained from qubit device measurements, however, severely impacting qubit device operability.

- Chapter 4 systematically studies the effect of biased cooling, which refers to the cool-down of the FES with a non-zero voltage applied at the TG, an aspect that has not yet been considered in undoped Si/SiGe FES. We correlate this effect with changes in the amount of trapped charges at the dielectric/semiconductor interface and investigate how the modified electrostatics influence the transport properties of the 2DEG in the Si/SiGe quantum well. Additionally, we provide an empirical model for the biased cooling effect. These insights are also relevant to qubit devices,

as the dielectric/semiconductor interface represents a potential source of charge noise. Finally, we present an outlook on possible applications of the biased cooling effect in quantum circuits.

- Chapter 5 introduces a new proximal charge sensor design, termed the asymmetric sensing dot. This sensor concept leverages a significantly reduced capacitive coupling to the drain reservoir, enabling a substantial boost in output signal compared to conventional sensor dots. We present the asymmetric sensing dot concept and provide Coulomb diamond measurements to quantify the reduction in capacitive coupling across two material platforms: undoped Si/SiGe and doped GaAs/(Al,Ga)As. Additionally, we demonstrate the high output signal of the ASD in charge sensing measurements on a nearby qubit-like double quantum dot.

- Chapter 6 demonstrates the functionality of one of the first qubit devices fabricated in an industrial setting at Infineon Technologies Dresden's 200 mm production line, leveraging the advantages of the Si/SiGe material platform and its compatibility with well-established industrial silicon processing techniques, aiming toward scaling up to a large number of qubits. Furthermore, we use this device to investigate the influence of the magnetic field on the few-electron energy spectrum of the quantum dot, allowing us to determine a lower bound for the local valley splitting, which is a key material property that can be reliably measured in qubit devices but is not accessible via FES measurements. The underlying factors determining valley splitting remain an active topic of ongoing research.

2
Fundamentals

In this chapter, we provide an overview of the fundamental concepts underlying the research presented in this thesis. We start by discussing the Si/SiGe heterostructures that serve as the foundation for our spin qubit devices and examine charge carrier control through the field-effect including how the transport properties of the FES are characterized. Next, we present the characteristics of single and double quantum dots. The single quantum dot is also introduced in the functionality of a highly sensitive charge sensor. We then address the impact of magnetic fields on the single quantum dot few-electron energy spectrum. The chapter concludes by describing the experimental setups and magneto-transport measurement techniques employed.

2.1 Si/SiGe Field-Effect Stack

The foundation for our qubit devices are $Si_{1-x}Ge_x$/Si/$Si_{1-x}Ge_x$ quantum well FES capable of hosting a two-dimensional electron gas (2DEG).
A unique property of silicon (Si) and germanium (Ge) is their ability to form $Si_{1-x}Ge_x$ alloys with arbitrary compositions, enabling band structure tuning. Both elements crystallize in the diamond lattice structure, with lattice constants of $a_{Si} = 5.431\,Å$ and $a_{Ge} = 5.657\,Å$, respectively. Si has a band gap of $E_{G,Si} = 1.11\,eV$, while Ge has a smaller band gap of $E_{G,Ge} = 0.66\,eV$. In pure Si, the conduction band minimum lies along the $\langle 100 \rangle$ crystallographic direction, whereas in pure Ge, it is along the $\langle 111 \rangle$ direction. However, in $Si_{1-x}Ge_x$ alloys, once the Si content surpasses approximately 15%, the conduction band minimum shifts to the $\langle 100 \rangle$ direction. This shift, combined with the ability to tune the band gap by adjusting the Ge content, facilitates band structure engineering tailored to specific device requirements. [33]
This material platform allows the formation of a quantum well (QW) capable of hosting a 2DEG by the growth of a semiconductor heterostructure. The QW consists of a thin Si layer enclosed between SiGe layers, forming a type-II band alignment. This alignment

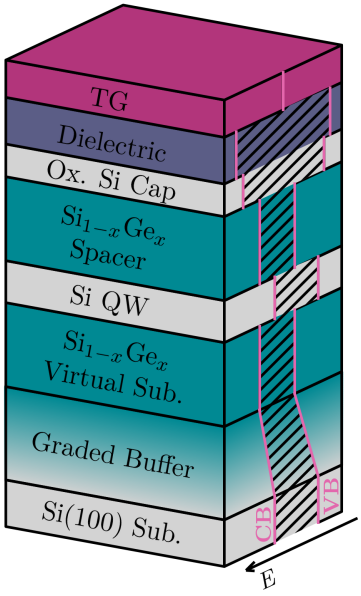

Figure 2.1: Cross-section schematic of an undoped Si/SiGe FESs. In the side view of the heterostructure, the band alignment of the conduction band (CB) and valence band (VB) across the different layers is illustrated, with the band gap represented as hatched regions.

confines electrons in the growth direction, leading to the formation of quantized energetic subbands. Due to the strong confinement, the energetic difference between the subbands is large enough that, within the operation window, only the first subband is populated, resulting in the formation of a 2DEG. A cross-sectional schematic of the undoped Si/SiGe FES with its band alignment is shown in Figure 2.1 with the growth direction from bottom to top. The epitaxial thin Si layer of the QW adapts its lattice constant to that of the relaxed SiGe layer beneath, resulting in tensile strain. This uniaxial strain induces a splitting of the sixfold degenerate conduction band minimum of Si into four equivalent in-plane valleys, which are energetically higher, and two valleys along the growth direction, which are energetically lower [33]. The remaining degeneracy of the two lower-lying valleys is also lifted, with the energy difference referred to as the valley splitting E_{VS}. This splitting results from a complex interplay between the electronic wave function and the properties of the QW heterostructure, which remains a subject of ongoing studies. Recent research points out that E_{VS} is highly sensitive to atomistic details [34–36].
In order to obtain relaxed $Si_{1-x}Ge_x$ with the desired Ge content x, a graded buffer is grown on a Si (100) substrate. This buffer gradually increases the Ge content before transitioning into a $Si_{1-x}Ge_x$ layer with a constant composition (virtual substrate). The resulting lattice mismatch during the composition change induces strain, which is relieved by the formation of dislocations extending along the growth direction of the crystal. The two most prominent types of dislocations are misfit dislocations and threading dislocations. Both dislocation types must either terminate at the crystal edges or intersect with another dislocation. Misfit dislocations typically propagate horizontally along the interface, while threading dislocations extend at an angle of approximately 60 degrees. As threading dislocations are more likely to penetrate the QW region, they pose a greater

challenge and are the dominant type impacting transport properties within Si/SiGe heterostructures [37, 38]. In addition to gradually increasing the Ge content within the graded buffer, introducing a virtual substrate between the buffer and the QW has been shown to significantly reduce threading dislocation density (TDD) in the QW. The virtual substrate allows threading dislocations to run out laterally of the crystal before reaching the QW region, with the reduction in TDD depending on the thickness of the virtual substrate. The heterostructure growth is completed with a Si cap layer, which becomes partially or fully oxidized. This cap protects the underlying SiGe from oxidation, as Ge forms an unstable, water-soluble oxide upon exposure to air, whereas Si forms a stable oxide layer that shields the structure.
Despite the structural confinement, no electrons are naturally present in the QW without additional steps to accumulate them. One method is modulation doping, where a dopant layer is embedded in the SiGe spacer during growth, spatially separated from the QW, inducing electrons within the QW. However, this approach has shown to be problematic regarding charge noise [39, 40] and gate hysteresis [40, 41]. This led to the adoption of gated undoped structures for qubit devices [42], an approach initially developed for quantum Hall effect studies [43], achieving record electron mobilities of up to $2.4 \times 10^6\,\mathrm{cm}^2/\mathrm{Vs}$ [44]. In this now commonly used approach, a metallic gate, which we will denote as top gate (TG), is fabricated on top of the heterostructure, separated by a dielectric layer, which allows for accumulation of electrons in the QW through the field-effect.

2.2 2DEG Accumulation via Field-Effect

The field-effect enables the accumulation and tuning of the carrier density in the 2DEG by applying a voltage to the TG. Fig. 2.2 illustrates the impact of the field-effect on the conduction band of an undoped Si/SiGe FES. For simplicity, the reference case of $U_{\mathrm{TG}} = 0\,\mathrm{V}$ is shown in panel a) with a flat band edge. The QW ground state lies above the Fermi level, resulting in no electrons (pink dots) being accumulated in the QW. Applying a $U_{\mathrm{TG}} \neq 0\,\mathrm{V}$ to the TG creates an electric field between the TG and the QW, which is kept at the reference potential. This is illustrated by pinning the deeper end of the QW (in the growth direction) at 0 V. The change in charge on the TG shifts its energy, and the resulting electric field induces a tilt in the conduction band between the TG and the QW. This tilt also shifts the ground state energy of the QW. In order to accumulate electrons within the QW, it is necessary to apply a $U_{\mathrm{TG}} > 0\,\mathrm{V}$ strong enough to drag the QW ground state below the Fermi energy ($U_{\mathrm{TG}} = U_{\mathrm{Acc}}$) as illustrated in panel b). Furthermore, to form a fully developed 2DEG, the system must overcome the metal-insulator transition [43, 45–48], which marks the phase change from insulating to metal-like conduction. This can be understood as requiring a critical electron density, n_{crit}, to overcome the inherently uneven potential landscape of the QW ground state. Initially, electrons fill isolated potential minima, and only after n_{crit} – which strongly depends on the FES properties – is exceeded, the electrons accumulate sufficiently to

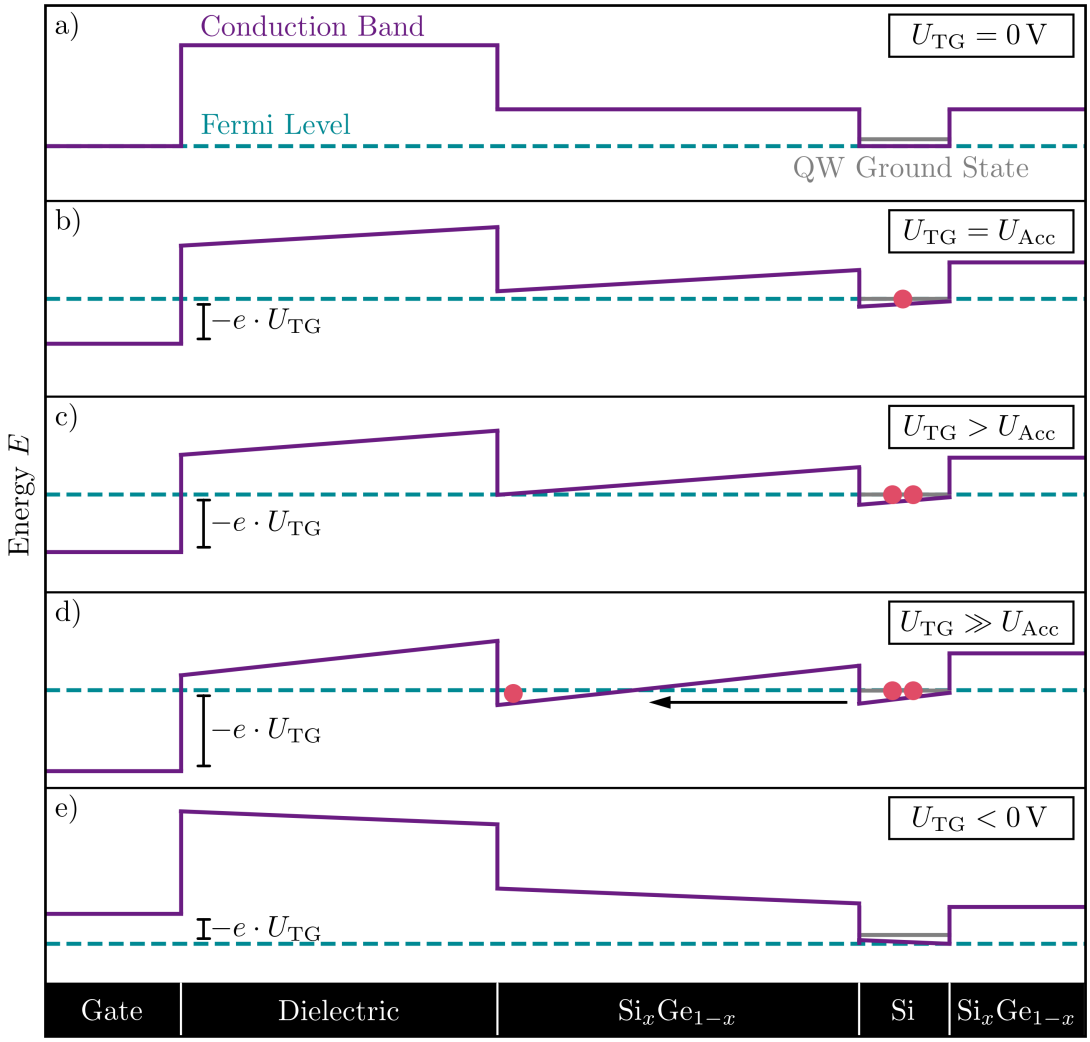

Figure 2.2: Field-effect impact on the conduction band of an undoped Si/SiGe FES. Panels a) to e) showcase the scenarios for different voltages U_{TG} applied at the TG, which are discussed in detail in the text. The purple line represents the conduction band edge for different regions of the gate stack, as indicated at the bottom of the figure. The dark gray line within the Si shows the confined ground state energy of the QW. The lower edge of the QW conduction band energy is fixed at 0 V. The blue dashed line illustrates the Fermi energy. The electrons, depicted as pink dots within the Si QW, represent the accumulation of the 2DEG.

form a uniformly connected 2DEG. Further increasing $U_{TG} > U_{Acc}$ increases the electron density n_e, illustrated in panel c). It has been observed that the TG and the QW behave similar to the two plates of a classical capacitor with a FES dependent capacitive coupling. Within this regime the n_e of the 2DEG within the QW depends linearly on the voltage U_{TG} applied at the TG [41, 49–52]. This approximation starts to break down as soon as the potential difference is strong enough for electrons to tunnel out of the QW, through the SiGe barrier, into the interface between the heterostructure and the dielectric, depicted in panel d). In this saturation regime, the n_e does not further increase with U_{TG} [41, 49–52]. Panel e) illustrates the scenario where a $U_{TG} < 0\,\mathrm{V}$ is applied. This shifts the TG upwards in energy and consequently raises the QW ground state, which does not result in the accumulation of electrons.
The field-effect not only enables the accumulation but also allows the modification of the electron density of the 2DEG within the QW in the FESs. For most applications, the operation range is restricted to the linear regime of the field-effect before saturation sets in. A large operation range is desirable to improve device tunability. Moreover, qubit applications – ultimately targeting the isolation of a single electron – are particularly interested in tunability within the low-density regime. This makes the U_{TG}-tunable n_e range a key property of the FES and an essential aspect of its characterization.

2.3 Field-Effect Stack Characterization via Hall-bar measurements

For the characterization of the FES, we utilize Hall-bar geometry magneto-transport measurements, which provide insights into the FES transport characteristics via the quantum Hall effect (QHE) and allow us to draw conclusions about FES properties, such as the TDD. A detailed derivation of the presented equations within this section can be found in [53, 54].
The foundation of these measurements is a conduction channel with well-defined width and length in the 2DEG. Since the FES are undoped, we can selectively accumulate the 2DEG exclusively beneath the TG. The gate geometry allows for the electrostatic definition of the shape of the accumulated, and thus conducting, regions. Fig. 2.3 a) shows a microscope image of a representative Hall-bar device, with the metal gates appearing in light yellow. The gate in the center is the TG, which defines the conduction channel by applying U_{TG}. The conduction channel has a width of $W = 20\,\mu\mathrm{m}$ and is divided into segments of length $L = 300\,\mu\mathrm{m}$. Each segment is equipped with electrical contacts at both ends, enabling direct electrical connection to the accumulated 2DEG in the QW. To achieve this, we utilize phosphorus-implanted and thus conducting regions. These implanted regions connect the outer metal gates, which serve as bond pads for wire bonding the device, to the accumulated QW beneath the TG. A corresponding region is representatively illustrated for one bond pad, outlined with a black frame. The corresponding layer stack for this region is illustrated in Fig. 2.3 b). The bond pads (orange) are fabricated, in contrast to

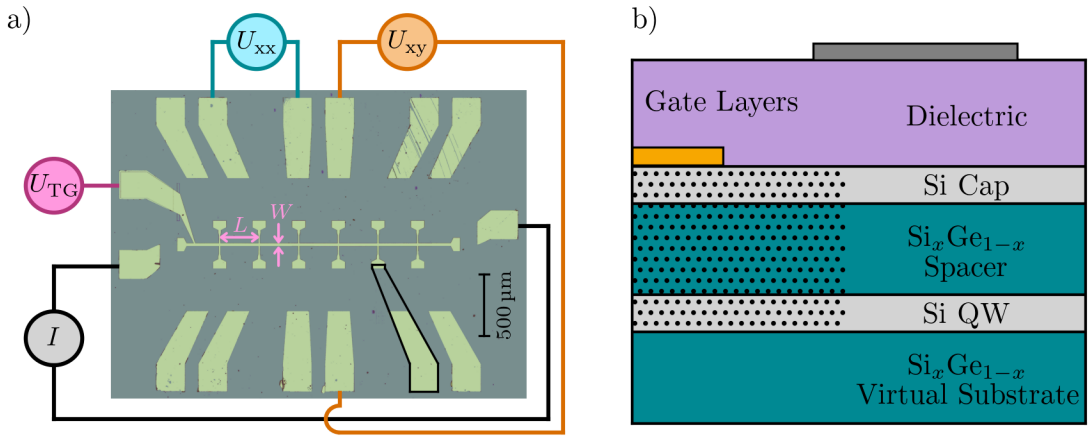

Figure 2.3: Hall-bar device layout and layer stack. a) Microscope image of a representative Hall-bar device. The light-yellow appearing regions are covered with metal gates, with its different layers depicted in panel b). The gate in the middle is the TG and electrostatically defines the conduction channel in the 2DEG by its shape. The outer metal pads are the bond pads, which are electrically connected to the TG accumulated region through implanted areas. An implanted area is representatively illustrated for one bond pad with a black frame and corresponds to the dotted region shown in panel b). The width $W = 20\,\mu\text{m}$ and length $L = 300\,\mu\text{m}$ of each Hall-bar segment is labeled in light pink. Additionally, a typical wiring configuration is illustrated: U_{TG} is applied at the TG, a current I is applied along the conduction channel, and contacts placed next to each other and opposite to each other are used to measure U_{xx} and U_{xy}, respectively. b) Schematic cross section of the layer stack. The bond pads (orange) are fabricated directly on top of the heterostructure and are in direct contact with implanted areas (dotted), enabling electrical connection to the QW. The TG is separated from the heterostructure by a dielectric layer and solely electrostatically defines the conduction channel. This channel overlaps with the implanted regions to allow for its electrical contact.

the TG (gray), directly on top of the heterostructure, with naturally formed oxides at the surface removed beforehand to ensure reliable electrical contact to the implanted regions (dotted). These implanted regions extend in depth to the QW and continue beneath parts of the TG. With the electrical contacts, we can apply a current I along the conduction channel and measure the voltage perpendicular to and along each segment of the channel to determine U_{xx} and U_{xy}, respectively (see Fig. 2.3 a)). This allows us to calculate the longitudinal resistivity $\rho_{xx} = \frac{U_{xx}}{I}\frac{W}{L}$ and the transversal resistivity $\rho_{xy} = \frac{U_{xy}}{I}$, which are the characteristic quantities measured in a Hall-bar experiment under the influence of a perpendicular magnetic field.
These quantities allow us to observe the characteristic QHE features and enable the extraction of the key 2DEG transport parameters: the electron density n_e and the electron mobility μ_e. Additionally, the presence of these features verifies the existence of a 2DEG

and allows to exclude parallel conduction channels. A typical measurement can be found in Sec. 3.1, shown in Fig. 3.2. At small magnetic fields, we are in the classical regime of the Hall effect, described by the Drude model. In this regime, ρ_{xx} remains constant, while ρ_{xy} shows the characteristic linear Hall behavior. This model derives

$$\rho_{xx} = \frac{m_e^*}{n_e \cdot e^2 \cdot \tau} = \frac{1}{n_e \cdot e \cdot \mu_e} \tag{2.1}$$

$$\rho_{xy} = \frac{B}{n_e \cdot e}, \tag{2.2}$$

where e represents the elementary charge, m_e^* the effective mass and τ the mean scattering time. The electron mobility is defined as $\mu_e = \frac{e \cdot \tau}{m_{e^*}}$. These relations enable the determination of n_e and μ_e from the slope of the Hall line and the longitudinal resistivity at $B = 0\,\mathrm{T}$:

$$n_e = \left(e \cdot \frac{\mathrm{d}\rho_{xy}}{\mathrm{d}B} \right)^{-1} \tag{2.3}$$

$$\mu_e = \left(n_e \cdot e \cdot \rho_{xx}|_{B=0} \right)^{-1}. \tag{2.4}$$

At sufficiently low temperatures and higher magnetic fields, the quantization of Landau levels with energy $E = \hbar\omega_c \left(l + \frac{1}{2} \right)$, where the cyclotron resonance is given by $\omega_c = \frac{eB}{m_e^*}$, can be resolved. This quantization results in the characteristic features of the QHE becoming observable. In the longitudinal resistivity, the typical Shubnikov-de Haas (SdH) oscillations appear, while the transversal resistivity ρ_{xy} exhibits the characteristic Hall-plateaus, which emerge simultaneously with the minima of the SdH oscillations. At these minima, transport along the Hall-bar becomes resistance-free, and the Hall resistance ρ_{xy} is quantized in integer fractions of the Klitzing constant $R_K = \frac{h}{e^2}$:

$$\rho_{xy} = \frac{1}{\nu} \frac{h}{e^2}, \tag{2.5}$$

where ν denotes the filling factor. The position of the minima of the SdH oscillations in the magnetic field is directly related to the electron density via $n_{e,qm} = \frac{\nu \cdot e \cdot B}{h}$. This provides an alternative method to evaluate n_e, which we denote as $n_{e,qm}$. By taking into account the degeneracy $d = 4$ in silicon, arising from the twofold valley and twofold spin degeneracies, we can derive

$$\left(\frac{1}{B_{i+4}} - \frac{1}{B_i} \right) = d \frac{e}{n_{e,qm} \cdot h}, \tag{2.6}$$

with i denoting the observable SdH minima, corresponding to filling factors that are multiples of four.

Our Hall-bar devices thus offer us a versatile platform for investigating the transport characteristics of FESs via the QHE and thus gaining insights into their properties.

2.4 Gate-defined Quantum Dot

The electrostatic control of the 2DEG provided by the metal gate on top of the FES offers the flexibility to not only use a single TG, as in the Hall-bar device, but also to introduce multiple gates allowing for great versatility. By reducing the gate size to the scale of tens to hundreds of nanometers, we can form quantum dots purely electrostatically within the FES. This is achieved by shape of several gates on the FES combined with applying different voltages to locally accumulate or deplete electrons, enabling the creation of complex potential landscapes.
Fig. 2.4 shows a schematics of the spatial potential distribution of a quantum dot (QD) in top view. A gate-defined QD is a small island of accumulated electrons confined in all three dimensions. In addition to being restricted in the growth direction of the FES by the size of the QW, it is locally confined within the QW plane by gates that create a local potential minimum. The size of this electron island can range from hundreds of electrons down to a single isolated electron, which forms the foundation of our spin qubit. The metal gates that confine the size of the QD are also typically used to define the tunneling barriers between the dot and potential neighboring QDs or reservoirs. In the illustrated scenario, the QD is both tunnel-coupled and capacitively coupled to a source and a drain reservoir. These reservoirs are regions of accumulated electrons that are electrically connected via implanted regions, as previously described for the Hall-bar, with the implanted regions deliberately positioned at a greater distance from the dot region to minimize the influence of dopants on the QD. Additionally, the QD is capacitively coupled to a dedicated gate, which contributes in defining the QD and enables its electrostatic tuning.
To understand the transport properties of a QD, it can be modeled as a metallic island with a radius r in the 2DEG, occupied by N electrons, thereby carrying a charge of $Q = -|e|N$. Detailed derivations of the equations presented within this model can be found in [53]. The electrostatic energy of the island with N electrons at an applied gate voltage U_{Gate} is described by

$$E_{\text{QD}}(N) = \frac{e^2 N^2}{2C} - |e| N \alpha_{\text{Gate}} U_{\text{Gate}}, \tag{2.7}$$

where the self-capacitance of the island is given by $C = 8\epsilon_0 \epsilon_r r$. Here, ϵ_0 is the vacuum permittivity, and ϵ_r is the dielectric constant of the host material. The constant α_{Gate}

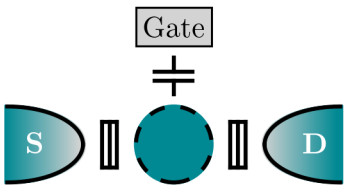

Figure 2.4: Single quantum dot. Schematics of the spatial potential distribution in top view. The QD, depicted as a blue circle, is both tunnel-coupled and capacitively coupled to the source and drain reservoirs (labeled S and D) and is additionally capacitively coupled to a gate.

the lever arm of the gate, which serves as conversion factor between the gate voltage and the shift in the energy of the QD. An important observation is that the electrostatic energy of the QD is quantized by the number of electrons confined on the island. This quantization arises solely from electrostatics and the fundamental quantization of charge. The energy required to add the Nth electron to the island is described by the electrochemical potential

$$\mu_N(U_{\text{Gate}}) = E_{\text{QD}}(N, U_{\text{Gate}}) - E_{\text{QD}}(N-1, U_{\text{Gate}}) \tag{2.8}$$

$$= \frac{e^2}{16\epsilon_0\epsilon_{\text{r}}}(2N-1) - |e|\alpha_{\text{Gate}}U_{\text{Gate}}. \tag{2.9}$$

This set of discrete electrochemical potentials is also referred to as Coulomb levels. The applied U_{Gate} shifts this ladder of levels towards lower energies for positive gate voltages and towards higher energies for negative gate voltages. The amount of energy necessary to load the next electron onto the island can be determined by the difference in electrochemical potential of two consecutive Coulomb levels is called charging energy

$$\Delta E_{\text{C}} = \mu_N(U_{\text{Gate}}) - \mu_{N-1}(U_{\text{Gate}}) \simeq \frac{e^2}{C}. \tag{2.10}$$

The ladder of Coulomb levels of the QD is illustrated in the schematic of the electrochemical potential landscape depicted in Fig. 2.5 a). The dot is separated from its two reservoirs by sharp tunnel barriers. The source and drain reservoirs are filled with electrons up to their respective electrochemical potentials, μ_{S} and μ_{D}, which can be independently tuned. Applying a source-drain voltage U_{SD} creates a bias window, defined as $\mu_{\text{S}} - \mu_{\text{D}} = -|e|U_{\text{SD}}$. In the illustrated scenario the N + 1th Coulomb level is within the bias window

$$\mu_{\text{S}} \geq \mu_{N+1} \geq \mu_{\text{D}}. \tag{2.11}$$

This allows electrons to tunnel from the source reservoir onto the QD and subsequently into the drain reservoir, creating a current flow through the QD. The Nth Coulomb level, being below the bias window, is occupied by an electron and does not contribute to transport, while the N + 1th Coulomb level, being above the bias window, also does not participate in transport. As the applied U_{Gate} increases, the entire ladder of Coulomb levels shifts to lower energies until the N + 1th Coulomb level moves below the bias window. This situation, illustrated in Fig. 2.5 b), leads to a suppression of current flow, the characteristic feature of the Coulomb blockade effect. The resulting current I through the QD at a fixed U_{SD} as a function of U_{Gate} is depicted in Fig. 2.5 f). The current flows through the QD whenever one of the Coulomb levels lies within the bias window and is blocked until the next level shifts into the bias window. The appearance of peaks is influenced by both the broadening caused by tunnel coupling and the effects of thermal broadening.

When U_{SD} is varied alongside U_{Gate}, altering the bias window, the characteristic diamond-shaped pattern of the Coulomb blockade appears, as shown in Fig. 2.5 g). The white

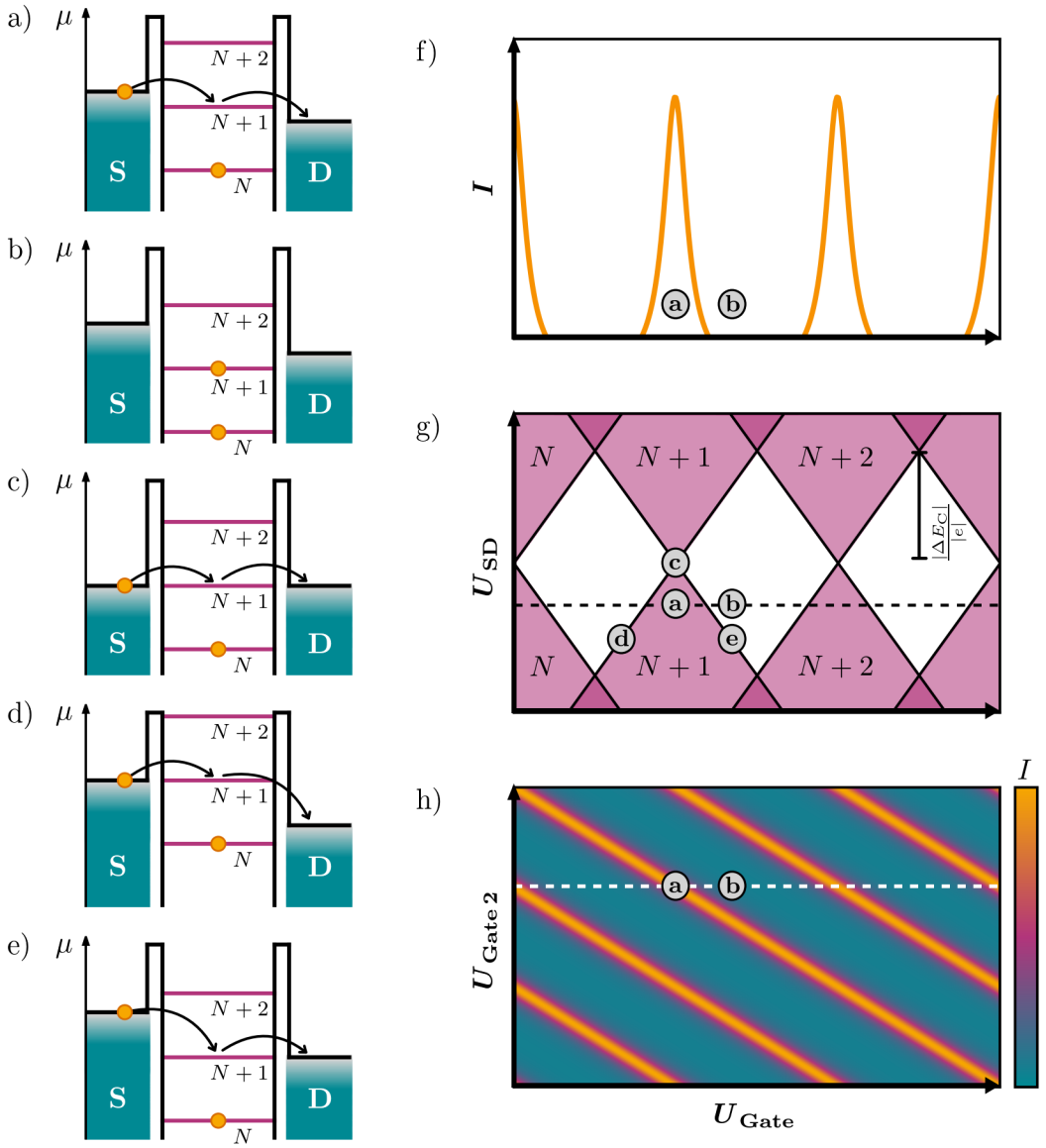

Figure 2.5: Transport through a single quantum dot. a) to e) Schematics of the electrochemical potential landscape for different scenarios of source-drain bias U_{SD} and gate voltage applied at the QD. f) Current through the QD at a fixed U_{SD}, showing regions of blocked current flow due to Coulomb blockade. g) Typical Coulomb diamond measurement resulting from varying both U_{Gate} and U_{SD}. Within the white regions, current flow is blocked, while in the light pink regions, a single Coulomb level contributes to transport. The corresponding electron occupation is denoted with N, and the charging energy with ΔE_{C}. In the darker pink regions, two Coulomb levels contribute. The black dashed line represents a cut through the measurement corresponding to panel f). h) Current in dependence of two gates capacitively coupled to the QD. The corresponding electron occupation is denoted with N. The white dashed line represents a cut through the measurement corresponding to panel f). The scenarios of the electrochemical potential landscapes shown in a) to e) are marked with gray circles in f) to h).

regions indicate no current flow, while the light pink regions correspond to current flowing through one level, and the darker pink regions to current flowing through two levels. The black dashed line illustrates a cross-section through the diamonds, corresponding to the current shown in panel f). In the case of $U_{SD} = 0\,V$, the source and drain electrochemical potentials align, $\mu_S = \mu_D$, as depicted in Fig. 2.5 c). As a result, current flow is only possible when a Coulomb level aligns with the source and drain electrochemical potentials and thus at a single U_{Gate}. With an increasing $|U_{SD}|$, i.e., increasing bias window, the gate voltage ranges allowing current flow become wider. Fig. 2.5 d) illustrates the onset of current flow as U_{Gate} increases, when Coulomb level $N + 1$ aligns with μ_S. Similarly, Fig. 2.5 e) depicts the last U_{Gate} position at this U_{SD} with current flow, corresponding to the alignment of the Coulomb level with μ_D. The opposite scenario occurs for the upper half ($U_{SD} > 0\,V$) of the Coulomb diamond, where alignment first happens with μ_D and later with μ_S, as in this case $\mu_D > \mu_S$. If the bias window is widened further, two Coulomb levels can simultaneously fall within the window, both contributing to transport. This is reflected in the darker pink regions. The voltage U_{SD}, which corresponds to the onset of this regime, i.e., the height of the Coulomb diamond, also allows us to determine ΔE_C, as at the crossover of two occupation regions the condition $|\mu_N - \mu_{N-1}| = |\mu_S - \mu_D|$ holds.
A further typical measurement for characterizing QDs involves additionally varying a second gate that is capacitively coupled to the QD, such as the gate primarily intended to define the tunnel barrier to one of the reservoirs. The typical appearance of such a measurement is shown in Fig. 2.5 h), with the Coulomb peaks forming diagonal lines. The white dashed line represents a cross-section at a fixed $U_{Gate\,2}$, corresponding to the current shown in panel f). Since both gates are capacitively coupled to the QD, they both shift the QD's Coulomb level ladder. However, due to a possible difference in their capacitive coupling to the QD, the levels can be shifted by different amounts. The slope of the Coulomb peaks provides insights into the relative coupling strengths of the two gates. The steeper the slope, the greater the influence of U_{Gate} compared to $U_{Gate\,2}$.
In the multi-electron regime, transport through a QD is very useful for its tuning and to gain insights in the dot's properties. However, when tuning the dot to the few-electron regime and ultimately to the last electron, the tunnel barriers become too opaque for the tunnel current to be detected. To monitor the physics of the dot in this regime, a second dot can be formed in close proximity and used as a charge sensor.

2.5 Charge Sensing utilizing a Quantum Dot as Sensor

The method of using a dot as a charge sensor relies on tracking the current through the sensor dot to detect changes in the electron occupation of a nearby QD.
A schematic representation of a sensor dot (pink) utilized to detect the charge state of a QD (blue) is illustrated in Fig. 2.6 a). The sensor dot (SD) is both tunnel-coupled and

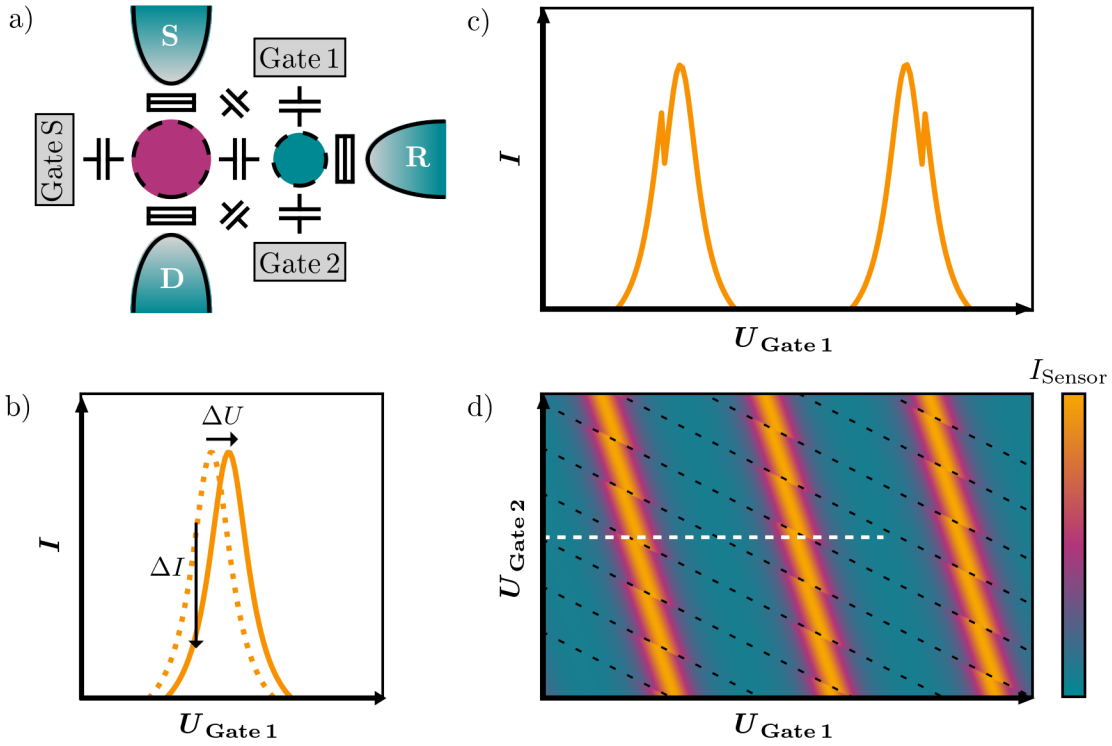

Figure 2.6: Charge sensing utilizing a quantum dot as sensor. a) Schematics of the spatial potential distribution of a QD (blue) and a second QD used as a sensor dot (pink) in top view. The dot, whose electronic state we aim to track, is both tunnel-coupled and capacitively coupled to a reservoir (R), from which it can load and unload electrons. Additionally, it is capacitively coupled to two gates in this simplified scenario. The sensor dot has its own two reservoirs, acting as source and drain, to which it is both tunnel-coupled and capacitively coupled. Furthermore, it is capacitively coupled to its own gate, named Gate S, as well as to the two gates of the QD. b) Working principle of charge sensing via a QD. Since the QD is electrostatically coupled to the sensor QD, the loading or unloading of an electron in the QD can be interpreted as an equivalent electrostatic change, ΔU, in $U_{\text{Gate},1}$. When the sensor's working point is set to the flank of one of its Coulomb peaks, this electrostatic change causes a shift in the peak position, resulting in a measurable ΔI. c) The resulting current through the sensor in dependence of $U_{\text{Gate},1}$ thus exhibits dips and peaks, depending on whether the sensor operates on the rising or falling flank, indicating a change in the electron occupation of the QD. d) The sensor current as a function of $U_{\text{Gate}\,1}$ and $U_{\text{Gate}\,2}$ (charge stability diagram), with sudden shifts in the sensor current indicating changes in the electron occupation of the QD, illustrated as black dashed lines. The white dashed line represents a cut through the measurement corresponding to panel c).

capacitively coupled to a source and drain reservoir, enabling current flow through it. Its tuning is controlled via a dedicated gate, referred to as gate S. The nearby QD is tunnel- and capacitively coupled to its own reservoir, allowing it to load and unload electrons. Importantly, for this process, no second reservoir is required. Electrons are loaded or unloaded when the gates capacitively coupled to the QD (gate 1 and gate 2) shift its Coulomb level ladder such that one of the levels aligns with the reservoir's electrochemical potential, μ_{R}. For charge sensing, it is crucial that the SD and QD are capacitively well coupled, which necessitates their proximity. Additionally, due to this proximity, gate 1 and gate 2 of the QD will typically also influence the SD. The fundamental idea of utilizing the QD as a charge sensor, illustrated in Fig. 2.6 b), relies on its Coulomb physics. When operated on a steep flank of one of its Coulomb peaks, the sensor becomes highly sensitive to electrostatic changes in its environment. Electrostatic changes, such as an electron loading or unloading from the nearby QD, can be interpreted as an equivalent change in voltage of one of the capacitively coupled gates. This change, ΔU, causes an abrupt shift of the Coulomb peak, leading to a sudden jump in the corresponding current through the SD. The stronger the capacitive coupling between the QD and SD, the larger the induced ΔU, and, as long as the SD remains on the flank of the Coulomb peak, the larger the resulting ΔI, enhancing the signal. Changing a gate voltage, e.g., $U_{\mathrm{Gate,1}}$, which shifts the QD's energy levels, also shifts the Coulomb peaks of the SD. The occupation change of the QD can be detected when the SD is in a sensitive position on the flanks of its Coulomb peak. Depending on whether this occurs on the rising or falling flank of the SD's peak, it results in either a dip or a peak in the SD's current, as illustrated in Fig. 2.6 c). At the top of the Coulomb peak or within the blocked regions between peaks, the sensor remains insensitive to changes in the electrostatic environment. This enables us to record a so-called charge stability diagram of the QD by measuring the SD current as a function of $U_{\mathrm{Gate\,1}}$ and $U_{\mathrm{Gate\,2}}$, as illustrated in Fig. 2.6 d). The occupation of the QD is reflected as sudden shifts in the diagonal lines of the SD's Coulomb peaks. These shifts allow for tracking charge transition lines, illustrated as black dashed lines, whenever an electron is loaded or unloaded from the QD. The white dashed line represents a cross-section through the measurement at a fixed $U_{\mathrm{Gate\,2}}$, corresponding to the current shown in panel c).
The dot, utilized as a charge sensor due to its high sensitivity to electrostatic changes, allows us to track occupation changes down to the last electron of the QD. Gate S provides additional tunability by shifting the SD's energy levels relative to the QD, enabling access to different sensitive regions. In principle, this tuning could be used dynamically, adjusting gate S while varying the QD gate voltage to continuously align the SD's Coulomb peaks, ensuring it remains on a flank for optimal sensitivity. However, this capability has not been utilized within this thesis.

2.6 Gate defined Double Quantum Dot

Building on the concept of charge sensing, we can extend our analysis to the charge configurations of two coupled QDs, forming a double quantum dot (DQD).

Fig. 2.7 illustrates a schematic top view of the spatial potential distribution of a DQD, consisting of two QDs arranged in series, each connected to its own reservoir. The QDs are both capacitively and tunnel-coupled to each other, as well as to their respective reservoirs. Additionally, each QD is controlled by an individual gate, allowing for charge configuration tuning within the system. However, these gates also exhibit capacitive cross-coupling, albeit to a lesser extent, to the opposite QD. A schematic of the electrochemical potential landscape of the DQD is depicted in Fig. 2.8 a), where N and M denote the electron occupation of the left and right QD, respectively, with $U_{SD} = 0\,V$. The left QD can change its occupation by exchanging an electron with its reservoir when one of its Coulomb levels aligns with the reservoir's electrochemical potential. The same principle applies to the right QD, as shown in Fig. 2.8 b). In both configurations, no current flow occurs between the source and drain reservoirs. However, by utilizing charge sensing, we can still detect these occupation changes. This results in the characteristic DQD charge stability diagram shown in Fig. 2.8 c). The honeycomb pattern of orange lines shows the charge transition lines, while the charge occupation remains fixed within the blue regions. In these regions, none of the two QDs Coulomb levels aligns with their respective reservoirs, as illustrated in Fig. 2.8 d). The tilt of the honeycomb lattice is determined by the capacitive cross-coupling between the gates. Current can only flow between the source and drain reservoirs at the so-called triple points, located at the edges of the honeycomb lattice where three charge occupation regions meet. At these points, the electrochemical potentials of both QDs and their respective reservoirs align, depicted in Fig. 2.8 e), enabling electron transport through the DQD.
The characteristic honeycomb pattern of the charge stability diagram not only offers essential insight into the charge configuration of a DQD system but will also prove useful in identifying unwanted, additional dots in the course of this work.

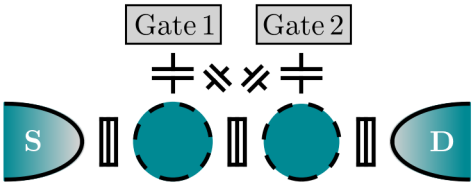

Figure 2.7: Double quantum dot. Schematics of the spatial potential distribution in top view. The QDs, depicted as blue circles, are tunnel-coupled and capacitively coupled to each other. Additionally, each dot is tunnel-coupled and capacitively coupled to either the source (S) or drain (D) reservoirs. Each dot is also capacitively coupled to gate 1 and gate 2.

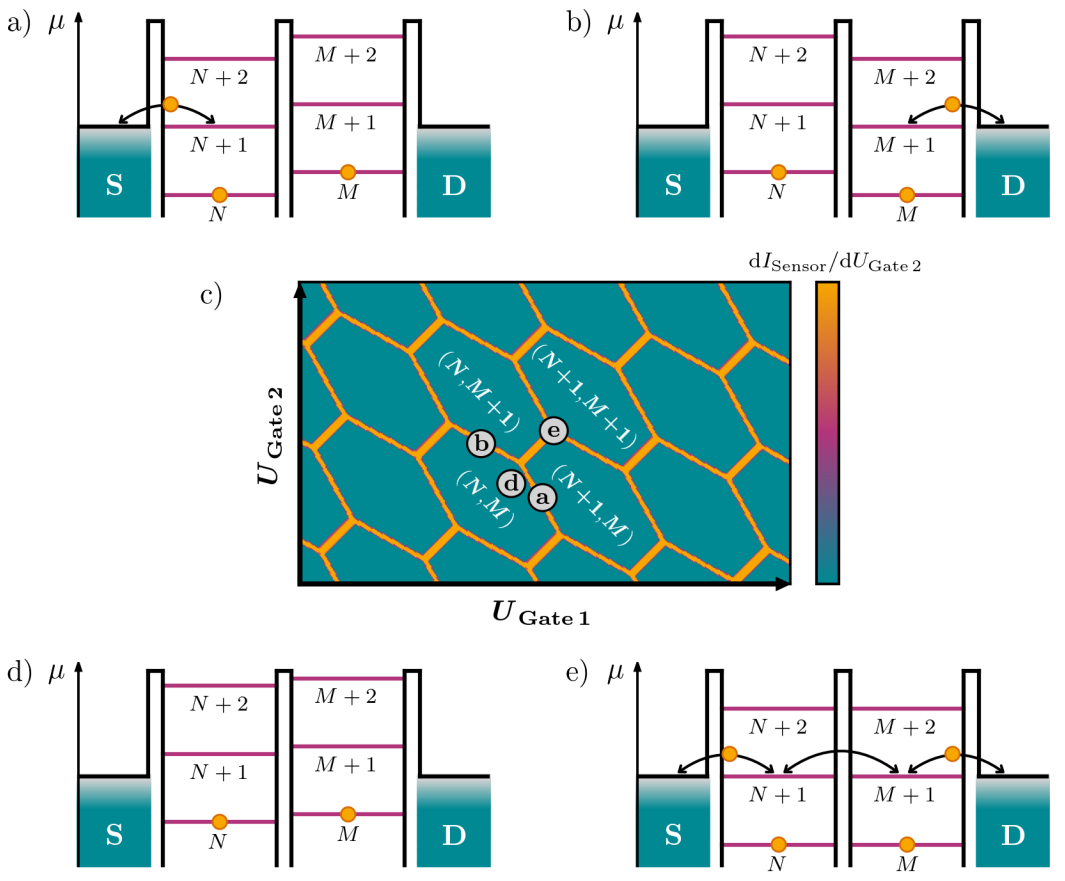

Figure 2.8: Charge configuration of a double quantum dot. a), b), d) and e) Schematics of the electrochemical potential landscape for different scenarios of gate voltages applied at the DQD. N and M denote the electron occupation of the left and right dot, respectively, forming the DQD. c) Charge stability diagram of the DQD. The sensor current is displayed as a function of $U_{\text{Gate 1}}$ and $U_{\text{Gate 2}}$. The orange lines, representing shifts in the sensor current, signify a change in the electron occupation of at least one of the dots. The scenarios of the electrochemical potential landscape are marked with gray circles.

2.7 Magnetic Field Impact on the Energy Spectrum of a Few-Electron Quantum Dot

The application of an in-plane magnetic field offers a pathway to investigate the spin configuration of the few-electron energy spectrum of a QD. To achieve this, we employ the method of magnetospectroscopy, which monitors changes in the dot's electrochemical potential. The description and corresponding equations presented in this section are adapted from [55].

In a magnetic field, in addition to the Coulomb interaction of the QD, the Zeeman effect depending on the spin state must be taken into account, with the associated energy given by $E_z = m_s g \mu_B B$, where m_s denotes the spin projection along the magnetic field, g represents the electron Landé-factor, and μ_B is the Bohr magneton. For each occupation N the Zeeman energy contribution E_N will be influenced by the magnetic field according to its ground state spin configuration. These changes will manifest as differences between two energy states, $E_N - E_{N-1}$ in the electrochemical potential of the charge transition $N-1 \rightarrow N$. The magnetic field dependence of the E_N and the resulting $E_N - E_{N-1}$ are depicted in Fig. 2.9. The magnetic field dependence of the $0 \rightarrow 1$ transition (black dashed line) is illustrated in Fig. 2.9 a) as the difference between the zero-electron ground state energy E_0 and the one-electron ground state energy E_1 magnetic field dependence. The zero-electron ground state remains constant since it has no spin. The one-electron ground state E_1 decreases with increasing magnetic field, as expected for a single-electron spin-down state $|S, m_s\rangle = |\frac{1}{2}, -\frac{1}{2}\rangle$. The $\mu_{0\rightarrow 1}$, i.e., $E_1 - E_0$, thus follows the behavior of E_1. With the second electron, a spin of opposite sign is added to the QD, forming a singlet ground state $|0, 0\rangle$ at zero magnetic field. This remains valid until the T_- triplet state is Zeeman-shifted by an amount equal to the zero-magnetic-field singlet-triplet splitting E_{ST}, becoming the new ground state $|1, -1\rangle$. The corresponding two-electron Zeeman contribution is illustrated in Fig. 2.9 b). The kink in the curve marks the transition between ground states, and the magnetic field value at this point allows for the determination of E_{ST}. The slope of the resulting electrochemical potential (see Fig. 2.9 b)) can be understood as it is proportional to $m_s(N) - m_s(N-1)$, a relationship that holds for any electron charge transition. Since it reproduces the kink, this slope enables the evaluation of E_{ST}. Fig. 2.9 c) shows the Zeeman energy contributions for the $2 \rightarrow 3$ transition. The three-electron Zeeman energy contribution E_3 exhibits a kink where its spin configuration changes from $|\frac{1}{2}, -\frac{1}{2}\rangle$ to $|\frac{3}{2}, -\frac{3}{2}\rangle$. The corresponding magnetic field at this kink allows for determining the three-electron excitation energy $E_{3/2}$. The resulting electrochemical potential reveals both kinks, originating from E_2 and E_3, giving access to both E_{ST} and $E_{3/2}$.

However, while the Zeeman contribution accounts for the magnetic field dependence of the few-electron energy spectrum, it is not sufficient on its own to derive the formulas needed to accurately fit the charge transition lines. The fitting formulas were derived based on a model that additionally incorporates the Coulomb energy contribution, the zero-magnetic-field energy of the excited spin states, and the energy shift induced by

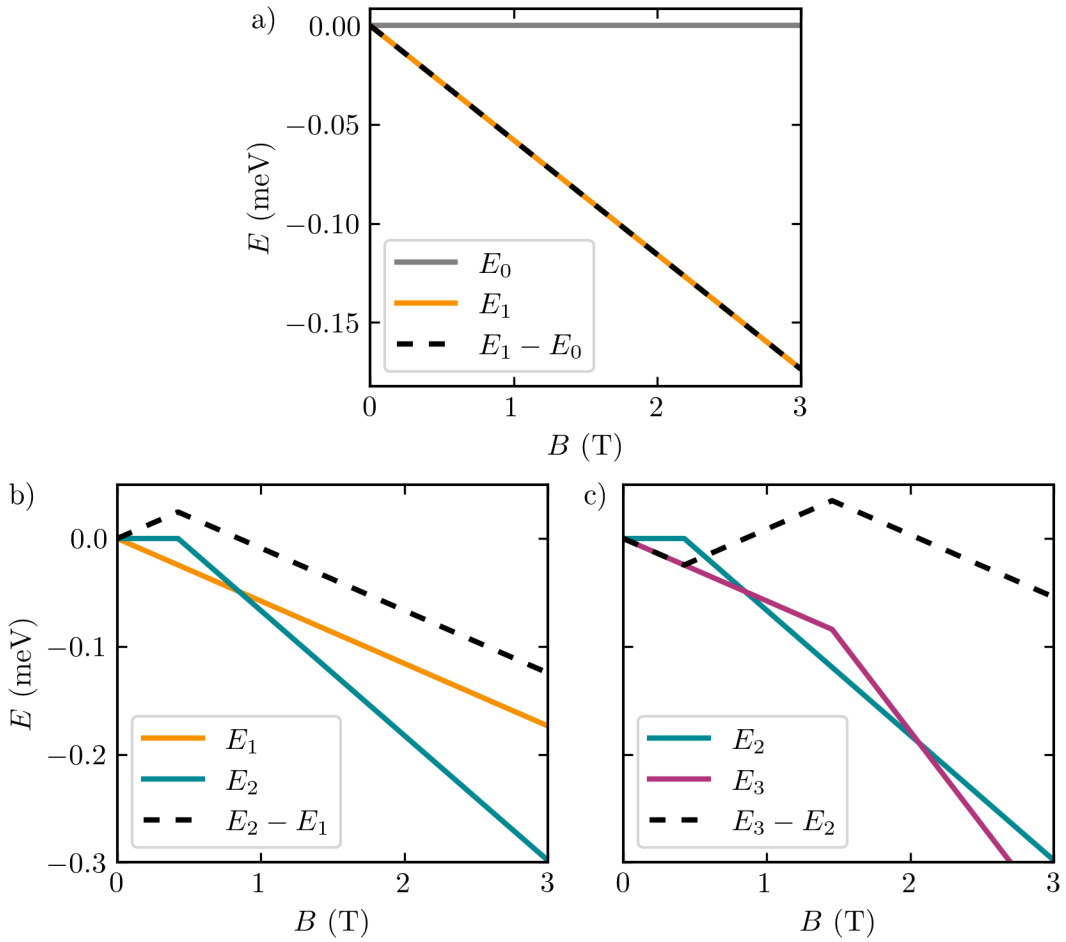

Figure 2.9: Magnetic field dependence of the few-electron ground state energies. The lines labeled with E_N depict the magnetic field dependence of the N-electron ground state energies of a QD. The dashed lines represent the difference $E_N - E_{N-1}$, corresponding to the measurable change in electrochemical potential during a charge transition $N-1 \rightarrow N$. A kink indicates a change in the spin configuration of the N-electron ground state energies, which also translates into a kink in the electrochemical potential. a) Charge transition $0 \rightarrow 1$. b) Charge transition $1 \rightarrow 2$. c) Charge transition $2 \rightarrow 3$.

the applied gate voltage. The gate voltages of the $0 \rightarrow 1$, $1 \rightarrow 2$, and $2 \rightarrow 3$ electron charging transitions are expressed as:

$$U_{0\rightarrow1}(B) = -\frac{\beta B g \mu_\mathrm{B} + 2\log(\mathrm{e}^{-\beta g \mu_\mathrm{B} B} + 1)}{2\alpha\beta} + U_0 \tag{2.12}$$

$$U_{1\rightarrow2}(B) = \frac{1}{\alpha\beta}\log\left(\frac{(\mathrm{e}^{\beta g \mu_\mathrm{B} B} + 1)\mathrm{e}^{\beta(\frac{1}{2} g \mu_\mathrm{B} B + E_\mathrm{ST})}}{\mathrm{e}^{\beta(g \mu_\mathrm{B} B + E_\mathrm{ST})} + \mathrm{e}^{2\beta g \mu_\mathrm{B} B} + \mathrm{e}^{\beta g \mu_\mathrm{B} B} + 1}\right) + U_0 \tag{2.13}$$

$$U_{2\rightarrow3}(B) = \frac{1}{\alpha\beta}\log\left(\frac{\mathrm{e}^{\beta(\frac{1}{2} g \mu_\mathrm{B} B - E_\mathrm{ST} + E_{3/2})}(\mathrm{e}^{\beta(g \mu_\mathrm{B} B + E_\mathrm{ST})} + \mathrm{e}^{\beta g \mu_\mathrm{B} B} + \mathrm{e}^{2\beta g \mu_\mathrm{B} B} + 1)}{(\mathrm{e}^{\beta g \mu_\mathrm{B} B} + 1)(2\mathrm{e}^{\beta(g \mu_\mathrm{B} B + E_{3/2})} + \mathrm{e}^{2\beta g \mu_\mathrm{B} B} + 1)}\right) + U_0 \tag{2.14}$$

where U_0 denotes a voltage offset, α represents the lever arm of the gate, and $\beta = 1/k_\mathrm{B}T$ is the Boltzmann factor. More details on the derivation can be found in [55].
The magnetic field dependence provides valuable insights into the spin configurations of the few-electron energy spectrum of a QD. Through magnetospectroscopy, we gain access to key parameters such as the two-electron singlet-triplet splitting energy E_ST and the first three-electron excitation energy $E_{3/2}$.

2.8 Experimental Setup and Magneto-Transport Measurement Techniques

The foundation for our experimental investigation is built upon the experimental setups and magneto-transport measurement techniques employed. In this section, we introduce the key concepts of these techniques and setups. Further details, particularly regarding the technical implementation, can be found in [56].

Cryostat Systems

We utilize three cryostat systems, a ^{4}He cryostat, a ^{3}He cryostat and a dilution cryostat, with different operating temperatures and magnetic field ranges, tailored for conducting magneto-transport measurements. Cooling in the ^{4}He cryostat is facilitated by the phase transition of liquid ^{4}He to the gaseous phase under reduced pressure, achieving an operating temperature of $T \approx 1.5\,\mathrm{K}$. The cryostat is equipped with a magnet capable of generating magnetic fields up to $B = \pm 5\,\mathrm{T}$. The ^{3}He cryostat operates on the same cooling principle but uses the helium isotope ^{3}He, which has a lower boiling temperature than ^{4}He, enabling an operating temperature of $T \approx 400\,\mathrm{mK}$. It supports magnetic fields up to $B = \pm 10\,\mathrm{T}$. The lowest temperatures are achieved in the dilution cryostat, which has a base temperature of $T < 7\,\mathrm{mK}$ and allows for magnetic fields up to $B = \pm 8\,\mathrm{T}$. Unlike

the other two cryostats, in this system the device is not in direct contact with the coolant but is thermalized via a cold finger. The cooling principle relies on the transition of ^{3}He atoms from a concentrated phase to a diluted phase in a ^{3}He/^{4}He mixture.

Hall-bar Device Measurements Technique

For the Hall-bar device measurements, we apply a current of 50 nA along the entire length of the Hall-bar. This is achieved using a lock-in amplifier outputting an AC signal at 17 Hz with a voltage amplitude of 5 V, combined with a 100 MΩ pre-resistor. Simultaneously, the longitudinal and transverse resistivity are measured using dedicated lock-in amplifiers phase-locked to the current-driving lock-in amplifier, with a time constant of 500 ms. We utilize a source-measure unit to adjust the voltage at the TG while concurrently monitoring potential leakage by measuring possible DC currents from the TG. Before measuring any QHE features, it is necessary to accumulate a 2DEG within the QW of the FES, as described previously in Sec. 2.2. To achieve this, we increase the TG voltage while tracking the current through the Hall-bar as an indicator of electron accumulation within the QW. Before accumulation, the current remains at zero. As the TG voltage increases, it stays zero until a FES dependent voltage threshold is reached, after which the current rises steeply and saturates at the set current limit of 50 nA. To establish a comparable measure across the FES for determining the lowest voltage at which the FES is fully accumulated, we define the accumulation voltage U_{Acc}, i.e., the accumulation point, as the voltage where the current through the Hall-bar channel exceeds 48 nA of the 50 nA applied by the lock-in amplifier. Based on QHE signatures and years of Hall-bar measurements, we have verified that this definition is sufficient to ensure the 2DEG is fully accumulated and beyond the metal-insulator transition (described in Sec. 2.2). To determine the electron density and mobility as a function of the TG voltage, we utilized two different measurement techniques. The first involves incrementally increasing the TG voltage step by step and sweeping the magnetic field at each TG voltage. This approach not only allows for the extraction of the electron density and mobility as a function of the TG voltage but also provides full access to QHE features. These features serve as a verification of the 2DEG and help exclude parallel conduction channels (see Sec. 3.1). While this method is insightful and necessary for the initial characterization of the FESs, it is also very time-consuming. To accelerate the measurement routine after the initial characterization, we employ a second approach based on continuously sweeping the TG voltage. By simultaneously measuring the transversal resistivity at $B = 1$ T, previously identified during the initial characterization as being within the classical regime of the QHE, we can determine the electron density as a function of the TG voltage. This is achieved by approximating the slope at each TG voltage value using these data points, combined with the fact that the transversal resistivity is zero at zero magnetic field. To evaluate the electron mobility, the longitudinal resistivity is measured during a separate TG sweep at a magnetic field of $B = 0$ T. Note that to also access the saturation regime of the field-effect (see Sec. 2.2), it is necessary to reset the FES with a thermal cycle between these two measurements. Nevertheless, since magnetic fields can only be swept

at comparatively low rates, this remains a very time-efficient measurement technique.

Qubit Device Measurement Technique

Qubit device measurements require the ability to individually control the voltage applied to multiple gates. This enables the creation of complex potential landscapes, such as those needed to form QDs and tunnel barriers. To achieve this, we utilize a voltage source capable of outputting multiple individually controllable DC voltages, combined with voltage dividers and adders to tailor the resolution. The current at the drain reservoirs is measured using an I/V converter with an amplification of 10^8 V/A and a cutoff frequency of 10 kHz. Additionally, the converter can apply a voltage to the drain, supplied by the voltage source. The cutoff frequency is selected to align with the limitations imposed by the DC lines in the dilution cryostat, which are restricted to approximately 8 kHz due to the filters, capacitors, and resistances installed in the system. In the ^{3}He cryostat, the measurement speed of the multimeter used to measure and digitize the output voltages from the I/V converter as well limits the frequency to below the chosen cutoff frequency. The selected amplification provides a measurable current range of ±100 nA, as the I/V converter can output voltages up to ±10 V. For the dilution cryostat, we utilize an AD converter card mounted directly in the PC, allowing for significantly faster sampling rates of up to 180 MSamples/s. Since the AD converter card is directly connected to the PC, it is necessary to isolate the measurement ground from the PC's grounding. This is achieved using an additional voltage amplifier placed between the I/V converter and the PC, with a minimum amplification factor of 10. This setup results in an overall amplification of 10^9 V/A for the current measurements and limits the measurable current to ±10 nA due to the maximum output voltage of the voltage amplifier. This current limit is still sufficient, as we do not intend to exceed it in order to protect the sample. Additionally, qubit operations typically operate with even lower currents, minimizing heating of the sample.

Our different measurement techniques, combined with the range of cryostat systems, offer a versatile platform for conducting various magneto-transport experiments. Whether for Hall-bar geometry FES characterization or qubit device measurements, they are well-suited to support the demands of quantum research.

3

Field-Effect Stacks for Quantum Circuit Applications

FES serve as the basis for realizing a variety of quantum circuits in semiconductor heterostructures, including semiconductor spin qubits [12, 16, 18, 32, 57–60]. The development of FES remains an active area of research, with ongoing advancements particularly tailored to qubit applications [34, 41, 48, 61–63]. Key characteristics of the 2DEG transport properties in FES, such as electron density and electron mobility, are not directly accessible in qubit device measurements. Other parameters, like the valley splitting – known to display a significant spatial in-plane variation [36] – can only be reasonably inferred through qubit experiments. Therefore, combining insights from both qubit and Hall-bar measurements is advantageous for optimizing the performance of FES-based qubit devices [24, 62, 63]. For qubit applications, a comprehensive understanding of impurities in the FES and the disorder potential fluctuations they induce in the QW is crucial. These factors play a decisive role in the precise control of charging energies, the position and shape of QDs, the occurrence of disruptive disorder dots, and the sources of charge noise. Especially, charge noise remains a prominent challenge for further improving qubit operation [17, 18, 64]. Furthermore, the operation window defined by the gate-tunable range of electron density is an important property for device tunability. It is restricted to the range before saturation due to tunneling towards the dielectric/heterostructure interface, as described in Sec. 2.2, sets in, which is known to introduce detrimental effects as on the operation and charge noise of the device [65, 66]. Moreover, the properties of the low-density regime have gained particular importance for qubit operation. The Hall-bar geometry measurable 2DEG properties allow us to draw conclusions about the characteristics of the FES. The gate-tunable range can be directly determined, while insights into the dominant scattering mechanisms can be inferred from the electron mobility. Additionally, the lower bound of the electron density tuning regime offers information about the potential fluctuations within the QW. FES characterization is indispensable as it provides deeper insights into the correlation between transport properties and the layer stack details. These insights facilitate optimization and

custom tailoring of the heterostructure to align with the specific demands of different applications.
In the following, we present a comparison of the transport properties of five selected FESs, fabricated on state-of-the-art heterostructures, and correlate the differences in their layer stack and fabrication details with their respective transport properties. The FESs are standard undoped $Si_{1-x}Ge_x$/Si/$Si_{1-x}Ge_x$ quantum well heterostructures for field-effect applications like quantum circuits. All of them are based on the same heterostructure concept, but featuring differences in the layer stack crucial for the transport properties.

3.1 Field-Effect Stack Overview and Transport Property Characterization

The FES concept, as previously discussed in Sec. 2.1, is further illustrated in Fig. 3.1. The abbreviations shown correspond to Tab. 3.1 summarizing the layer stack details of the five FESs. We chose the five FESs to differ in a variety of properties regarding their heterostructure as well as the fabrication. FES A and D were grown by chemical vapor deposition and further processed in a semi-industrial environment at the *IHP - Leibniz-Institut für innovative Mikroelektronik*. FES B and C were grown by molecular beam epitaxy and subsequently fabricated by our group in an academic clean room, while FES E is a commercially purchased wafer from *Lawrence Semiconductors Research Labs*, further processed by our group. One key difference to highlight is the absence of an (oxidized) Si cap for FES A and D. Additionally, these two FESs differ in their QW growth temperatures, resulting in a longer wait time between the barrier and QW growth for FES A compared to D. It can be suggested that the longer wait time makes FES A more susceptible to impurities, such as nitrogen or oxygen, being incorporated near the QW.
The characterization of the FESs was done by Hall-bar geometry magneto-transport

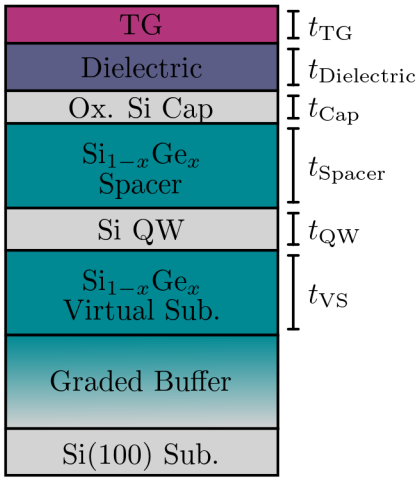

Figure 3.1: Cross-section schematic of the undoped Si/SiGe FESs. Details on the investigated five FESs are listed in Tab. 3.1.

FES	A	B	C	D	E
Dielectric (method)	SiOx (HDP)	AlOx (ALD)	AlOx (ALD)	SiOx (HDP)	AlOx (ALD)
TG material	TiN	Ti/Au	Ti/Au	TiN	Ti/Au
t_{TG} (nm)	30	10/100	10/100	30	10/100
$t_{Dielectric}$ (nm)	10	20	50	10	20
t_{Cap} (nm)	0	1.5	1.5	0	2
t_{Spacer} (nm)	33	45	45	37	30
t_{QW} (nm)	7	12	12	8	10
t_{VS} (µm)	3.1	0.78	0.8	3.1	2
x	0.34	0.26	0.32	0.34	0.30
Heterostr. growth	CVD (semi-industrial)	MBE (academic)	MBE (academic)	CVD (semi-industrial)	CVD (industrial)
Fabrication	semi-industrial	academic	academic	semi-industrial	academic

Table 3.1: Overview of the five undoped SiGe/Si/SiGe quantum well FES summarizing their differences in the layer stack. The abbreviations are introduced in Fig. 3.1.

measurements at a temperature of 1.5 K (^{4}He cryostat) using standard lock-in techniques (as described in Sec. 2.3 and Sec. 2.8). A representative example of a magneto-transport measurement, performed on a duplicate of FES A at a temperature of $T = 400\,\mathrm{mK}$ (^{3}He cryostat), displaying the characteristic quantum Hall effect features in the longitudinal resistivity ρ_{xx} and transversal resistivity ρ_{xy} is shown in Fig. 3.2. The typical Shubnikov-de Haas (SdH) oscillations are clearly visible in the longitudinal resistivity ρ_{xx}, while the transversal resistivity ρ_{xy} exhibits the characteristic Hall-plateaus that emerge simultaneously to the minima of the SdH oscillations.
These measurements enable the extraction of key 2DEG transport parameters, such as electron density n_e and electron mobility μ_e (as described in Sec. 2.3). Additionally, they confirm that transport occurs exclusively within the 2DEG and thus allow to exclude a parallel conductance channel. This can be demonstrated in two ways: first, by comparing the electron density n_e, extracted from the slope of ρ_{xy}, with the electron density $n_{e,\,qm}$ derived from the SdH oscillations (see Sec. 2.3). A discrepancy between the two values would suggest the presence of an additional parallel conduction channel besides the 2DEG. Second, a clear indication is provided by the SdH oscillations reaching zero, signifying completely resistance-free transport, which is a strong indication that transport occurs solely in the Landau-quantized 2DEG. The ρ_{xx} in Fig. 3.2 clearly shows zero resistivity for oscillations beyond a magnetic field of $B = 1.5\,\mathrm{T}$. In combination with the evaluation of $n_{e,\,qm}$ and n_e closely matching, the presence of a parallel conduction path beside the 2DEG can be ruled out.
Furthermore, due to the high electron mobility and the chosen measurement temperature,

the Landau level broadening is narrow enough to observe the degeneracy, characteristic for strained Si (see Sec. 2.1), lifting with increasing magnetic field. The minima of the SdH oscillations reaching zero correspond to Landau levels ν = 12, 8, 6, 4, 3 and 2 indicating that the fourfold degeneracy in spin and valley states is gradually lifted by the increasing magnetic field. Given the state-of-the-art valley splitting in such devices, it is likely that spin splitting occurs before valley splitting. During the lifting of degeneracies, it can be observed that, for example, at the filling factor $\nu = 5$, a Hall plateau begins to form. However, due to the Landau level broadening, the corresponding SdH oscillation is not fully developed yet, as it does not reach zero resistivity. Additionally, some of the Hall-plateaus exhibit overshoots in the transversal resistivity. This phenomenon likely arises from more than one Landau level coexisting and contributing to the transport. Details on this can be found in [67].
Overall, magneto-transport measurements that provide access to the quantum Hall effect are invaluable for characterizing the 2DEG transport properties of FESs in relation to the applied TG voltage. They allow us to evaluate key quality metrics of the 2DEG, making them an ideal tool for understanding how variations in heterostructure layer stack and fabrication details influence transport characteristics.

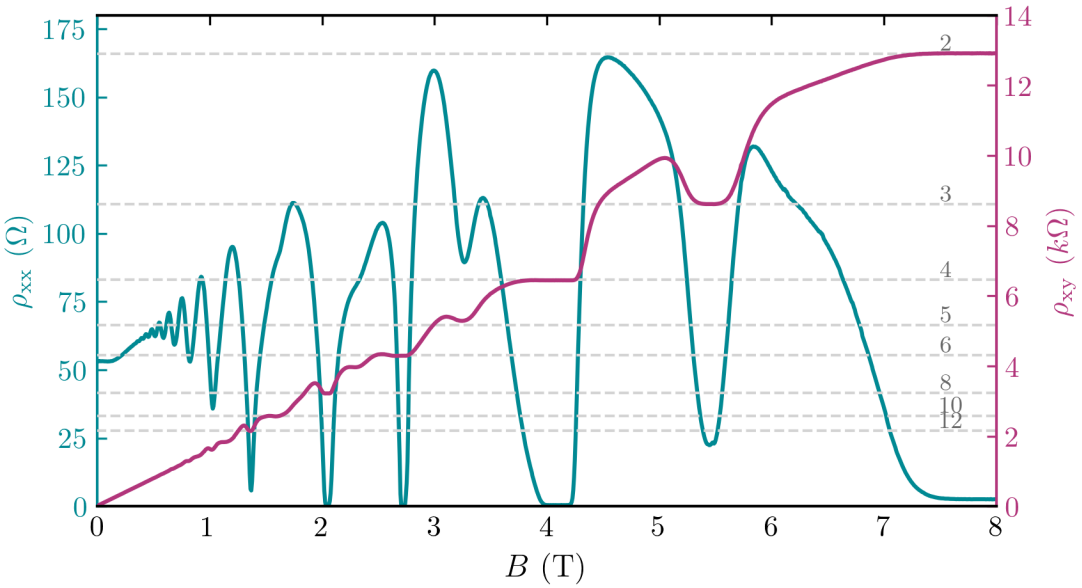

Figure 3.2: Representative example of quantum Hall effect features in the longitudinal resistivity ρ_{xx} and transversal resistivity ρ_{xy} measured on a duplicate of FES A. The measurement was performed at a temperature of T = 400 mK and a TG voltage within the linear regime of U_{TG} = 0.95 V. The electron density and mobility derived from this measurement are $n_e = 3.9 \times 10^{11}$ 1/cm^2 and $\mu_e = 3.0 \times 10^5$ cm^2/Vs.

3.2 Electron Density Tuning Regime and Dominant Scattering Mechanism

By leveraging the quantum Hall effect, we can assess the electron density tuning regime for the FES and infer the dominant scattering mechanisms influencing electron transport through mobility measurements. The tuning range and corresponding mobility are crucial indicators of FES performance and suitability for applications like quantum circuits. In this section, we will compare the transport and tuning properties of the five FESs, correlating their stack designs with transport characteristics, which highlights the importance of the FES layer stack and fabrication details for their applications.
The electron density tuning regime is defined by the TG voltage tunable range of n_e lying within the linear regime, i.e., not being affected by tunneling of electrons out of the QW and thus hysteretic behavior. Staying within this operation window allows for reproducible tuning of n_e by the TG voltage. A larger n_e range is beneficial as it provides a wider tuning scope, allowing for greater control, especially in advanced quantum applications.
The electron density in dependence of the TG voltage for all five FESs is shown in Fig. 3.3. For all FES the typical behavior of a linear increase of n_e with the applied TG voltage U_{TG} transitioning into a saturation, as already discussed in Sec. 2.2, can be observed. However, when comparing the electron density tuning regimes of the five FES devices, the difference in the minimum electron density $n_{e,\,min}$ and maximum electron density $n_{e,\,max}$ defining beginning and end of the linear electron density tuning regime, i.e., operation window, becomes clearly visible. Whereas the capacitive coupling of the TG to the 2DEG, which shows as the slope of the linear regime, and absolute TG of the operation window can be tailored within certain extent by the oxide material and thickness, the accessible $n_{e,\,min}$ and $n_{e,\,max}$ are closely linked to the heterostructure growth details.
Comparing the minimum electron density of the five FES in Fig. 3.3 the lowest value is observed for FES D followed by FES A, B, C and E. The corresponding $n_{e,\,min}$ values, which we evaluate at the accumulation point U_{Acc} (see definition in Sec. 2.8), are presented in Tab. 3.2. We chose the definition of U_{Acc} to ensure a fully accumulated 2DEG, i.e., being beyond the characteristic metal-insulator transition of gated semiconductors, allowing a metal-like conduction (see Sec. 2.2). At this point, we want to emphasize that $n_{e,\,min} > n_{crit}$, where n_{crit} corresponds to the critical electron density of the metal-insulator transition. Since n_{crit} is challenging to determine and lacks unified standards for experimental measurement, we defined U_{Acc} to provide a well-defined and comparable metric for Hall-bar measurements, based on a conductivity threshold along the Hall-bar channel.
Fig. 3.4 illustrates the impact of potential fluctuations of the conduction band edge on the 2DEG accumulation. Fig. 3.4 a) illustrates the scenario below the accumulation point, where the Fermi energy E_F is lying within the energetic span of the potential fluctuations, leading to a non-uniform "puddle"-like occupation of the potential minima by electrons. To fully accumulate the 2DEG, the entire energy range of the potential fluctuations must

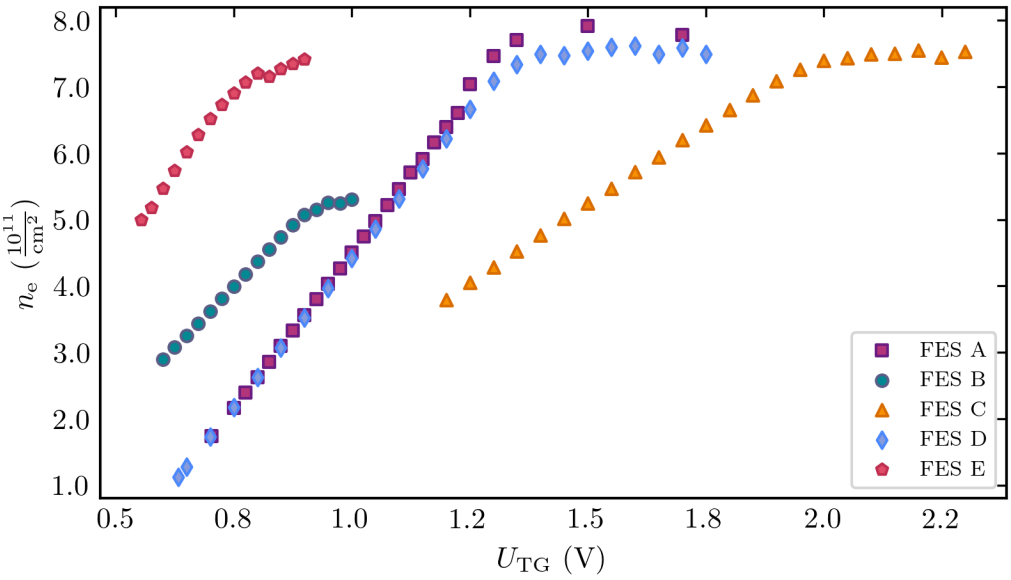

Figure 3.3: Comparison of the electron density tuning regime for the five FESs. The electron density n_e is shown in dependence of the applied TG voltage U_{TG}.

FES	A	B	C	D	E
$n_{e,\,min}$ ($\frac{10^{11}}{cm^2}$)	1.7	2.9	3.8	1.1	5.0
$n_{e,\,max}$ ($\frac{10^{11}}{cm^2}$)	7.7	5.0	7.3	7.1	6.7
$\mu_{e,\,min}$ ($\frac{10^5 cm^2}{Vs}$)	1.4	0.6	0.3	0.9	0.3
$\mu_{e,\,max}$ ($\frac{10^5 cm^2}{Vs}$)	3.4	1.0	0.7	3.9	0.6
TDD ($\frac{10^7}{cm^2}$)	<0.6	1.4	5.0	<0.6	—

Table 3.2: Comparison of the five FESs in their minimum electron density $n_{e,\,min}$, maximum electron density $n_{e,\,max}$, minimum electron mobility $\mu_{e,\,min}$, maximum electron mobility $\mu_{e,\,max}$ and threading dislocation density TDD. The minimum electron density is defined as the electron density at the accumulation point. The maximum electron density is defined as the lowest electron density deviating more than 2% from a linear fit through the linear regime. The minimum and maximum electron mobility are evaluated at $n_{e,\,min}$ and $n_{e,\,max}$ respectively. The TDD was evaluated via etch pit count measurements by our partners at the *IHP - Leibniz-Institut für Innovative Mikroelektronik*.

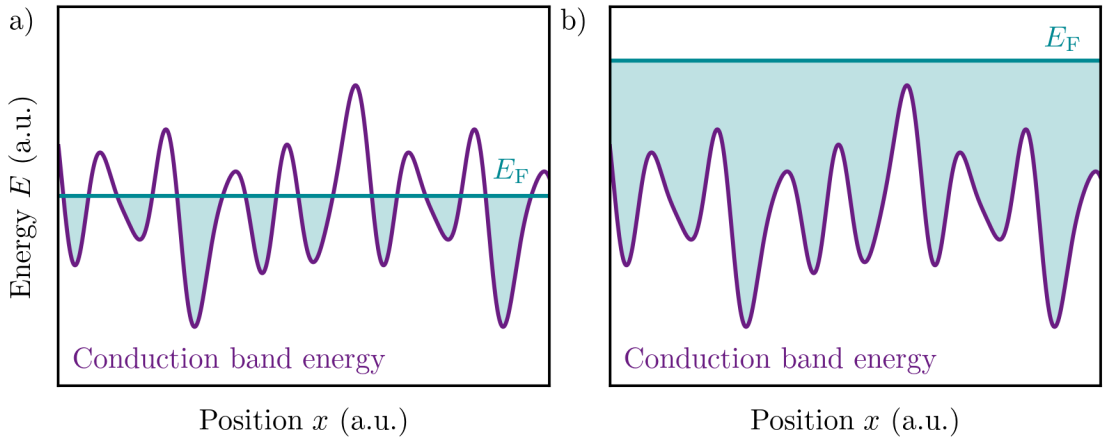

Figure 3.4: Impact of potential fluctuations of the conduction band edge on the 2DEG accumulation. The purple line sketches the conduction band edge energy impacted by surrounding defects inherent to the heterostructure. The Fermi energy determining the occupied states (light blue) is shown as blue line. a) The scenario of a Fermi energy lying within the energetic span of the potential fluctuations leading to non-uniform "puddle"-like occupation of the potential minima by electrons. b) The scenario of a Fermi energy lying above the energetic span of the potential fluctuations leading to a uniform accumulation of electrons across the whole conduction band.

be shifted below the Fermi energy, as depicted in Fig. 3.4 b). This allows for uniform accumulation of electrons across the whole conduction band. The larger the energetic span of the potential fluctuations, the further the conduction band needs to be shifted below E_F, and consequently, the higher the minimum electron density at U_{Acc} becomes. This makes $n_{e,\,min}$ an insightful quality factor for any kind of defects or impurities especially in vicinity of the QW impacting the 2DEG conduction band potential. The comparison of the $n_{e,\,min}$ for the five FES indicates that FES D exhibits the lowest extent of potential fluctuations, while they progressively increase for FES A, B, C, and E, with FES E being the most affected by potential fluctuations.
One of the most prominent dislocations within these heterostructures known to deteriorate the transport properties of the QW are threading dislocations [37, 38], previously described in more detail in Sec. 2.1. Threading dislocations passing through the QW alter the potential landscape of the QW ground state, leading to increased potential fluctuations. The threading dislocations density (TDD) for FES B and C were measured by our partners at the *IHP - Leibniz-Institut für Innovative Mikroelektronik* via etch pit count measurements. The results are shown in Tab. 3.2. For FES A and D they can estimate an upper limit of TDD based on heterostructures grown by the same fabrication recipe. The TDDs show that FES A and D posses less threading dislocations than FES B and this one even less than FES C. This matches the expectation from the observed $n_{e,\,min}$.
The reduced TDD of FES A and D can be attributed to the thicker virtual substrate layer in these two FESs compared to FES B, C and E, which is known to be beneficial for

reducing the TDD (see Sec. 2.1). The virtual substrate thickness t_{VS} is more than three times thicker (see Tab. 3.2). A thicker virtual substrate allows more threading dislocations to laterally leave the crystal without entering the QW region. The increase in TDD of FES C compared to B, both inheriting a very similar virtual substrate thickness, could be caused by the increase in Ge content as it was observed to correlate to an increased TDD [38].
Comparing FES A and D, which were fabricated very similar, the observation of a higher $n_{e,\,min}$ for FES A is likely not caused by a difference in TDD. The main difference between those two FES is, as previously mentioned, a longer wait time between the SiGe barrier growth and the growth of the Si QW due to the varied growth temperature. During this longer wait time it is more likely for impurity atoms like e.g. oxygen to contaminate the growth. These impurities especially as they are in close vicinity to the QW are expected to be adverse for the the transport properties [47]. The increased $n_{e,\,min}$ of FES A compared to FES D strengthens the assumption that more impurities are located close to QW.
For the commercially grown FES E no TDD measurement is available, but when considering the previous trend in $n_{e,\,min}$, it can be suggested that it is the most affected by potential fluctuations and thus probably inherits the most impurities or defects in the vicinity of the QW. This could be caused by an increased TDD compared to the other four FESs or contamination with impurities.
Further insights into the heterostructures can be gained by comparing the maximum electron density of the five FESs, which marks the end of the linear tuning regime and occurs when tunneling from the QW to the dielectric interface sets in. We evaluated this as the first n_e to deviate by more than 2% from the fitted linear regime. The corresponding values for the five FESs are presented in Tab. 3.2. The $n_{e,\,max}$ is known to be directly correlated to the Ge content x [49]. This can be understood as with increasing x the energetic height of the SiGe barrier to overcome increases and tunneling sets in for higher electron densities. Comparing the x of the five FES shown in Tab. 3.1 and the $n_{e,\,max}$ shown in Tab. 3.2 the correlation between Ge content and $n_{e,\,max}$ is clearly observable.
The impact of the depth of the QW, i.e., the thickness t_{Spacer} of the upper SiGe barrier, on $n_{e,\,max}$ has not yet been fully systematically studied in Si/$Si_{1-x}Ge_x$ heterostructures. First results indicate that, unless the QW depth is shallow enough for direct tunneling to set in, $n_{e,\,max}$ does not depend on the spacer thickness [49, 51, 68]. For the five FES no direct tunneling, which would manifest as no distinct linear regime occurring in the n_e dependence on the U_{TG}, is observed and thus no impact of t_{Spacer} on $n_{e,\,max}$ is expected.
A new aspect, to our knowledge not yet systematically studied, is the impact of the absence of a Si cap on the $n_{e,\,max}$. We do not observe any adverse effect of the absence of a Si cap on the $n_{e,\,max}$. To the contrary, FES A and D show the highest maximum electron densities. The absence of the Si cap could be assumed to reduce the amount of unoccupied states at the dielectric/heterostructure interface and thus decrease the tunneling probability of electrons from the QW to the interface, which could be beneficial for $n_{e,\,max}$. However, this assumptions is up to further testing as FES A and D distinguish in too many parameters from FES B, C and D to attribute this to the absence of a Si cap.

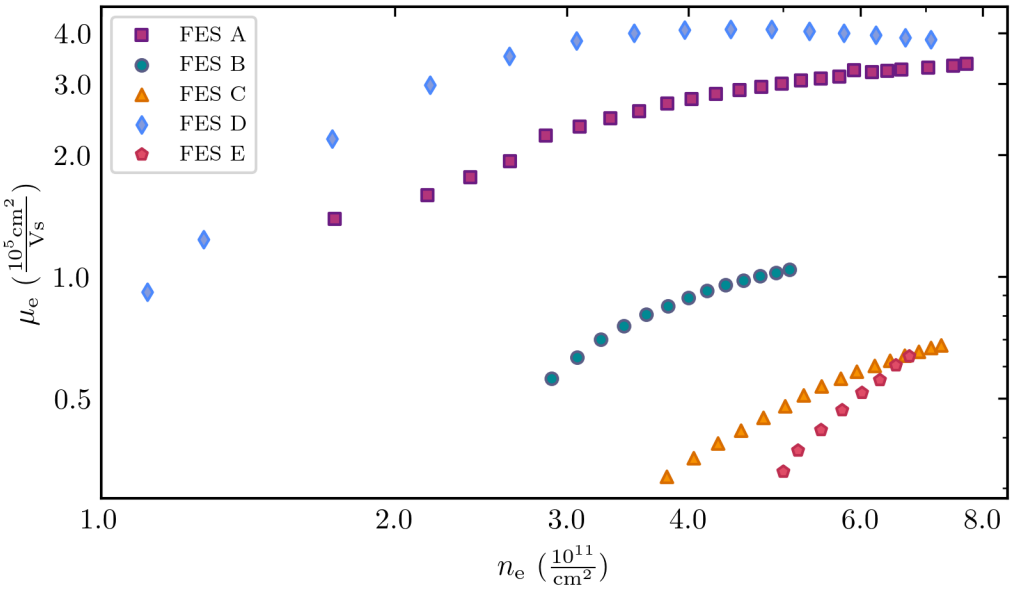

Figure 3.5: Comparison of the electron mobility μ_e for the five FESs as a function of the electron density n_e within the linear regime, plotted on a double logarithmic scale.

The second key quality feature for assessing the FES operation region beside the electron density tuning regime is the corresponding electron mobility. It serves as a key metric how scattering impacts electron transport, providing further important insights for drawing conclusions about the FES.
Fig. 3.5 shows the electron mobility μ_e for the five FESs in dependence of the respective n_e within the linear regime. As μ_e is dependent on n_e (see Sec. 2.3), comparing μ_e between the five FESs is only meaningful when considering it as a function of n_e. We observe that the μ_e accessible within the linear n_e regime increases in the sequence from FES E, C, B, A to D. The minimum electron mobility $\mu_{e,\,min}$ and the maximum electron mobility $\mu_{e,\,max}$ for the five compared FESs, evaluated at $n_{e,\,min}$ and $n_{e,\,max}$ respectively, are summarized in Tab. 3.2. Since the μ_e is directly related to the number of scattering events, the observed increase in μ_e indicates a reduction in the number of scattering centers that disrupt electron transport within the 2DEG of the FESs.
To gain deeper insights into the origin of the dominant scattering mechanisms within the FESs, we can evaluate the μ_e as a function of n_e. It is an empirical observation deduced from other material platforms like GaAs/AlGaAs structures, Si MOSFETs and doped Si heterostructures [51] that the μ_e follows a power-law dependence on n_e

$$\mu_e \propto n_e^{\alpha}, \tag{3.1}$$

with the exponent α being insightful for the scattering mechanism [51]. To allow for a direct comparison of the slopes between the different FESs, Fig. 3.5 is presented as a double logarithmic plot. Two different scattering mechanisms that prevail in such

FESs can be distinguished by the steepness of their slopes [38, 47, 48]: First, long-range scattering caused by charges trapped at the heterostructure/dielectric interface, which manifests as a steep increase in μ_e with n_e, as these charges can be effectively shielded by the increasing number of electrons within the 2DEG. Second, short-range scattering arising from defects or impurities located near the QW, leading to a more gradual increase in μ_e with increasing n_e, as these scattering centers are less effectively shielded by additional electrons within the 2DEG. Long-range scattering typically dominates in the low-electron-density regime, whereas both long-range and short-range scattering can dominate at higher electron densities.
Comparing the slopes of the five presented FESs it can be observed that FES D, inheriting the highest overall electron mobility, shows the expected steep increase of μ_e in the regime of lower n_e transitioning into a flat slope in the high n_e regime. It can be deduced that transport within FES D is dominated by long-range scattering for lower n_e and dominated by short-range scattering for higher n_e. In comparison with the other FESs, a trend shows that as the overall μ_e decreases, the clear distinction between the two slope regimes diminishes, resulting in a progressively more uniform slope. This suggests that the FESs become increasingly dominated by short-range scattering throughout the entire linear n_e regime.
This trend indeed matches our previous observations on the $n_{e,\,min}$, evident as both properties are greatly impacted by scattering centers in vicinity of the QW: The more the transport properties are impacted by defects in vicinity to the QW the larger the $n_{e,\,min}$ and the more uniform the slope of μ_e. As previously discussed, these observations match the trend of increasing TDD throughout the FESs. Comparing FES A and D, likely inheriting a similar amount of TDD, the more pronounced impact of short-range scattering for FES A can be understood by the increased amount of impurity atoms caused by the delay time in between the QW and barrier growth. An adverse effect on the electron mobility has already been observed for a contamination with oxygen atoms [47]. By placing FES E within this trend it strengthens the previous assumption of being impacted the most compared to the other FESs by defects or impurities in vicinity to the QW.
Comparison of the five FESs highlights that, although all represent state-of-the-art designs for field-effect applications, they display significant variation in electron density tuning regimes and corresponding mobility. This underscores the strong correlation between transport properties and layer stack as well as fabrication details. Further exploration, such as the impact of a missing Si cap in certain FESs, could provide valuable insights for further optimization and tailoring of FESs for their field-effect applications like quantum circuits.

4

Impact of Biased Cooling on Field-Effect Devices

FESs, which are the foundation of our semiconductor spin qubits, offer purely electrostatic gate-tunability of electric carriers down to the nanoscale. This underscores the importance of a precise understanding of the electrostatics generated by gate tuning, which is increasingly recognized as critical for the stable operation of quantum circuits [18, 61, 62, 64–66, 69, 70]. In undoped gated devices, the gate dielectrics interfacing with the silicon-based semiconductor play a key role. In particular, the interface between the typically polycrystalline dielectric and the single-crystalline semiconductor has garnered growing attention, as charge traps at this interface can significantly impact device performance, influencing both gate-tunability and charge noise in quantum circuits. Typically, FESs are cooled down with zero bias applied to the gates. *Biased cooling* represents the cool-down under a non-zero applied gate voltage. Biased cool-down has been studied for modulation-doped GaAs/AlGaAs quantum well heterojunctions in the context of the operation of 2DEGs [71–74] and of quantum point contacts [75, 76]. In these works, the observed impact on the operation of the devices have been phenomenologically linked to the presence of dopant-induced defects and to leakage of Schottky gates. The statistical nature of dopant-induced defects and of the presence of leakage has limited the application of biased cooling as an additional degree of freedom for the device operation. More recently, in particular for spin qubit quantum circuits, FES based on undoped semiconductor heterostructures and including oxide-based dielectrics instead of Schottky gates are used [42, 70, 77]. The absence of dopant-induced defects and the dielectric/semiconductor interface in the FES create an electrostatic environment in which biased cooling had not yet been considered at the beginning of my dissertation. The growing interest in this topic is also reflected in a only recently published report of biased cooling-depending shifts of the turn-on voltage in a single electron transistor device [78].

In this chapter, we systematically study the effect of biased cooling on the charge state of the dielectric/semiconductor interface as well as the impact of the modified electrostatics

on the transport properties of the 2DEG in the Si/SiGe QW. We particularly discuss the impact of biased cooling on the electron density and the electron mobility under gate-tuning of the 2DEG, as well as on the temporal stability, saturation behavior and reproducibility of the 2DEG density. Additionally, we present an empirical model based on charge traps at the dielectric/semiconductor interface, which includes all experimental trends observed in our systematic study. For the investigation we select three of the five previously presented FES – A, B, and C – focusing on key characteristic differences. These FESs differ in the presence of a Si cap, the dielectric material and its thickness, and the epitaxy method used for the heterostructures (CVD vs. MBE). They also vary in Ge content and SiGe barrier thickness. Furthermore, FES A was grown and fabricated at a different facility than FES B and C. Our results show that biased cooling can provide an useful tuning parameter for field-effect devices and quantum circuits especially for qubit applications. Furthermore, they contribute to a better understanding of correlations between FES operation and the properties of the dielectric/semiconductor interface.
The biased cooling investigations were conducted at a temperature of 1.5 K using our ^{4}He cryostat, combined with the Hall-bar geometry measurement technique described in Ch. 2.8. The complete series of biased cooling measurements for all three FESs, along with a detailed list of all determined values and further analysis, can be found in the master's thesis of L. Zinkl [79], whom I collaborated with on this topic and whose master's thesis I supervised. The main findings discussed in the subsequent chapter are also published in [80, 81].

4.1 Impact of Biased Cooling on the 2DEG Characteristics

We find the heterostructures in all three FESs to be conducting at room temperature for any U_{TG} value, even at $U_{\mathrm{TG}} = 0\,\mathrm{V}$. At the contrary, we observe the conductance of the heterostructure to freeze-out during the cool-down to 1.5 K, stating that the 2DEGs are normally off at $U_{\mathrm{TG}} = 0\,\mathrm{V}$. To explore the influence of the biased cooling on the transport properties of a 2DEG, we apply a non-zero voltage at the TG while cooling down the FESs from room temperature to 1.5 K. We refer to this voltage applied during the cool-down as *biased cooling voltage* U_{BC}. We cooled down the FESs various times with varying U_{BC} and determined the electron density as a function of the applied TG voltage (U_{TG} sweep) at 1.5 K for each cool-down. These measurements were performed for all three FES A, B and C. Fig. 4.1 a) representatively shows the results for FES A. The FES cooled down with the commonly used $U_{\mathrm{BC}} = 0\,\mathrm{V}$ shows the state-of-the-art behavior of a 2DEG accumulating within the Si QW at a positive U_{TG} (see Sec. 3.2). As seen in Fig. 4.1 a), we find the characteristic behavior of a linear increase of n_{e}, followed by a saturation, to be independent of the applied U_{BC}. In quantum Hall experiments for selected negative and positive U_{BC}, we have verified that the electron density contributing to the transport after cooling down with a non-zero U_{BC} is exclusively located in the QW 2DEG, excluding

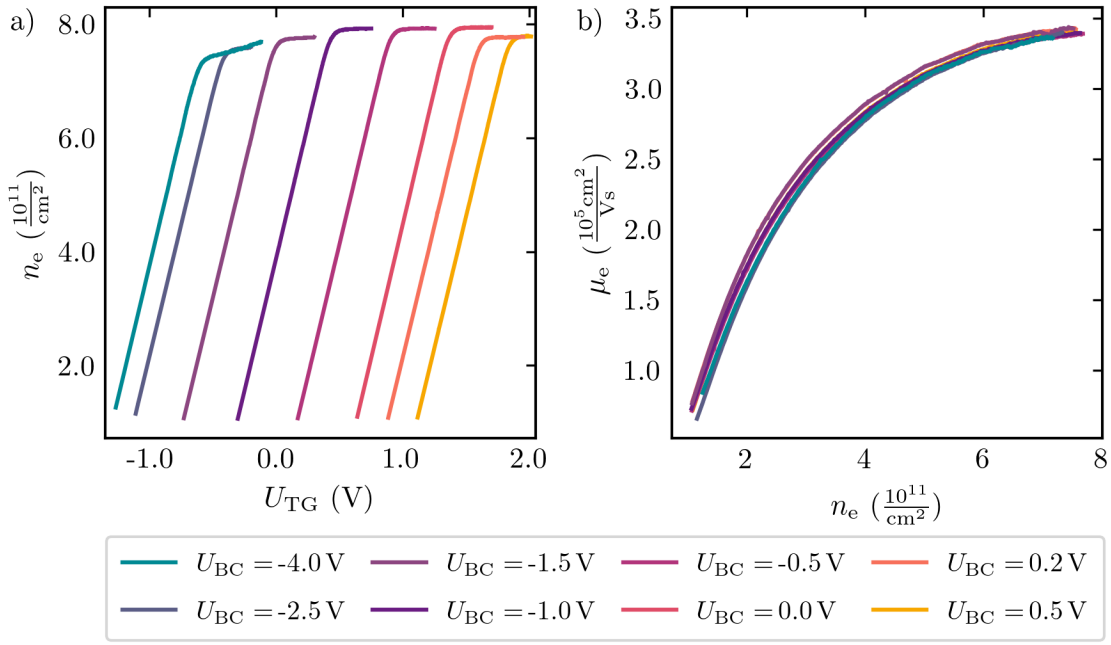

Figure 4.1: Impact of biased cooling on the electron density and the mobility of the 2DEG, representatively shown for FES A at 1.5 K. The definitions of the different voltages and of $n_{e,max}$ are found in the text. a) 2DEG density n_e as a function of U_{TG} for different biased cooling voltages U_{BC}. b) 2DEG mobility μ_e dependence on n_e within the linear capacitive coupling regime ($n_e < n_{e,max}$) for different biased cooling voltages U_{BC}.

measurable, biased cooling-induced parallel conductance. Comparing the electron density curves, we observe a shift induced by U_{BC}. For positive biased cooling voltages applied during the cool-down, the electron density curves shift towards more positive/higher U_{TG}, whereas for negative biased cooling they shift towards more negative/lower U_{TG}. The shift increases with the absolute value of the U_{BC} applied during cool-down.
In the remainder of this chapter, we focus on the linear electron density tuning regime, which is the operation region for most field-effect device applications, including quantum circuits. We have verified that the 2DEG densities n_e are reproducible within cool-downs in all three FESs (no hysteresis of the electron density in a U_{TG} sweep). They are also reproducible among separate cool-downs for a given U_{BC} value. Across all FES, we observe no systematic dependence of the minimum electron density $n_{e,min}$ as well as of the maximum electron density $n_{e,max}$ on U_{BC}. Also, the slope of the 2DEG density's U_{TG}-dependence - which represents the capacitive coupling between the TG and the 2DEG - is unaffected by biased cooling with $U_{BC} \neq 0\,V$ for all three FESs (see Fig. 4.1 a) representatively for FES A). In Fig. 4.1 b), we report the 2DEG mobility μ_e as a function of n_e for all tested U_{BC}, representatively for FES A. No impact of U_{BC} on the μ_e is observed.
To summarize the key features observed for the three FESs and representatively shown

for stack A in Fig. 4.1: The main consequence of the biased cooling effect is a shift of the field-effect tuned 2DEG density compared to $U_{BC} = 0\,V$, the shift increasing with the absolute value of U_{BC}. At the same time, the U_{TG}-tunable n_e range, the capacitive coupling between the TG and the 2DEG and the μ_e at each given n_e are unaffected by U_{BC}. Finally, the heterostructures are conductive at room temperature, while this conductivity vanished during the cool-down. At this point it should be highlighted that these observations are identical in all three FESs, although they differ with respect to the presence of a Si cap, the dielectric material and its thickness as well as in the epitaxy method of the heterostructures (CVD vs. MBE), their Ge content and the thicknesses of the SiGe barrier (see Fig. 3.1 and Tab. 3.1). Also FES A has been grown and fabricated in different facility than FES B and C.
A plausible source for the observed experimental phenomenology is an additional static U_{BC}-dependent electric field which superimposes onto the field resulting from U_{TG} at the QW at 1.5 K. The charge causing this static field needs to be adjustable by the applied U_{BC} at room temperature, to explain the U_{BC}-dependent shift of the accumulation voltage U_{Acc} (defined in Sec. 2.8). At the same time, to guarantee the observed parallel shift - i.e., constant capacitive coupling - of the U_{TG} sweeps in Fig. 4.1 a), this charge must be independent of U_{TG} at 1.5 K. Since we verified via quantum Hall traces that no measurable parallel conductance channel occurs at 1.5 K after cooling down with $U_{BC} \neq 0\,V$, i.e., that transport occurs solely within the 2DEG, this additional charge must be immobile under device operation at 1.5 K. In case this hypothetical charge would build-up in the vicinity of the QW after cooling down with $U_{BC} \neq 0\,V$, we would expect a variation in the potential fluctuations affecting the 2DEG in correlation to U_{BC}. As we experimentally find the 2DEG mobility at higher 2DEG densities (Fig. 4.1 b)) and also the minimum 2DEG density $n_{e,min}$ (Fig. 4.1 a)) to be unaffected by U_{BC} in all three FESs, we conclude that the charge build-up occurs further away from the QW and is homogeneously distributed. Given that the SiGe barrier is undoped, the most plausible locations are the thin oxidized Si cap and the heterostructure interface with the polycrystalline dielectric oxide. As FES A, in contrast to B and C, does not contain a (oxidized) Si cap, but nevertheless shows the same behavior under the influence of biased cooling, we exclude the necessity of a Si cap for this effect. Hence, from the previously acquired requirements we conclude that the charges induced at room temperature by the U_{BC} are localized at the interface between the heterostructure and the polycrystalline dielectric. This interface meets all the criteria. It has been previously shown to host a large enough density of trap states to allow for charge build-ups up to a screening of the capacitive coupling between the TG and the 2DEG [41, 49–51]. Its location in between the TG and the QW allows the electric field of the trapped interface charges to statically superimpose the electric field of the TG effectively, without being to close to the QW to influence the 2DEG mobility and the minimum 2DEG density. We have verified in 1D Schrödinger-Poisson simulations that the introduction of a fixed charge density at the dielectric/heterostructure interface allows to mimic the experimental behavior reported in Fig. 4.1 a). The corresponding simulations are presented in [79]. The required charge density is of the order of $10^{11-12}\,1/cm^2$, in accordance with reports on charge traps [41, 49–51] and capacitance-voltage estimations for the oxide used in

FES A. Since all three heterostructures are conductive at room temperature, positive as well as negative U_{BC} may induce the hypothetical charges exerting the static electric field by loading or unloading trap states at the interface. At the contrary, the freeze-out of the conductance of the heterostructure during the cool-down to 1.5 K, suppresses this loading mechanism of interface trap states.

4.2 Empirical Model for Biased Cooling of Undoped QW Heterostructures

Based on this hypothesis, we develop a model for the biased cooling effect in the following. Our model relies on the fact that the TG and the interface between the heterostructure and the dielectric act like a classical capacitor at room temperature. Essential ingredients of the model are sketched in Fig. 4.2. The mechanism for loading and unloading the interface at room temperature - and hence before the freeze-out of the heterostructure - are sketched in Fig. 4.2 a). Panel 4.2 a) i) shows the conductance band edge energy of the heterostructure stack (dark purple line) for $U_{\mathrm{BC}} = 0\,\mathrm{V}$, with the ground state energy of the Si QW depicted in dark gray. For simplicity, we illustrate this reference case with a flat band edge. These interface states (sketched as purple circles) are populated up to the Fermi energy (blue dashed line) with electrons (pink dots). A non-zero applied U_{BC} at the TG results in a tilt of the band edge in the sketches. In the case of a $U_{\mathrm{BC}} < 0\,\mathrm{V}$ this lifts a certain amount Q of occupied interface states above the Fermi energy (non-equilibrium situation) shown in panel 4.2 a) ii). Due to the room temperature conductivity of the FES, these electrons will, however, quickly unload from the interface. This results in a less negative/more positive charge configuration at the interface. As a consequence, two properties of the classical capacitor formed by the TG and the dielectric/heterostructure interface manifest, as sketched in panel 4.2 a) iii): First, the band bending between the TG and the interface steepens in the dielectric compared to panel 4.2 a) ii) proportionally to the charge reconfiguration. Second, outside of the capacitor - i.e., below the interface (in the heterostructure) - there is no electric field. Hence, the conduction band is flat again, as in panel 4.2 a) i). In exact analogy, for $U_{\mathrm{BC}} > 0\,\mathrm{V}$, the applied electric field leads to pushing unoccupied interface states containing Q charges below the Fermi energy (see panel 4.2 a) iv)) in non-equilibrium. The charge reconfiguration resulting from the room temperature conductivity of the FES hence adds the amount Q of electrons to the interface (see Fig. 4.2 a) v)). Thus, we end up in a more negative charge configuration at the interface compared to panel 4.2 a) i). The model in Fig. 4.2 a) highlights two features, which are key to explain the experimental observations: The applied U_{BC} changes the charge state at the interface. Also, the energetic position of the TG relative to the QW ground state energy changes as a function of the applied U_{BC}, while flat band conditions are retained between the interface and the QW. Note that both features result from the fact that the TG and the dielectric/heterostructure interface behave like the plates of a classical capacitor before freeze-out.

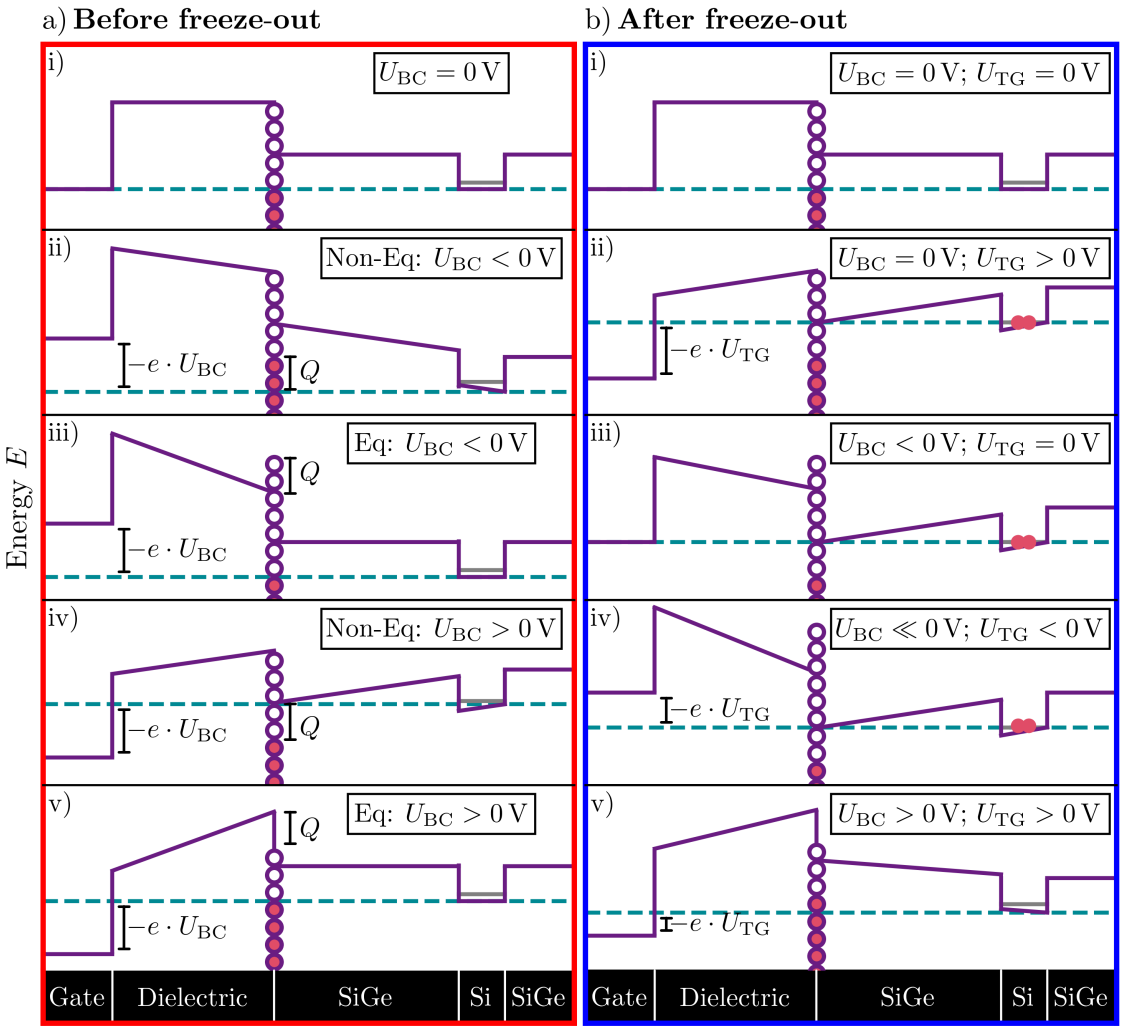

Figure 4.2: Empirical model of the biased cooling effect. The panels i)-v) in a) and b) are discussed in detail in the text. The purple line depicts the conduction band edge for different regions of the gate stack indicated at the bottom of the figure. The dark gray line within the Si represents the confined ground state energy of the QW. We chose to fix the lower end of the QW conduction band energy at 0 V. The blue dashed line illustrates the Fermi energy. The empty purple circles between the dielectric and the SiGe depict empty trap states at the dielectric/heterostructure interface. Electrons are shown as pink colored dots and can fill these states at the interface. a) Impact of U_{BC} applied before freeze-out of the heterostructure. At these temperatures, the heterostructure is conductive. Each panel i) to v) illustrates a distinct equilibrium or non-equilibrium for specific U_{BC} situations. The charge Q results from electrons, which are loaded to or unloaded from the interface due to the applied U_{BC}. b) Impact of U_{BC} after freeze-out of the conductivity of the heterostructure. At the typical device operation temperature 1.5 K, the electrons at the interface then can not be loaded or unloaded anymore. Each panel i) to v) illustrates a specific scenario of combination of U_{BC} and U_{TG}. Electrons within the Si QW illustrate the accumulation of the 2DEG.

Moving now to temperatures cold enough to freeze-out the conductance of the heterostructure, a major consequence for our model is the suppression of loading or unloading of the trap states at the interface via the heterostructure. Hence, the charges Q trapped at the interface states before cool-down will then be insensitive to the U_{TG} applied after freeze-out. Fig. 4.2 b) i), as a reference, shows the scenario of a FES which was cooled down with $U_{\mathrm{BC}} = 0\,\mathrm{V}$, keeping $U_{\mathrm{TG}} = 0\,\mathrm{V}$ after freeze-out. The charge density at the interface is non-zero and the QW ground state is above the Fermi energy. Hence no electrons are accumulated in the QW. In order to accumulate electrons within the QW, it is necessary to apply a positive U_{TG} strong enough to drag the QW ground state below the Fermi energy as illustrated in panel 4.2 b) ii). Importantly, since the interface states can not be loaded after freeze-out, the empty interface states pushed below the Fermi level will stay unoccupied, leaving the electric field induced by the electrons trapped at the interface unaffected by U_{TG} variations. The electron accumulation in the QW is sketched as pink dots. The density of accumulated electrons in the 2DEG located in the QW is proportional to U_{TG}, experimentally resulting in the typical FES electron density curve shown for $U_{\mathrm{BC}} = 0\,\mathrm{V}$ in Fig. 4.1 a). Next, Fig. 4.2 b) iii) illustrates the case of a negative U_{BC}. Compared to $U_{\mathrm{BC}} = 0\,\mathrm{V}$, the diminished electron density at the interface leads to a less negative electric field superimposing the field created by U_{TG}. This is visible as an additional downwards tilt of the conduction band. The tilt drags the QW ground state closer to the Fermi energy. Now, a less positive U_{TG} (e.g., $U_{\mathrm{TG}} = 0\,\mathrm{V}$) is required to accumulate electrons within the QW, in line with the electron density curves being shifted towards more negative U_{TG} in the experiment, as observed in Fig. 4.1 a). For even stronger negative U_{BC} applied during cool-down, Fig. 4.2 b) iv) illustrates the ability to already accumulate electrons in the QW at negative U_{TG}, capturing the experimental observation that the electron density curves are shifted even further towards negative U_{TG}. Fig. 4.2 b) v) shows the opposite scenario of a positive U_{BC} applied during the cool-down. The increased electron density at the interface causes a stronger shielding of the U_{TG} compared to $U_{\mathrm{BC}} = 0\,\mathrm{V}$, resulting in the experimentally observed shift of the electron density curves towards more positive U_{TG} (see Fig. 4.1 a)).
Summarizing our experimental observations and the empirical model, applying U_{BC} at room temperature traps an amount of charges $Q = C_{\mathrm{BC}} \cdot U_{\mathrm{BC}}$ at the dielectric/heterostructure interface (see Fig. 4.2 a) ii) to v)), where C_{BC} is the capacitive coupling between the TG and the conductive heterostructure during biased cool-down, before freeze-out. After freeze-out, the charge trapping mechanism is suppressed, turning Q into being insensitive to U_{TG} (applied to the FES at 1.5 K). The constant, static electric field created by the trapped charges $Q(U_{\mathrm{BC}})$ then superimposes the field imposed with a U_{TG} sweep (see Fig. 4.2 b)). This is equivalent to stating that the accumulation voltage U_{Acc} of the 2DEG will be shifted exactly by U_{BC} with respect to $U_{\mathrm{BC}} = 0\,\mathrm{V}$. As a consequence, our model predicts a linear relationship between $\Delta U_{\mathrm{Acc}} = U_{\mathrm{Acc}} - U_{\mathrm{Acc},\,U_{\mathrm{BC}}=0\,\mathrm{V}}$ and U_{BC}, with a slope $s = 1$. In Fig. 4.3, we test this prediction by displaying ΔU_{Acc} for all three FESs. The linear relationship is indeed verified in a significant range of U_{BC}. Also, the slopes s are only slightly smaller than 1, with $s = 0.9\,\mathrm{V/V}$ for FES A and C and $s = 0.8\,\mathrm{V/V}$ for FES B. This slight deviation seems to indicate that C_{BC} is a bit smaller than the

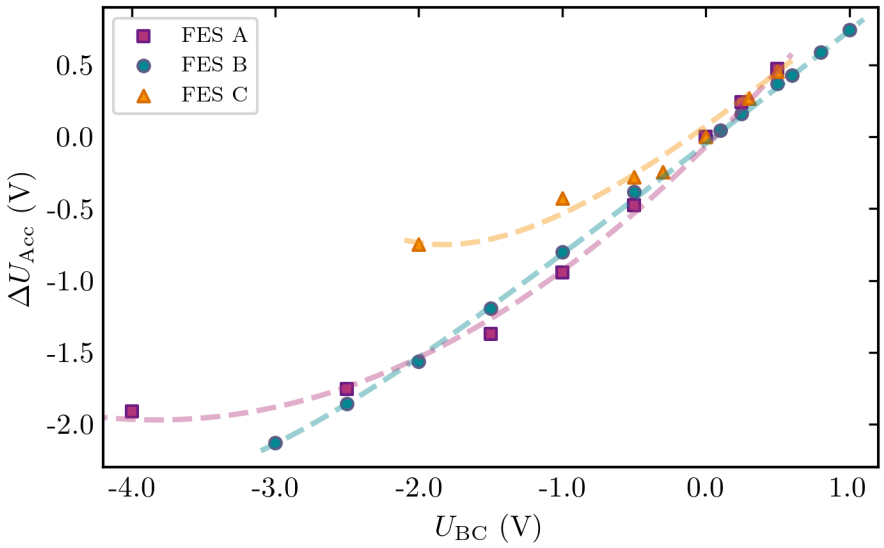

Figure 4.3: Shift of the 2DEG accumulation point ΔU_{Acc} as a function of U_{BC} for all three FESs. The dashed lines are guides to the eyes.

capacitive coupling at 1.5 K. As a second feature of Fig. 4.3, we observe a deviation from the linear relationship beyond a certain negative value of U_{BC} for each FES. This suggests that the amount of interface states per energy interval decreases for larger negative U_{BC} and thus lower energies in Fig. 4.2 b). Hence, less charges are unloaded from trap states at the interface at room temperature for these U_{BC}. Note that FES A does not include a Si cap, while FES B and C do and that they were fabricated at different facilities with different fabrication methods and dielectrics. Both, the deviation from linearity of ΔU_{Acc} and the slight variation of the capacitive coupling between 1.5 K and warmer temperatures (slope $s < 1$) thus seem to sensitively depend on non-systematic and subtle details of the FES fabrication.

4.3 Tunability of the FES Operation Region after Freeze-Out

Up to here, based on the experimental observations, we have concluded that the amount of trapped charges Q at the dielectric/heterostructure interface does not change when varying $U_{\mathrm{TG}} > U_{\mathrm{BC}}$ at 1.5 K. To test this observation in more detail, we investigate whether, after a given cool-down with U_{BC}, the trapped charge density at the interface n_{Int} can be influenced at 1.5 K when applying $U_{\mathrm{TG}} = U_{\mathrm{D}}$ *beyond the depletion of the 2DEG* ($U_{\mathrm{D}} < U_{\mathrm{Acc}}$). A related experimental approach has recently been used to homogenize local accumulation voltages in quantum circuits without biased cooling [66, 82]. We denote $U_{\mathrm{Acc,\,sweep\,\#\,=\,0}}$ as the accumulation point observed after biased cooling with U_{BC},

tied to its corresponding value of n_{Int}. We then interpret any deviation of the 2DEG accumulation point observed after applying U_{D} ($U_{\mathrm{D}} < U_{\mathrm{Acc,\,sweep\,\#\,=\,0}}$) as an indicator for a modification of n_{Int} at 1.5 K. Experimentally, we perform a series of U_{TG} sweeps at 1.5 K, within the same cool-down. Each sweep i starts from a value $U_{\mathrm{TG}} = U_{\mathrm{D}}$ beyond the depletion of the 2DEG, before the 2DEG is driven into accumulation again, to record the corresponding accumulation point $U_{\mathrm{Acc,\,sweep\,\#\,=\,i}}$. In the accumulation, we explicitly avoided to enter the saturation regime where tunneling between the 2DEG and the interface sets in. Such sweep series were carried out on FES A and FES C, each time for most of the biased cooling voltages tested on that FES (see Fig. 4.1 for FES A).
For each sweep i, we evaluated the relative deviation of the accumulation point of the 2DEG:

$$U_{\mathrm{Acc}}^{\mathrm{Dev}}(\text{sweep \#=i}) = \frac{U_{\mathrm{Acc,\,sweep\,\#\,=\,i}} - U_{\mathrm{Acc,\,sweep\#\,=\,0}}}{U_{\mathrm{Acc,\,sweep\,\#\,=\,0}} - U_{\mathrm{BC}}}. \tag{4.1}$$

Fig. 4.4 a) exemplarily reports observed values of $U_{\mathrm{Acc}}^{\mathrm{Dev}}$ for two separate biased cool-downs of FES A, $U_{\mathrm{BC}} = 0$ V and $U_{\mathrm{BC}} = -0.5$ V. The sweeps are numbered consecutively (sweep #) in chronological order starting at zero for the accumulation point obtained directly after biased cool-down at U_{BC}. The chronological series of sweeps i contains random variations of the depletion voltages U_{D} between sweeps to test the impact of the magnitude of U_{D} on n_{Int}. Also, some of the U_{D} values are used twice or more times in one series, to also resolve the role of such repetitions on n_{Int}. For $U_{\mathrm{BC}} = 0$ V the series of 11 sweeps contains three different values of U_{D}, randomly varied and repeated. For $U_{\mathrm{BC}} = -0.5$ V the series of 10 sweeps contains a random succession of 10 different U_{D} values.
For both series - which represent different U_{BC} and hence two different initial n_{Int} - we observe that $U_{\mathrm{D}} > U_{\mathrm{BC}}$ tend to shift the 2DEG accumulation point towards more positive U_{TG} ($U_{\mathrm{Acc}}^{\mathrm{Dev}} > 0$). Equally, $U_{\mathrm{D}} < U_{\mathrm{BC}}$ tend to shift the accumulation point towards lower U_{TG} ($U_{\mathrm{Acc}}^{\mathrm{Dev}} < 0$). At the same time, the effective action of the applied U_{D} seems to be statistical. Meaning that applying a certain value of U_{D} may shift the accumulation point, but will not necessarily do so. For both FES A and C, we find the magnitude of $U_{\mathrm{Acc}}^{\mathrm{Dev}}$ as well as the probability for a variation of $U_{\mathrm{Acc}}^{\mathrm{Dev}}$ to correlate with the magnitude of U_{D}. Also, there is a clear trend that the more often the FES is subjected to a given value of U_{D}, the higher the probability to observe a non-zero $U_{\mathrm{Acc}}^{\mathrm{Dev}}$ and even a comparatively larger $U_{\mathrm{Acc}}^{\mathrm{Dev}}$. Finally, the data show that the action of successive U_{D} add up. In Fig. 4.4 a), for both U_{BC}, $U_{\mathrm{Acc}}^{\mathrm{Dev}}$ ends up to reach up to -10 % after the tenth sweep with mostly negative U_{D}.
We used the same constant U_{TG} sweep rate in all experiments, meaning that increasing magnitudes of U_{D} and higher sweep numbers i both imply that the FES spends more time being subjected to voltages $< U_{\mathrm{Acc,\,sweep\,\#\,=\,0}}$. To address the influence of this aspect of duration, we performed the additional measurement series Fig. 4.4 b) on FES A, where we vary the duration for which a constant U_{D} is applied. The cool-down was conducted under $U_{\mathrm{BC}} = -0.5$ V and three values of $U_{\mathrm{D}}(-0.1\,\mathrm{V}, -1.5\,\mathrm{V}, -2.5\,\mathrm{V})$ were tested. For each U_{D}, a series of three sweeps was performed: applying U_{D} during 3 min before the sweep # = 1, 0.2 min before sweep # = 2 and 10 min before sweep # = 3. For the comparatively small

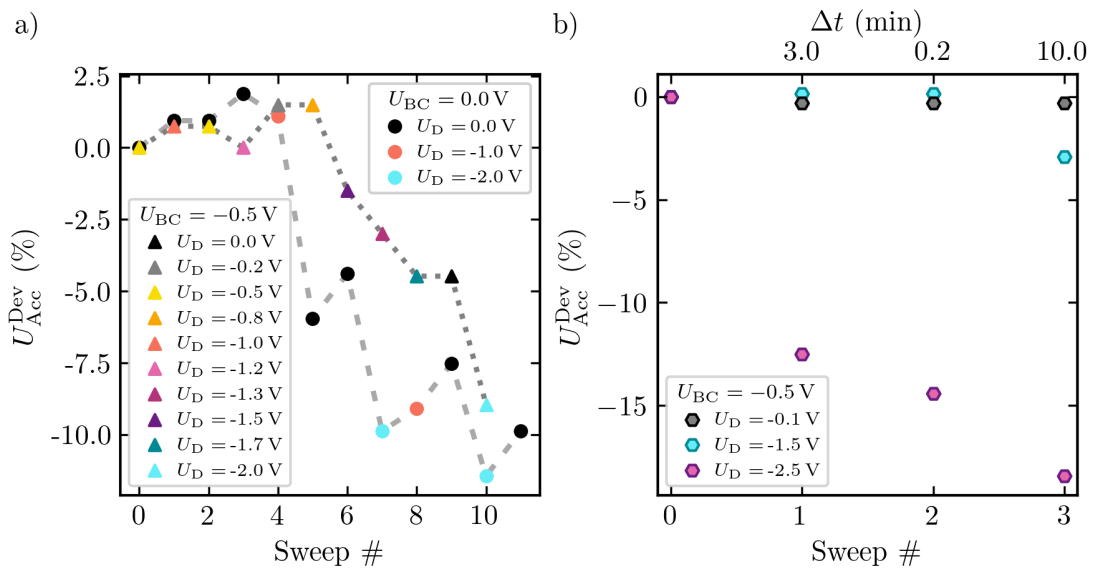

Figure 4.4: Impact of varying depletion voltages U_{D} on the accumulation point at 1.5 K. a) Different accumulation sweeps started from depletion at U_{D} without thermal cycle of the device, representatively shown for FES A. The data are shown for two biased cool-downs. The results for $U_{\mathrm{BC}} = 0\,\mathrm{V}$ are coded with circles, for $U_{\mathrm{BC}} = -0.5\,\mathrm{V}$ with triangles. We show the relative deviation of the accumulation point $U_{\mathrm{Acc}}^{\mathrm{Dev}}$ [see Eq. (4.1)] for each sweep. Each sweep is started from a specific depletion voltage U_{D}, color coded in the figure. The light gray dashed line for $U_{\mathrm{BC}} = 0\,\mathrm{V}$ and the dark gray dotted line for $U_{\mathrm{BC}} = -0.5\,\mathrm{V}$ serve as guide to the eye. b) Relative deviation of the accumulation point $U_{\mathrm{Acc}}^{\mathrm{Dev}}$ for different durations Δt spent at U_{D}, shown for $U_{\mathrm{BC}} = -0.5\,\mathrm{V}$ on FES A. The results are shown for three different values of U_{D}, color coded in the figure.

$U_{\mathrm{D}} = -0.1\,\mathrm{V}$, no observable deviation of the accumulation point is induced, independently of the duration of application of U_{D}. For a stronger $U_{\mathrm{D}} = -1.5\,\mathrm{V}$, we see that only the longest (10 min) and simultaneously last (sweep # = 3) exposure to U_{D} induces a deviation of the 2DEG accumulation point. For the strongest tested $U_{\mathrm{D}} = -2.5\,\mathrm{V}$, 3 min (sweep # = 1) are sufficient to induce a significant deviation $U_{\mathrm{Acc}}^{\mathrm{Dev}}$. The shorter duration of 0.2 min in sweep # = 2 now also has an impact, slightly larger per time than (sweep # = 1). Compared to the series with $U_{\mathrm{D}} = -0.1\,\mathrm{V}$ and $-1.5\,\mathrm{V}$ this observation may indicate that the statistical rate of the electrostatic process underlying $U_{\mathrm{Acc}}^{\mathrm{Dev}}$ is significantly enhanced for all durations at this larger depletion voltage $U_{\mathrm{D}} = -2.5\,\mathrm{V}$. The third sweep, which has a duration of 10 min, further increases $U_{\mathrm{Acc}}^{\mathrm{Dev}}$, but with less impact per time on $U_{\mathrm{Acc}}^{\mathrm{Dev}}$ than the sweeps # = 1 and # = 2, although sweep # = 3 is added to the previous two. We interpret this behavior as an indication for a saturation of the electrostatic effect on n_{Int}, at a given U_{D}.

Summarizing the results of the experiments discussed in Fig. 4.4, we demonstrate that n_{Int} - which is initialized at room temperature by the choice of U_{BC} - may be modified

during experiments at 1.5 K, by applying a depleting voltage $U_{TG} = U_D$. At the same time, varying U_{TG} while the 2DEG is accumulated does not modify n_{Int}. The impact of U_D is strongly statistical. Increasing the duration of U_D, repeating its application and also increasing the U_D-magnitude increases the probability of the process. In our view, all these experimental signatures strongly hint towards a modification of n_{Int} via tunneling of electrons between the trap states and the QW.

4.4 Conclusion on the Biased Cooling Effect

In conclusion, we have demonstrated that the biased cooling of undoped QW heterostructures creates a static electric field which superimposes on any gate action at the device operation temperature of 1.5 K. While the magnitude of the static electric field scales with the biased cooling voltage U_{BC} applied at room temperature, it is insensitive to the TG voltage U_{TG} action at operation temperature. As a result, the accumulation voltage U_{Acc} of the 2DEG is reproducibly tunable with U_{BC}, allowing to set U_{Acc} to be positive as well as negative. The shift of U_{Acc} depends linearly on U_{BC} in a wide range. Also, the capacitive coupling of the FES at device operation temperature is not modified by biased cooling. As a consequence, the whole linear U_{TG}-characteristic of the 2DEG density n_e can be shifted deterministically. Importantly, the main measurables of the U_{TG}-tuned 2DEG remain unchanged compared to $U_{BC} = 0$ V: We did not detect any influence of U_{BC} on the minimal measurable 2DEG density $n_{e,min}$, on the maximal field-effect tunable density $n_{e,max}$, nor on the 2DEG mobility within the whole range from $n_{e,min}$ to $n_{e,max}$ or on the temporal stability of any chosen $n_e(U_{TG})$ within this density range.
As we discuss in an empirical model, all our experimental observations are consistent with a charge $Q = C_{BC} \cdot U_{BC}$ being created at the dielectric/heterostructure interface at room temperature via loading or unloading of charge traps. Importantly, the loading and unloading mechanisms are suppressed at the device operation temperature. In addition, the charge is homogeneously distributed, such that it does neither impact $n_{e,min}$, nor the 2DEG mobility or $n_{e,max}$. Notably, the mechanism is qualitatively identical, although the three investigated FESs differ (see Tab. 3.1). In particular the presence of an (oxidized) Si cap at the dielectric/heterostructure interface does not impact the mechanism. While the trapped charge Q is insensitive to variations of U_{TG} in the accumulated 2DEG at the device operation temperature of 1.5 K, we have shown that Q can be modified by applying a voltage U_D to the depleted QW. Our experiments indicate that the modification of Q occurs via tunneling between the dielectric/heterostructure interface and the QW.
Our model should apply to any undoped semiconductor heterostructure. The ability to shift the operation range of the FES deterministically and reproducibly without affecting the quality features of the 2DEG represents an interesting additional degree of freedom for optimization of gate operation windows. It for example allows to shift "normally on" devices to a "normally off" operation regime [70]. It has also been shown to allow to avoid initializations of 2DEG in a metastable capacitive coupling [70] or leakage regimes in Coulomb blockade devices with integrated charge sensors [83]. Applying the biased

cooling effect does not require to cycle the device at room temperature. It is sufficient to apply U_{BC} above the freeze-out temperature of the heterostructure to induce the loading of Q at the interface.

4.5 Outlook towards Applications in Quantum Circuits

FES-based quantum circuits with multiple gates, such as current overlapping gate layout designs for scalable fault-tolerant and long distance spin qubit operations, require reproducible operation voltages for each gate and are sensitive to large voltage differences applied between neighboring gates during device tuning. The biased cooling effect applied to individual gates in such devices could be a new and advantageous degree of freedom for tuning.
To gain insights into the impact of biased cooling on individual gates in quantum circuit devices we simulated the electric potential V and electric field distribution E with and without biased cooling. The simulated FES consists of a 10 nm thick QW followed by a 25 nm thick SiGe barrier and the 25 nm thick dielectric chosen as SiOx. On top of this stack two individual gates are placed surrounded by air. The gates were chosen to have dimensions typical for state-of-the-art qubit applications. Their width is 100 nm, height 30 nm and length reaching 300 nm in the simulated volume. The electrostatic simulation solves Maxwells equation using the finite element method with respect to the different material properties implemented via their different permittivities. In order to implement the change of trapped charges Q by biased cooling we incorporate, in accordance to our empirical model, a interface charge density $\Delta\rho_{BC}$ at the SiGe/SiOx interface. The interface charge density is located below the gate spanning the same dimensions as the gate. The dielectric/heterostructure interface was chosen to be free of charge in the case of no biased cooling $U_{BC} = 0\,\mathrm{V}$, which is a valid simplification as the main ingredient of biased cooling is the change of the trapped charges Q and the value of trapped states is strongly heterostructure dependent. The value of $\Delta\rho_{BC}$ was chosen to resemble the same electric potential V and z-component of the electric field E_z, evaluated in the middle of the QW and centered under the gates, for biased cooling voltages to perfectly shift the TG influence by the value of U_{BC} i.e. acting like a perfect capacitor before and after freeze-out. Fig. 4.5 a) shows the simulated electric potential and electric field in a cut plane through the FES comparing the influence of gate 1 cooled down conventional without biased cooling - i.e. with $\Delta\rho_{BC}$ being zero - and a voltage applied at the gate of $U_{TG} = 1\,\mathrm{V}$ to gate 2 with $U_{TG} = 0.5\,\mathrm{V}$ and a $\Delta\rho_{BC} = 4.4 \times 10^{11}\,1/\mathrm{cm}^2$ (shown in red) being equivalent to negative biased cooling with $U_{BC} = -0.5\,\mathrm{V}$. The normalized electric field distribution is shown as white arrows at the interfaces between the different layers indicated on the right. Comparing the two gates, it can be seen that biased cooling allows to drastically alter the potential as well as the electric field distribution throughout the FES, while keeping it the same within the QW plane beneath the gates. This effect

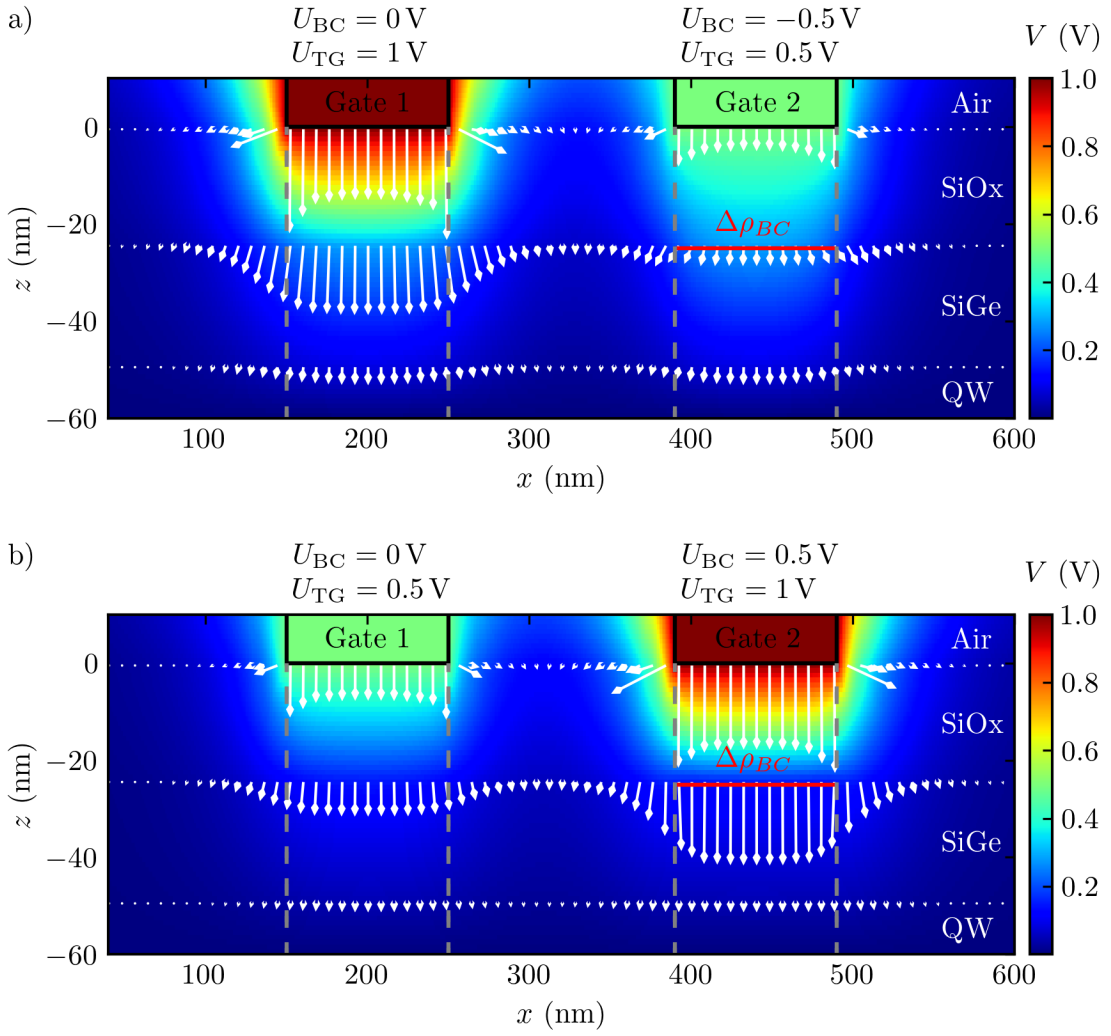

Figure 4.5: Comparison of the simulated potential and electric field distribution for gates with and without biased cooling. The electric potential V and the electric field distribution E (normalized white arrows) are shown for a typical FES based quantum circuit application. The gray lines are guides to the eyes for the gate width through the FES stack. a) Negative biased cooling: Gate 1 shows the reference case of a gate cooled down without biased cooling $U_{BC} = 0\,V$ and with a voltage of $U_{TG} = 1\,V$ applied. Gate 2 is set to $U_{TG} = 0.5\,V$ and possesses a interface charge density $\Delta\rho_{BC} = 4.4 \times 10^{11}\,1/cm^2$, depicted in red, at the SiOx/SiGe interface, which is induced by cooling down with $U_{BC} = -0.5\,V$. b) Positive biased cooling: Gate 1 shows the reference case of a gate cooled down without biased cooling $U_{BC} = 0\,V$ and with a voltage of $U_{TG} = 0.5\,V$ applied. Gate 2 is set to $U_{TG} = 1\,V$ and possesses a interface charge density $\Delta\rho_{BC} = -4.4 \times 10^{11}\,1/cm^2$, depicted in red, at the SiOx/SiGe interface, which is induced by cooling down with $U_{BC} = 0.5\,V$.

can also be reproduced for simulating positive biased cooling. Fig. 4.5 b) illustrates the scenario of gate 1 being cooled down conventional without biased cooling and a voltage applied at the gate of $U_{\mathrm{TG}} = 0.5\,\mathrm{V}$ in contrast to gate 2 with $U_{\mathrm{TG}} = 0.5\,\mathrm{V}$ applied and a $\Delta\rho_{\mathrm{BC}} = -4.4 \times 10^{11}\,1/\mathrm{cm}^2$ being equivalent to cooling with $U_{\mathrm{BC}} = 0.5\,\mathrm{V}$.
The biased cooling effect thus allows us to engineer the potential landscape as well as the electric field distribution, while keeping them unaltered within the QW and thus the 2DEG. This new degree of freedom could be advantageous in different aspects. Especially, as utilizing the biased cooling effect only comes with a limited overhead of thermally cycling above the freeze-out temperature of the heterostructure. A beneficial use case of biased cooling can be homogenizing the pinch-off voltages across the device. This could compensate for unwanted variations between the gates in the fabrication as well as the different distance between the 2DEG an the gates in overlapping gate designs with gates stacked in different layers. Furthermore, as biased cooling allows to shift the operation window of each individual gate the distinct functionalities of different gates can be addressed by biased cooling in the way that the typically very different voltage values being necessary for the different functionalities can be homogenized across the sample. The advantages of homogenizing the voltages in a FES-based quantum circuit are threefold: First, it could effectively reduce the risk of leakage in the device. Second, it could reduces the risk of local tunneling towards the dielectric/heterostructure interface, which is known to introduce detrimental effects as on the operation and charge noise of the device [65, 66]. Third, it could help the implementation of virtual gates during device tuning.
A further advantage is that the interface charge density induced by biased cooling may reduce spatial smearing of the electric potential within the QW plane. Indeed, in Fig. 4.6 a) and b) we see that negative biased cooling helps to reduce spatial smearing of V as well as E_{z} within the QW plane. At the same time the x- and y-component of the electric field are reduced in their spatial smearing (see App. A.1). This sharper definition of the potential within the QW should ease the definition and tunability of few-electron QDs. For positive biased cooling voltages the opposite effect of an increased spatial smearing of V and E_{z} within the QW plane can be observed in the simulations, which can be seen in Fig. 4.6 c) and d). The influence on the x- and y-component of the electric field, which also experience increased smearing, is shown in App. A.1. However, in terms of charge noise positive biased cooling could be beneficial as the dielectric/heterostructure interface is known to have a crucial impact. First experiments [75, 78] indicate sweet spots in the charge noise utilizing positive biased cooling. Our model suggests that robustly trapping charges at the interface helps to prevent charges hopping between different unoccupied states making this preliminary observed effect evident.
It will be exciting to see the applications of biased cooling on quantum circuits in the near future and see how exploiting this effect not only helps to shift the operation window of individual gates and engineering the trapped charges at the dielectric/heterostructure interface with various advantages, but also which further use cases will arise.

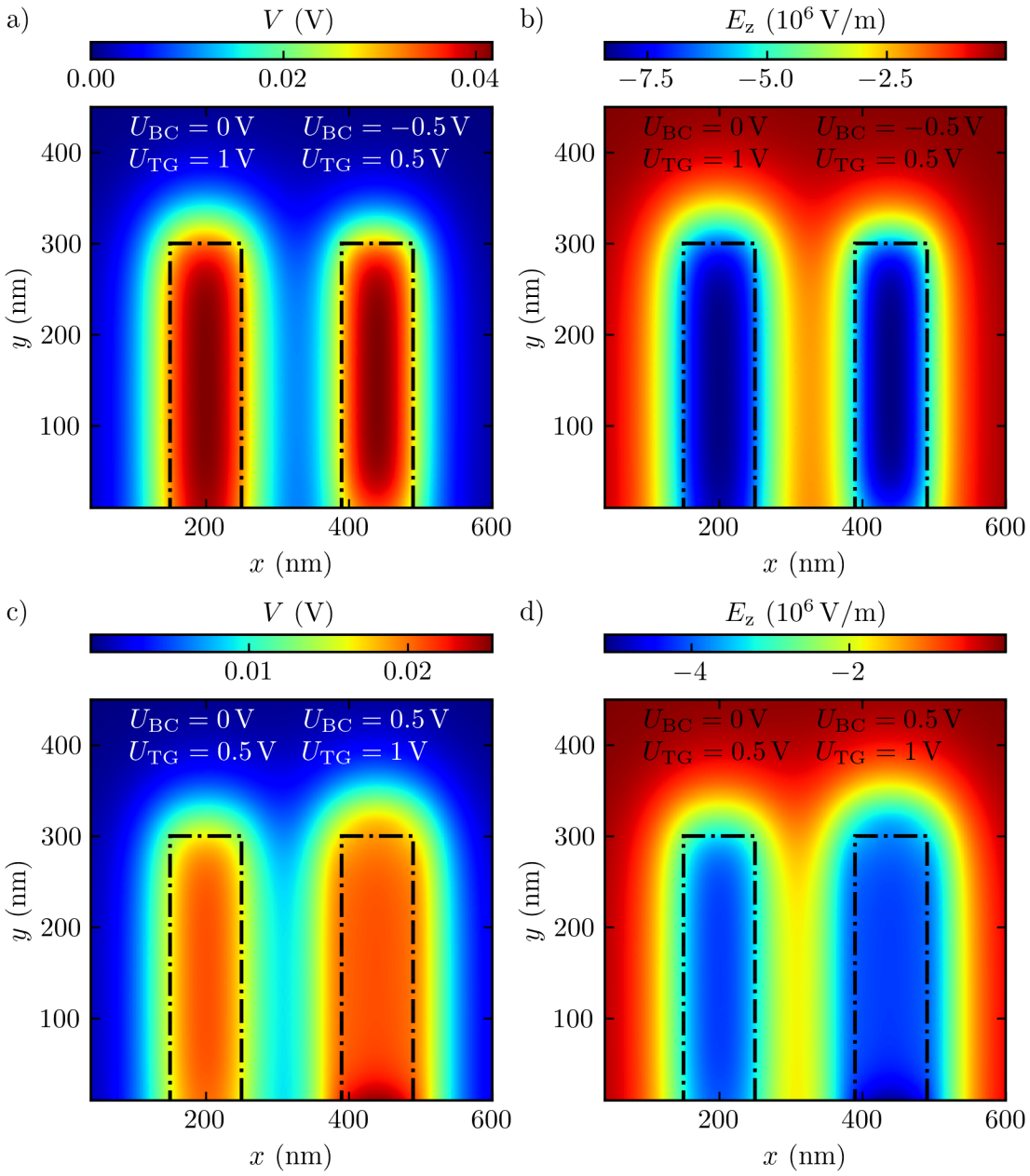

Figure 4.6: Comparison of the simulated electric potential distribution V and z-component of the electric field E_z within the QW plane below two gates with and without biased cooling. The black dash-dotted lines illustrate the gate positions on top of the FES. a), b) Negative biased cooling: Gate 1 (left) shows the reference case of $U_{BC} = 0\,\mathrm{V}$ and a voltage of $U_{\mathrm{TG}} = 1\,\mathrm{V}$ applied. Gate 2 (right) is set to $U_{TG} = 0.5\,\mathrm{V}$ and possesses a $\Delta\rho_{\mathrm{BC}}$ at the SiOx/SiGe interface equivalent to $U_{\mathrm{BC}} = -0.5\,\mathrm{V}$. The corresponding electric potential distribution V and z-component of the electric field are shown in panel a) and b), respectively. c), d) Positive biased cooling: Gate 1 shows the reference case of $U_{BC} = 0\,\mathrm{V}$ and a voltage of $U_{\mathrm{TG}} = 0.5\,\mathrm{V}$ applied. Gate 2 is set to $U_{TG} = 1\,\mathrm{V}$ and possesses a $\Delta\rho_{\mathrm{BC}}$ at the SiOx/SiGe interface equivalent to $U_{\mathrm{BC}} = 0.5\,\mathrm{V}$. The corresponding electric potential distribution V and z-component of the electric field are shown in panel c) and d), respectively.

5

Asymmetric Sensing Dot: New Charge Sensor Design with High Output Voltage

Fast and high-fidelity qubit readout is an essential building block of qubit architectures. With scalability gaining importance, additional demands emerge also for gate-defined quantum dots, requiring efficient use of the limited space and cooling power within cryostats.

For readout, the spin information of the spin qubits can be translated into charge information – a process known as spin-to-charge conversion. This can be achieved either through Pauli spin blockade [84, 85] or via energy-selective tunneling to a reservoir, referred to as Elzerman readout [86]. The resulting charge information can be tracked using proximal charge sensors, either a quantum point contact (QPC) [87, 88] or a QD, often referred to as a single-electron transistor (SET) [89, 90] in this context, capacitively coupled to the measured spin qubit. Due to their higher sensitivity, SETs have increasingly become the preferred choice. The conductivity change in the QPC or SET can be measured either through a baseband approach [16, 32], typically by tracking the current, or via radio frequency (RF) readout [90, 91] by incorporating a resonator to the proximal charge sensor. More recently, dispersive gate sensing techniques [92, 93] have also been used, avoiding the need for a proximal charge sensor by utilizing the RF response of a resonator directly connected to a gate of the qubit quantum dot. The usage of RF and dispersive readout enables high bandwidth, but these approaches require significant space and involve a complex readout periphery due the use of resonators, posing challenges for scalability. While it cannot yet match RF and dispersive readout in bandwidth, baseband readout is a strong contender for scalable architectures given its significantly smaller size and reduced complexity.

A well-established and commonly used technique for baseband readout is a voltage-biased sensor dot (see Sec. 2.5), i.e., SET, with a current amplification stage at room temperature. The main limitations of this approach are the limited output signal and bandwidth constraints caused by the sensor dot's resistance in combination with the capacitance of the cryostat wiring to room temperature. An alternative approach is to operate the sensor

dot with a current bias instead of a voltage bias and use voltage as the readout signal. Since voltage amplifiers can be built more compact and energy-efficient than current amplifiers in an integrated circuit, this enables amplification directly within the cryostat, closer to the sensor dot. Shorter signal lines and amplification entirely at cryogenic temperatures reduce noise and improve bandwidth, enhancing readout fidelity and reducing readout time. A detailed technical discussion, including a comparison of different transistor technologies for amplification, can be found in the doctoral thesis of E. Kammerloher [77]. In addition, increasing the output signal presents another potential improvement. It could allow for even lower total power consumption, enabling more simultaneous qubit readouts, or enhance readout fidelity in the baseband readout approach, as the power requirement is primarily determined by amplifier gain and sensitivity.
Building on the advantages of a current-biased sensor with a voltage output, we introduce a new proximal charge sensor design, the asymmetric sensing dot (ASD), which aims to achieve a high output signal and overcome the current limitations of conventional sensor dots in this regard. This new sensor concept leverages a significantly reduced capacitive coupling to the drain reservoir, enabling a substantial boost in output signal. In this chapter, we present the ASD concept along with a simulation-guided device design approach that effectively translates this concept into a practical device layout. We further provide Coulomb diamond measurements to quantify the reduction in capacitive coupling across two material platforms: undoped Si/SiGe and doped GaAs/(Al,Ga)As. Additionally, we demonstrate the high output signal of the ASD in charge sensing measurements on a nearby qubit-like DQD.
The ASD investigations on Si/SiGe, presented in this chapter, were performed at a temperature of about 400 mK using our ^{3}He cryostat in conjunction with the previously described qubit measurement technique (see Ch. 2.8). The complementary ASD measurements on GaAs/(Al,Ga)As were conducted at a temperature of about 50 mK. Details on the corresponding experimental setup are presented in [77]. This project took place in close collaboration with our partners at the *Rheinisch-Westfälische Technische Hochschule Aachen*. The main findings discussed in the subsequent chapter and further details on the simulation-guided device design are also published in the two articles [83, 94].

5.1 New Asymmetric Sensor Design Concept and Simulation-Guided Device Design

A conventional sensor dot (CSD) used as proximal charge sensor consists, as previously discussed in Sec. 2.5, of a dot in the multi-electron regime which is capacitively coupled to a metallic gate G and capacitively as well as tunnel coupled to two reservoirs. To facilitate signal amplification, the ASD concept, unlike the more commonly used voltage-biased sensor dot that produces a current output signal (see Sec. 2.5), is based on current-biased readout, yielding a voltage as the output signal. Fig. 5.1 illustrates the corresponding wiring concept. In order to detect an electrostatic change in the environment inducing

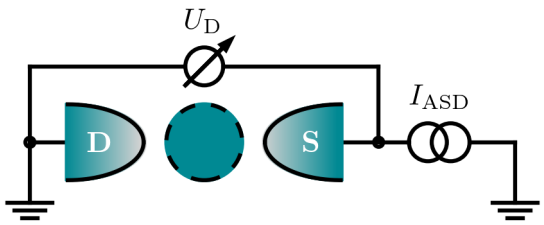

Figure 5.1: Schematic of the ASD wiring concept. The output voltage is detected, which is necessary to maintain a constant current flow between the source and drain reservoir through the dot (blue circle). The reservoirs are depicted as semi-ellipsis, labeled S for the source and D for the drain.

a conductivity change in the sensor, the source-drain voltage necessary to maintain a constant current flow is measured.
CSDs, illustrated in Fig. 5.2 a) in a top-view of the spatial potential, are usually characterized by a comparable distance and capacitive coupling to both the source and drain reservoirs $C_{D,CSD} \approx C_S$. The corresponding potential landscape, depicted in Fig. 5.2 b), consists as key element of the ladder of the dots Coulomb levels, which can be shifted by ΔU_G, bordered by sharp tunnel barriers to the source and drain reservoirs with their electrochemical potentials defining the bias window (see Sec. 2.4). We choose to fix the source potential to the measurement ground. This is an arbitrary choice that simplifies defining the bias window exclusively through U_D, which is the relevant parameter for the ASD concept. The current through the CSD in dependence of ΔU_D and U_G is characterized by the well known symmetric Coulomb diamonds (see Fig. 5.2 c)), as previously discussed in Sec. 2.4. In order to estimate the corresponding output voltage $\Delta U_{D,CSD}$ of the CSD an electrostatic change in its surrounding, e.g., an electron jump in a close by DQD, can be envisioned as an equivalent electrostatic change in U_G. As the current through the CSD is fixed, a ΔU_G will lead to a corresponding $\Delta U_{D,CSD}$ along the Coulomb diamond edge. Thus the slope of the chosen diamond edge is the defining quantity for the magnitude of $\Delta U_{D,CSD}$. According to the constant interaction model, the slopes of the Coulomb diamonds are directly linked to the dots capacitive coupling to its environment. The positive slope and negative slope are defined by $C_G/(C_\Sigma - C_D)$ and $-C_G/C_D$, respectively, where C_Σ represents the dot's total capacitance to ground [57]. From this, we can conclude that a decrease in C_D is directly related to an increase in the negative slope of the Coulomb diamonds, and consequently, an increase in the output voltage.
This leads to the fundamental idea of the ASD concept to increase the output signal: an asymmetrically capacitively coupled dot to its source and drain reservoirs, with a significantly reduced capacitive coupling to the drain reservoir while maintaining the capacitive coupling to the source reservoir ($C_{D,ASD} \ll C_S$). An increase in the distance between the dot and the drain reservoir, as illustrated in Fig. 5.2 d), allows to effectively decrease their capacitive coupling. However, simply increasing the width of the barrier between the dot and the drain reservoir would also render the tunnel barrier opaque,

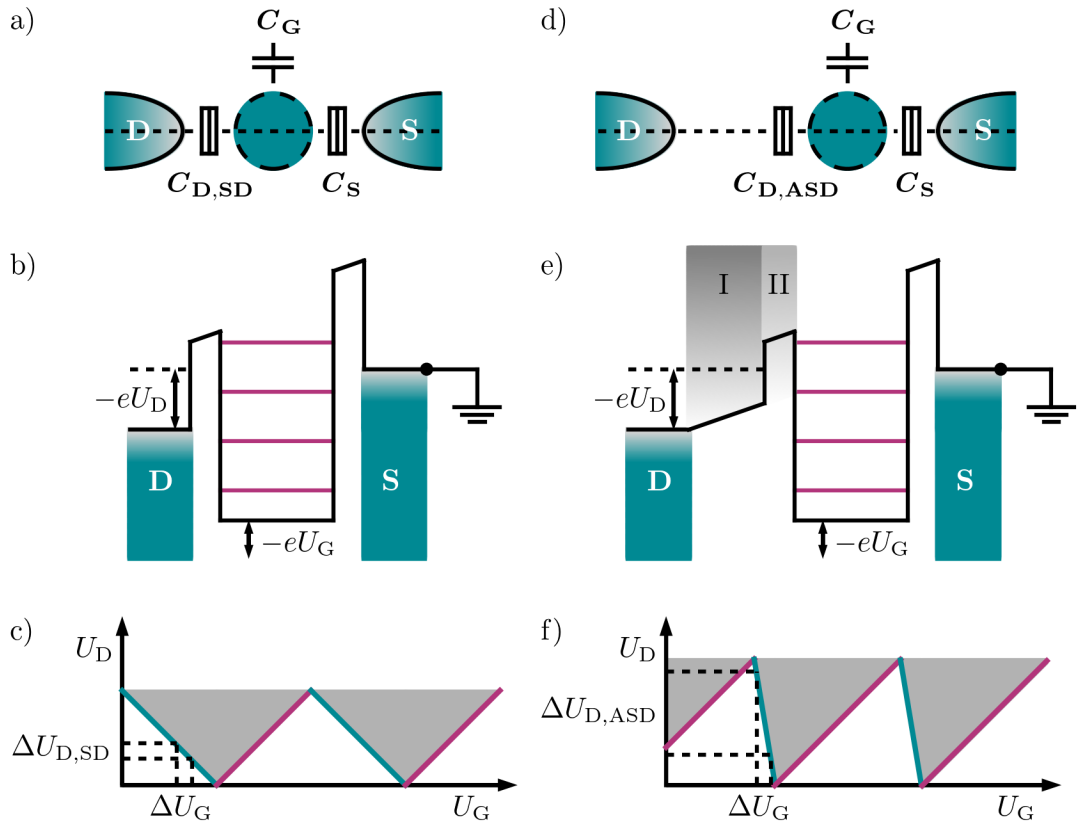

Figure 5.2: ASD concept in comparison to a CSD. a), d) Schematics of the spatial potential distribution in top view, showing a CSD in panel a) and the ASD in panel d). The reservoirs are depicted as semi-ellipses, labeled S for the source and D for the drain. The dot, illustrated as a blue circle, is tunnel-coupled and capacitively coupled to both the source and drain reservoirs and is additionally capacitively coupled to a gate, abbreviated as G. The ASD concept differs from the sensor dot by an increased spatial distance between the dot and its drain reservoir. b), e) Schematics of the potential landscape with an applied bias of U_D between source S and drain D for a CSD in panel c) and the ASD in panel d). In the CSD, the drain is separated from the dot by a sharp tunneling barrier. In contrast, the ASD features a compound barrier structure, where region I, termed the slide, is followed by a sharp tunnel barrier in region II that controls tunneling. In both cases, the ladder of the dot's Coulomb levels (pink lines) can be shifted by the gate voltage U_G. c), f) Schematic Coulomb diamonds for both sensor concepts. No current flow occurs in the white regions due to Coulomb blockade. Single-electron transport current flows in the light gray regions. Blue and pink lines mark the edges of the diamond-shaped Coulomb blockade regions. An equivalent shift ΔU_G on the U_G-axis results in an enhanced shift $\Delta U_{D,ASD}$ for the ASD compared to $\Delta U_{D,CSD}$, in current bias mode.

causing the sensor to become non-functional. The challenge is to implement a reduced $C_{\mathrm{D,ASD}}$ while maintaining the dot confinement and a sufficient tunnel coupling to the drain reservoir. To achieve this, we proposed the concept of a compound drain barrier, which is subdivided in two destined regions, I and II, as depicted in Fig. 5.2 e). Barrier region I, termed *slide*, increases the distance to the drain reservoir from the dot with a gradually decreasing potential, while barrier region II maintains the sharp tunnel barrier and confinement. Exploiting this new barrier design, the highly reduced C_{D} ($C_{\mathrm{D,ASD}} \ll C_{\mathrm{D,SD}}$) leads to Coulomb diamonds appearing tilted due to its significantly steeper negative slope (see Fig. 5.2 f)). For the same electrostatic change in the environment of the ASD, equivalent to ΔU_{G}, this results in the desired significantly increased output voltage swing of the ASD compared to the CSD ($\Delta U_{\mathrm{D,ASD}} \gg \Delta U_{\mathrm{D,CSD}}$), which is only limited by the charging energy of the corresponding Coulomb diamond.
This appealing concept comes with the downside of a complex potential landscape, which could be extremely challenging to implement in an actual device design. Typically, the design of new device layouts relies on adapting previous successful devices and the evaluation through transport measurements. This approach has a relatively slow feedback cycle and is often prone to requiring numerous iterations for optimization. For the development of the ASD device layout we made use of a simulation-based device design approach, developed by our partners at the *Rheinisch-Westfälische Technische Hochschule Aachen*, capable of electrostatically modeling a target potential, taking into account the gate structure, heterostructures, doping, reservoirs, and applied bias. It allows to predict the electrostatic potential landscape, optimize the gate layout and make it robust to unavoidable fabrication imperfections without the need for resource-costly fabrication iterations. More details on the simulation-guided device design are published in [94]. Utilizing the electrostatic simulations M. Neul and I. Seidler at the *Rheinisch-Westfälische Technische Hochschule Aachen* developed a ASD qubit device design (ASD SiGe) custom-tailoring the drain barrier potential region featuring the desired slow and monotonically declining transition to the drain reservoir, effectively creating a micron-scale electron slide with sharp tunnel barriers defining the dot, depicted in Fig. 5.3 a). The corresponding device design, illustrated in Fig. 5.3 b) with its potential landscape, is tailored for an undoped Si/SiGe heterostructure with a global TG and incorporates the desired potential landscape along the predicted electron path showcased as dashed line as well as a dedicated area to tune a nearby DQD (white dashed circles).

5.2 Experimental Demonstration in undoped Si/SiGe

Moving forward, we aim to experimentally verify the reduction in capacitive coupling to the drain reservoir proposed by the ASD concept. The simulation-guided ASD qubit device design (ASD SiGe) was fabricated on an undoped Si/SiGe heterostructure to test device functionality and assess the achievable reduction in coupling to the drain

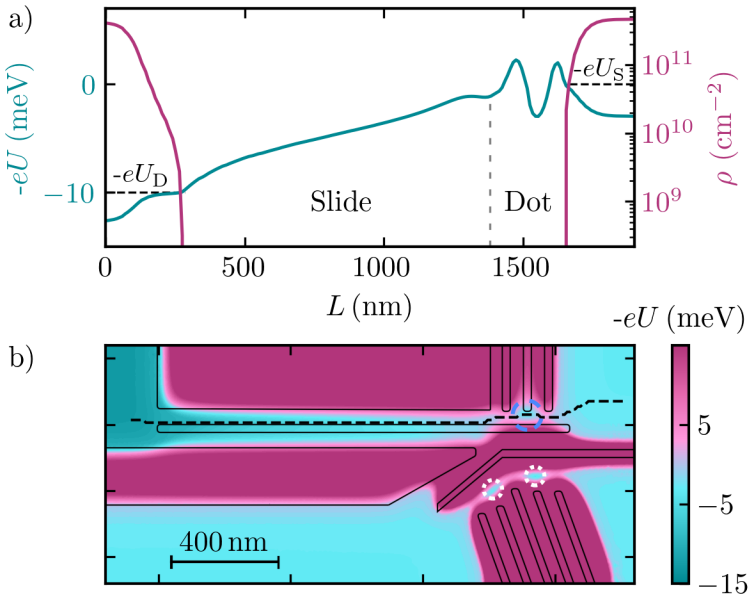

Figure 5.3: ASD concept realization by a simulated device design. a) Simulated ASD potential landscape with an applied bias of U_D between source S and drain D. Potential (blue) and charge-carrier density (pink) along the path length L. b) Simulated potential landscape of the ASD device design for an undoped Si/SiGe heterostructure with a global top gate (not shown). The gate design is outlined in black. The blue dashed line illustrates the position of the sensor dot and the black dashed line the current path, shown in panel a), through the sensor and slide region. The white dashed line depicts the position of a DQD dots, which can be formed adjacent to the sensor in ASD tuning. The device design and simulations were conducted by M. Neul and I. Seidler at the *Rheinisch-Westfälische Technische Hochschule Aachen*.

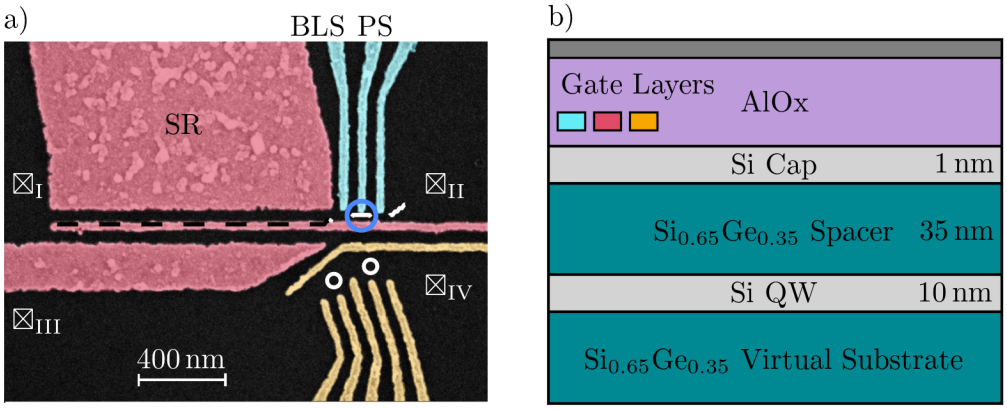

Figure 5.4: ASD device layout and layer stack in Si/SiGe. a) False-colored scanning electron image of a device fabricated in the same manner as the ASD SiGe device, illustrating the gate layout. A global TG isolated by AlOx is not shown. The blue circle indicates the position of the sensor dot, while the white circles show the dot positions of a potential DQD. The drain and source reservoirs are labeled $\boxtimes_{\mathrm{I}}$ and $\boxtimes_{\mathrm{II}}$ for the sensor current path and $\boxtimes_{\mathrm{III}}$ and $\boxtimes_{\mathrm{IV}}$ for the DQD current path. The dashed line represents a possible electron trajectory through the sensor. The scanning electron image was taken by our partners at the *Rheinisch-Westfälische Technische Hochschule Aachen*. b) Schematic cross section of the layer stack. The gate layer colors correspond to the colors in a) and their vertical position illustrates the gate layer plane they were fabricated in. The grey colored gate corresponds to the global TG not shown in the scanning electron image in panel a). The metal gates in the first gate layer are separated from the heterostructure by 10 nm of AlOx, and the second gate layer is separated from the first by 50 nm AlOx.

reservoir. In order to do so, we will present a series of Coulomb diamond measurements, transitioning the sensor from a CSD to an ASD configuration, as proof-of-principle for the coupling reduction and discuss details of the tilted appearing ASD Coulomb diamonds.

Fig. 5.4 a) depicts a false-colored SEM image of the ASD SiGe device layout. The sensor dot (position illustrated by the blue circle) is formed by the light blue colored gates, from which gate PS serves as the plunger gate for the sensor dot levels. The two surrounding gates control the sharp tunnel barriers. The sensor dot's source reservoir $\boxtimes_{\mathrm{II}}$ is in a common distance, while its drain reservoir $\boxtimes_{\mathrm{I}}$ can be tuned in its distance to the dot by the pink colored gates. Those allow to form the drain reservoir in a similar distance to the dot as the source reservoir (conventional symmetrical tuning) or push it further away by creating a slide potential (asymmetric tuning). The dashed line illustrates a possible electron path connecting the sensor's source and drain in the asymmetric tuning. The orange gates can be used to define and manipulate the nearby DQD (dot positions illustrated as white circles) with its two reservoirs $\boxtimes_{\mathrm{III}}$ and $\boxtimes_{\mathrm{IV}}$. An additional global TG is fabricated in a second gate layer on top in order to accumulate the undoped

heterostructure. A schematic cross section of the ASD SiGe device with its gate layer stack and heterostructure is illustrated in Fig. 5.4 b). The global TG is separated from the first gate layer by a 50 nm thick layer of AlOx, while the first gate layer is separated from the heterostructure by 10 nm. The gate layout was fabricated at the *Rheinisch-Westfälische Technische Hochschule Aachen* on a Si/SiGe heterostructure MBE-grown by our group. The functional heterostructure consists of a 10 nm natural Si QW on a virtual substrate of the composition $Si_{0.65}Ge_{0.35}$, separated from the interface by a 35 nm thick spacer of the same composition and a 1 nm thick oxidized Si cap. More details on the device fabrication and heterostructure growth can be extracted from [83].
As a proof-of-principle measurement we initially characterize the ASD SiGe device under voltage bias by conducting a Coulomb diamond measurement series intended to proof the achievable reduction in capacitive coupling to the drain reservoir. These measurements are performed by varying the drain potential U_D at the reservoir ⊠$_I$ in dependence of the plunger gate PS voltage, while keeping the reservoir ⊠$_{II}$ fixed at $U_S = 0\,V$. Initially, the device is tuned in CSD configuration with symmetrically positioned reservoirs relative to the dot. To achieve this, the voltage on the slide gate SR is increased to a value $U_{SR} = 0.34\,V$ high enough to accumulate electrons beneath it, thereby forming a reservoir close to the dot. The gate BLS ($U_{BLS} = 0.2\,V$) is used to define the tunneling barrier. In this CSD configuration the ASD SiGe device shows the typical symmetric Coulomb diamonds (see Sec. 2.4), depicted in Fig. 5.5 a). To transition from a CSD configuration to an intermediate sensor dot (ISD) configuration and finally to an ASD configuration, the slide is activated by reducing the voltage on gate SR, which pushes the drain reservoir further away from the sensor dot. Simultaneously, the voltage on barrier gate BLS is increased to retain a similar tunneling rate for transport through the sensor. All other voltages (listed in Tab. A.1 in App. A.2) were kept the same during the Coulomb diamond series. The Coulomb diamonds in the ISD configuration with a $U_{SR} = 0.24\,V$ and $U_{BLS} = 0.29\,V$ are depicted in Fig. 5.5 b) and in the ASD configuration with a $U_{SR} = 0.215\,V$ and $U_{BLS} = 0.4\,V$ in Fig. 5.5 c). Comparing the CSD to the ISD and finally the ASD configuration it clearly shows that the negative edge of the Coulomb diamonds becomes progressively steeper and the diamonds appear more tilted. For all three diamonds, we determine the negative Coulomb diamond slopes, depicted as white lines, by fitting the $I = 50\,pA$ contour, which represents the best compromise between low current operation of the device and a sufficient signal-to-noise ratio. To improve the accuracy of the extracted contours on the diamond edges, we additionally utilized a modified version of Akima's algorithm (Makima) [95, 96] to increase the data point resolution along the U_{PS}-axis. Evaluating the largest diamond edge for each configuration we get slopes of $g_{CSD} = -0.68\,V/V$ for the CSD configuration, $g_{ISD} = -3.2\,V/V$ for the ISD configuration and $g_{ASD} = -8.0\,V/V$ for the ASD configuration. The reduction of g_{ASD} in comparison to g_{CSD} indicates the desired reduction of C_D by a factor of $C_{D,CSD}/C_{D,ASD} \approx 12$, which should be directly proportional to the increase in the achievable output voltage. In addition to the desired increasing tilt observed during the Coulomb diamond series, the positive diamond edges are noted to become progressively less sharply defined. Moreover, in the ASD configuration, a bias window ($0 < U_D < U_T \approx 1\,mV$), illustrated by white dashed

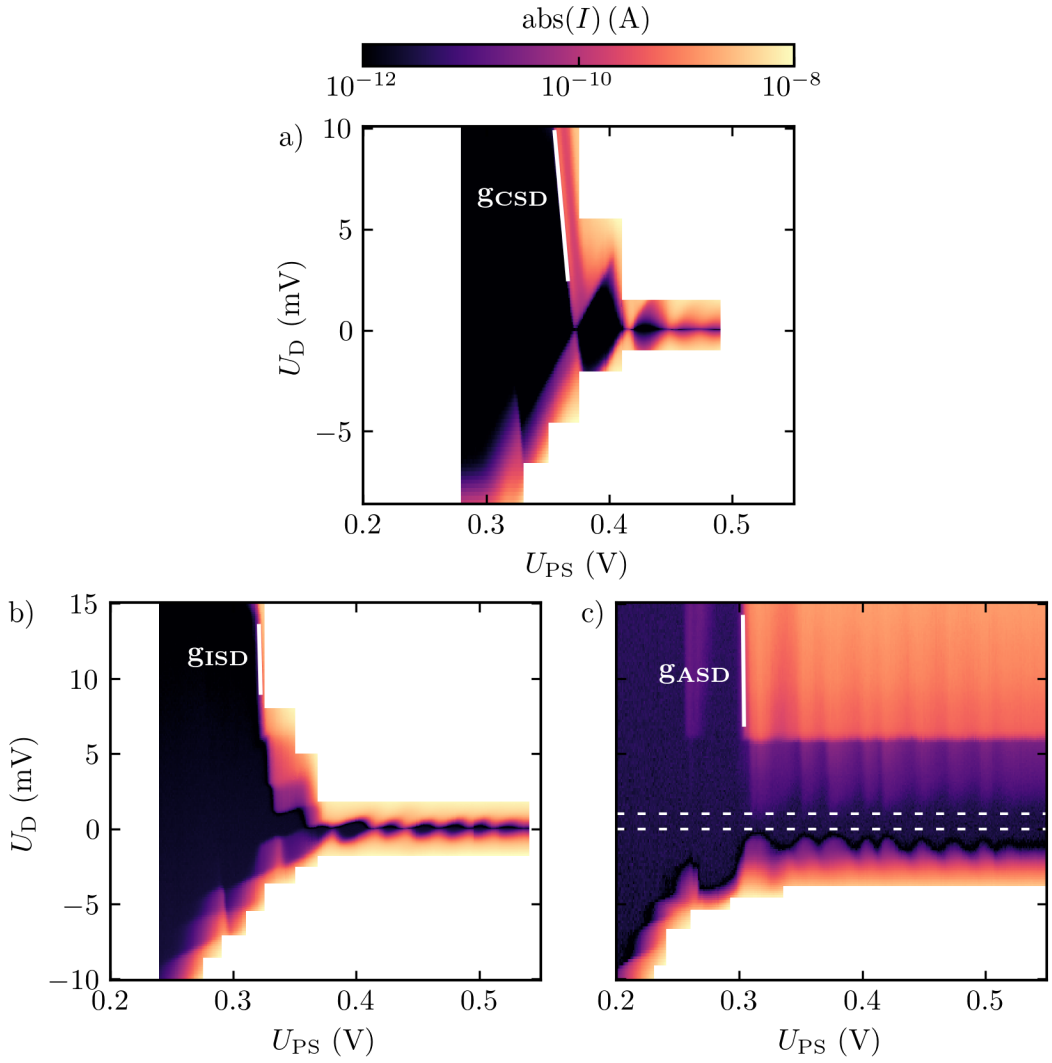

Figure 5.5: Coulomb diamond measurement series of the ASD SiGe device tuning the sensor dot from a symmetric to an asymmetric configuration. To do so the gate potential of SR is step-wise decreased and simultaneously the gate potential of BLS is adjusted to maintain the same tunnel rate for transport through the sensor dot. All other voltages applied at the device were kept the same. The measurements are performed by varying the drain potential U_D at the reservoir ⊠$_I$ while keeping the reservoir ⊠$_{II}$ at $U_S = 0\,V$. All three measurements share the same colorbar and were performed at a temperature of $T = 400\,mK$. The white lines indicate the negative slopes of the corresponding Coulomb diamonds linearly fitting the $I = 50\,pA$ contour. a) Symmetrically tuned sensor dot with gate voltages $U_{SR} = 0.34\,V$ and $U_{BLS} = 0.2\,V$. The negative slope evaluates to be $g_{CSD} = -0.68\,V/V$. b) Intermediately tuned sensor dot with gate voltages $U_{SR} = 0.24\,V$ and $U_{BLS} = 0.29\,V$. The negative slope evaluates to be $g_{ISD} = -3.2\,V/V$. c) Asymmetrically tuned sensor dot with gate voltages $U_{SR} = 0.215\,V$ and $U_{BLS} = 0.4\,V$. The negative slope evaluates to be $g_{ASD} = -8.0\,V/V$. The white dashed lines illustrate a U_D region without current flow arising in the asymmetrically tuned Coulomb diamonds.

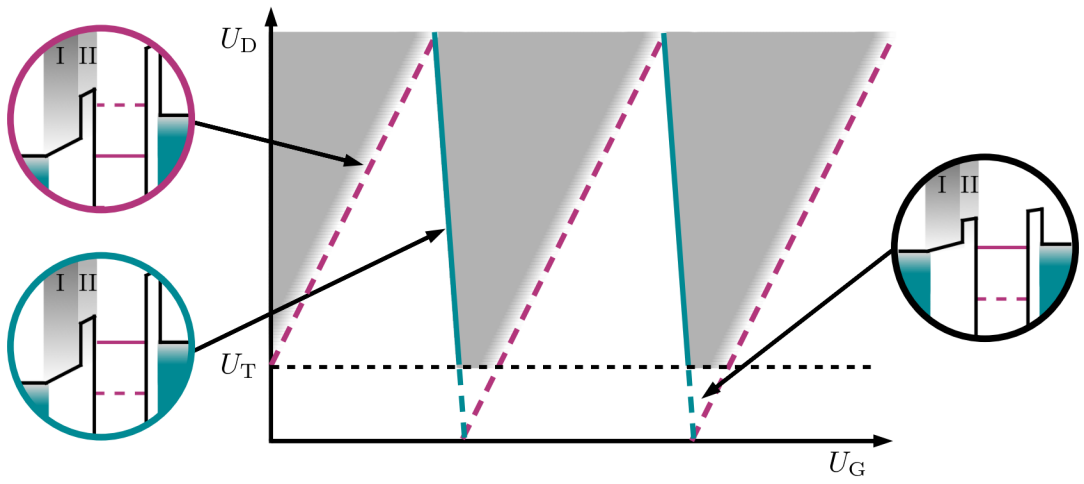

Figure 5.6: Characteristic features of an ASD Coulomb diamond measurement. Schematic of Coulomb diamonds expected for the ASD. Single electron current flows in the light gray regions is separated by blue solid lines (diamond edges with negative slope) and pink dashed lines (diamond edges with positive slope) from Coulomb blockade regions in white. The gradual fading of color toward the diamond edges with positive slopes illustrates a diminishing current flow. The white current-free region is extended by the threshold voltage U_T (black dashed line). Three insets in pink, blue and black frames depict details of the ASD potential landscape (compare Fig. 5.2 e)) at the diamond edges with positive slope, diamond edges with negative slope and the current-free bias window in the region of small U_D, respectively. Within the inserts the Coulomb blockade energy level depicted as solid line contributes to the transport, whereas the one depicted with a dashed line lies without the bias window and thus does not contribute to transport.

lines, with blocked transport, becomes apparent. These observations can be attributed to the characteristics of the compound drain barrier in the ASD configuration.
Fig. 5.6 illustrates the correlation between the potential landscape and Coulomb diamonds in the ASD configuration. We focus on $U_D > 0$, since the ASD is intended to operate within this bias regime. The potential landscape corresponding to the negative Coulomb diamond slope (blue), i.e., the desired working point for readout, is depicted in the blue inset and illustrates that at this diamond edge the dot's energy level aligns with the electrochemical potential of the source reservoir. Tunneling through the thin barrier II becomes possible at sufficiently high bias, allowing the electron to pass through region I and relax into the drain reservoir. At the opposing diamond edge, i.e., the positive slope (pink line), the energy level in the dot approaches the electrochemical potential of the drain, as illustrated in the pink inset. Tunneling through barrier I, in addition to barrier II, becomes exponentially difficult. Hence, the current flow progressively decreases towards the diamond edge. The black inset depicts the low bias configurations, below the dashed black line. The inset shows a state where the dot's energy level is within the bias window

and can potentially contribute to the current flow. However, tunneling is nearly impossible due to the combined barrier thickness of regions I and II. The compound drain barrier becomes transparent only above a threshold U_{T}, when a sufficiently large gradient is formed in region I by the bias voltage.
The Coulomb diamond measurement series demonstrates that the ASD SiGe device can be tuned from a CSD to an ASD configuration by adjusting the voltage on only two gates. Moreover, the measurements validate the ASD concepts goal of significantly reducing the capacitive coupling to the drain reservoir, achieving a reduction factor of approximately $C_{\mathrm{D,CSD}}/C_{\mathrm{D,ASD}} \approx 12$. Additionally, we correlated the arising ASD Coulomb diamond features of a fading diamond edge and a current free bias window to the potential landscape of the compound ASD drain barrier potential.

5.3 Experimental Demonstration in doped GaAs/(Al,Ga)As

Complementary to the ASD SiGe qubit device measurements, the ASD concept was also incorporated in a doped GaAs/(Al,Ga)As qubit device (ASD GaAs). Supporting the previous results of the ASD SiGe device, we will present a Coulomb diamond comparison to evaluate the achievable reduction in coupling to the drain reservoir, highlighting the adaptability of the ASD concept as well as serving as further proof-of-principle. Additionally, we will demonstrate charge sensing operation with the ASD on a DQD. The presented measurements on the ASD GaAs qubit device were performed by E. Kammerloher at the *Rheinisch-Westfälische Technische Hochschule Aachen*.
Fig. 5.7 a) shows a false-colored scanning electron microscope image of a device fabricated in the same manner as the ASD GaAs qubit device illustrating the gate layout. The conceptional structure of the gate layout is the same as for the ASD SiGe qubit device. The light blue gates define the sensor dot (blue circle), the pink gates the slide region allowing to tune the distance to the drain reservoir $\boxtimes_{\mathrm{II}}$, while the source reservoir $\boxtimes_{\mathrm{I}}$ is positioned in a common distance. A potential electron path through the sensor is illustrated by the dashed line. The orange gates can be used to define and manipulate a nearby DQD (white circles) with its reservoirs $\boxtimes_{\mathrm{III}}$ and $\boxtimes_{\mathrm{IV}}$. Although the conceptual structure of the gate layout remains the same, the ASD GaAs device features a completely different design due to the distinct requirements of the material platform. The primary difference arises from the approximately three times smaller effective mass of GaAs compared to Si, which is addressed by a larger gate layout. Additionally, the doping of the heterostructure eliminates the need for a global TG. These differing requirements for the same concept underscore the advantages of the simulation-guided device design, on which this layout is also based (further details can be found in [77]). A schematic cross section of the ASD GaAs device with its gate layer stack and heterostructure is illustrated in Fig. 5.7 b). The gate layout was fabricated at the *Rheinisch-Westfälische Technische Hochschule Aachen* on a doped GaAs/(Al,Ga)As heterostructure MBE-grown at the

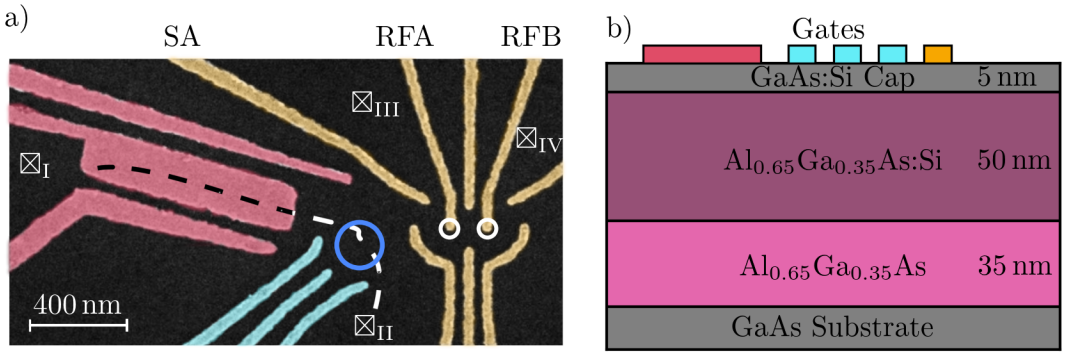

Figure 5.7: ASD device layout and layer stack in GaAs/(Al,Ga)As. a) False-colored scanning electron image of a device fabricated in the same manner as the ASD GaAs device illustrating the gate layout. The blue circle indicates the position of the sensor dot, while the white circles show the dot positions of a DQD. The drain and source reservoirs are labeled $\boxtimes_{\mathrm{I}}$ and $\boxtimes_{\mathrm{II}}$ for the sensor current path and $\boxtimes_{\mathrm{III}}$ and $\boxtimes_{\mathrm{IV}}$ for the DQD current path. The dashed line represents a possible electron trajectory through the sensor. The scanning electron image was taken by our partners at the *Rheinisch-Westfälische Technische Hochschule Aachen*. b) Schematic cross section of the layer stack. All gates are fabricated in the same gate layer.

Ruhr-Universität Bochum. The heterostructure consists of a GaAs substrate, followed by a 35 nm thick $Al_{0.65}Ga_{0.35}As$ layer, a 50 nm thick Si modulation-doped $Al_{0.65}Ga_{0.35}As$ layer, and a 5 nm thick Si-doped GaAs cap. The 2DEG is formed 90 nm below the interface at the GaAs/$Al_{0.65}Ga_{0.35}As$ interface. More details on the device fabrication and heterostructure growth can be found in [83].
As for the ASD SiGe qubit device, the ASD GaAs qubit device is initially characterized under voltage bias through Coulomb diamond measurements, aiming to evaluate the achievable reduction in capacitive coupling to the drain reservoir. These measurements are conducted by varying the drain potential U_{D} at reservoir $\boxtimes_{\mathrm{I}}$ as a function of the applied voltage on gate SA, while keeping reservoir $\boxtimes_{\mathrm{II}}$ fixed at $U_{\mathrm{S}} = 0\,\mathrm{V}$. Fig. 5.8 presents a comparison of the ASD GaAs device sensor in the CSD configuration in panel a) and the ASD configuration in panel b). The transition between these configurations was achieved by adjusting the slide gate voltages, which were set to zero in the CSD configuration and tuned up for the ASD configuration. More details on the device tuning can be found in [77, 83]. When the reservoirs are symmetrically tuned relative to the sensor dot in the CSD configuration, the typical Coulomb diamond pattern is observed (see Sec. 2.4). As the drain reservoir is pushed further away and the slide is activated, a steepening of the negative Coulomb diamond edge becomes apparent, resulting in the tilted appearance of the diamonds, similar to the ASD SiGe device. Additionally, similar to the observation in Si/SiGe a blockade region within the bias window ($0 < U_{\mathrm{D}} < U_{\mathrm{T}} \approx 360\,\mu\mathrm{V}$) emerges. Fitting the negative slope to the $I = 100\,\mathrm{pA}$ contour for both configurations yields $g_{\mathrm{CSD}} = -0.30\,\mathrm{V/V}$ in the CSD configuration

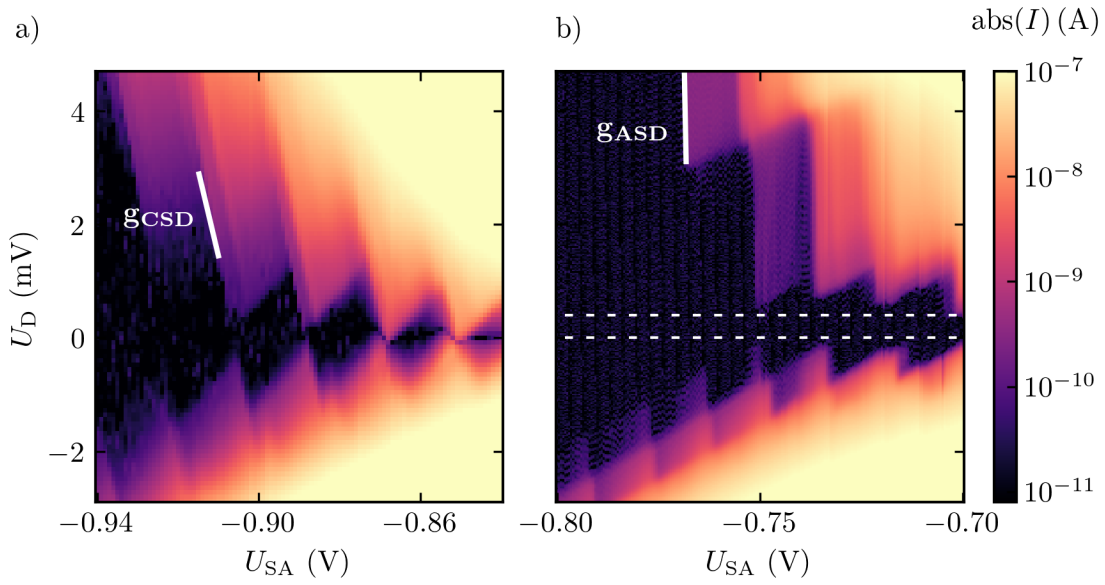

Figure 5.8: Coulomb diamond comparison for the ASD GaAs device between CSD and ASD configurations. In the asymmetric configuration the slide gates were tuned up, whereas they were set to zero volt in the symmetric configuration. The measurements are performed by varying the drain potential U_D at the reservoir ⊠$_I$ while keeping the reservoir ⊠$_{II}$ at measurement ground potential. Both measurements share the same colorbar and were performed at a temperature of $T = 50\,\mathrm{mK}$. The white lines indicate the negative slopes of the corresponding Coulomb diamonds linearly fitting the $I = 100\,\mathrm{pA}$ contour. a) Symmetrically tuned Coulomb diamond with the negative slope evaluated to be $g_{CSD} = -0.30\,\mathrm{V/V}$. b) Asymmetrically tuned Coulomb diamond with the negative slope evaluated to be $g_{ASD} = -3.96\,\mathrm{V/V}$. The white dashed lines illustrate a U_D region without current flow arising in the asymmetrically tuned Coulomb diamonds. Measurements were performed by E. Kammerloher at the *Rheinisch-Westfälische Technische Hochschule Aachen*.

and $g_{ASD} = -3.96\,\mathrm{V/V}$ in the ASD configuration. This indicates a reduction in C_D by a factor of $C_{D,CSD}/C_{D,ASD} \approx 13$. These measurements serve as a proof-of-principle, complementing those conducted on the ASD SiGe device. Moreover, they demonstrate that the ASD concept functions with equal efficiency on both material platforms.
As the next step, we aim to demonstrate charge sensing operation using the ASD. To achieve this, a DQD is configured utilizing the orange-colored gates, and the ASD is subsequently readjusted. Further details of the tuning procedure are provided in [83]. For charge sensing operation with the ASD, it is crucial to switch to current-biased operation, as previously shown in Fig. 5.1, to take advantage of the high output voltage swing. We chose $I_{ASD} = 500\,\mathrm{pA}$. With the ASD set to a sensitive position a charge stability diagram of the DQD using gates RFA and RFB is recorded, depicted in Fig. 5.9 a), by recording the output voltage U_D. The ASD allows to clearly resolve the regions of the different

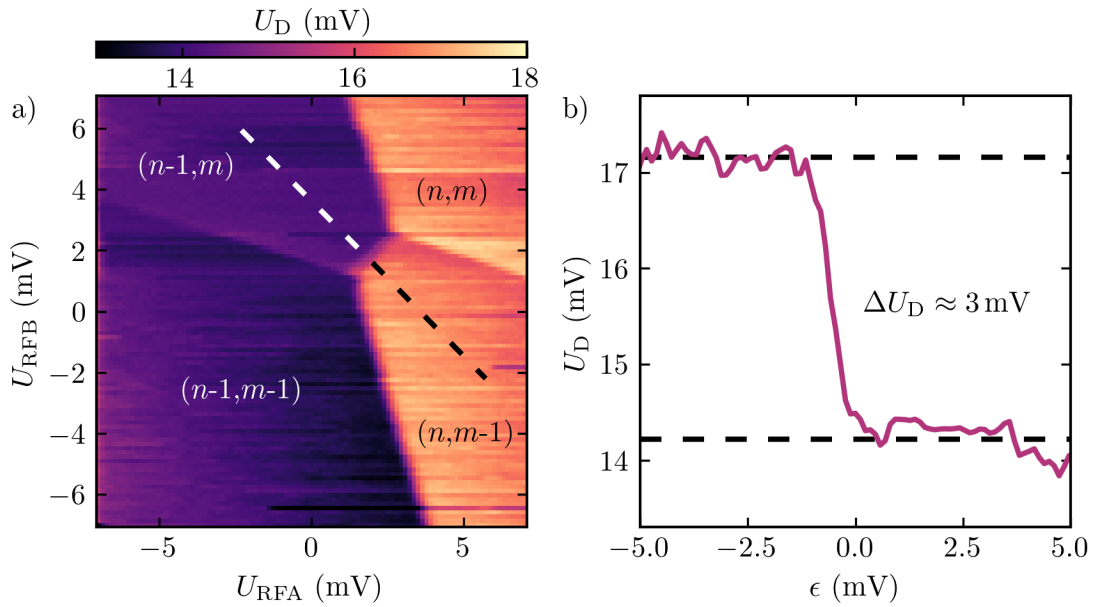

Figure 5.9: Charge sensing using a current-biased ASD in the ASD GaAs device. a) Charge stability diagram of a nearby multi-electron DQD recorded with the ASD operated in current bias (I_{ASD} = 500 pA), using the voltage drop U_D across the sensor as the signal (median adjustment per scan-line). (n,m) denotes the occupation of the DQD with n and m being the occupation of the left and right dot, respectively. The dashed line illustrates a possible detuning axis ϵ across an inter-dot transition of the DQD. b) U_D drop along the detuning axis ϵ (linear background subtracted) resulting in an output voltage of $\Delta U_D \approx 3$ mV across the inter-dot transition of the DQD. Measurements were performed by E. Kammerloher at the *Rheinisch-Westfälische Technische Hochschule Aachen*.

DQD occupations denoted with (n, m) by charge sensing. Fig. 5.9 b) displays the voltage swing across a inter-dot transition of the DQD (dashed line in Fig. 5.9 a)), corresponding to a qubit state change when the DQD is used as a ST-qubit. The observed voltage swing is $\Delta U_D \approx 3$ mV, which we expect to be an order of magnitude larger than that of a CSD in this configuration due to the observed one order of magnitude difference in capacitive coupling to the drain reservoir.

5.4 Conclusion on the Asymmetric Sensing Dot

We introduced a new proximal charge sensor design based on the concept of an asymmetrical capacitive coupling of the sensor dot to its reservoirs. The achievable decrease in coupling to the drain reservoir is directly proportional to the expected increase in output voltage. We demonstrate a successful implementation of an ASD gate concept in a DQD device for the two material platforms undoped Si/SiGe and doped GaAs/(Al,Ga)As evidenced by the drain capacitance reduction by factors of 12 and 13 compared to CSD

operation, respectively. This underscores the adaptability of the ASD concept as well as highlights that the ASD concept is equally efficient across material platforms. Both gate layouts were developed using a simulation-guided device design approach, which enabled the effective implementation of the ASD concept into actual device layouts, tailored to the distinct requirements of each material platform. Moreover, we demonstrate charge sensing operation with the ASD on a DQD with a large output voltage swing of $\Delta U_D \approx 3\,\mathrm{mV}$. The enhanced output signal makes the ASD a promising candidate for advancing the performance of the baseband readout approach in the context of scalable quantum computing.

6

Industrial Device Fabrication: Demonstrator Device

The Si/SiGe material platform offers a key advantage in terms of industrial compatibility, as it builds on well-established silicon processing techniques, enabling seamless integration with existing semiconductor manufacturing technologies. Moreover, it allows for the integration of electronics on the same chip due to its compatibility with standard CMOS technology, enabling efficient co-fabrication of qubits and control electronics. These characteristics make the platform especially promising for scalability, as they suggest the potential for reproducible fabrication and the parallel production of large qubit arrays within established semiconductor infrastructure.

To take the next step toward scaling up to a large number of qubits, we have partnered with industry and academia within the QUASAR consortium. This collaboration focuses on transferring academic expertise into the fabrication of industrial-grade devices. The joint goal is the development of a semiconductor quantum processor with a shuttling-based scalable architecture, utilizing industrial fabrication to bridge the gap between research concepts and large-scale implementation. As part of this effort, we introduce one of the first qubit devices of the QUASAR consortium, fabricated in an industrial setting at Infineon Technologies Dresden's 200 mm production line. Referred to as the industrial demonstrator device (IDD), this smaller prototype serves to test functionality before progressing toward larger structures. In this chapter, we demonstrate successful device operation by first tuning a QD to function as a proximal charge sensor and then using it to reliably tune a neighboring QD down to the last electron, establishing the foundation for a spin qubit.

Moreover, the IDD enables us to investigate the influence of the magnetic field on the few-electron energy spectrum of the QD and, in turn, gain insights into the magnetic-field-dependent spin configurations via a method called magnetospectroscopy [36, 55, 63, 97–100]. In doing so, we also determine a lower bound for the local valley splitting, a key material property that can be reliably measured in qubit devices, while it is not accessible via FES measurements. Valley splitting energies in gate-defined QDs formed in Si/SiGe

heterostructures has been observed to vary significantly, ranging from below 10 µeV to more than 200 µeV [16, 36, 55, 63, 97–99, 101]. A comprehensive understanding of the factors that influence the valley splitting is essential, as a sufficiently large valley splitting energy is crucial for preserving spin information and ensuring high-fidelity qubit operations [16, 102–105]. However, the mechanisms governing valley splitting are not yet fully understood and remain a key focus of ongoing research.
The characterization of the IDD, presented in the following chapter, was performed at a base temperature below 7 mK using our dilution cryostat in conjunction with the previously described qubit measurement technique (see Ch. 2.8). A presentation of the first tuning steps, the detailed tuning voltages and an additional noise characterization for the IDD can be found in the master's thesis of V. Stieß [106], with whom I worked on this topic and supervised her thesis.

6.1 Industrial Demonstrator Device

The current state-of-the-art device designs involve defining gates across multiple layers. This approach enables more compact layouts and facilitates enhanced tunability and controllability, particularly in the few-electron regime. In the IDD, a three-layer gate structure is used to define two adjacent QDs, each connected to its own pair of reservoirs. A false-colored scanning electron image of a device fabricated in the same manner as the IDD is shown in Fig. 6.1 a). The two QDs are located beneath the shared top gate, labeled AccDots and shown in light blue, in the second gate layer, with one positioned at its overlap with the plunger gate PL and the other at its overlap with the plunger gate PR, both situated in the first gate layer and depicted in yellow. The shared top gate facilitates electron accumulation within the dot region, while the plunger gates serve a dual purpose: defining the QDs and enabling the tuning of their properties such as electron occupancy. The two QD regions are separated by the purple gate within the first gate layer, labeled BG, which also confines the dots along their x-dimension. This design does not include dedicated gates to define the outer dimensions of the dots in the x-direction, besides the inherent limitation due to the width of AccDots. This restriction affects the tunability of the QDs shapes, a factor that will become apparent during the tuning process. The barrier gates within the first gate layer, labeled TBL, BBL, TBR, and BBR, and depicted in dark blue, are designed to confine the QDs in the y-direction and define the tunnel barriers between the QDs and their respective reservoirs. Independent tuning of electron accumulation within the reservoirs, labeled $\boxtimes_{\text{I-IV}}$, is achieved via the orange-colored gates labeled SDAcc, which are electrically connected outside the depicted area. Gates in the third gate layer, named MAccG, are used to establish the connection via accumulation between the reservoir regions of SDAcc and their respective implanted regions, which serve as ohmic contacts located approximately 60 µm away, reducing the interference of the dopant atoms with the active device region where the QDs are formed. The pink-colored gates, forming a pinch-off plane around the other gates in the first gate layer, are dedicated to suppressing parasitic current paths. A schematic cross-section of the IDD

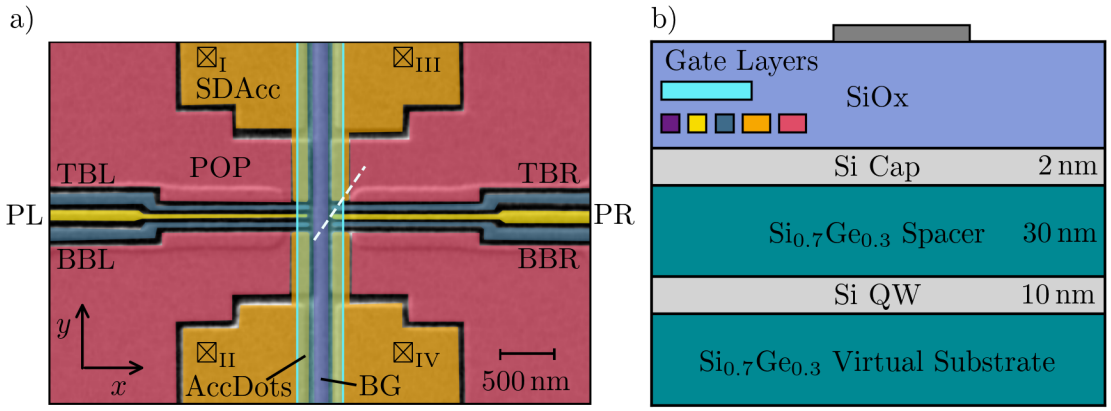

Figure 6.1: Industrial demonstrator device layout and layer stack. a) False-colored scanning electron image of a device fabricated in the same manner as the demonstrator device illustrating the gate layout. Labels $\boxtimes_{\mathrm{I-IV}}$ mark the source and drain reservoirs. The semi-transparent light blue gate is positioned in a gate layer plane above the other gates and separated by a dielectric layer, as illustrated in panel b). The white dashed line indicates the line cut through the device sketched in panel b). The scanning electron image was taken by P. Muster at *Infineon Technologies Dresden*. b) Schematic cross section of the layer stack. The gate layer colors correspond to the colors in a) and their vertical position illustrates the gate layer plane they were fabricated in. The gray colored gate is beyond the frame of the scanning electron image shown in panel a). The SiOx thickness between the heterostructure and first gate layer, the first and second gate layer and the second and third gate layer are respectively 10 nm, 10 nm and 300 nm.

device, illustrating its heterostructure and gate layer stack along the white dashed line, is shown in Fig. 6.1 b). The heterostructure and the three gate layers are separated by SiOx insulating layers, with thicknesses of 10 nm, 10 nm, and 300 nm, respectively, between the heterostructure and the first gate layer, the first and second gate layers, and the second and third gate layers. The heterostructure of the commercially purchased benchmark wafer, grown by *Lawrence Semiconductors Research Labs*, features a functional layer stack comprising a 10 nm-thick natural Si QW embedded between a $Si_{0.7}Ge_{0.3}$ virtual substrate and a 30 nm-thick spacer layer of the same composition. During fabrication, the Si cap layer on top is thinned to approximately 2 nm. Additional details on the device fabrication process within the industrial production line can be found in [107].

6.2 Few-Electron Tuning Regime

Within this section, we showcase the capability of the IDD device to tune a QD to the last-electron regime, leveraging charge sensing to precisely identify this state.
As the IDD design provides each of the two QDs with its own set of reservoirs, it enables interchangeable use without a predefined role as either the sensor dot (SD) or the target for

tuning to the few-electron regime. We chose to tune the left quantum dot as SD and the right as few-electron quantum dot (FEQD). Despite the novelty of the industrial device, the configuration of all gates was remarkably straightforward, enabling the tuning of QDs into the multi-electron regime on both sides. The left QD was configured as a sensor with minimal additional tuning required, being brought into a sensitive position for charge sensing, while the right QD underwent gradual tuning to reliably reach the last-electron regime. During the tuning to the last electron, the fact that both QDs have their own reservoirs enables simultaneous current detection through both dots. As the right dot is tuned from the multi-electron regime to reduce its electron occupancy, Coulomb blockade, visible in transport on the right, begins to appear as charge sensing lines in the SD, confirming proper charge sensing operation. Additionally, it should be emphasized that the device exhibited excellent reproducibility, with the voltages required for tuning both QDs closely matching the precharacterization performed at the *Rheinisch-Westfälische Technische Hochschule Aachen* by T. Huckemann. The fact that this precharacterization was conducted in a different setup and during a separate cool-down further underscores the device's consistent performance. Overall, the IDD demonstrated excellent stability and reproducibility throughout the straightforward tuning process. A detailed description of the first tuning steps including the complete set of chosen voltages as well as noise characterization is described in the master's thesis of V. Stieß [106].
The main challenge throughout the tuning process stemmed from the formation of a significant number of disorder dots, which could only be partially resolved despite extensive tuning efforts. As previously described in Sec. 3.2, the ground state energy of the conduction band inherits potential fluctuations caused by defects or impurities, particularly in the vicinity of the QW. The magnitude of these fluctuations is a key limiting factor for 2DEG transport properties and also impacts quantum dot devices, where pronounced potential fluctuations facilitate the formation of disorder dots. If a dot forms due to confinement within one of the potential minima, rather than being defined electrostatically by the gates, it is commonly referred to as a disorder dot. They are typically quite challenging to overcome by tuning, as they can form directly beneath a single gate, making them primarily influenced by the voltage applied to that gate. Eliminating the disorder dot beneath this gate imposes a restriction on the applicable voltage range, which is often incompatible with the tuning requirements of the intended electrostatically defined dot. The observation of significant potential fluctuations in the benchmark wafer grown by *Lawrence Semiconductors Research Labs* aligns with findings from FES measurements conducted via quantum Hall characterization on FES E using a similar wafer from this foundry, as presented in Sec. 3.2. These measurements similarly concluded that the wafer's transport properties were severely impacted by potential fluctuations. Even though the observation of disorder dots is primarily linked to the heterostructure used and highlights the adoption of a different heterostructure as the main improvement for future devices, we identified two ideas for an adjusted device design during the tuning process that could further enhance the tunability of next-generation industrial device designs, thereby simplifying the tuning process even in the presence of disorder dots.

The first suggestion for improving the device design involves dividing the AccDots gate into two separate gates, each dedicated to one of the dots. This adjustment could help reduce the number of disorder dots, particularly between gates, by enhancing the electron accumulation beyond the extent of potential fluctuations. Additionally, meeting the differing requirements of the SD in the multi-electron regime and the second dot in the few-electron regime with a single gate is inherently challenging. The second design improvement could involve implementing additional gates to restrict the outer dot dimensions in the x-direction. The advantage of this approach would be threefold: Firstly, it would simplify confinement, particularly during tuning to the last-electron regime. Secondly, it would allow for greater control over the shape of the dots, which, due to the current device layout, tend to form elliptically. Thirdly, it could enhance the sensitivity of charge sensing by enabling the dots to be brought closer together.
Despite the challenges in the tuning process due to disorder dots and device design limitations, we successfully tuned the right dot to the last electron by leveraging the left dot as sensor. Fig. 6.2 presents the charge stability diagram of the FEQD as it is tuned down to the last electron, showing its dependence on the voltages applied to its plunger gate PR and barrier gate BBR. The corresponding charge transition lines (highlighted with light blue and blue dashed lines) are clearly visible against the background of the SDs Coulomb blockade peak. The corresponding electron occupation is indicated by N. Within this tuning configuration the barrier defined by gate BBR is opaque suppressing tunneling to the corresponding reservoir. Thus the charge transitions take place by loading/unloading of electrons from the reservoir $\boxtimes_{\mathrm{III}}$, whose tunnel barrier is defined by gate TBR. We identify the lowest-lying line as the $0 \rightarrow 1$ transition line, as no further transitions are observed below it. This was confirmed by an additional measurement at even lower voltages applied to gate PR, with the SD tuned for increased sensitivity in this lower voltage regime. The slope of the charge transition lines reveal that U_{PR} has a more dominant impact on the FEQD compared to U_{BBR}. This matches our observations during the tuning process that the FEQD is well-centered underneath the plunger gate PR, predominantly influenced by this gate and, to a lesser extent, equally affected by its barrier gates. Furthermore, we observe that the charge transition lines exhibit slightly different slopes, with the light blue highlighted lines being marginally steeper than the blue ones. This can be attributed to the aforementioned assumed ellipticity of the QDs. Adding an electron can influence the QD's shape - specifically its ellipticity - causing it to respond differently to changes in the barrier gate.
Within the few-electron regime, non-uniform spacing between charge transition lines, i.e., addition energies, reflecting shell-like energy level filling as seen in artificial atoms, in addition to the charging energy from Coulomb blockade, has been observed [98, 108]. Within this model, the first four electrons occupy s-like states, with the s-shell being fourfold degenerate due to valley and spin degeneracy, requiring only the charging energy for their occupation. For the first electron occupying the p-level ($N = 5$), not only the charging energy but also the energy corresponding to the single-particle level spacing between the s- and p-shell must be provided. The p-level is eightfold degenerate, being twofold degenerate due to spatial symmetry [53] (orbital degeneracy) and fourfold

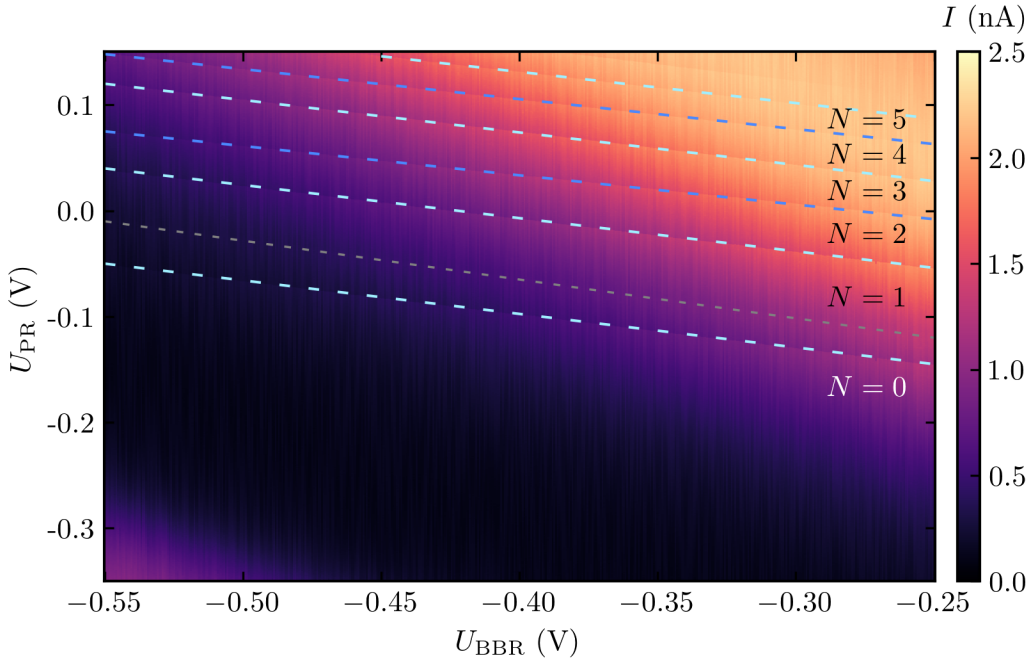

Figure 6.2: Charge stability diagram of the demonstrator device in the few-electron regime. The current corresponds to the SD serving as a sensor for the FEQD. Blue and light blue dashed lines highlight the charge transition lines, with the corresponding electron occupations denoted as N. The dashed line depicted in gray marks a charge transition line of an adjacent disorder dot.

degenerate due to spin and valley degeneracy. Thus, the subsequent electrons up to $N = 12$ require only the charging energy to be loaded onto the QD. According to this framework, for a QD in the few-electron regime up to $N = 5$, equal level spacing is expected, except for the $4 \rightarrow 5$ transition to show an enlarged distance to the $3 \rightarrow 4$ transition reflecting its increased addition energy. Contrarily, we observe the distance between $0 \rightarrow 1$ and $1 \rightarrow 2$ being the only one noticeably enlarged (see Fig. 6.2). One of the key assumptions of this model is the nearly perfect two-dimensional spherical symmetry of the QD [109]. Thus not being able to observe this behavior strengthens our suggestion of elliptical QDs being favored by this device design, which is in accordance to the prediction of a reduced degree of symmetry leading to a different shell-like structure [109].
Additionally, alongside the charge transition lines of the FEQD, we observe a weaker line with a different slope, highlighted by a gray dashed line. This transition originates from a disorder dot in the vicinity of the FEQD. From the charge stability diagram in Fig. 6.2, we can infer that the disorder dot is located further away from the SD than the FEQD, as indicated by the weaker transition line. Furthermore, it can be deduced that the disorder dot is more strongly influenced by gate PR than by gate BBR.
To confirm the assignment of charge transition lines, we recorded an additional charge stability diagram by varying the barrier gate TBR, while keeping $U_{\mathrm{BBR}} = -0.32\,\mathrm{V}$ fixed.

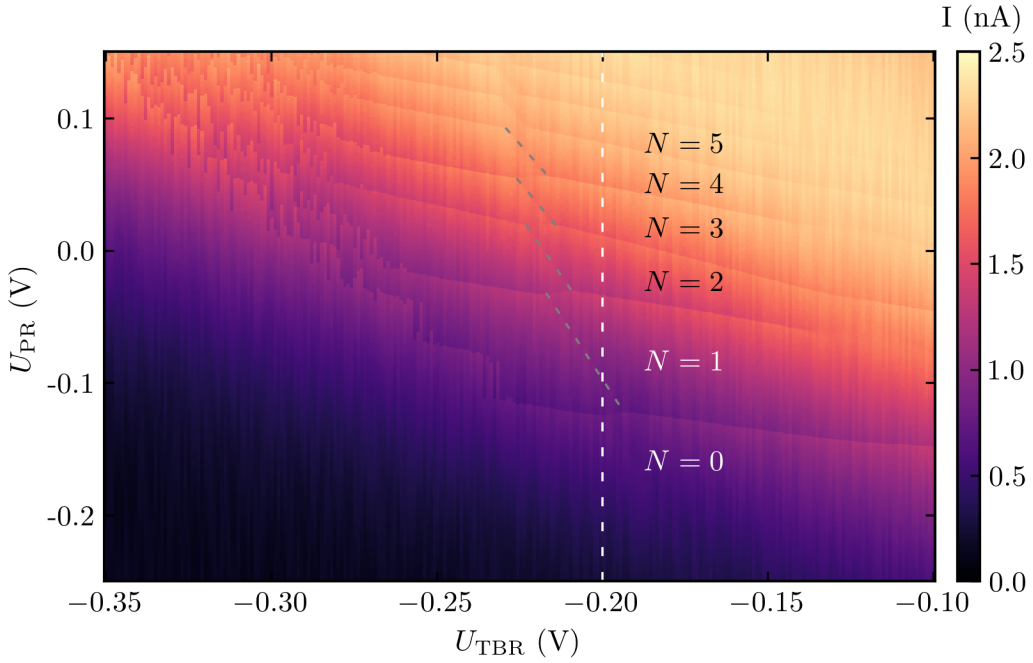

Figure 6.3: Charge stability diagram of the demonstrator device in the few-electron regime. The current corresponds to the SD serving as a sensor for the FEQD. The occupation of the QD is denoted as N. The white dashed line indicates the $U_{\mathrm{TBR}} = -0.2\,\mathrm{V}$ chosen for the charge stability diagram in Fig. 6.2. The dashed line depicted in gray marks the charge transition lines of an adjacent disorder dot.

The corresponding charge stability diagram with a slightly retuned SD is presented in Fig. 6.3. The set of charge transition lines corresponding to the FEQD is clearly resolved, with its occupancy labeled as N. Additionally, a distinct charge transition line, highlighted with a gray dashed line, is visible, exhibiting a different slope and thus clearly originating from a different QD. A comparison of the charge transition lines at $U_{\mathrm{TBR}} = -0.2\,\mathrm{V}$ (white dashed line) with those at $U_{\mathrm{BBR}} = -0.32\,\mathrm{V}$ in Fig. 6.2 confirms our earlier assignment of the charge transition lines, particularly that the gray line originates from a different most likely disorder dot.
Moreover, Fig. 6.3 allows us to infer that the FEQD is more strongly influenced by gate PR than by gate TBR and matches its previously described position, well-centered beneath gate PR. Furthermore, as already evident in Fig. 6.2, we observe that the FEQD charge transition lines are not parallel and additionally that their slopes change depending on the applied gate voltages. This leads to the interpretation that the shape of the FEQD, i.e, ellipticity, not only changes with the electron occupancy, as previously noted, but also deforms in response to the surrounding gate potentials.
Additionally, we gain further insights into the location of the disorder dot. The data shows that it is electrostatically more influenced by gate TBR than by gate PR. Combined with the previous observation in Fig. 6.2, where it appeared to be more influenced by gate PR

than by gate BBR, we can conclude that the disorder dot is most likely located between gate TBR and gate PR. It can be observed that the steepness of the disorder dot's charge transition line decreases with increasing U_{PR} and decreasing U_{TBR}. From this change in slope, we deduce that the influence of gate PR increases while the influence of gate TBR diminishes, leading to the interpretation that the disorder dot shifts slightly closer to gate PR and further away from gate TBR.
Within the U_{TBR} range of $-0.22\,\mathrm{V}$ to $-0.18\,\mathrm{V}$, the disorder dot and the FEQD exhibit characteristic features of a DQD (see Sec. 2.6). The DQD pattern reveals that the two dots are capacitively coupled and weakly tunnel-coupled. The spacing between the triple points along the inter-dot transition reflects the strength of the capacitive coupling. Given the faint visibility of the inter-dot transitions, we conclude that the tunnel coupling is weak.
A prominent feature visible in Fig. 6.3 is the upward bending and fraying of the FEQD's charge transition lines as U_{TBR} decreases. As the bottom barrier BBR is already opaque with decreasing voltage on gate TBR we reduce the tunnel coupling to the reservoir the electrons are loaded/unloaded from. With the tunneling barrier increasing, the probabilistic behavior of the tunneling process along the sweep direction (negative to positive U_{PR}) becomes apparent, resulting in the frayed lines. The bending towards higher PR voltages is caused by the fact that gate PR also acts on the tunnel barrier, albeit to a lesser extent than gate TBR. A higher U_{PR} increases the tunnel coupling, allowing the electrons to load at higher PR voltage values where sufficient tunnel coupling is achieved.
A valuable conclusion that can be drawn from the point at which the lines begin to fray as U_{TBR} decreases is whether they belong to the same few-electron dot. An additional electron on the FEQD increases the tunnel coupling, causing the charge transition lines to fray at lower TBR voltage values as the occupancy increases. Consequently, for charge transition lines corresponding to the same QD, it is expected that the fraying sets in at progressively lower barrier voltages. Observing this behavior once again confirms the correct assignment of the charge transition lines to the FEQD.
This underscores that we successfully tuned the IDD in a configuration with a SD capable of charge sensing of a FEQD tuned down to the last electron, despite the challenges originating in the chosen heterostructure leading to disorder dots.

6.3 Magnetic field dependence of the Few-Electron Energy Spectrum

With the FEQD tuned to the last electron, applying an in-plane magnetic field allows to study the effects of spin configurations on the few-electron energy spectrum of the FEQD. This magnetospectroscopy tracks changes in the ground state energy of the different charge occupations of a FEQD as a function of an external in-plane magnetic field.
In order to access information about changes in ground state energy, magnetospectroscopy tracks the change of a QDs electrochemical potential, which correspond to the differences

in ground state energy between two charge occupations (see Sec. 2.7). The QD's ladder of discrete levels in electrochemical potential is reproduced by its charge transition lines. Hence, we can gain information on the spin configurations by measuring the charge transition lines as a function of the plunger gate voltage and the in-plane magnetic field.
As this method relies on the ability to precisely determine changes in the charge transition lines, we aim to tunnel couple the QD to only one reservoir, which serves as a fixed electrochemical potential reference to determine the QD's charge transitions in reference to. Additionally, we aim to limit the electron temperature, as higher electron temperatures result in broadened lines. To achieve this, we restrict the magnetic field sweep rate, as rapid sweeping can heat the device, and we select a small bias voltage. The magnetic field is chosen in-plane to conduct this study as with an out-of-plane magnetic field applied Hall physics would disturb the observations. We find that the tuning requirements are already met in the previously presented tuning of the FEQD. For the magnetospectroscopy measurements, we set the barrier gate voltages to $U_{\mathrm{BBR}} = -0.32\,\mathrm{V}$ and $U_{\mathrm{TBR}} = -0.2\,\mathrm{V}$, with a slightly retuned SD achieved by varying U_{PL}. Although the disorder dot is present in this configuration, it should not disturb the measurements.
Our initial approach to recording magnetospectroscopy is presented in Fig. 6.4 a), where the first four charge transitions were recorded simultaneously. The measurement was conducted by continuously and repeatedly sweeping U_{PR} at a sweep rate of $15\,\mathrm{mV\,s^{-1}}$ and a resolution of $300\,\mu\mathrm{V}$. Simultaneously, the magnetic field was swept at a rate of $100\,\mu\mathrm{T\,s^{-1}}$. While the charge transition lines are clearly visible, the expected change in the charge transitions, which lies in the range of hundreds of microvolts to millivolts, is not directly discernible in this measurement. A representative line cut at 0.53 T is shown in Fig. 6.4 b). The dips in current along the Coulomb peak of the SD, corresponding to the charge transition lines, are clearly visible and allow their U_{PR} positions to be fitted using a Fermi function, represented by the colored lines. The charge transition line of the disorder dot, barely visible in 6.4 a), can also be identified as a small dip at approximately $U_{\mathrm{PR}} = -0.09\,\mathrm{V}$. The extracted progression of the different charge transition lines with magnetic field, determined through the Fermi fit, suggests a trend for the $0 \rightarrow 1$ transition. For the other transitions, no discernible trend is observed. We identified that the U_{PR} resolution is insufficient, limiting the accuracy of the determined charge transition line positions in U_{PR}. Enhancing the resolution is necessary to enable a more reliable analysis of all transitions. We primarily chose the approach of measuring all lines simultaneously to account for a potential global drift of the QD's charge transition lines during the sweep. Such drift, could dominate over the changes induced by the magnetic field, potentially masking them. Since a global drift would affect all charge transition lines uniformly, it could be corrected by referencing the $0 \rightarrow 1$ transition, which is expected to appear as a straight line. This drift could then be extracted and subtracted from the data to isolate the magnetic field's effects. However, no significant drift was observed that would severely distort the line shapes. Thus, we developed an alternative approach, scanning each line separately. This method reduces the U_{PR} range, enabling a significantly increased resolution while still keeping the measurement time reasonable.

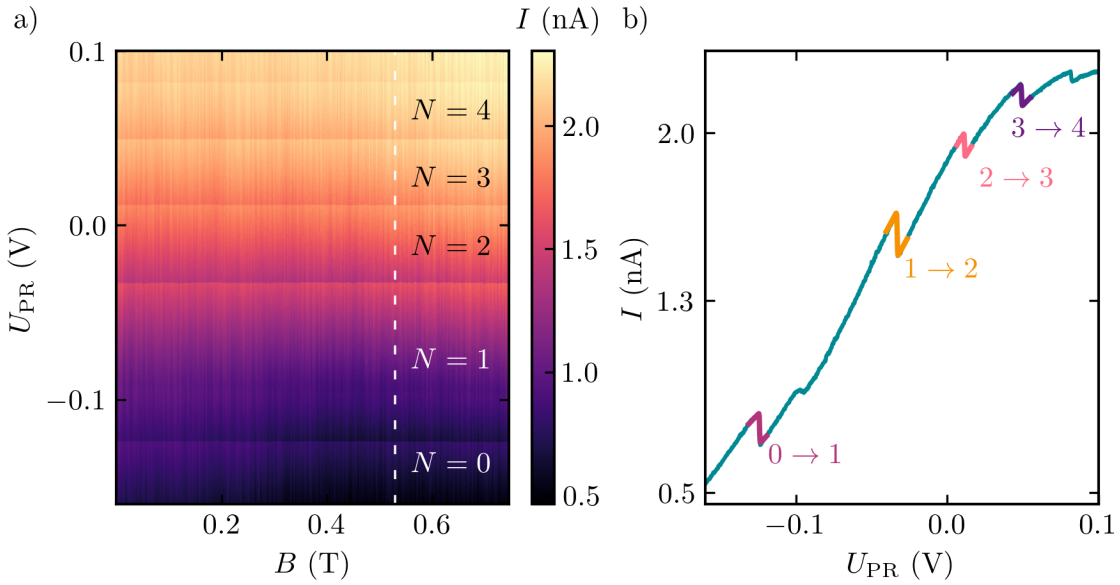

Figure 6.4: Magnetospectroscopy performed simultaneously on the first four charge transitions. a) Magnetic field dependence of the first four charge transitions of the right QD determined via varying the corresponding plunger gate voltage U_{PR}. The electron occupation is labeled by N. The charge transitions appear as lines showcasing a dip in the current of the SD. b) Representative example of a single U_{PR} sweep at the magnetic field of $B = 0.53$ T corresponding to the line cut illustrated as white dashed line in panel a). The dips in the Coulomb peak flank of the SD correspond to the different charge transitions of the FEQD. For each charge transition the corresponding fit to extract its U_{PR} position is illustrated. The smaller dip visible between the $0 \rightarrow 1$ and $1 \rightarrow 2$ transition corresponds to the disorder dot.

In our next attempt, we measured each charge transition line separately with a tenfold increase in U_{PR} resolution to $\delta U_{PR} = 30\,\mu$V with a corresponding sweep rate of $1.5\,\text{mV}\,\text{s}^{-1}$. Simultaneously, we doubled the magnetic field sweep rate to $200\,\mu\text{T}\,\text{s}^{-1}$ without any loss in resolution by additionally incorporating measurements during both the forward sweep of U_{PR} towards positive values and the back sweep returning to the starting position. Fig. 6.5 illustrates the drastically improved quality of the fit and the extracted positions of the transitions, representatively for the $0 \rightarrow 1$ transition, by comparing the two approaches. Panel a) shows the results from the initial approach, where all charge transition lines were measured simultaneously, while panel b) shows the results from the improved approach, where each charge transition line was recorded separately. The comparison clearly demonstrates a significantly reduced error (root mean square error with 95 % confidence bounds) and a decreased spread in the data points, which are expected to align along a straight line with a negative slope (see Sec. 2.7). At this point, it should be emphasized that no filters need to be applied to the data to extract the U_{PR} positions of the transitions prior to using the Fermi fit.

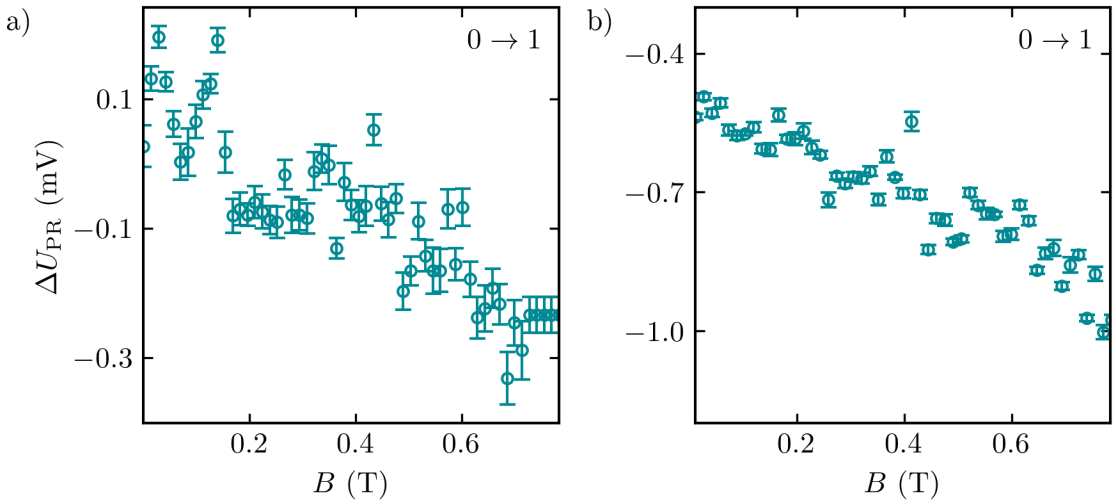

Figure 6.5: Improvement on the quality of the fit determining the charge transition position exemplarily shown for the $0 \to 1$ transition. The U_{PR} position of the charge transition is determined for each magnetic field value via a Fermi function. The corresponding error bar visualizes the root mean square error with 95 % confidence bounds. a) Extracted charge transition line from the measurement shown in Fig. 6.4 a) with a plunger gate voltage resolution of $\delta U_{\mathrm{PR}} = 300\,\mu\mathrm{V}$. b) Extracted charge transition line with an ten times increased plunger gate voltage resolution of $\delta U_{\mathrm{PR}} = 30\,\mu\mathrm{V}$.

With this improved method, we can now reliably track the charge transition lines as a function of the magnetic field. Fig. 6.6 a), c), and e) present the measurements for the $0 \to 1$, $1 \to 2$, and $2 \to 3$ transitions, respectively. The changes in the charge transition lines are easily observable directly from the data. Extracting the corresponding progression of each charge transition line, presented in panels b), d), and f) as pink dots, reveals clearly resolved behavior consistent with the expectations described in Sec. 2.7. This is further reflected in the good agreement with the corresponding fits shown as blue lines.

For the $0 \to 1$ charge transition, we observe the typical behavior of the Zeeman effect on a single spin-down state, evidenced by the linear decrease with the magnetic field. Fitting this behavior allows us to extract the lever arm $\alpha \approx 0.1\,\mathrm{eV\,V^{-1}}$. This value aligns with our evaluation from Coulomb diamond measurements on the FEQD, as well as the value obtained during precharacterization performed at the *Rheinisch-Westfälische Technische Hochschule Aachen*. The expected kink in the $1 \to 2$ charge transition, originating from the anti-crossing of the singlet and lowest triplet state, stands out as a prominent feature. The magnetic field at which the kink occurs allows us, even visually, to estimate the two-electron singlet-triplet splitting E_{ST}, providing a lower bound on the single-electron valley splitting E_{VS} [55, 98]. Matching this estimate, we determine $E_{\mathrm{ST}} \approx 50\,\mu\mathrm{eV}$ from the fit. Additionally, the fit provides another estimate of the lever arm, which aligns with the previously obtained value. The estimated E_{VS} is consistent with

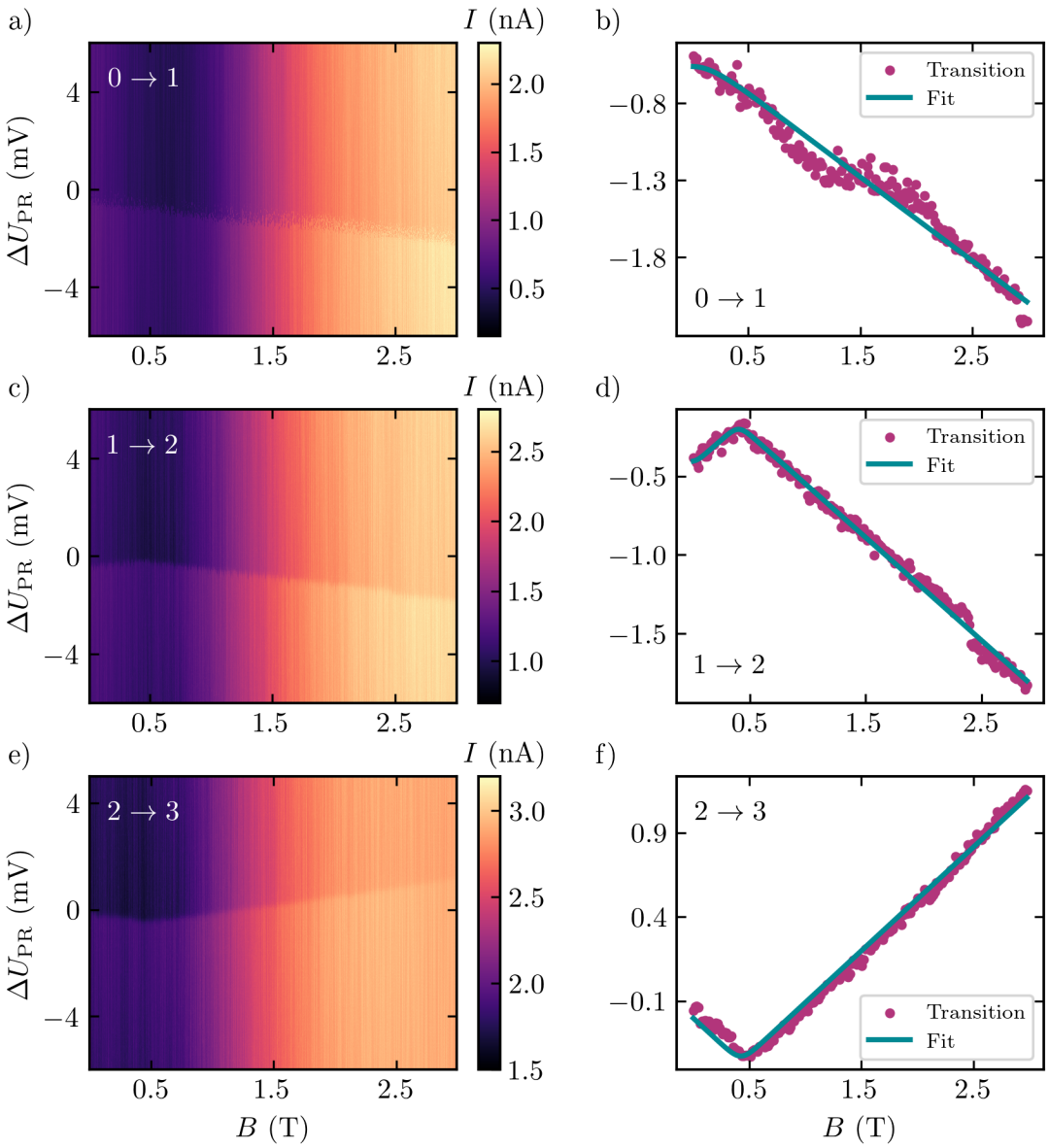

Figure 6.6: Magnetospectroscopy on the first three charge transitions individually. a), c) and e) Magnetic field dependence of the $0 \rightarrow 1$ transition in a), $1 \rightarrow 2$ transition in b) and $2 \rightarrow 3$ transition in c) of the right QD determined via varying the corresponding plunger gate voltage U_{PR}. The charge transition appears as lines showcasing a dip in the current of the SD. b), d) and f) Via Fermi fit extracted trajectory (pink dots) of the corresponding transitions in a), c) and e), respectively. The blue line illustrates the fit of the transitions to their predicted behavior, described in Sec. 2.7.

previous observations on the same batch of heterostructures in other devices fabricated by an academic process at the *Rheinisch-Westfälische Technische Hochschule Aachen* [36]. The $2 \rightarrow 3$ charge transition is expected to exhibit, as described in Sec. 2.7, two kinks: the first corresponding to the two-electron singlet-triplet splitting and the second reflecting the energy of the zero-magnetic-field excited state. We are able to observe the first kink, which further validates the previously estimated E_{ST}. Additionally, the fit once again confirms our estimation of the lever arm. However, the second kink is not observed, which also explains the slight deviation in the fit. This absence can be attributed to the fact that the first excited state is associated with the first excited orbital energy, expected to be in the range of mV [16, 36, 110], corresponding to magnetic fields beyond the capabilities of our setup and most other setups. The fits of the three lines additionally provide a rough estimate of the electron temperature $T_{\mathrm{e}} \approx 50\,\mathrm{mK}$.
The magnetospectroscopy measurements not only confirm the successful tuning of the FEQD to the last electron but also reveal valuable insights into the spin configurations and the few-electron energy spectrum of the FEQD. Furthermore, they provide an estimate of the important quantity of the valley splitting. Particularly noteworthy is that neither the elliptical shape of the FEQD nor the presence of the nearby disorder dot leads to any significant deviations from the predicted behavior of the charge transition lines.

6.4 Conclusion on the Industrial Demonstrator Device

The IDD showcases its ability to efficiently tune a QD to the last electron, forming the foundation for spin qubits, and to perform state-of-the-art charge sensing, enabling reliable readout of the electronic state. Additionally, magnetospectroscopy offered valuable insights into the spin configurations of the few-electron energy spectrum.
The tuning process of the IDD was remarkably straightforward, showcasing state-of-the-art charge noise [106, 107], excellent stability, and high reproducibility across cool-downs and setups. Besides the already excellent performance of the IDD, we proposed two potential device design adjustments for the next generation of devices, which could further optimize its tunability and performance, particularly in terms of charge sensing sensitivity and dot confinement. The magnetospectroscopy measurements, utilized for the first time in Regensburg and established within our group, were conducted with outstanding data quality. They enabled access to the spin configuration in the few-electron regime as a function of the magnetic field and provided an estimate of a lower bound on the valley splitting $E_{\mathrm{ST}} \approx 50\,\mu\mathrm{eV}$, a critical parameter for qubit operation. This value confirms insights from a spatial mapping conducted on the same batch of heterostructures [36].
As the main challenge during the tuning process arose from the disorder dots linked to the choice of heterostructure, it will be particularly interesting to investigate devices of the next generations based on heterostructures manufactured within the QUASAR consortium by our partner, *IHP - Leibniz-Institut für innovative Mikroelektronik*. As

presented in Sec. 3.2, they exhibit less disorder and show overall improved transport properties, comparable to some of the best reported to date for qubit applications. It will be equally interesting to test the performance of these heterostructures in terms of valley splitting energies, since energies of $\approx 200\,\mu\text{eV}$ have been reported [16, 63], while the commercial wafer used here turned out to have comparatively lower values.
Overall, as one of the first qubit devices fabricated in an industrial setting at *Infineon Technologies Dresden*'s 200 mm production line, it also demonstrates the compatibility of heterostructure-based spin qubit devices with industrial CMOS technology. This compatibility is promising for rapid scalability and seamless integration of electronics on the same chip, paving the way for future advancements in quantum computing.

7

Conclusion and Outlook

Scalability of the qubit systems remains the central challenge in quantum computing, requiring a shift from proof-of-principle implementations to providing a route towards large-scale systems with millions of qubits to enable fault-tolerant computing. This thesis contributes to this effort by addressing building blocks for scalable Si/SiGe spin qubit device architectures.

We first presented a detailed analysis of five undoped FESs, which serve as the foundation for realizing various quantum circuits in semiconductor heterostructures, including semiconductor spin qubits. We examined the correlation between transport properties and layer stack properties as well as fabrication details. A comparison of the five FESs underscores that, although all represent state-of-the-art designs for field-effect applications, they display significant variation in their transport properties. A thorough understanding of FES properties is therefore crucial for further optimization and tailoring to specific applications. In particular for spin qubit applications, a comprehensive understanding of impurities in the FES and the disorder potential fluctuations they induce in the QW is essential, making FES A and D, produced by *IHP - Leibniz-Institut für innovative Mikroelektronik* attractive for quantum circuit applications. These factors play a decisive role in the precise control of charging energies, the position and shape of QDs, the occurrence of disruptive disorder dots, and the sources of charge noise. Especially in terms of scalability, achieving a high degree of uniformity in FES properties is essential, as the focus shifts from operating a few qubits at selected locations to integrating many qubits across large-scale architectures.

Building on this, we examined the effect of biased cooling on three selected FESs from the batch previously studied, an effect that has not yet been considered in undoped Si/SiGe. At operation temperature, biased cooling induces a static electric field within the FES, resulting from charge reconfiguration at the semiconductor/heterostructure interface at temperatures preceding heterostructure freeze-out. As a result, the field-effect tunable range of the 2DEG electron density can be deterministically shifted, while

the 2DEG quality markers, such as electron mobility and the temporal stability of the 2DEG density, remain unaffected. Moreover, we developed an empirical model describing the biased cooling effect, which is anticipated to be transferable to any undoped semiconductor heterostructure. With its ability to shift the operation window of individual gates and engineer trapped charges at the dielectric/heterostructure interface, the biased cooling effect offers diverse application possibilities in qubit devices. Shifting the operation window could compensate for unwanted variations between gates during fabrication, as well as differences in gate layers and their respective distances to the 2DEG. Homogenizing the operation window voltages for different gates offers several advantages: it reduces the risk of leakage in the device, facilitates the implementation of virtual gates during device tuning, and can lower the likelihood of local tunneling towards the dielectric/heterostructure interface, which is known to introduce detrimental effects on device operation and charge noise. Furthermore, the operation window of individual gates could be shifted according to their distinct functionality. In addition, the engineering of trapped charges at the semiconductor/heterostructure interface by biased cooling can be advantageous, as negative biased cooling reduces the spatial smearing of the potential distribution and electric field within the QW plane, whereas positive biased cooling could reduce charge noise.

Turning to the building block of qubit readout, we introduced a new proximal charge sensor concept tailored for the baseband approach, the asymmetric sensing dot. This concept exploits an asymmetrical capacitive coupling between the sensor dot and its reservoirs, enabling a drastically increased output signal compared to conventional sensor dots, and is predestined to incorporate classical electronics of the readout circuitry on chip. We successfully implemented the ASD concept in two DQD devices on two material platforms, undoped Si/SiGe and doped GaAs/(Al,Ga)As, demonstrating a drain capacitance reduction by factors of 12 and 13 compared to CSD operation, respectively. This underscores the adaptability of the ASD concept and highlights its equal efficiency across different material platforms. Moreover, we achieved charge sensing operation with the ASD on a DQD, obtaining a large output voltage swing of $\Delta U_D \approx 3\,\mathrm{mV}$. The significantly enhanced output signal establishes the ASD as a promising candidate for advancing the performance of the baseband readout approach in the context of scalable quantum computing.

As the last key aspect of this work, we presented one of the first devices fabricated in an industrial setting at Infineon Technologies Dresden's 200 mm production line as part of the QUASAR collaboration, the Industrial Demonstrator Device. It showcased its ability to efficiently tune a QD to the last electron, forming the foundation for spin qubits, while at the same time enabling state-of-the-art charge sensing for reliable readout of the electronic state. The tuning process of the IDD was remarkably straightforward, showcasing state-of-the-art charge noise, excellent stability, and high reproducibility across cool-downs and setups. Besides the excellent performance of the IDD, we proposed two design adjustments to further improve its tunability and performance in terms of charge sensing sensitivity and dot confinement. Additionally, we performed magnetospectroscopy measurements to gain access to the spin configuration in the few-electron regime as a function of the magnetic

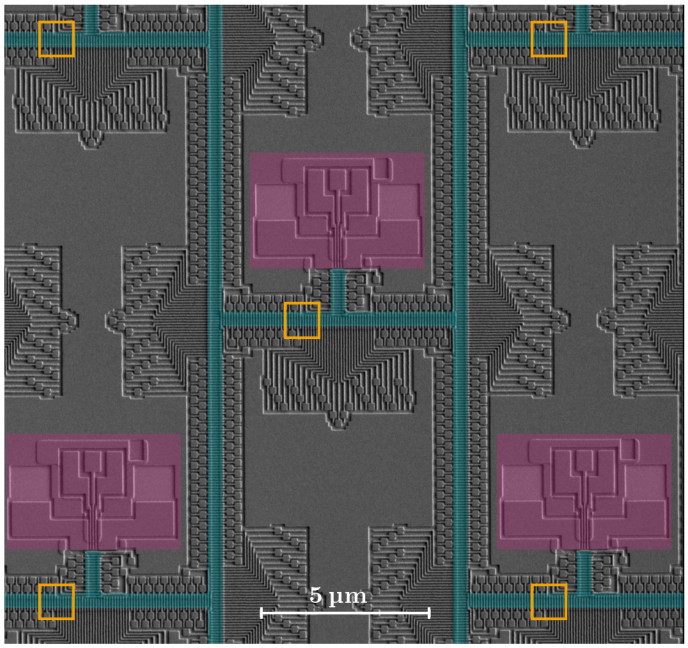

Figure 7.1: False-colored scanning electron image of an electron beam lithography test for the shuttling-based qubit architecture of the QUASAR project. The blue regions represent shuttling lanes, orange rectangles indicate manipulation zones, and pink areas mark the readout zones. The scanning electron image was taken by P. Muster at *Infineon Technologies Dresden*.

field and provided an estimate of a lower bound on the valley splitting, a crucial parameter for qubit operation. The IDD demonstrates the compatibility of heterostructure-based spin qubit devices with industrial CMOS technology, highlighting the potential of Si/SiGe spin qubits for rapid scalability and seamless integration of electronics on the same chip.
The next step, building on the promising IDD within our QUASAR consortium, which strives for a semiconductor quantum processor with a shuttling-based scalable architecture [29, 111], is to fabricate a complete spin qubit architecture. One of the first electron beam lithography tests for this architecture is shown in a false-colored scanning electron micrograph in Fig. 7.1. The design follows a sparse architecture approach that enables two-dimensional qubit connectivity via electron shuttling [30–32, 105] and supports the integration of classical electronics at cryogenic temperatures. The lanes of adjacent gates, highlighted in blue, serve as shuttling lanes that allow electrons, along with their spin information, to be moved across the chip. To accomplish this, every fourth gate is electrically connected, while four phase-shifted sinusoidal signals applied to the resulting gate sets enable the continuous translation of the electron within the QD. Since electrons can be shuttled across the device, dedicated zones for initialization/readout, and manipulation can be implemented. The initialization and readout zones consist of a sensor dot, corresponding reservoirs, and a micromagnet, with their positions highlighted

in pink. The manipulation zones, located where two individually controlled sections of the shuttling lane meet and complemented by micromagnets, enable single- and two-qubit gate operations. A detailed description of the individual components, operation concept, and scaling perspectives of the shuttling-based architecture, can be found in [29].
The IDD's successful device operation and its excellent performance make the implementation of this architecture promising in the near future. This allows leveraging the advantages of industrial fabrication as well as the manufacturing expertise for classical electronics in co-designing quantum and classical hardware. By scaling up to full architectures, the demand for device uniformity further increases, emphasizing the importance of a thorough selection of the FES as the fundamental device building block. Identifying the most suitable FES as a basis is crucial for further improving the operation of the architecture. A promising next step is transitioning from the commercially purchased benchmark wafer used for the IDD to heterostructures fabricated within the QUASAR consortium by our partner *IHP - Leibniz-Institut für innovative Mikroelektronik*. These heterostructures were identified in this thesis to exhibit lower disorder and overall improved transport properties, comparable to some of the best reported to date for qubit applications. The biased cooling effect, besides providing fundamental insights into electrostatics in the FES, can be leveraged in various ways depending on the specific region within this architecture as it enables shifting the operation window of individual gates and engineering trapped charges at the dielectric/heterostructure interface. Moreover, the ASD can be seamlessly incorporated into this architecture. The slightly increased space requirement compared to the CSD is accommodated by the dedicated readout zones and the sparse architecture, while also allowing the close integration of the baseband readout circuitry. This allows us to fully exploit the ASD concept within this architecture, benefiting from its drastically increased output voltage.
With scalable qubit architectures increasingly taking shape and continuous advancements in the field, the path toward fault-tolerant quantum computing is becoming increasingly tangible. As it continues to evolve, quantum computing could push the boundaries of science and computation, leading to groundbreaking technologies and ultimately offering deeper insights into the fundamental principles shaping our understanding of the physical world.

A Appendix

A.1 Addition to the Simulation of the Biased Cooling Effect

This section covers further details on the simulation of biased cooling, described in Sec. 4.5, presenting the simulated x- and y-component of the electric field within the QW plane.
Fig. A.1 illustrates the comparison of the electric field distribution within the QW plane below two gates with and without biased cooling for the x- and y-component. Gate 1 on the left serves as a reference without biased cooling, while gate 2 on the right represents the case with biased cooling. For negative biased cooling the comparison is depicted in Fig. A.1 a) and b) for the x- and y-component of the electric field, respectively. Fig. A.1 c) and d) illustrate the comparison for positive biased cooling for the x- and y-component of the electric field, correspondingly. It can be observed that, as for the electric potential V and the z-component of the electric field E_z, the spatial smearing increases for positive biased cooling and decreases for negative biased cooling compared to $U_{BC} = 0\,V$.

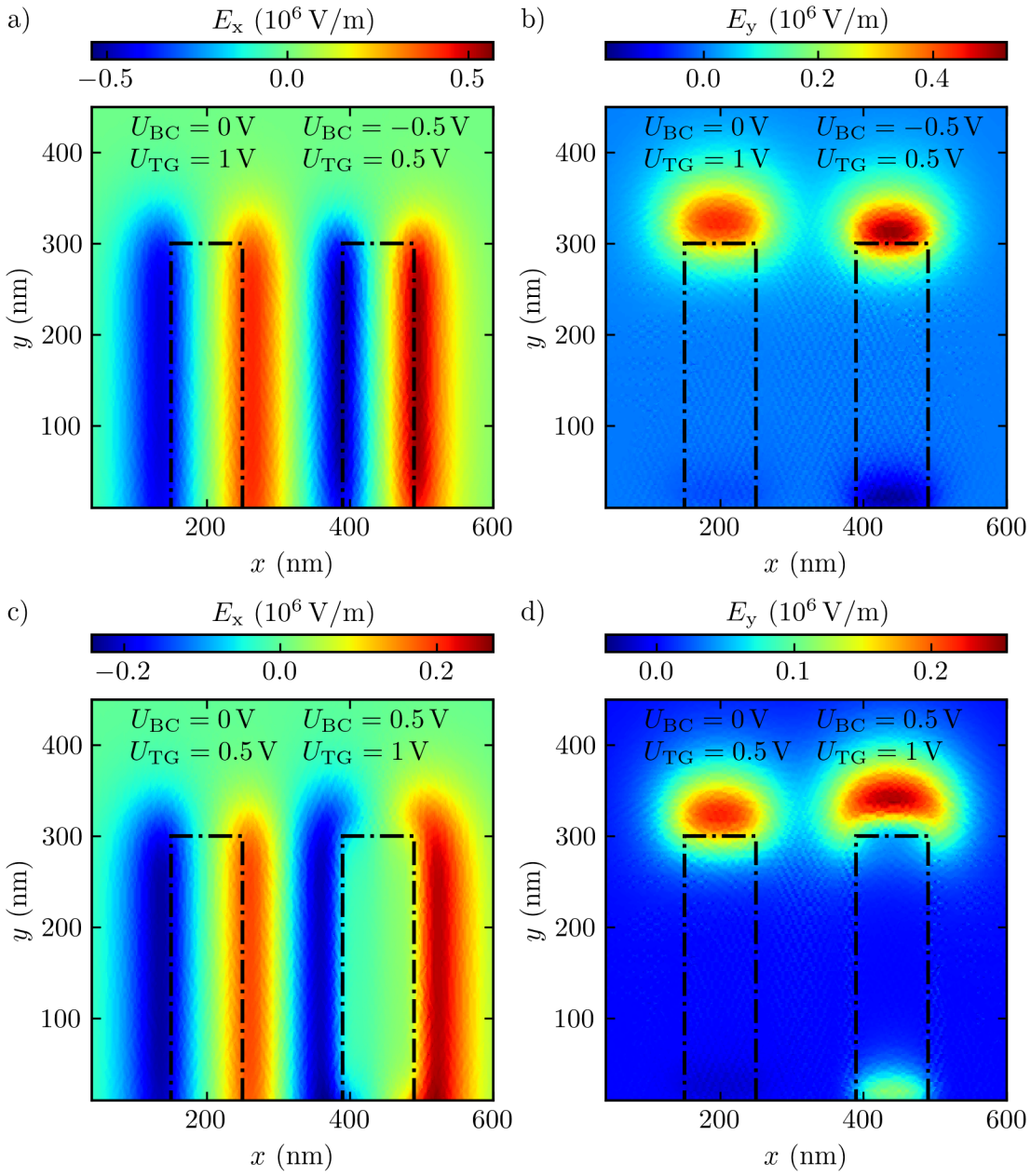

Figure A.1: Comparison of the simulated x and y-component of the electric field E within the QW plane below two gates with and without biased cooling. The black dash-dotted lines illustrate the gate positions on top of the FES. a), b) Negative biased cooling: Gate 1 (left) shows the reference case of $U_{BC} = 0$ V and a voltage of $U_{TG} = 1$ V applied. Gate 2 (right) is set to $U_{TG} = 0.5$ V and possesses a $\Delta\rho_{BC}$ at the SiOx/SiGe interface equivalent to $U_{BC} = -0.5$ V. The corresponding x- and y-component of the electric field are shown in panel a) and b), respectively. c), d) Positive biased cooling: Gate 1 shows the reference case of $U_{BC} = 0$ V and a voltage of $U_{TG} = 0.5$ V applied. Gate 2 is set to $U_{TG} = 1$ V and possesses a $\Delta\rho_{BC}$ at the SiOx/SiGe interface equivalent to $U_{BC} = 0.5$ V. The corresponding x- and y-component of the electric field are shown in panel c) and d), respectively.

A.2 ASD Tuning Details

This section provides an overview of the gate voltages applied at the ASD SiGe device during the Coulomb diamond measurement series presented in Fig. 5.5 tuning the sensor dot from a symmetric to an asymmetric configuration described in Sec. 5.2.
Fig. A.2 presents a false-colored scanning microscope electron image of a device fabricated in the same manner as the ASD SiGe device illustrating the gate layout with corresponding gate names. A global gate, referred to as TG, within the second gate layer and isolated by AlOx, is not shown. The gate voltages were kept constant during the Coulomb diamond measurement series, except for the voltages on gates SR and BLS, which were varied to tune the system from a symmetric to an asymmetric configuration as described in Sec. 5.2. The voltage U_{PS} and the drain voltage U_{D} applied at $\boxtimes_I$ were swept to measure the Coulomb diamonds (see Fig. 5.5). The voltages applied to the other gates, which remained constant, are listed in Tab. A.1.

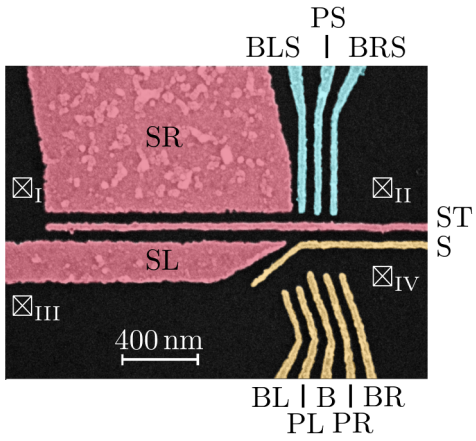

Figure A.2: False-colored scanning electron microscope image of a device fabricated in the same manner as the ASD SiGe device illustrating the gate layout with corresponding gate names. A global gate in a second gate layer named TG isolated by AlOx is not shown. The drain and source reservoirs are labeled $\boxtimes_{\mathrm{I}}$ and $\boxtimes_{\mathrm{II}}$ for the sensor current path and $\boxtimes_{\mathrm{III}}$ and $\boxtimes_{\mathrm{IV}}$ for the DQD current path.

Gate name	TG	BRS	ST	S	SL	BL	PL	B	PR	BR
Voltage (V)	0.45	0.25	0.55	-0.18	-0.05	-0.15	0.12	-0.24	0.12	-0.15

Table A.1: Device tuning details for the Coulomb diamond measurement series of the ASD SiGe device shown in Fig. 5.5 giving a gate voltage overview. The gate names are illustrated in Fig. A.2.

A.3 Device Overview

An overview of the wafer and device fabrication details for all devices discussed in this thesis is presented in this section. Tab. A.2 lists the device names used in this thesis alongside their internal device names, wafer names, and the facilities responsible for wafer growth and device fabrication, as well as details related to the fabrication process.

Device Name	Wafer Name	Internal Device Name	Wafer Growth	Fabrication	Fabrication Recipe
FES A	SJZ397#1#B W5	Mitte1	IHP	IHP	proprietary to IHP
FES B	R2175	A2	UR	UR	see [79]
FES C	R2151	D3	UR	UR	see [79]
FES D	SJZ411#1#C W9	X14-2	IHP	IHP	proprietary to IHP
FES E	4840R	LR1	LSRL	UR	see [79]
ASD SiGe	R2164	P83A3	UR	RWTH	see [83]
ASD GaAs	B14722	ASD04	Ruhr-Universität Bochum	RWTH	see [83]
Hero	5568 W13	QW-Accu3 G1 W13 Hero Device	LSRL	Infineon Technologies Dresden	see [107]

Table A.2: Overview of the wafer and device fabrication details of the presented devices. The abbreviation UR stands for *Universität Regensburg*, IHP for *IHP - Leibniz-Institut für Innovative Mikroelektronik*, RWTH for *Rheinisch-Westfälische Technische Hochschule Aachen* and LSRL for *Lawrence Semiconductors Research Labs*.

Bibliography

[1] M. Born and P. Jordan, *Zur Quantenmechanik*, Z. Physik **34**, 858 (1925).

[2] W. Heisenberg, *Über quantentheoretische Umdeutung kinematischer und mechanischer Beziehungen*, Z. Physik **33**, 879 (1925).

[3] P. A. M. Dirac, *The fundamental equations of quantum mechanics*, Proc. R. Soc. Lond. A **109**, 642 (1925).

[4] M. Born, W. Heisenberg, and P. Jordan, *Zur Quantenmechanik. II*, Z. Physik **35**, 557 (1926).

[5] R. P. Feynman, *Simulating physics with computers*, Int. J. Theor. Phys. **21**, 467 (1982).

[6] D. Deutsch and R. Jozsa, *Rapid solution of problems by quantum computation*, Proc. R. Soc. Lond. A **439**, 553 (1992).

[7] L. K. Grover, *A fast quantum mechanical algorithm for database search*, STOC'96: Proceedings of the twenty-eighth annual ACM symposium on Theory of Computing, 212 (1996).

[8] P. W. Shor, *Polynomial-time algorithms for prime factorization and discrete logarithms on a quantum computer*, SIAM J. Comput. **26**, 1484 (1997).

[9] D. P. DiVincenzo, *The physical implementation of quantum computation*, Fortschr. Phys. **48**, 771 (2000).

[10] T. D. Ladd, F. Jelezko, R. Laflamme, Y. Nakamura, C. Monroe, and J. L. O'Brien, *Quantum computers*, Nature **464**, 45 (2010).

[11] N. P. de Leon, K. M. Itoh, D. Kim, K. K. Mehta, T. E. Northup, H. Paik, B. S. Palmer, N. Samarth, S. Sangtawesin, and D. W. Steuerman, *Materials challenges and opportunities for quantum computing hardware*, Science **372**, 253 (2021).

[12] K. Flensberg, F. von Oppen, and A. Stern, *Engineered platforms for topological superconductivity and Majorana zero modes*, Nat. Rev. Mater. **6**, 944 (2021).

[13] B. M. Terhal, *Quantum error correction for quantum memories*, Rev. Mod. Phys. **87**, 307 (2015).

[14] D. Loss and D. P. DiVincenzo, *Quantum computation with quantum dots*, Phys. Rev. A **57**, 120 (1998).

[15] C. B. Simmons, J. R. Prance, B. J. van Bael, T. S. Koh, Z. Shi, D. E. Savage, M. G. Lagally, R. Joynt, M. Friesen, S. N. Coppersmith, and M. A. Eriksson, *Tunable spin loading and T_1 of a silicon spin qubit measured by single-shot readout*, Phys. Rev. Lett. **106**, 156804 (2011).

[16] A. Hollmann, T. Struck, V. Langrock, A. Schmidbauer, F. Schauer, T. Leonhardt, K. Sawano, H. Riemann, N. V. Abrosimov, D. Bougeard, and L. R. Schreiber, *Large, tunable valley splitting and single-spin relaxation mechanisms in a Si/Si$_x$Ge$_{1-x}$ quantum dot*, Phys. Rev. Appl. **13**, 034068 (2020).

[17] J. Yoneda, K. Takeda, T. Otsuka, T. Nakajima, M. R. Delbecq, G. Allison, T. Honda, T. Kodera, S. Oda, Y. Hoshi, N. Usami, K. M. Itoh, and S. Tarucha, *A quantum-dot spin qubit with coherence limited by charge noise and fidelity higher than 99.9 %*, Nature Nanotech. **13**, 102 (2018).

[18] T. Struck, A. Hollmann, F. Schauer, O. Fedorets, A. Schmidbauer, K. Sawano, H. Riemann, N. V. Abrosimov, Ł. Cywiński, D. Bougeard, and L. R. Schreiber, *Low-frequency spin qubit energy splitting noise in highly purified ^{28}Si/SiGe*, npj Quantum Inf. **6**, 40 (2020).

[19] A. R. Mills, C. R. Guinn, M. J. Gullans, A. J. Sigillito, M. M. Feldman, E. Nielsen, and J. R. Petta, *Two-qubit silicon quantum processor with operation fidelity exceeding 99 %*, Sci. Adv. **8**, eabn5130 (2022).

[20] L. Petit, M. Russ, G. H. G. J. Eenink, W. I. L. Lawrie, J. S. Clarke, L. M. K. Vandersypen, and M. Veldhorst, *Design and integration of single-qubit rotations and two-qubit gates in silicon above one kelvin*, Commun. Mater. **3**, 82 (2022).

[21] X. Xue, M. Russ, N. Samkharadze, B. Undseth, A. Sammak, G. Scappucci, and L. M. K. Vandersypen, *Quantum logic with spin qubits crossing the surface code threshold*, Nature **601**, 343 (2022).

[22] A. Noiri, K. Takeda, T. Nakajima, T. Kobayashi, A. Sammak, G. Scappucci, and S. Tarucha, *Fast universal quantum gate above the fault-tolerance threshold in silicon*, Nature **601**, 338 (2022).

[23] S. G. J. Philips, M. T. Mądzik, S. V. Amitonov, S. L. de Snoo, M. Russ, N. Kalhor, C. Volk, W. I. L. Lawrie, D. Brousse, L. Tryputen, B. P. Wuetz, A. Sammak, M. Veldhorst, G. Scappucci, and L. M. K. Vandersypen, *Universal control of a six-qubit quantum processor in silicon*, Nature **609**, 919 (2022).

[24] H. C. George, M. T. Mądzik, E. M. Henry, A. J. Wagner, M. M. Islam, F. Borjans, E. J. Connors, J. Corrigan, M. Curry, M. K. Harper, D. Keith, L. Lampert, F. Luthi, F. A. Mohiyaddin, S. Murcia, R. Nair, R. Nahm, A. Nethwewala, S. Neyens, B. Patra, R. D. Raharjo, C. Rogan, R. Savytskyy, T. F. Watson, J. Ziegler, O. K. Zietz, S. Pellerano, R. Pillarisetty, N. C. Bishop, S. A. Bojarski, J. Roberts, and J. S. Clarke, *12-spin-qubit arrays fabricated on a 300 mm semiconductor manufacturing line*, Nano Lett. **25**, 793 (2025).

[25] L. M. K. Vandersypen, H. Bluhm, J. S. Clarke, A. S. Dzurak, R. Ishihara, A. Morello, D. J. Reilly, L. R. Schreiber, and M. Veldhorst, *Interfacing spin qubits in quantum dots and donors – hot, dense, and coherent*, npj Quantum Information **3**, 34 (2017).

[26] M. Veldhorst, H. G. J. Eenink, C. H. Yang, and A. S. Dzurak, *Silicon CMOS architecture for a spin-based quantum computer*, Nat. Commun. **8**, 1766 (2017).

[27] F. Borsoi, N. W. H., V. John, M. Meyer, S. Motz, F. van Riggelen, A. Sammak, S. L. de Snoo, G. Scappucci, and M. Veldhorst, *Shared control of a 16 semiconductor quantum dot crossbar array*, Nature nanotechnology **19**, 21 (2024).

[28] J. M. Boter, J. P. Dehollain, J. P. van Dijk, Y. Xu, T. Hensgens, R. Versluis, H. W. Naus, J. S. Clarke, M. Veldhorst, F. Sebastiano, and L. M. Vandersypen, *Spiderweb array: a sparse spin-qubit array*, Phys. Rev. Applied **18**, 024053 (2022).

[29] M. Künne, A. Willmes, M. Oberländer, C. Gorjaew, J. D. Teske, H. Bhardwaj, M. Beer, E. Kammerloher, R. Otten, I. Seidler, R. Xue, L. R. Schreiber, and H. Bluhm, *The SpinBus architecture for scaling spin qubits with electron shuttling*, Nat. Commun. **15**, 4977 (2024).

[30] I. Seidler, T. Struck, R. Xue, N. Focke, S. Trellenkamp, H. Bluhm, and L. R. Schreiber, *Conveyor-mode single-electron shuttling in Si/SiGe for a scalable quantum computing architecture*, npj Quantum Inf. **8**, 100 (2022).

[31] R. Xue, M. Beer, I. Seidler, S. Humpohl, J.-S. Tu, S. Trellenkamp, T. Struck, H. Bluhm, and L. R. Schreiber, *Si/SiGe qubus for single electron information-processing devices with memory and micron-scale connectivity function*, Nat. Commun. **15**, 2296 (2024).

[32] T. Struck, M. Volmer, L. Visser, T. Offermann, R. Xue, J.-S. Tu, S. Trellenkamp, Ł. Cywiński, H. Bluhm, and L. R. Schreiber, *Spin-EPR-pair separation by conveyor-mode single electron shuttling in Si/SiGe*, Nat. Commun. **15**, 1325 (2024).

[33] F. Schäffler, *High-mobility Si and Ge structures*, Semicond. Sci. Technol. **12**, 1515 (1997).

[34] M. P. Losert, M. A. Eriksson, R. Joynt, R. Rahman, G. Scappucci, S. N. Coppersmith, and M. Friesen, *Practical strategies for enhancing the valley splitting in Si/SiGe quantum wells*, Phys. Rev. B **108**, 125405 (2023).

[35] J. Klos, J. Tröger, J. Keutgen, M. P. Losert, N. V. Abrosimov, J. Knoch, H. Bracht, S. N. Coppersmith, M. Friesen, O. Cojocaru-Mirédin, L. R. Schreiber, and D. Bougeard, *Atomistic compositional details and their importance for spin qubits in isotope-purified silicon quantum wells*, Adv. Sci. **11**, 2407442 (2024).

[36] M. Volmer, T. Struck, A. Sala, B. Chen, M. Oberländer, T. Offermann, R. Xue, L. Visser, J.-S. Tu, S. Trellenkamp, Ł. Cywiński, H. Bluhm, and L. R. Schreiber, *Mapping of valley splitting by conveyor-mode spin-coherent electron shuttling*, npj Quantum Inf. **10**, 61 (2024).

[37] V. Lang, *Characterisation of two-dimensional electron systems in natural and isotopically pure Si/SiGe heterostructures*, Diploma Thesis (Ludwig-Maximilian-Universität München, 2008).

[38] S.-H. Huang, T.-M. Lu, S.-C. Lu, C.-H. Lee, C. W. Liu, and D. C. Tsui, *Mobility enhancement of strained Si by optimized SiGe/Si/SiGe structures*, Appl. Phys. Lett. **101**, 042111 (2012).

[39] A. Wild, J. Sailer, J. Nützel, G. Abstreiter, S. Ludwig, and D. Bougeard, *Electrostatically defined quantum dots in a Si/SiGe heterostructure*, New J. Phys. **12**, 113019 (2010).

[40] A. Wild, *Development of robust spin qubits in SiGe heterostructures*, Doctoral Thesis (Technische Universität München, 2013).

[41] A. Wild, J. Kierig, J. Sailer, J. W. Ager, E. E. Haller, G. Abstreiter, S. Ludwig, and D. Bougeard, *Few electron double quantum dot in an isotopically purified ^{28}Si quantum well*, Appl. Phys. Lett. **100**, 143110 (2012).

[42] B. M. Maune, M. G. Borselli, B. Huang, T. D. Ladd, P. W. Deelman, K. S. Holabird, A. A. Kiselev, I. Alvarado-Rodriguez, R. S. Ross, A. E. Schmitz, M. Sokolich, C. A. Watson, M. F. Gyure, and A. T. Hunter, *Coherent singlet-triplet oscillations in a silicon-based double quantum dot*, Nature **481**, 344 (2012).

[43] T. M. Lu, J. Liu, J. Kim, K. Lai, D. C. Tsui, and Y. H. Xie, *Capacitively induced high mobility two-dimensional electron gas in undoped Si/$Si_{1-x}Ge_x$ heterostructures with atomic-layer-deposited dielectric*, Appl. Phys. Lett. **90**, 182114 (2007).

[44] M. Y. Melnikov, A. A. Shashkin, V. T. Dolgopolov, S.-H. Huang, C. W. Liu, and S. V. Kravchenko, *Ultra-high mobility two-dimensional electron gas in a SiGe/Si/SiGe quantum well*, Appl. Phys. Lett. **106**, 092102 (2015).

[45] K. Lai, W. Pan, D. C. Tsui, S. Lyon, M. Mühlberger, and F. Schäffler, *Linear temperature dependence of the conductivity in Si two-dimensional electrons near the apparent metal-to-insulator transition*, Phys. Rev. B **75**, 033314 (2007).

[46] L. A. Tracy, E. H. Hwang, K. Eng, G. A. ten Eyck, E. P. Nordberg, K. Childs, M. S. Carroll, M. P. Lilly, and S. Das Sarma, *Observation of percolation-induced two-dimensional metal-insulator transition in a Si MOSFET*, Phys. Rev. B **79**, 235307 (2009).

[47] X. Mi, T. M. Hazard, C. Payette, K. Wang, D. M. Zajac, J. V. Cady, and J. R. Petta, *Magnetotransport studies of mobility limiting mechanisms in undoped Si/SiGe heterostructures*, Phys. Rev. B **92**, 035304 (2015).

[48] Y. Huang and S. Das Sarma, *Understanding disorder in silicon quantum computing platforms: scattering mechanisms in Si/SiGe quantum wells*, Phys. Rev. B **109**, 125405 (2024).

[49] T. M. Lu, C.-H. Lee, S.-H. Huang, D. C. Tsui, and C. W. Liu, *Upper limit of two-dimensional electron density in enhancement-mode Si/SiGe heterostructure field-effect transistors*, Appl. Phys. Lett. **99**, 153510 (2011).

[50] C.-T. Huang, J.-Y. Li, K. S. Chou, and J. C. Sturm, *Screening of remote charge scattering sites from the oxide/silicon interface of strained Si two-dimensional electron gases by an intermediate tunable shielding electron layer*, Appl. Phys. Lett. **104**, 243510 (2014).

[51] D. Laroche, S.-H. Huang, E. Nielsen, Y. Chuang, J.-Y. Li, C. W. Liu, and T. M. Lu, *Scattering mechanisms in shallow undoped Si/SiGe quantum wells*, AIP Adv. **5**, 107106 (2015).

[52] Y.-H. Su, K.-Y. Chou, Y. Chuang, T.-M. Lu, and J.-Y. Li, *Electron mobility enhancement in an undoped Si/SiGe heterostructure by remote carrier screening*, J. Appl. Phys. **125**, 235705 (2019).

[53] T. Ihn, *Semiconductor nanostructures: quantum states and electronic transport* (Oxford University Press, 2012).

[54] R. Gross and A. Marx, *Festkörperphysik* (De Gruyter, 2014).

[55] T. McJunkin, E. R. MacQuarrie, L. Tom, S. F. Neyens, J. P. Dodson, B. Thorgrimsson, J. Corrigan, H. E. Ercan, D. E. Savage, M. G. Lagally, R. Joynt, S. N. Coppersmith, M. Friesen, and M. A. Eriksson, *Valley splittings in Si/SiGe quantum dots with a germanium spike in the silicon well*, Phys. Rev. B **104**, 085406 (2021).

[56] A. Schmidbauer, *Evaluation of scalable gate architecture components for Si/SiGe spin qubits*, Doctoral Thesis (Universität Regensburg, 2024).

[57] R. Hanson, L. P. Kouwenhoven, J. R. Petta, S. Tarucha, and L. M. K. Vandersypen, *Spins in few-electron quantum dots*, Rev. Mod. Phys. **79**, 1217 (2007).

[58] A. Manchon, H. C. Koo, J. Nitta, S. M. Frolov, and R. A. Duine, *New perspectives for Rashba spin-orbit coupling*, Nature Mater. **14**, 871 (2015).

[59] G. Scappucci, C. Kloeffel, F. A. Zwanenburg, D. Loss, M. Myronov, J.-J. Zhang, S. de Franceschi, G. Katsaros, and M. Veldhorst, *The germanium quantum information route*, Nat. Rev. Mater. **6**, 926 (2021).

[60] D. Thureja, A. Imamoglu, T. Smoleński, I. Amelio, A. Popert, T. Chervy, X. Lu, S. Liu, K. Barmak, K. Watanabe, T. Taniguchi, D. J. Norris, M. Kroner, and P. A. Murthy, *Electrically tunable quantum confinement of neutral excitons*, Nature **606**, 298 (2022).

[61] D. Degli Esposti, B. Paquelet Wuetz, V. Fezzi, M. Lodari, A. Sammak, and G. Scappucci, *Wafer-scale low-disorder 2DEG in ^{28}Si/SiGe without an epitaxial Si cap*, Appl. Phys. Lett. **120**, 184003 (2022).

[62] B. P. Wuetz, D. Degli Esposti, A. M. J. Zwerver, S. V. Amitonov, M. Botifoll, J. Arbiol, A. Sammak, L. M. K. Vandersypen, M. Russ, and G. Scappucci, *Reducing charge noise in quantum dots by using thin silicon quantum wells*, Nat. Commun. **14**, 1385 (2023).

[63] D. Degli Esposti, L. E. A. Stehouwer, Ö. Gül, N. Samkharadze, C. Déprez, M. Meyer, I. N. Meijer, L. Tryputen, S. Karwal, M. Botifoll, J. Arbiol, S. V. Amitonov, L. M. K. Vandersypen, A. Sammak, M. Veldhorst, and G. Scappucci, *Low disorder and high valley splitting in silicon*, npj Quantum Inf. **10**, 32 (2024).

[64] L. Kranz, S. K. Gorman, B. Thorgrimsson, Y. He, D. Keith, J. G. Keizer, and M. Y. Simmons, *Exploiting a single-crystal environment to minimize the charge noise on qubits in silicon*, Adv. Mater. **32**, 2003361 (2020).

[65] L. Massai, B. Hetényi, M. Mergenthaler, F. J. Schupp, L. Sommer, S. Paredes, S. W. Bedell, P. Harvey-Collard, G. Salis, A. Fuhrer, and N. W. Hendrickx, *Impact of interface traps on charge noise and low-density transport properties in Ge/SiGe heterostructures*, Commun. Mater. **5**, 151 (2024).

[66] M. Meyer, C. Déprez, T. R. van Abswoude, I. N. Meijer, D. Liu, C.-A. Wang, S. Karwal, S. Oosterhout, F. Borsoi, A. Sammak, N. W. Hendrickx, G. Scappucci, and M. Veldhorst, *Electrical control of uniformity in quantum dot devices*, Nano Lett. **23**, 2522 (2023).

[67] J. Sailer, A. Wild, V. Lang, A. Siddiki, and D. Bougeard, *Quantum Hall resistance overshoot in two-dimensional (2D) electron gases: theory and experiment*, New J. Phys. **12**, 113033 (2010).

[68] Y.-H. Su, Y. Chuang, C.-Y. Liu, J.-Y. Li, and T.-M. Lu, *Effects of surface tunneling of two-dimensional hole gases in undoped Ge/GeSi heterostructures*, Phys. Rev. Mater. **1**, 044601 (2017).

[69] E. J. Connors, J. J. Nelson, H. Qiao, L. F. Edge, and J. M. Nichol, *Low-frequency charge noise in Si/SiGe quantum dots*, Phys. Rev. B **100**, 165305 (2019).

[70] M. Prager, M. Trottmann, J. Schmidt, L. Ebnet, D. Schuh, and D. Bougeard, *Gating of two-dimensional electron systems in (In,Ga)As/(In,Al)As heterostructures: the role of intrinsic (In,Al)As deep donor defects*, Phys. Rev. Appl. **16**, 064028 (2021).

[71] A. R. Long, J. H. Davies, Kinsler, M., Vallis, S., and M. C. Holland, *A simple model for the characteristics of GaAs/AlGaAs modulation-doped devices*, Semicond. Sci. Technol. **8**, 1581 (1993).

[72] E. Buks, M. Heiblum, and H. Shtrikman, *Correlated charged donors and strong mobility enhancement in a two-dimensional electron gas*, Phys. Rev. B **49**, 14790 (1994).

[73] E. Buks, M. Heiblum, Y. Levinson, and H. Shtrikman, *Scattering of a two-dimensional electron gas by a correlated system of ionized donors*, Semicond. Sci. Technol. **9**, 2031 (1994).

[74] P. T. Coleridge, *Correlation lengths for scattering potentials in two-dimensional electron gases*, Semicond. Sci. Technol. **12**, 22 (1997).

[75] M. Pioro-Ladrière, J. H. Davies, A. R. Long, A. S. Sachrajda, L. Gaudreau, P. Zawadzki, J. Lapointe, J. Gupta, Z. Wasilewski, and S. Studenikin, *Origin of switching noise in GaAs/$Al_xGa_{1-x}As$ lateral gated devices*, Phys. Rev. B **72**, 115331 (2005).

[76] C. Buizert, F. H. L. Koppens, M. Pioro-Ladriére, H.-P. Tranitz, I. T. Vink, S. Tarucha, W. Wegscheider, and L. M. K. Vandersypen, *In situ reduction of charge noise in GaAs/$Al_xGa_{1-x}As$ Schottky-gated devices*, Phys. Rev. Lett. **101**, 226603 (2008).

[77] E. Kammerloher, *Improving the output signal of charge readout for quantum computing in electrostatically defined quantum dots with a new sensing dot concept*, Doctoral Thesis (RWTH Aachen University, 2021).

[78] J. Ferrero, T. Koch, S. Vogel, D. Schroller, V. Adam, R. Xue, I. Seidler, L. R. Schreiber, H. Bluhm, and W. Wernsdorfer, *Noise reduction by bias cooling in gated Si/Si_xGe_{1-x} quantum dots*, Appl. Phys. Lett. **124**, 204002 (2024).

[79] L. Zinkl, *Biased cooling studies in undoped Si/SiGe field-effect devices for quantum circuits*, Master's Thesis (Universität Regensburg, 2024).

[80] L. K. Diebel, L. G. Zinkl, A. Hötzinger, F. Reichmann, M. Lisker, Y. Yamamoto, and D. Bougeard, *Impact of biased cooling on the operation of undoped silicon quantum well field-effect devices for quantum circuit applications*, arXiv:2408.14844 (2024).

[81] L. K. Diebel, L. G. Zinkl, A. Hötzinger, F. Reichmann, M. Lisker, Y. Yamamoto, and D. Bougeard, *Impact of biased cooling on the operation of undoped silicon quantum well field-effect devices*, AIP Adv. **15**, 035301 (2025).

[82] M. Meyer, C. Déprez, I. N. Meijer, F. K. Unseld, S. Karwal, A. Sammak, G. Scappucci, L. M. K. Vandersypen, and M. Veldhorst, *Single-electron occupation in quantum dot arrays at selectable plunger gate voltage*, Nano Lett. **23**, 11593 (2023).

[83] E. Kammerloher, A. Schmidbauer, L. Diebel, I. Seidler, M. Neul, M. Künne, A. Ludwig, J. Ritzmann, A. Wieck, D. Bougeard, L. R. Schreiber, and H. Bluhm, *Sensing dot with high output swing for scalable baseband readout of spin qubits*, Phys. Rev. Appl. **22**, 024044 (2024).

[84] J. R. Petta, A. C. Johnson, J. M. Taylor, E. A. Laird, A. Yacoby, M. D. Lukin, C. M. Marcus, M. P. Hanson, and A. C. Gossard, *Coherent manipulation of coupled electron spins in semiconductor quantum dots*, Science **309**, 2180 (2005).

[85] A. C. Johnson, J. R. Petta, C. M. Marcus, M. P. Hanson, and A. C. Gossard, *Singlet-triplet spin blockade and charge sensing in a few-electron double quantum dot*, Phys. Rev. B **72**, 165308 (2005).

[86] J. M. Elzerman, R. Hanson, L. H. van Willems Beveren, B. Witkamp, L. M. K. Vandersypen, and L. P. Kouwenhoven, *Single-shot read-out of an individual electron spin in a quantum dot*, Nature **430**, 431 (2004).

[87] B. J. van Wees, H. van Houten, C. W. Beenakker, J. G. Williamson, L. P. Kouwenhoven, D. van der Marel, and C. T. Foxon, *Quantized conductance of point contacts in a two-dimensional electron gas*, Phys. Rev. Lett. **60**, 848 (1988).

[88] M. Field, C. G. Smith, M. Pepper, Da Ritchie, J. E. Frost, G. A. Jones, and D. G. Hasko, *Measurements of Coulomb blockade with a noninvasive voltage probe*, Phys. Rev. Lett. **70**, 1311 (1993).

[89] M. A. Kastner, *The single-electron transistor*, Rev. Mod. Phys. **64**, 849 (1992).

[90] R. J. Schoelkopf, P. Wahlgren, A. A. Kozhevnikov, P. Delsing, and Prober, *The radio-frequency single-electron transistor (RF-SET): A fast and ultrasensitive electrometer*, Science **280**, 1238 (1998).

[91] D. J. Reilly, C. M. Marcus, M. P. Hanson, and A. C. Gossard, *Fast single-charge sensing with a rf quantum point contact*, Appl. Phys. Lett. **91**, 162101 (2007).

[92] J. I. Colless, A. C. Mahoney, J. M. Hornibrook, A. C. Doherty, H. Lu, A. C. Gossard, and D. J. Reilly, *Dispersive readout of a few-electron double quantum dot with fast RF gate sensors*, Phys. Rev. Lett. **110**, 046805 (2013).

[93] G. Zheng, N. Samkharadze, M. L. Noordam, N. Kalhor, D. Brousse, A. Sammak, G. Scappucci, and L. M. K. Vandersypen, *Rapid gate-based spin read-out in silicon using an on-chip resonator*, Nat. Nanotechnol. **14**, 742 (2019).

[94] I. Seidler, M. Neul, E. Kammerloher, M. Künne, A. Schmidbauer, L. K. Diebel, A. Ludwig, J. Ritzmann, A. D. Wieck, D. Bougeard, H. Bluhm, and L. R. Schreiber, *Tailoring potentials by simulation-aided design of gate layouts for spin-qubit applications*, Phys. Rev. Appl. **20**, 044058 (2023).

[95] H. Akima, *A New method of interpolation and smooth curve fitting based on local procedures*, J. ACM **17**, 589 (1970).

[96] H. Akima, *Bivariate interpolation and smooth surface fitting based on local procedures*, Commun. ACM **17**, 26 (1974).

[97] Z. Shi, C. B. Simmons, J. R. Prance, J. King Gamble, M. Friesen, D. E. Savage, M. G. Lagally, S. N. Coppersmith, and M. A. Eriksson, *Tunable singlet-triplet splitting in a few-electron Si/SiGe quantum dot*, Appl. Phys. Lett. **99**, 233108 (2011).

[98] M. G. Borselli, R. S. Ross, A. A. Kiselev, E. T. Croke, K. S. Holabird, P. W. Deelman, L. D. Warren, I. Alvarado-Rodriguez, I. Milosavljevic, F. C. Ku, W. S. Wong, A. E. Schmitz, M. Sokolich, M. F. Gyure, and A. T. Hunter, *Measurement of valley splitting in high-symmetry Si/SiGe quantum dots*, Appl. Phys. Lett. **98**, 123118 (2011).

[99] D. M. Zajac, T. M. Hazard, X. Mi, K. Wang, and J. R. Petta, *A reconfigurable gate architecture for Si/SiGe quantum dots*, Appl. Phys. Lett. **106**, 223507 (2015).

[100] B. Paquelet Wuetz, M. P. Losert, S. Koelling, L. E. A. Stehouwer, A.-M. J. Zwerver, S. G. J. Philips, M. T. Mądzik, X. Xue, G. Zheng, M. Lodari, S. V. Amitonov, N. Samkharadze, A. Sammak, L. M. K. Vandersypen, R. Rahman, S. N. Coppersmith, O. Moutanabbir, M. Friesen, and G. Scappucci, *Atomic fluctuations lifting the energy degeneracy in Si/SiGe quantum dots*, Nat. Commun. **13**, 7730 (2022).

[101] E. H. Chen, K. Raach, A. Pan, A. A. Kiselev, E. Acuna, J. Z. Blumoff, T. Brecht, M. D. Choi, W. Ha, D. R. Hulbert, M. P. Jura, T. E. Keating, R. Noah, B. Sun, B. J. Thomas, M. G. Borselli, C. Jackson, M. T. Rakher, and R. S. Ross, *Detuning axis pulsed spectroscopy of valley-orbital states in Si/SiGe quantum dots*, Phys. Rev. Appl. **15**, 044033 (2021).

[102] D. Culcer, Ł. Cywiński, Q. Li, X. Hu, and S. Das Sarma, *Quantum dot spin qubits in silicon: multivalley physics*, Phys. Rev. B **82**, 155312 (2010).

[103] P. Huang and X. Hu, *Spin relaxation in a Si quantum dot due to spin-valley mixing*, Phys. Rev. B **90**, 235315 (2014).

[104] M. L. V. Tagliaferri, P. L. Bavdaz, W. Huang, A. S. Dzurak, D. Culcer, and M. Veldhorst, *Impact of valley phase and splitting on readout of silicon spin qubits*, Phys. Rev. B **97**, 245412 (2018).

[105] V. Langrock, J. A. Krzywda, N. Focke, I. Seidler, L. R. Schreiber, and Ł. Cywiński, *Blueprint of a scalable spin qubit shuttle device for coherent mid-range qubit transfer in disordered Si/SiGe/SiO_2*, PRX Quantum **4**, 020305 (2023).

[106] V. Stieß, *Few-electron spin qubit device tuning in academic cleanroom and industrially produced Si/SiGe quantum circuits*, Master's Thesis (Universität Regensburg, 2024).

[107] T. Huckemann, P. Muster, W. Langheinrich, V. Brackmann, M. Friedrich, N. D. Komerički, L. K. Diebel, V. Stieß, D. Bougeard, C. Dahl, L. R. Schreiber, and H. Bluhm, *Industrially fabricated single-electron quantum dots in Si/Si-Ge heterostructures*, arXiv: 2410.16913 (2024).

[108] R. C. C. Leon, C. H. Yang, J. C. C. Hwang, J. C. Lemyre, T. Tanttu, W. Huang, K. W. Chan, K. Y. Tan, F. E. Hudson, K. M. Itoh, A. Morello, A. Laucht, M. Pioro-Ladrière, A. Saraiva, and A. S. Dzurak, *Coherent spin control of s-, p-, d- and f-electrons in a silicon quantum dot*, Nat. Commun. **11**, 797 (2020).

[109] L. P. Kouwenhoven, D. G. Austing, and S. Tarucha, *Few-electron quantum dots*, Rep. Prog. Phys. **64**, 701 (2001).

[110] J. P. Dodson, H. E. Ercan, J. Corrigan, M. P. Losert, N. Holman, T. McJunkin, L. F. Edge, M. Friesen, S. N. Coppersmith, and M. A. Eriksson, *How valley-orbit states in silicon quantum dots probe quantum well interfaces*, Phys. Rev. Lett. **128**, 146802 (2022).

[111] F. Ginzel, M. Fellner, C. Ertler, L. R. Schreiber, H. Bluhm, and W. Lechner, *Scalable parity architecture with a shuttling-based spin qubit processor*, Phys. Rev.B **110**, 075302 (2024).

List of Publications

9. **L. K. Diebel**, L. G. Zinkl, A. Hötzinger, F. Reichmann, M. Lisker, Y. Yamamoto, and D. Bougeard
Impact of biased cooling on the operation of undoped silicon quantum well field-effect devices
AIP Advances **15**, 035301 (2025)

8. T. Huckemann, P. Muster, W. Langheinrich, V. Brackmann, M. Friedrich, N. D. Komerički, **L. K. Diebel**, V. Stieß, D. Bougeard, C. Dahl, L. R. Schreiber, and H. Bluhm
Industrially fabricated single-electron quantum dots in Si/Si-Ge heterostructures
IEEE Electron Device Letters, under review (arXiv:2410.16913) (2024)

7. E. Kammerloher, A. Schmidbauer, **L. Diebel**, I. Seidler, M. Neul, M. Künne, A. Ludwig, J. Ritzmann, A. Wieck, D. Bougeard, L. R. Schreiber, and H. Bluhm
Sensing dot with high output swing for scalable baseband readout of spin qubits
Physical Review Applied **22**, 024044 (2024)

6. M. Neul, I. V. Sprave, **L. K. Diebel**, L. G. Zinkl, F. Fuchs, Y. Yamamoto, C. Vedder, D. Bougeard, and L. R. Schreiber
Local laser-induced solid-phase recrystallization of phosphorus-implanted Si/SiGe heterostructures for contacts below 4.2 K
Physical Review Materials **8**, 043801 (2024)

5. J. Mornhinweg, **L. Diebel**, M. Halbhuber, M. Prager, J. Riepl, T. Inzenhofer, D. Bougeard, R. Huber, and C. Lange
Mode-multiplexing deep-strong light-matter coupling
Nature Communications **15**, 1847 (2024)

4. J. Mornhinweg, **L. Diebel**, M. Halbhuber, J. Riepl, E. Cortese, S. De Liberato, D. Bougeard, R. Huber, and C. Lange
Sculpting ultrastrong light-matter coupling through spatial matter structuring
Nanophotonics **13**, 1909 (2024)

3. I. Seidler, M. Neul, E. Kammerloher, M. Künne, A. Schmidbauer, **L. K. Diebel**, A. Ludwig, J. Ritzmann, A. D. Wieck, D. Bougeard, H. Bluhm, and L. R. Schreiber
Tailoring potentials by simulation-aided design of gate Layouts for spin qubit applications
Physical Review Applied **20**, 044058 (2023)

2. J. Raab, F. P. Mezzapesa, L. Viti, N. Dessmann, **L. K. Diebel**, L. Li, A. G. Davies, E. H. Linfield, C. Lange, R. Huber, and M. S. Vitiello
Ultrafast terahertz saturable absorbers using tailored intersubband polaritons
Nature Communications **11**, 4290 (2020)

1. G. B. Osterhoudt, **L. K. Diebel**, M. J. Gray, X. Yang, J. Stanco, X. Huang, B. Shen, N. Ni, P. J. W. Moll, Y. Ran, and K. S.Burch
Colossal Bulk Photovoltaic Effect in a Weyl Semimetal
Nature Materials **18**, 471 (2019)

Conference Proceedings

2. A. Mistroni, F. Reichmann, Y. Yamamoto, M. H. Zöllner, G. Capellini, **L. Diebel**, D. Bougeard, and M. Lisker
Low disorder and high mobility 2DEG in Si/SiGe fabricated in 200 mm BiCMOS pilot line
ECS Transactions **114**, 123 (2024)

1. F. Reichmann, A. Mistroni, Y. Yamamoto, P. Kulse, S. Marschmeyer, D. Wolansky, O. Fursenko, M. H. Zöllner, G. Capellini, **L. Diebel**, D. Bougeard, and M. Lisker
Advancing Si spin qubit research: process integration of Hall bar FETs on Si/SiGe in a 200 mm BiCMOS pilot line
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Laura Diebel