

FERMILAB-TM-2226

MCM II and the Trip chip

J. Estrada, C. Garcia, B. Hoeneisen and P. Rubinov

22 August 2002

DØ note 4009

Abstract

We describe the development of the electronics that will be used to read out the Fiber Tracker and Preshower detectors in Run IIb. This electronics is needed for operation at 132ns bunch crossing, and may provide a measurement of the z coordinate of the Fiber Tracker hits when operating at 396ns bunch crossing. Specifically, we describe the design and preliminary tests of the Trip chip, MCM IIa, MCM IIb and MCM IIc. This document also serves as a user manual for the Trip chip and the MCM.

Contents

1	Introduction	3
2	The Trip chip	3
2.1	Schematics	3
2.2	Registers	3
2.3	Pipeline control	4
2.4	Other characteristics	6
2.5	Stand-alone tests of the Trip chip.	7
2.5.1	Characteristics of the cross-talk transient.	7
2.5.2	Work-arounds.	9
2.5.3	Work-around <i>c</i>	10
2.5.4	Work-around <i>d</i>	12
3	MCM II	13
3.1	Tests of MCM IIa	13
3.1.1	FPGA RAM test	13
3.1.2	ADC tests	14
4	Configuration of the FPGA's	19
4.1	Overview	19
4.2	Hardware	19
4.3	Firmware in LVDS_MUX CPLD's	19
4.4	Details	20
5	Fiber Tracker z measurement	21
5.1	Introduction	21
5.2	Hardware	21
5.3	Performance	22
5.4	Can z be used in the trigger?	25
5.5	Monte Carlo studies of the z measurement	25
5.6	Conclusion on the z measurement	26
6	Conclusions	28

1 Introduction

Visible Light Photon Counters (VLPC's) detect the light from the scintillators in the Central Fiber Tracker, and Central and Forward Preshower detectors of the DØ experiment. In total, these detectors have one hundred and one thousand channels. The VLPC output charges are currently amplified by "SIFT" and "SVX" chips in Multi Channel Modules (MCM's) on Analog Front End boards (AFE's). The SIFT chips will not meet the DØ specifications when the Tevatron goes to operation with 132ns bunch crossing.[1] The options are discussed in [2]. Finally it was decided to replace all AFE's.

To this end a new MCM (hereafter MCM IIa) was designed, built and tested[3], and a new chip was designed and tested by Abderrezak Mekkaoui (hereafter "Trip" chip) to replace the SIFT and SVX chips.

Once the Trip chip footprint became known, two new versions of MCM II were designed and built to test the Trip chips in real operating conditions: MCM IIb with two bare die Trip chips, and MCM IIc with one packaged Trip chip (as two packaged chips do not fit on the MCM). The goal is to populate a current AFE board (hereafter AFE I) with 8 MCM II's and test the system during the October 2002 shutdown.

The next step is to design a AFE II board by "embedding" the MCM II's into AFE I, and removing 8 LVDS_MUX CPLD's, 8 VSVX CPLD's, and 4 dual-FIFO's.

This note describes the design and preliminary tests of MCM IIa, MCM IIb, MCM IIc and the Trip chip.

2 The Trip chip

2.1 Schematics

All designs described in this document are available. Please contact the authors for the full schematics. The specifications of the Trip chip are in [3].

2.2 Registers

The lines to read and write to the Trip chip registers are PRGCLKB, PRGOUT, PRGIN, PRGCONTROL and PRGRESET. See Figure 1. PRGCONTROL must be held high during readout and writing to the shift registers. The high-to-low transition of PRGCLKB latches PRGIN and PRGOUT. PRGIN is the serial input to the shift register. PRGOUT is the serial output. PRGRESET high resets all registers to their default values listed in Table 1. Table 2 lists

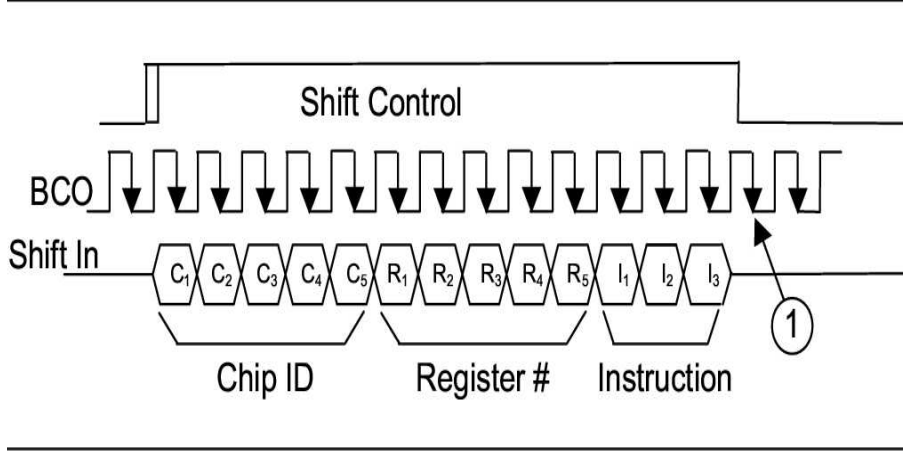


Figure 1: Timing diagram for writing or reading Trip chip registers. From top to bottom: PRGCONTROL, PRGCLKB and PRGIN.

the instruction set for the Trip chip registers. The instructions Reset and Set set all registers to 0 or 255 and are of little use. The Trip Chip ID is 01010 binary or 10 decimal. The most significant bit comes first for the Chip ID and Register #. The least significant bit comes first for the Instruction.

2.3 Pipeline control

This section is taken from [4]. The Trip chip has an analog pipeline with a depth programmable from 1 to 48. The controls on the pipeline are PR2, SKIPB, MOVEDATA, PIPE_RESET, PIPE_CLK and PR1.

A given cell is reset while PIPE_CLK is high, takes a first sample of the preamp 2A output when the clock goes low, and takes a second sample when the clock goes back high, which also advances the pipeline to the next cell.

The SKIPB control, issued by a L1 trigger signal, is used to remove a “hit” cell from the pipeline. SKIPB is normally high during acquisition, and is pulsed low to store a cell. SKIPB must go low and return high between front end clocks, *i.e.* while PIPE_CLK is low.

If PR1 is high at the low to high transition of PIPE_CLK (PR1 should subsequently be lowered), the pedestal cell readout is initiated. When PR1 is raised a second time, the next PIPE_CLK low to high transition initiates the signal readout. These readouts are clocked by MUXCLK.

We do not use MOVEDATA to return the cell read out back into the pipeline. Instead we reset the pipeline using PIPE_RESET after the end of digitization.

A special cell, the “pedestal cell”, is reserved for acquiring the pedestal

Register	name	default	comment
1	IBP	130 dec	preamp current
2	IBBNFoll	120 dec	preamp feedback current
3	IFF	66 dec	preamp feedback current
4	IBPIFF1REF	160 dec	preamp reset strength
5	IBPOPAMP	138 dec	current of opamps
6	IBPFol2	24 dec	opamp feedback current
7	IFFP2	42 dec	opamp feedback current
8	IBCOMP	87 dec	comparator current
9	VREF	170 dec	opamp + in
10	VTH	170 dec	comparator threshold
11[5..0]	PIPEDELAY	31 dec	pipeline depth
11[9..6]	GAIN	0111 bin	preamp/analog opamp gain
12[3..2]	IRSEL	11 bin	current of read pipeline ampl
12[1..0]	IWSEL	11 bin	current of write pipeline ampl

Table 1: Default values of the Trip chip registers.

Instruction	Code
Write	001
Set	010
Reset	101
Read	100
Default	110

Table 2: Instruction set for the Trip chip registers.

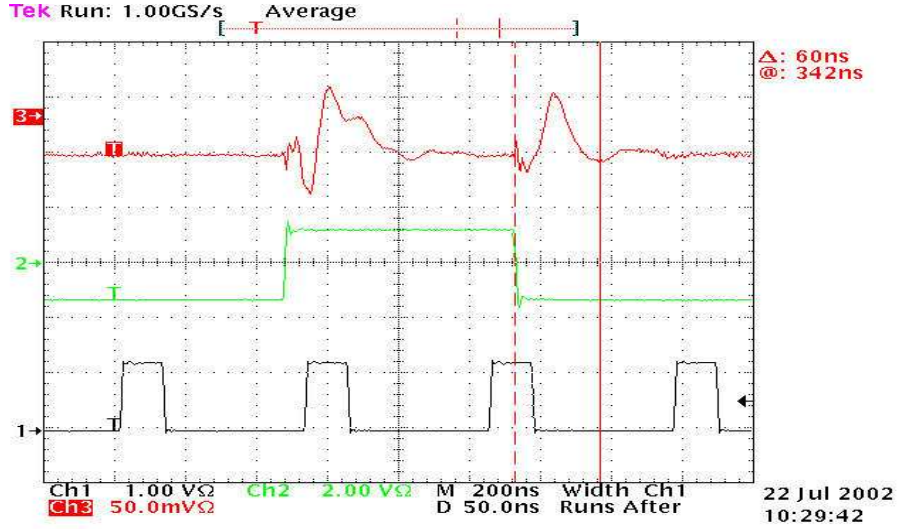


Figure 2: Top curve: channel 32 output showing transients. Second curve: discriminator enable DIGENL. When DIGENL is high (low) all discriminator outputs are high (low). Preamplifiers and opamps 2B are in reset. DIGENU is disabled. No charge injection is applied.

only. The signal is obtained by subtracting the charge in the cell removed by the L1 trigger and the charge in the pedestal cell. The pedestal cell must be refreshed periodically. This is accomplished with the PR2 control line. If PR2 is high when SKIPB transitions from low to high, then normal acquisition is inhibited for that clock cycle. The normally intended pipeline acquisition cell is skipped over and the pedestal cell instead is placed in the pipeline for acquisition of the pedestal. Thus one cycle of deadtime is incurred by refreshing the pedestal cell. If this is done during a beam gap, deadtime can be avoided. For the mode of operation described in this note we do not use PR2.

2.4 Other characteristics

The pipeline channels are read out in this order (with MUXRESETB high and clocked by the rising edge of MUXCLK): 31, 30, 29... for MUXBUFOUT_L and 0, 1, 2, 3... for MUXBUFOUT_U.

The Trip chip pad Dout0 outputs channel 0 on DIGENU and channel 16 on DIGENL; Dout1 outputs channel 1 on DIGENU and channel 17 on DIGENL, and so on.

For default register settings the current on VDDA was 101mA. For the

idle chip the VDDD current was 14mA. The current of VDD_D of MCM IIc with one Trip chip was 181mA without clocks and 340mA with clocks.

With the preamp and 2a opamps at highest gain we observed 890mV at the output of the pipeline for 100fC input charge.

2.5 Stand-alone tests of the Trip chip.

On the very first submission the Trip chip performed just as designed, with one exception: there is a strong crosstalk between the discriminator switching and the input of opamps 2a and 2b and/or the preamplifier or follower. This crosstalk problem is exacerbated by the fact that with no signal all 16 discriminator outputs switch at the same time when they are enabled.

2.5.1 Characteristics of the cross-talk transient.

The peak amplitude of the crosstalk is $\approx 70\text{mV}$ referred to the output of channel 32, which is equivalent to $\approx 42\text{fC}$ referred to the input of the preamplifiers, and falls to 10% in $\approx 60\text{ns}$. If the reset of the opamps is removed before the transient decays, large DC offsets are obtained, except at three times measured from the last discriminator disabling: $\approx 20\text{ns}$, $\approx 30\text{ns}$ and $\approx 50\text{ns}$.

For the following tests we disable DIGENU permanently, apply a long enable pulse to DIGENL and observe the output of channel 32. See Figure 2. All 16 discriminator output lines are switching at the same time. We observe the following:

- The amplitude of the transient decreases by a factor 2.5 when the gain of the preamplifier is lowered.
- The amplitude of the transient is approximately the same when the preamplifier is, or is not, in reset.
- The amplitude of the transient decreases by a factor 3 when the 33pF external capacitor connected to the input of channel 32 is removed.
- Once the 33pF capacitor is removed, the transient does not change significantly when the wire bond to the input pad of channel 32 is removed.
- The amplitude of the transient drops by a factor 3 when the wire bonds from all 16 discriminator outputs are removed. Also the duration of the transient reduces from approximately 70ns to 38ns.

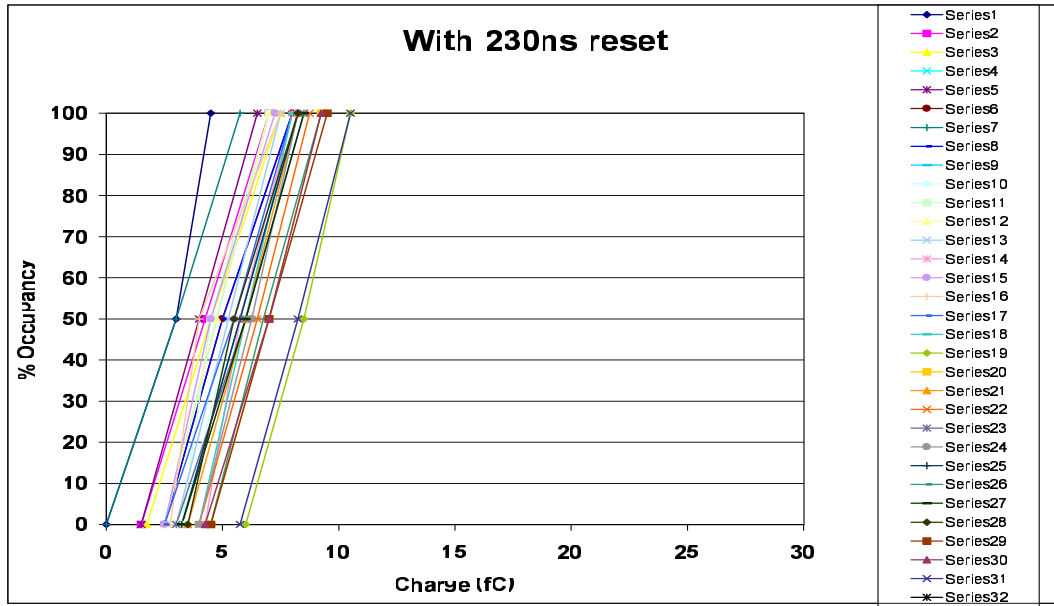


Figure 3: Discriminator turn-on curves for very long resets.

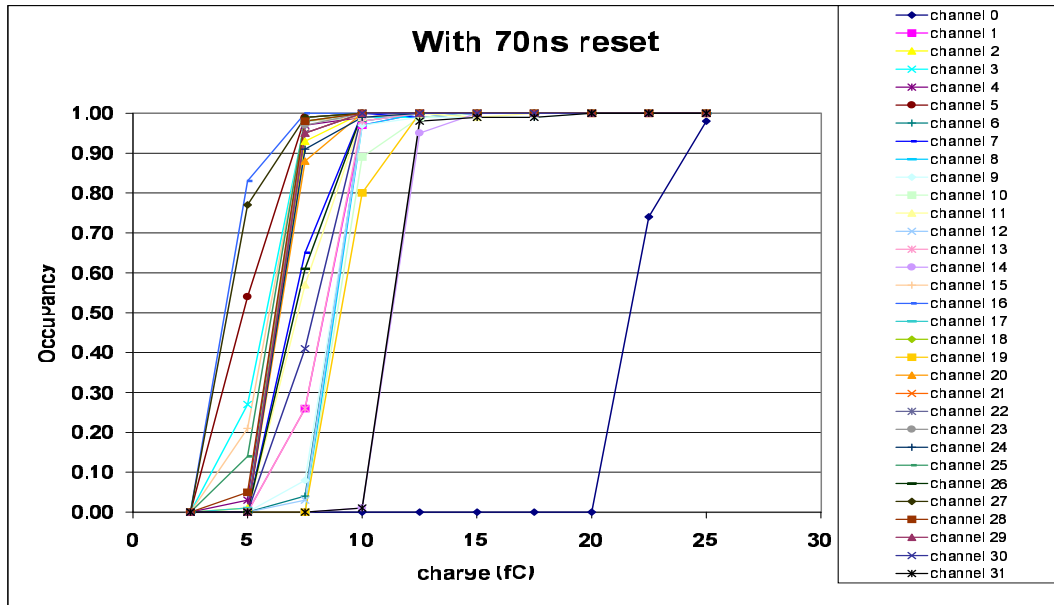


Figure 4: Discriminator turn-on curves for resets extending 50ns after the last discriminator disable. The total reset period is 70ns.

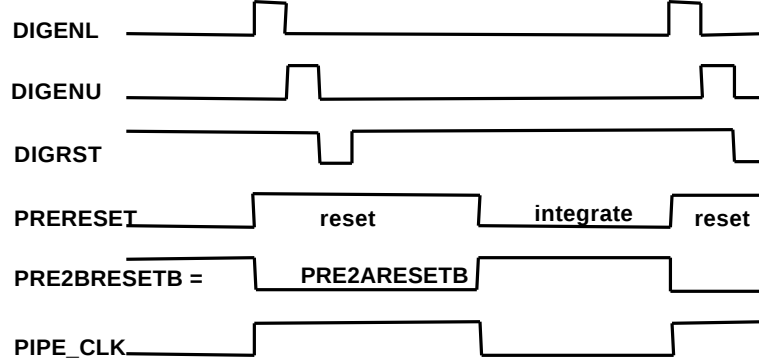


Figure 5: The clocks used for the measurement had 10ns discriminator enables and 70ns resets. For 132ns operation we will use 8.25ns discriminator enables and 66ns resets.

2.5.2 Work-arounds.

The following work-arounds have been studied:

- a) Never disable both discriminator banks at the same time, thus avoiding the simultaneous switching of all outputs. This means that one of the discriminator banks is enabled, and might switch, during the charge integration window. In this mode of operation the preamplifier is reset at the same time as the opamps. We have observed that if this occurs the crosstalk invalidates the firing of the discriminators of **several** channels on the next crossing and affects the analog outputs of the “hit” and neighboring channels. Modes with continuous discriminator firing are also observed. This mode of operation is not usable.
- b) Operate the Trip chip as designed but with the preamplifier and opamp resets extending at least 70ns past the disable of the discriminators so that the transient has decayed. This mode of operation is usable for 396ns bunch crossing period and otherwise meets all specifications. From Figure 3 we observe that the discriminator threshold could be set as low as $\approx 11\text{fC}$.
- c) Operate the Trip chip as designed but with the preamplifier and opamp resets extending 50ns past the disable of the discriminators, thus catching the transient as it crosses zero and its amplitude has attenuated to $\approx 10\text{fC}$. The entire reset period would be about 16.5ns (for two discriminator enables using a $8/132\text{ns} = 61\text{MHz}$ clock) plus $3 \cdot 16.5\text{ns}$ for the subsequent reset, giving a total of 66ns. The usable window for

R1=130	R2=10	R3=1	R4=160	R5=100	R6=24
R7=42	R8=87	R9=170	R10=226	R11,12=454	

Table 3: Values of the Trip chip registers used for the measurements in work-around *c*.

charge integration (once $\approx 15\text{ns}$ are subtracted for preamplifier, opamp and comparator risetimes) is $\approx 51\text{ns}$ which (barely) meets the detector requirements. More details are given below.

- d) Same as work-around *a*, but with the clocks shown in Figure 6 so that the different clocks have their transitions offset in time. This mode of operation meets all specifications with some reservations to be discussed below. This is a fall-back option.

2.5.3 Work-around *c*.

The following performance has been obtained for one Trip chip on a test board with the clocks shown in Figure 5 and at maximum gain. This mode of operation corresponds to work-around *c*. The register settings are shown in Table 3. The chip was backplated and all inputs were loaded with 33pF capacitors (results were substantially the same with no back plating; with no external input capacitors the noise is reduced).

- Discriminator threshold settable at $\approx 15\text{fC}$ (except for channel 0 which is way off) with the following contributions: $\approx 5\text{fC}$ due to noise (this is about 4 times the root-mean-square noise), plus $\approx 5.5\text{fC}$ due to peak channel-to-channel threshold variation, plus $\approx 4.5\text{fC}$ channel spread due to the transient, plus a small contribution due to gain variations between channels and drift. See Figure 4. It was verified that the anomaly of channel 0 is due to the transient. It was also observed that channel 0 is anomalous in the two Trip chips tested.
- The pipeline output is linear from $\approx 0.15\text{V}$ to $\approx 1.2\text{V}$ which is equivalent to a span of 122fC with the preamp and opamps set at the highest gains.
- The widow for charge acquisition was measured to be 12ns (for 50% firing of dicriminators at 20fC), 54ns (for 50% firing of discriminators at 40fC), and 35ns (for a drop by 20% of the pipeline output). Add 6ns for the intended clocks for 132ns operation, see Figure 5.

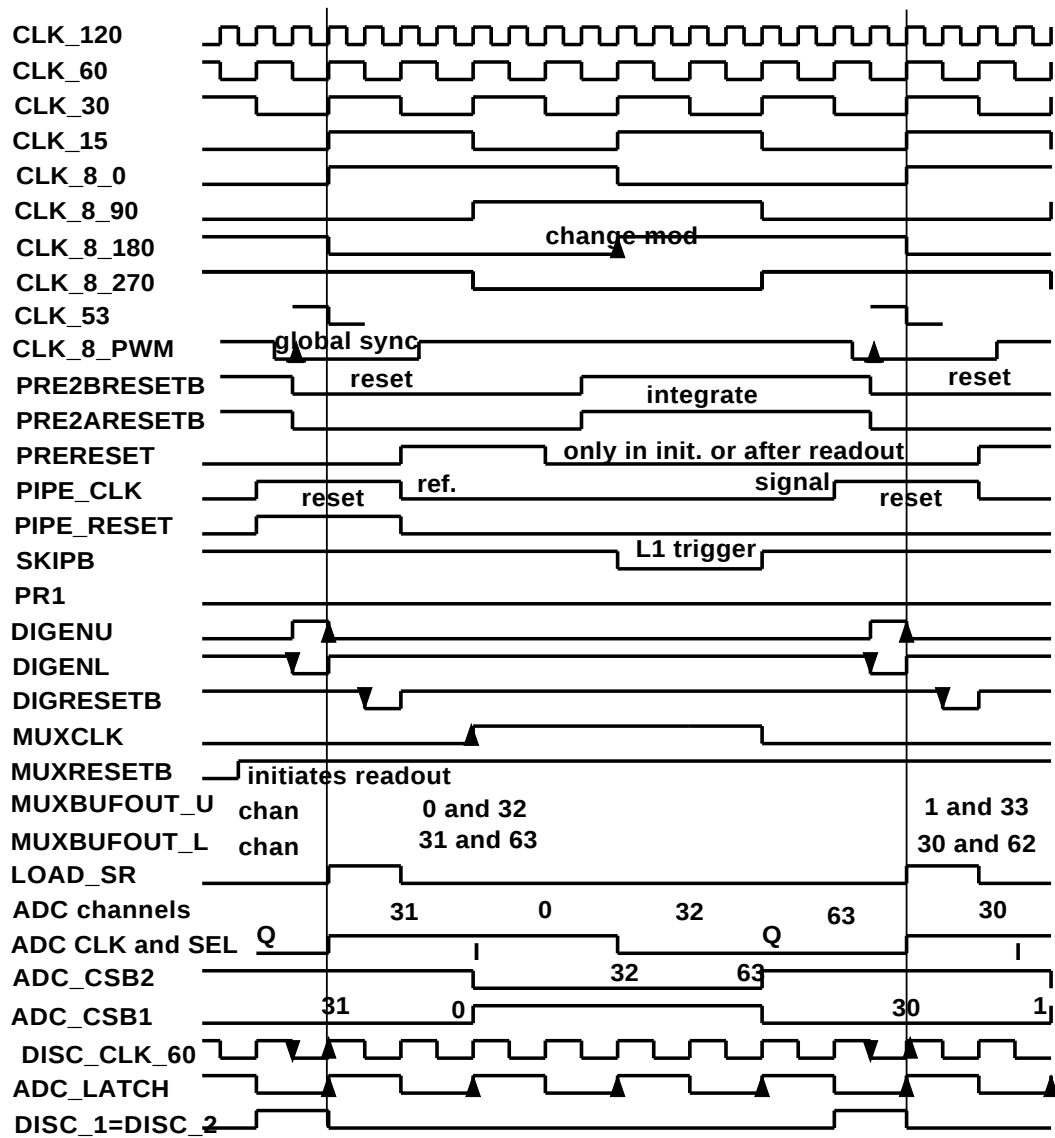


Figure 6: Clocks used to test the MCM IIb. Note: All clocks to the Trip chip were advanced by 8.25ns from those shown here to compensate for delay in the Trip chip.

R1=130	R2=120	R3=66	R4=160	R5=138	R6=24
R7=42	R8=10	R9=160	R10=234	R11,12=454	

Table 4: Values of the Trip chip registers used for the measurements in work-around d .

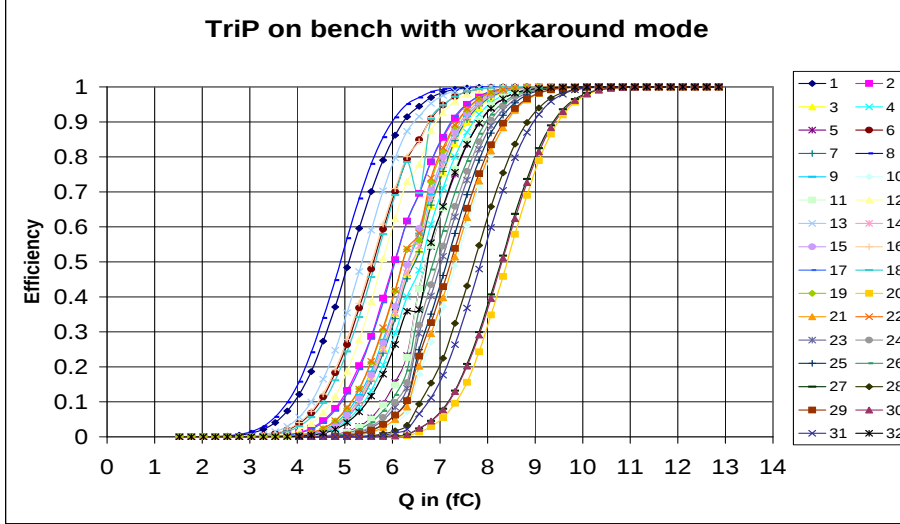


Figure 7: Probability that the discriminator fires as a function of injected charge. Inputs are loaded with 33pF capacitors. Measurement by Abderrezak Mekkaoui.

- Due to the transient, the exact time at which the resets are ended is found to be critical.
- The pipeline clock can be equal to PRERESSET and there is still 5ns of tolerance.

2.5.4 Work-around d .

The clocks used were similar to the ones shown in Figure 6. Note that DIGENU and DIGENL are never both disabled, thus avoiding the transient described previously. The registers were set as shown in Table 4. All chip specifications were met. The discriminator turn-on curves are shown in Figure 7. The peak-to-peak variation in channel threshold is 3.3fC. The rms noise is ≈ 1 fC with 33pF input capacitors. The threshold can be set as low as ≈ 10 fC. Both the digital and analog performance is noise limited:

cross-talk does not limit the performance. Stable and reliable operation is observed.

However this is not the design mode of operation. Allowing discriminators to fire within the acquisition window is dangerous in a complex system due to crosstalk between digital and analog circuits.

3 MCM II

The schematics and layout are in the area `D0server4` → `projects` → `TriggerElectronics` → `132NS`. The schematics and layout of MCM IIa are in files `Mcmii.dsn`, and the gerber files are in `MCMII_20010809.zip`.

The schematics and layout of MCM IIb are in `MCMIIb_20020703.zip`.

The schematics of MCM IIc are in `MCMIIc_20020711.zip`, and the gerber files `MCMIIc-GBR20020711.zip`.

The MCM IIa FPGA firmware can be found in `FPGA6_17AUG01.ZIP`. The MCM IIc FPGA firmware can be found in `FPGAMCMC_21AUG2002.2.ZIP`.

3.1 Tests of MCM IIa

We used one MCM IIa mounted on an AFE for the tests described here. Figure 8 shows schematically the reading and control chain. The whole system was controlled from a PC running Windows and using a `bit3` interface for the communication with the VME crate where the 1553 Controller and the Sand-Alone Sequencer (SASeq) were housed. The 1553 Controller was used to control the power to the MCM. The SASeq was responsible for the data acquisition.

The FPGA was programmed to mimic the data of the SVX (currently in use at $D\emptyset$ for data taking). The 8 bit SVX data bus was used to send the data to the SASeq. The FPGA also controls the two ADC's, receives their digital data through a 10 bits bus, and stores this data in its internal memory until it is ready to be sent to the sequencer. The two channels of each ADC receive the data coming from the Trip chips (not installed in MCM IIa).

3.1.1 FPGA RAM test

The FPGA used is a Xilinx Spartan II XC2S30. It has 6 internal RAM memory blocks with 4KB each. We tested writing and reading the RAM at 132ns to see if it can be used as a digital pipeline for the discriminator information.

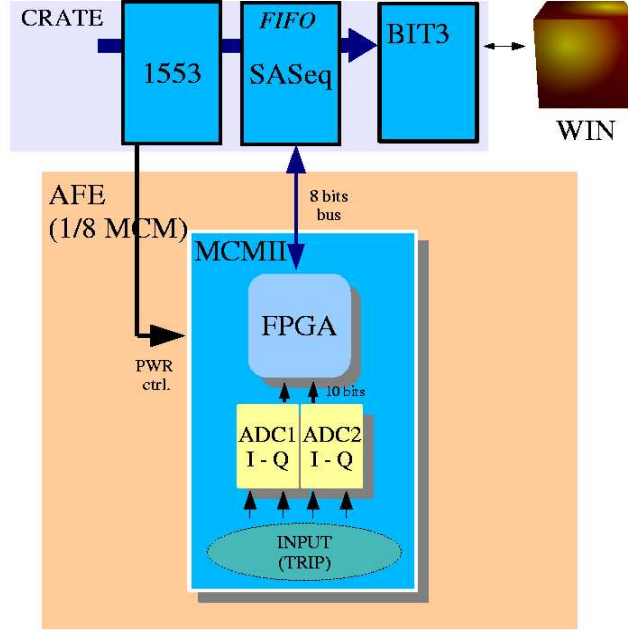


Figure 8: Components of the data acquisition chain.

For the writing process we stored in memory the result of a counter from 0 to 200 continuously during acquire mode, in such a way that the memory block was filled several times and the values of every cell changed in each cycle. After a while, at a random point, we stopped the writing cycle and the reading process was performed, over the previous 256 words, the readout of each memory address was done twice, in order to also check reading failures between the FPGA and the SASeq. This whole procedure was performed 100000 times and we found no errors.

3.1.2 ADC tests

We have two Analog Devices AD9201 ADC's in the MCMII. This chip is dual channel, has 10-bit resolution, and is capable of running at 20 MHz. The chip has an internal reference voltage and the input voltage range can be set from 0 to 2V. We used a 0 to 1V span in these tests. Conversion is done in three clock cycles (pipeline latency). The ADC's will sample the analog output of the pipeline in the Trip chip and the digitalized data is sent to the FPGA. In the following sections we describe the different tests done on the ADCs.

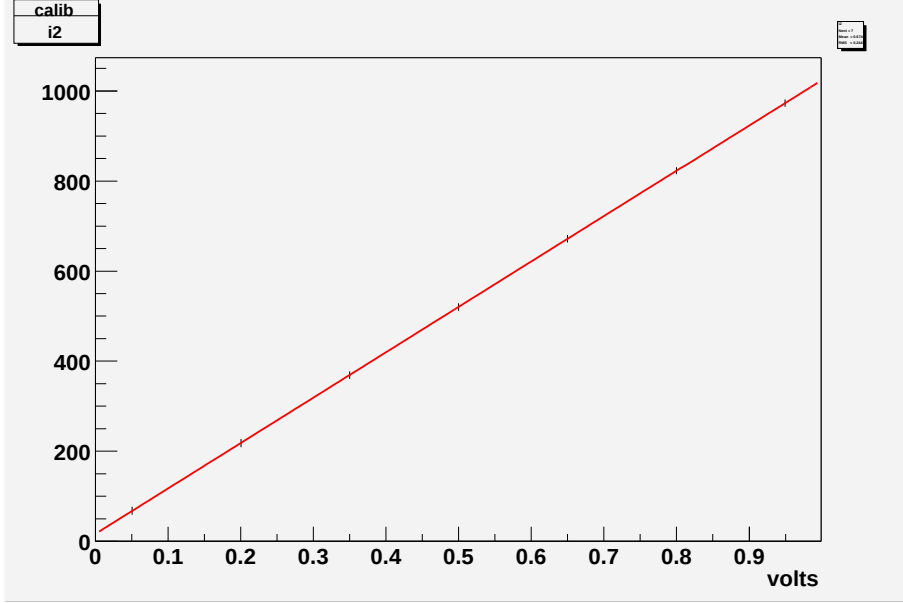


Figure 9: ADC calibration.

Linearity and calibration. As a first step we made a calibration on both channels of the two ADC's. They present very similar signatures. We show in Figure 9 one example representative of the four channels.

In order to get this calibration we used a DC power supply, and we injected the different fixed voltages directly to the input of the ADC's. The digitalized values were read through the complete reading chain. The results show that the 10 bits correspond to 1V range, as expected.

Noise. For fixed input voltages we measured the ADC output several times, and the width (RMS) in this distribution is the noise in our system. Figure 10 shows the pedestal with the minimum width achieved for a fixed voltage of approximately 0.5 V. The noise in this case was 2.6 ADC counts rms. Full scale is 1024 counts. This is not the intrinsic noise of the ADC as can be seen by shorting the input directly on the chip. The intrinsic noise is less than 1 count.

Non-linearity. For the analysis of the differential non linearity we used a triangular wave form signal as represented in Figure 11. Note that the higher and lower values of this ramp exceeds the dynamic range of the ADCs. This was done to avoid the digitalization of the non-perfect peaks. Due to the linearity in the signal we can expect, in the ideal case, a uniform distribution for the ADC counts in the whole dynamic range. Figure 12 shows the actual result of this analysis in one channel. We can see that the global behavior is

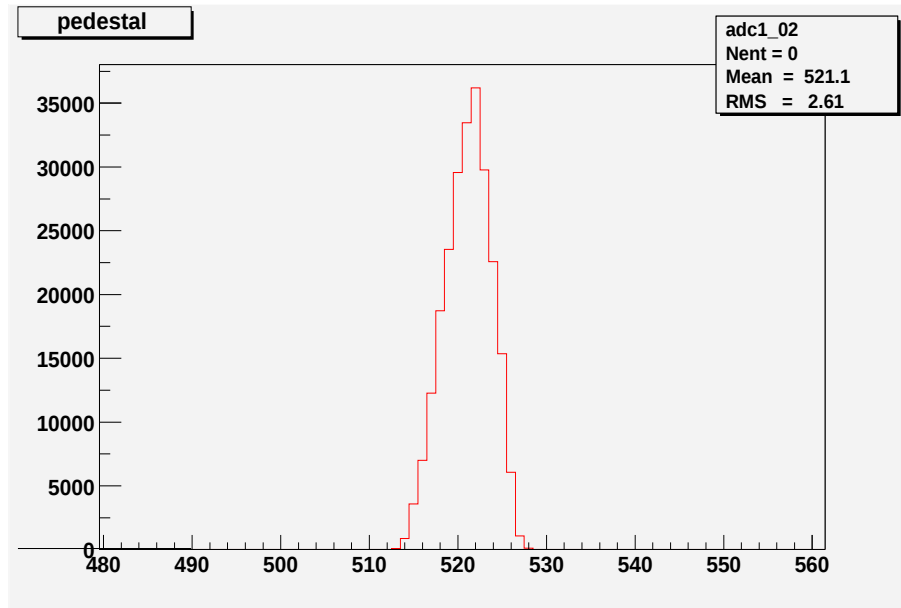


Figure 10: ADC output distribution for a fixed input voltage of 0.5 V.

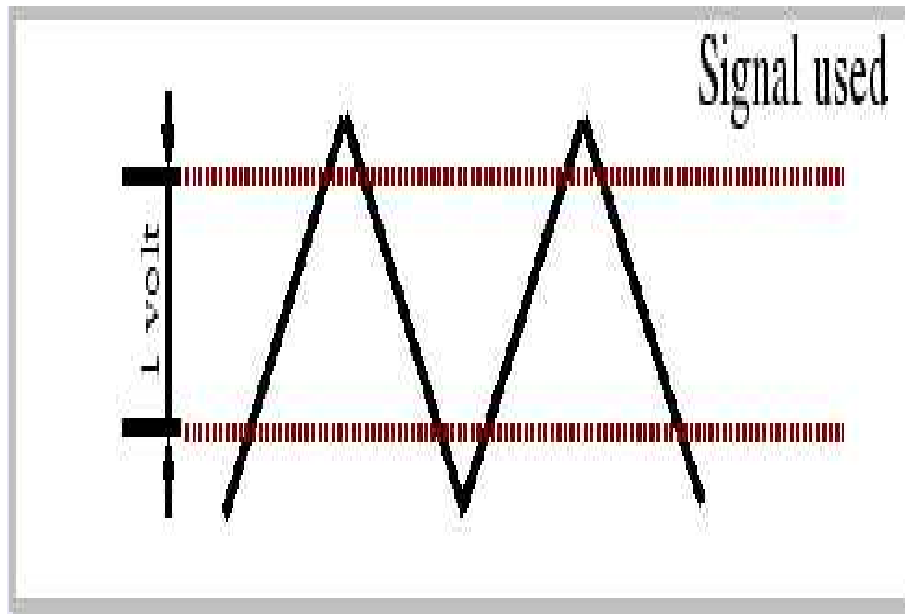


Figure 11: Input signal used for the differential non-linearity test. The horizontal lines show the dynamic range limit in the ADC.

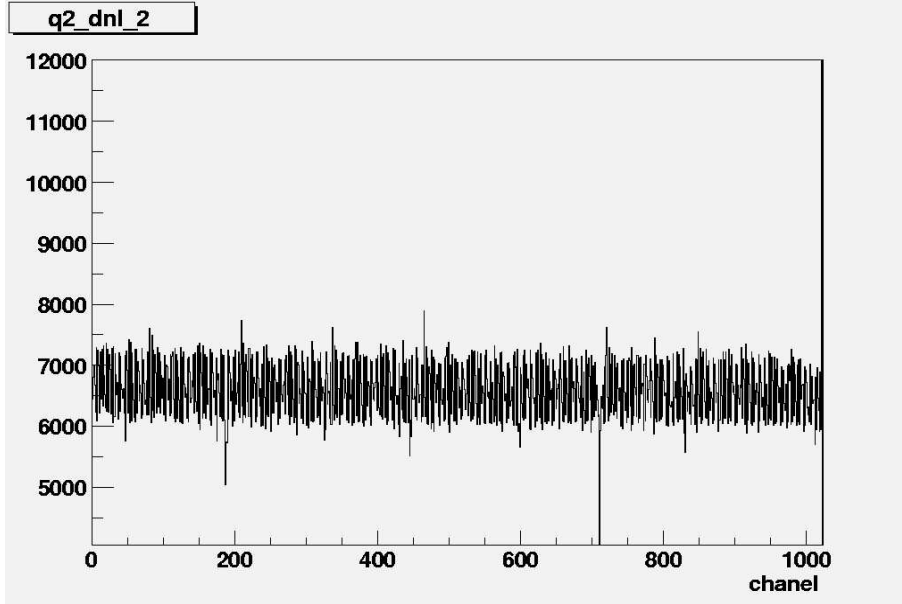


Figure 12: Differential non-linearity results. The general behavior is good, but there are some clear deviations from the flat line expected in the ideal case.

quite good except for a few isolated features, *e.g.* the feature around channel 180. This feature is considered to be intrinsic to the ADC because it could be observed in both channels.

Asymmetry. Another information that can be extracted from this test is the least significant bit odd-even asymmetry. We took the difference of every channel count from the mean and plotted the distributions of these difference for odd and even channels separately. Figure 13 shows the result.

Crosstalk. Another important check is the effect of the signal present in one channel on another channel in the same ADC. For this test we used again the ramp signal mentioned above in one channel and a fixed voltage in the other. We changed the magnitude of the ramp signal and looked for changes in the pedestal of the other one. Figure 14 shows the non visible effect on the pedestal for three different signal values in the other channel.

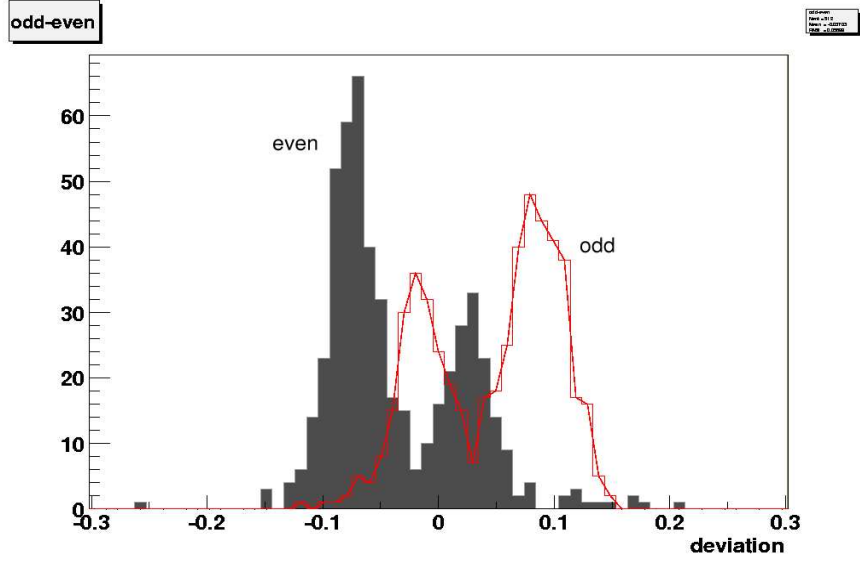


Figure 13: Difference (in per-cent) between the odd and even ADC channels in the differential nonlinearity test. The x -axis corresponds to relative deviations from the mean.

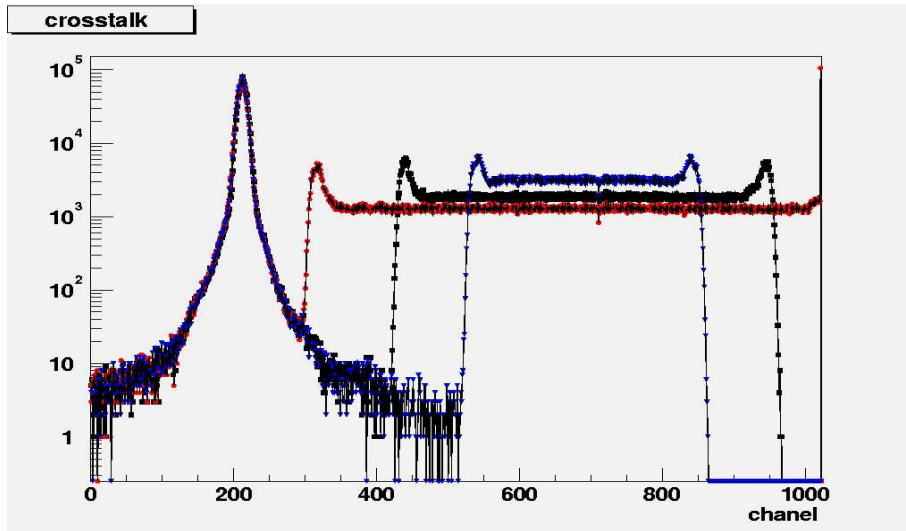


Figure 14: Crosstalk between the two channels of an ADC. On the left we show the readout of the channel with a fixed voltage. On the right we show the readout of the channel with a ramp input for three ramp amplitudes. No pedestal variation is observed.

4 Configuration of the FPGA's

4.1 Overview

One Xilinx XC18V04 4Mbit PROM is used to configure all 8 FPGA's on turn-on, one in Master-serial mode and 7 in Slave-serial mode using a daisy-chain. Each of the FPGA's has its own configuration bit-stream because each has different LVDS_MUX bit assignments, *i.e.* different "personalities". The PROM is programmed using its JTAG port either directly from a computer and download cable, or via the 1553 link and the command "Program PROM". A switch selects among these modes.

A register of Trip1 or Trip2 (or the configuration of the FPGA on MCM x via its JTAG port) is written to using the command "Write to MCM x". This command takes 5 bits, leaving 3 bits of the byte to specify which MCM.

To prevent accidental re-programming of the PROM we issue the command "Do not re-program the PROM" after power-up. In addition the XC18V04 has an initial bit sequence designed to prevent accidental programming.

4.2 Hardware

Daughter board on AFE I board with

- 1 Xilinx XC18V04VQ44C 4Mbit PROM with JTAG and serial interfaces (\$26.6)
- 1 Xilinx XC9536XL-10VQ44C CPLD to latch 4 bits from the PIC_DAT bus (\$0.99)
- 1 Texas Instruments REG113NA-3.3 3.3V regulator (\$1.5)
- 1 28-DIP socket extender

The schematic of the daughter board can be found in → MCM → MCM-schematic → MCMIIc → MCM_II_FIRMWARE_DESIGN.zip and the gerber files in → MCM → Layout → MCM_II_FIRMWARE_4_PCB_FAB.zip.

4.3 Firmware in LVDS_MUX CPLD's

One daisy-chain for series configuration of the 8 FPGA's is implemented in the AFE I through the LVDS_MUX CPLD's using the MCM_SHARER buses and one of the LVDS driver lines.

One 4-bit 3-way demultiplexer is used to choose Trip1, Trip2 or the JTAG of the FPGA. D-flip-flops then latch these 4 bits of the PIC_DAT bus. The PIC_DAT bus is then free for other chores.

4.4 Details

With one 1553 instruction fill up to 32 words into the dual-port-RAM starting at the address in the register BASE_ADDR. Each word is 16 bits wide. Use only the LSByte for information (as is done at present).

Place command “Write to MCM x” into the command queue (starting at 0x0050 as seen from the 1553 side or 0x00A0 as seen from the PIC14000 microcontroller) and a non-zero word into the “Execute Command List” location (0x0057 LSByte as seen from 1553 side, or 0x00AE from microcontroller side).

The PIC14000 polls 0x00AE. If it is non-zero it reads and executes the command in the command queue starting at 0x00A0. It reads the LSBytes starting at the BASE_ADDR corresponding to the command with the aid of the “helper” CPLD. When the 8 bits are on the PIC_DAT bus the PIC14000 strobes, via the “helper”, the LVDS_MUX CPLD x which demultiplexes and latches 4 of the bits. Note that 2 of the PIC_DAT lines are used for the demultiplexer to choose among Trip1, Trip2 or the FPGA, 4 lines are used for PRGCLKB, PRGIN, PRGCONTROL and PRGSET if Trip, or 3 of the lines are used for TCK, TMS, TDI if we are writing to the JTAG interface of the FPGA. One line of the PIC_DAT bus is reserved for readback of PRGOUT or TDO.

One command has PRGCLKB high and the next has PRGCLKB low to latch the bit into the register. (At a future date we can be more clever and let the microcontroller issue the two signals.)

The next-to-last 8-bit “word” brings PRGCONTROL low releasing control over the register. The last 8-bit “word” is zero indicating to the PIC14000 that the command has terminated.

Note that writing to a register can take several 1553 instructions.

To reprogram the PROM we need a different command: “Program PROM”. The CPLD on the piggy-back board is strobed by CMD_STROBE (if not used at present). Otherwise the program is the same as for “Write to MCM x”.

Note that the FPGA’s can be programmed in three ways:

- a) Master-slave serial on power-up.
- b) Master-slave serial on command through 1553 → JTAG of XC18V04 PROM. Configuration is initiated by the CF_B pin of the XC18V04.

- c) Via 1553 $\rightarrow$ JTAG of FPGA x.

5 Fiber Tracker z measurement

5.1 Introduction

In this Section we present a feasibility study for adding a timing measurement to the Trip chip to determine a coarse z in the D0 Fiber Tracker. The Trip chip has been designed for 132ns beam crossing and has a pipeline 48 cells deep. The Tevatron may continue operating at 396ns and never make the transition to 132ns. Consequently we will probably be operating the D0 detector with many minimum bias events every crossing. Then occupancy of the fiber tracker limits its ability to separate real tracks from combinatoric background. A way to alleviate this problem is to add a z measurement. We study the possibility of determining z using the time at which the discriminator of the Trip chip fires.

The idea is this: Every bunch crossing, *i.e.* every 396ns, place the integrated charge on one pipeline cell and, during the reset period, place an analog voltage related to the time delay of the trigger discriminator on another cell. At 396ns bunch crossing the present pipeline is sufficiently deep to do this. Also the deadtimeless nature of the pipeline allows reading out two cells each L1 trigger. This note evaluates the resolution in z achievable with this time measurement.

Note that the added functionality of the chip would be available only for 396ns operation. Operation at 132ns is not compromised, but there is insufficient time to readout the delay information during the reset period, and the pipeline is insufficiently deep.

5.2 Hardware

To add the time measurement functionality to the Trip chip we need, for each channel, a current source (active from the end of the reset period until the discriminator flip-flop changes state), a capacitor (to store the time signal), a reset MOS-FET, a follower opamp, and a switch to toggle the pipeline from the charge measurement to the time measurement (synchronized by PIPE_RESET). For each L1 trigger two SKIPB pulses are sent to the pipeline, one to remove the capacitors with the amplitude information, and one to remove the capacitors with the time information. On readout, the first PR1 pulse initiates the readout of the pedestals, and the second PR1 pulse initiates the readout of the amplitudes. A MOVEDATA pulse switches

Position	direct	reflected
A	$52.5 \pm 3.6 \text{ ns}$	81.5ns
B	$54.4 \pm 5.0 \text{ ns}$	2975.5ns
C	$57.5 \pm 4.3 \text{ ns}$	71.5ns
D	$65 \pm 5.0 \text{ ns}$	n.a.
E	$66 \pm 4.5 \text{ ns}$	n.a.

Table 5: Delays of direct and reflected photon bunches. The time reference is arbitrary. For points D and E the two photon bunches are merged. The root-mean-square width of the direct (or merged) pulse is also shown.

to time readout. Then the third PR1 pulse initiates the readout of pedestals and the fourth PR1 pulse initiates the readout of times. PIPE_RESET returns the capacitors to the pipeline and resets it. The silicon real estate is available on the present Trip chip, so no extensive redesign of the Trip chip is necessary. No new chip pads are required. This extra functionality is of low risk and should cost one or two more submissions of the chip (the first together with the SVX IV). No additional hardware is necessary, only software. The proposed readout of amplitude plus time-delay will not extend the readout deadtime of the experiment since we are eliminating the ” “virtual SVX”.

5.3 Performance

Let us estimate the performance. We consider 5 points distributed along a 252cm scintillating fiber: A at 14cm (0cm is nearest to VLPC), B at 70cm, C at 127cm, D at 183cm and E at 238cm. The time delay of the direct and reflected photon bunches are as shown in Table 5[5]. Note that the velocity of the peak of the first bunch of photons is 16.6cm/ns. The estimated[5] average number of photons reaching the VLPC’s in the direct and reflected bunches are given in Table 6 for a track crossing the axis of the fiber.

Quiz: A bunch of photons arrives with a normal time distribution with standard deviation σ and an average number of photons $\bar{n}$. How well can the “arrival time” be determined? As an example use $\bar{n} = 8$ (direct bunch) and $\sigma = 4.3 \text{ ns}$ corresponding to a pulse with a total of ≈ 14 photoelectrons. The answer depends on what we mean by “arrival time”.

- Answer 1. If “arrival time” is the mean time of arrival then the answer is $\sigma/\sqrt{\bar{n}} = 1.5 \text{ ns}$ corresponding to a resolution $\Delta z = 25 \text{ cm}$.
- Answer 2. Use an integrating amplifier and a discriminator with its

Position	direct	reflected	total
A	28	9	37
B	16	8	24
C	8	6	14
D	22	n.a.	22
E	30	n.a.	30

Table 6: Mean number of photons in direct and reflected bunches.

threshold set at half-maximum, *i.e.* at $\bar{n}/2$. The total number of photons is **not** known. The answer is $\approx 1.7\sigma/\sqrt{\bar{n}} = 2.6\text{ns}$ corresponding to a resolution $\approx \Delta z = 43\text{cm}$ if the amplitude information is **not** used to correct for the discriminator time walk. This is a representative resolution that is achievable at the time of the L1 trigger when the amplitude information has still not been read from the Trip chip.

- Answer 3. Use an integrating amplifier and a discriminator with its threshold set at half-maximum, *i.e.* at $\bar{n}/2$. The total number of photons **is** known. The answer is $\approx \sigma/\sqrt{\bar{n}} = 1.5\text{ns}$ corresponding to a resolution $\approx \Delta z = 25\text{cm}$ if the amplitude information **is** used to correct for the discriminator time walk. This is a representative resolution that is achievable during off-line tracking.

The discriminator delay depends on the number of photoelectrons in the bunch. We measured the following time delay with the comparator current register IBCOMP set at 10 (it could be set higher for shorter time walks):

$$t = A \cdot [1 - \exp(-B/q)] \quad (1)$$

where q is the charge **above** threshold in fC, t is the delay in ns, and $A = 16.86$ and $B = 4.714$. This time delay is shown in Table 7 assuming 7fC per photoelectron and a threshold of 15fC. At voltages below the discriminator threshold the amplifier behaves as an integrator. Then the time walk (fitted to the measured times in Table 7 has the form

$$t \approx \frac{1}{n-1} \cdot (T + t_2 + t_3 + \dots + t_n) \quad (2)$$

with $T = 11\text{ns}$ for a threshold of $\approx 10\text{fC}$. Here t is the time at which the discriminator fires after receiving the first photon at t_1 , the second photon at $t_2, \dots$ and the n 'th photon at t_n . Note that here n is the number of photons arriving before the discriminator fires.

Photons	discriminator delay
3	9.2ns
4	5.1ns
5	3.5ns
6	2.7ns
7	2.2ns
8	1.8ns
9	1.6ns
10	1.4ns
12	1.1ns
16	0.8ns

Table 7: Discriminator time walk after arrival of n photons at $t = 0$.

We are interested in the first half of the distribution of arriving photons. For the sake of simplicity, let us approximate the number of photons arriving per unit time by $dn/dt = at$. Then the number of photons that have arrived until time t is $n = \frac{1}{2}at^2$ and the time at which the discriminator fires is

$$t \approx \frac{1}{n}(11\text{ns} + \int_0^t t \cdot at \cdot dt) \quad (3)$$

where we have neglected the “-1” in the denominator of 2 and replaced the sum by an integral. Doing the integral and solving for t we obtain

$$t \approx \left(\frac{6T}{a} \right)^{\frac{1}{3}} \quad (4)$$

In Table 8 we list the slope a of arriving photons, the number n of photons that have arrived prior to the discriminator firing, and the time-walk t of the discriminator using Equation 4. The resolution Δz was obtained conservatively from $(16.6\text{cm/ns})\sigma/\sqrt{n} + dz$ with σ from Table 5 and n from Table 8. The first term is due to the random arrival time of the first n photons and dz is due to the error in the correction of the time walk (which uses the amplitude information). At C the approximation $dn/dt = at$ breaks down so we have recalculated the error Δz accordingly. Note that the discriminator fires at a time close to the peak of the first photon bunch, see Table 5.

For an offset track with half the photons we obtain the delays and resolutions shown in Table 9.

It is important to note that preamplifier noise and cross talk are common to the amplitude and time measurements so their effect on the measured z

Position	a	n	t	Δz
A	2.3	10.8	3.1ns	21cm
C	0.67	7.2	5ns	35cm
E	2.1	10.5	3.2ns	25cm

Table 8: Data for a track on the fiber axis. The number of photons per unit time received during the leading edge of the photon pulse is at . Also shown are the number n of photons received before the discriminator fires and the time walk t of the discriminator.

Position	a	n	t	Δz
A	1.15	8.6	3.9ns	23cm
C	0.38	4	7ns	45cm
E	1.05	10.5	3.2ns	26cm

Table 9: Same as Table 8 for an offset track with half the number of photons. In this example the number of photons are 19 at A, or 7 at C, or 15 at E.

is **canceled** to first order when the time-walk correction is applied. Only opamp noise and differential cross talk to the digital and analog opamps is of concern.

5.4 Can z be used in the trigger?

All Δz quoted above assume that the discriminator time-walk has been subtracted. This time-walk is a function of the amplitude of the pulse. As an example, compare the time-walks at A and C in Table 9. The time-walk correction is 7ns - 3.9ns corresponding to 52cm. The amplitude is also needed to obtain the error Δz . The amplitude is read out of the Trip chip after an L1 trigger. Therefore a z measurement using only the time information (with no time-walk correction and no error Δz) is of limited use to form a L1 trigger.

5.5 Monte Carlo studies of the z measurement

In Figure 15 we show a histogram of the photon arrival time for a track crossing the center of a fiber of length 252cm[5]. A Monte Carlo study was done assuming an average of 7 photoelectrons for a track traversing the axis of the fiber with photon arrival times drawn from the distribution of Figure 15 and with the **measured** response of the Trip chip discriminator. The results

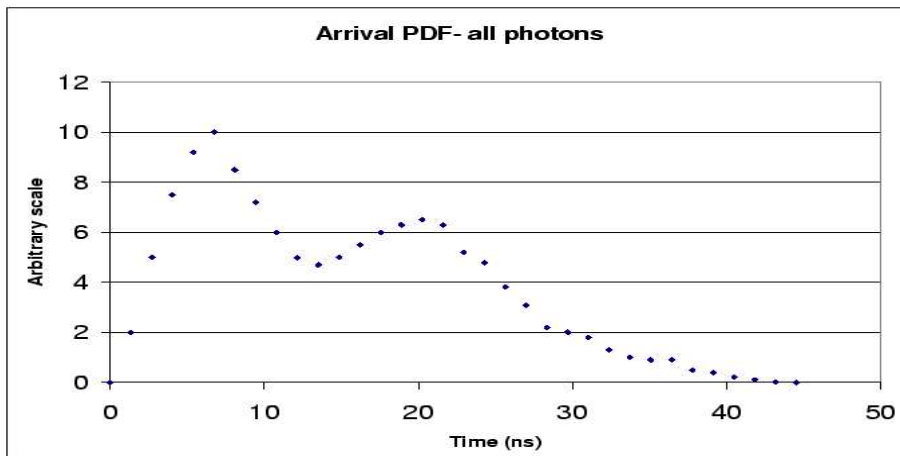


Figure 15: Histogram of photon arrival time (arbitrary t_0) for a track at $\eta = 0$ and a fiber length of 252cm.[5]

are shown in Figures 16 and 17. From Figure 17 we obtain a resolution (at one standard deviation) due to photon fluctuations of 1.5ns or $\Delta z = 25\text{cm}$ for a singlet hit. This accuracy is obtained after the discriminator time-walk correction (note that at the ends of a fiber we obtain ≈ 2.5 times more photons).

5.6 Conclusion on the z measurement

To obtain the z coordinate we take the total measured trigger delay and subtract the trigger time-walk, which is obtained from the measured amplitude. Note that this correction is important, see Tables 8 and 9. Note that the amplitude necessary for the time-walk correction is only available after the L1 trigger when it is read out of the Trip chip. We estimate a total error of $\approx \Delta z = 30\text{cm}$ for a doublet cluster. Thus we can effectively **triple** the Fiber Tracker channels off-line at little cost or risk. The z information can be used as follows: as hits are added to a 3D track a probability, based on the z information, is updated. When this probability drops below a threshold the track is dropped.

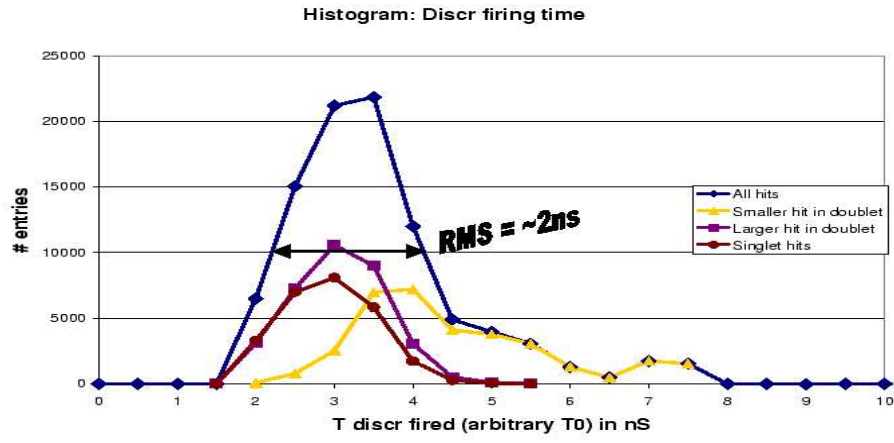


Figure 16: Histogram of the time (arbitrary t_0) at which the discriminator fires for all hits, smaller hit in doublet, larger hit in doublet and single hits. A total of 7 photoelectrons on average is assumed for a track on the fiber axis.

6 Conclusions

The first submission of the Trip chip meets all specifications which is a major achievement by its designer, Abderrezak Mekkaoui. Operation is stable and reliable. The discriminator threshold can be set as low as 10fC, see Figure 7. However the mode of operation does not correspond to the original design. We feel that operating the Trip chip with discriminators firing during the charge integration window is risky in a large and complex system due to possible cross-talk from digital to analog circuits. We therefore recommend a second submission of the Trip chip to change a NOR gate by an OR gate in each channel. A problem with PIPE_RESET can also be addressed.

In this second submission of the Trip chip we also recommend adding functionality to the chip, *i.e.* the measurement of the time delay from the end of the reset period until the discriminator flip-flop changes state. This extra functionality does not change significantly the present design of the Trip chip and is of low risk. The silicon real-estate is available and no new chip pads are required. This extra functionality would add the capability of measuring z in the Fiber Tracker with a resolution of $\approx 30\text{cm}$ for a doublet when operated at 396ns bunch crossing. Operation at 132ns is not compromised but the z measurement is not available at 132ns. The measurement of z would be useful to reduce combinatoric background during off-line 3D tracking. No extra hardware is required, only software.

A 2-bit coarse z measurement for the L1 trigger would require a more extensive re-design of the Trip chip and would have limited value because the amplitude dependent discriminator-walk correction is not available at L1 nor can the amplitude dependent error Δz be estimated.

At present our test setup has an MCM IIa and an MCM IIc installed on an AFE I. An MCM IIb will be installed next week. Communication has been established between a PC and the MCM's (including the "SVX" bus, FPGA registers and Trip registers). The AFE and MCM firmware is in place and fully operational. Analog and digital signals of all channels of both banks are captured, formatted and read out reliably through the Sequencer. MCM IIa and MCM IIc performed as designed. Quantitative system tests with MCM IIb and MCM IIc will follow.

Added note: The results of the very first system test of MCM IIc installed on an AFE I (including firmware and data-acquisition-system) is shown in Figure 18. Note that the rms noise is $\approx 0.4\text{fC}$ and the peak-to-peak spread in the threshold is 1.3fC for the bank of 16 channels tested.

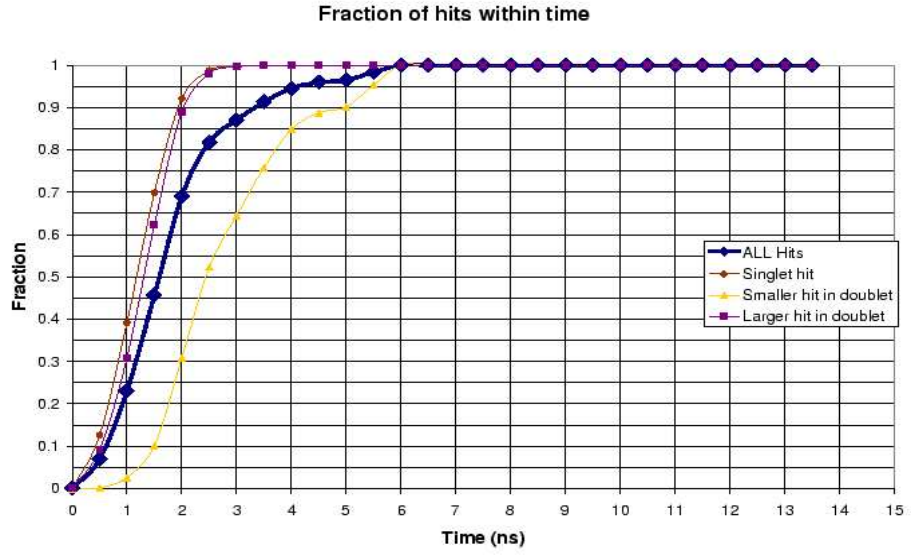


Figure 17: Probability that the discriminator has fired as a function of time (arbitrary t_0) for all hits, singlet hits, smaller hit in doublet, and larger hit in doublet. A total of 7 photoelectrons on average is assumed for a track on the fiber axis.

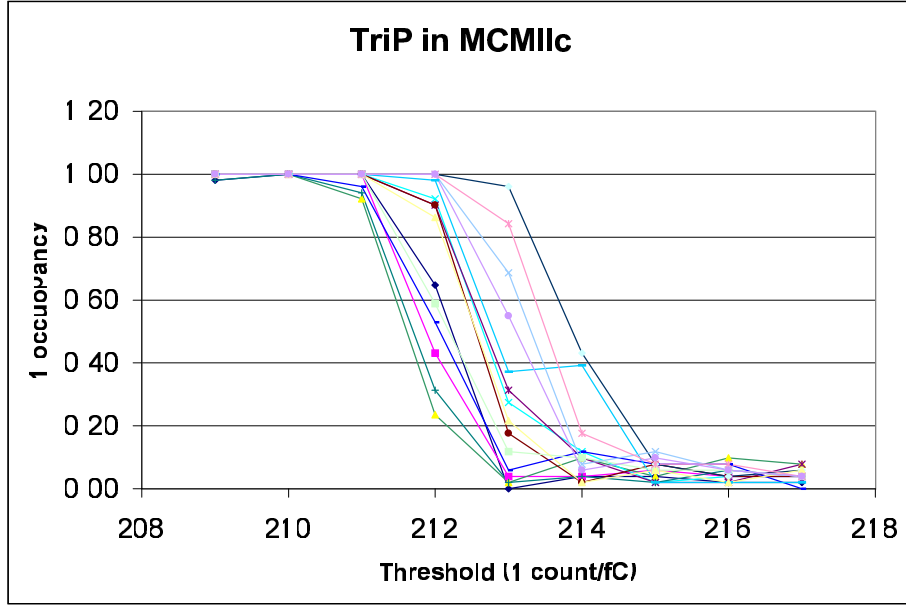


Figure 18: Probability that the discriminator fires as a function of the ADC count of register VTH (comparator threshold voltage). One ADC count is equal to -1.0fC .

References

- [1] P. Rubinov and B. Hoeneisen, DØ note 3897.
- [2] B. Hoeneisen and Paul Rubinov, DØ note 3773.
- [3] P. Rubinov and B. Hoeneisen, DØ note 3898.
- [4] Document by Tom Zimmerman dated 29 April 2002.
- [5] Monte Carlo provided by Alan Bross.