



Development of a gating grid driver of TPC for exotic beam experiments

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Abstract The Multi-purpose Time Projection Chamber (TPC) for nuclear Astrophysical and Exotic beam experiments (MATE) is being upgraded for the decay and active target experiments at the Heavy Ion Research Facility in Lanzhou (HIRFL). We have developed a gating grid driver to control the transitions between the closed and open states of the gating grid of the MATE-TPC to detect interesting rare decay events from a large amount of implanted ions. The gating grid driver is mainly composed of a digital control unit and a high-voltage switch unit. The digital control unit responds to the external trigger and generates control signals for the operation of the high-voltage control part based on the presetting instruction. The high-voltage switch unit is connected to two negative high voltages with different values and changes the voltages of neighboring wires of the gating grid based on the request for closing or opening the gate. A 500 ns switching time of the gating grid driver has been achieved from the closed to open state. The duration of the open state can be adjusted from 1 μ s to 99 ms based on the experimental requirements. This gating grid driver can be used in a particle detector with a high voltage bias of up to ± 3000 V.

1 Introduction

New-generation radioactive ion beam (RIB) facilities are capable of producing a broad range of nuclei with energies ranging from sub-MeV to a few GeV per nucleon, opening up new exciting fields and frontiers in nuclear physics and nuclear astrophysics. The intensities of RIB beams are many orders of magnitude lower than that of beams of stable par-

ticles, severely limiting the luminosity of experiments. The low intensity of RIB has to be compensated by high detection efficiencies and thicker targets. A time projection chamber (TPC) [1] is a well-suited device for such a purpose. It is widely used in many nuclear physics experiments to measure charged particles emitted in nuclear collisions [2–4]. TPCs have the advantage of 4π acceptance for the reaction products, three-dimensional track reconstruction, and insensitivity to electron background [5]. These features make it possible to study the structure and exotic decay of the most exotic nuclei using a TPC. A Multi-purpose time projection chamber for the nuclear Astrophysical and Exotic beam experiments (MATE) [6] has been developed to study the rare decay modes and nuclear reactions induced by radioactive isotopes at the Heavy Ion Research Facility in Lanzhou (HIRFL) [7]. In the decay measurement, the number of implanted ions in the TPC is often several orders of magnitude higher than the number of candidate decay events. In addition, the ionization density of a heavy ion stopped in the TPC active volume is one or two orders of magnitude larger than that of low-energy light particles emitted in the decay, such as protons or alpha particles. It is very difficult to detect the interesting rare decay events from a large amount of background produced by the implanted ions.

In the studies of nuclear reaction, a TPC often serves as an active target, acting as a target for the reaction and at the same time as a detection medium for the reaction products. Since the heavy ion beams are injected into the TPC directly, the exposure of the TPC to the high-rate beams with intensities from 10^5 to 10^6 counts per second (cps) poses a challenge. Although the thick gaseous electron multipliers (GEMs) are robust against discharges even at high particle rates [8], the ion backflow [9] from the amplification region into the drift volume becomes a serious issue. It can distort the drift electric

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field and subsequently deteriorate the track quality. One of our beam tests revealed that the ion backflow suppression by the double-layer GEM in the MATE was not sufficient when the beam rate exceeded 2×10^5 cps. The reaction events of interest are typically at the order of a few tens per second even when the beam intensity reaches 10^6 cps. If the TPC only operates when interesting candidate events appear, the ion backflow will significantly be reduced.

A gating grid is a set of wires which can control the transmission of electrons between the drift region and the amplification region [10, 11]. When auxiliary detectors detect a candidate event, the gating grid is opened to allow the normal operation of the TPC [12–14]. Otherwise, the gating grid remains closed, and no signal can be detected by the TPC [15]. By using a gating grid, the TPC only operates for a fraction of candidate events, allowing the use of higher beam intensity. As the ion of the amplification region drifts to the drift region at a time scale of 100 μ s, much slower than the electron signal in the TPC, a gating grid can also be used to control the ion backflow. Therefore, a gating grid is well suited for the RIB experiments.

The gating grid driver is an important component of the gating grid. It changes the voltages of the two sets of gating grid wires to control the closed and open states of the gating grid. In this work, we report the design and the performance of the gating grid driver developed for MATE-TPC.

2 Design of the gating grid

A schematic diagram of the MATE-TPC with a gating grid is shown in Fig. 1. The MATE-TPC has an active volume of 300 mm \times 300 mm \times 200 mm (height) surrounded by a wire field cage [6]. A stack of two thick GEMs mounted on the top of the readout plate is used for amplifying primary electrons via avalanche. The GEM has a thickness of 400 μ m. The hole diameter of the GEM is 300 μ m with a pitch of 700 μ m. In the setup, both the transfer gap (distance between the two GEMs) and the induction gap (distance between the last GEM and the anode plate) are 2 mm. The length of the drift region from the cathode to the cage bottom is 200 mm. The gating grid is placed between the drift region and the amplification region to control the transmission of electrons or ions between these regions. The gating grid is designed to be 10 mm above the surface of the top GEM, which can be adjusted based on the requirements of experiments.

The gating grid is made of gold-plated Cu-Be wires with a diameter of 70 μ m and length of 35 cm. These wires are separated by a pitch of 2 mm and stretched along the beam direction in experiments. The wires are divided into two sets of gating grid wires interlaced with each other. Two different voltages, $V \pm \Delta V$, are applied to the two sets of wires, respectively. V is the reference voltage of the gating grid,

while $2\Delta V$ is the voltage difference between the two sets of wires. By changing ΔV from 0 to a certain value, the gating grid transits from the open state to the closing state.

To predict the performance of the gating grid, we use Garfield++ [16] to simulate the electric field distribution and the electron trajectory when the gating grid is set at the open or closing states, respectively. The voltage on the drift cathode and mesh plane (bottom of the field cage) of the TPC field cage is -5000 V and -1270 V, respectively. The reference voltage of the gating grid is -1200 V. The two sets of wires of the gating grid are biased with two different voltages of -1200 V $+$ ΔV and -1200 V $-$ ΔV , respectively. The working gas in our simulations is a mixture of 95% helium and 5% carbon dioxide at a pressure of 200 mbar.

Figure 2 (left) shows the distribution of the equipotential surfaces of the potentials in the field cage and the electric field lines when the same voltages ($\Delta V = 0$ V) are applied to the two sets of wires. We can see that the drift electric field lines pass through the wires into the electron multiplication layer (GEM foils). Figure 2 (right) shows the trajectories of electrons considering the electron diffusion in the gas.

When there is a voltage difference ($2\Delta V$) between the two sets of wires ($\Delta V > 0$ V), some of the electrons are absorbed by the positive wires and cannot reach the GEM foils. When the voltage difference is large enough, the electron transmittance approaches 0. Figure 3 shows the distribution of the equipotential surfaces and the electric field lines when the voltage difference between the two groups of wires reaches 160 V. It can be seen that the electrons are almost completely absorbed by the positive electrode wires according to the simulation results.

We simulate the variation of electron transmittance with the voltage difference between the two sets of wires ($2\Delta V$). The reference voltage is -1200 V. The result is shown in Fig. 4. According to the simulation results, the gating grid can block almost all electrons, and electron transmittance decreases to less than 0.02% when $\Delta V > 75$ V. Based on this, the voltage difference for closing the gating grid is determined. In addition to the requirement of a voltage difference of 150 V, the reference voltage of the driver is also required to achieve an absolute maximum output voltage of ~ 3000 V. The transition between the closing state and the open state should be as small as possible to minimize the dead time of the MATE-TPC.

3 Gating grid driver

The gating grid driver is the core device of the gating grid, which controls the transitions between the closing and open states of the gating grid wires. As shown in Fig. 5, the gating grid driver is mainly composed of two units, a digital control unit and a high-voltage switch unit, which are mounted on a

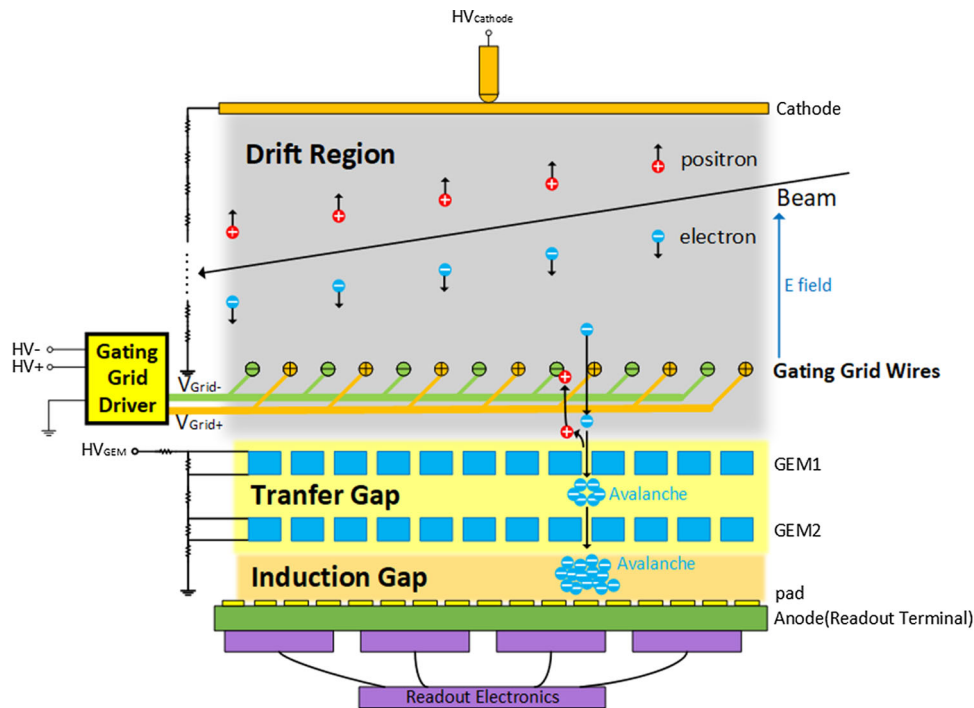


Fig. 1 The schematic diagram of the MATE-TPC with a gating grid

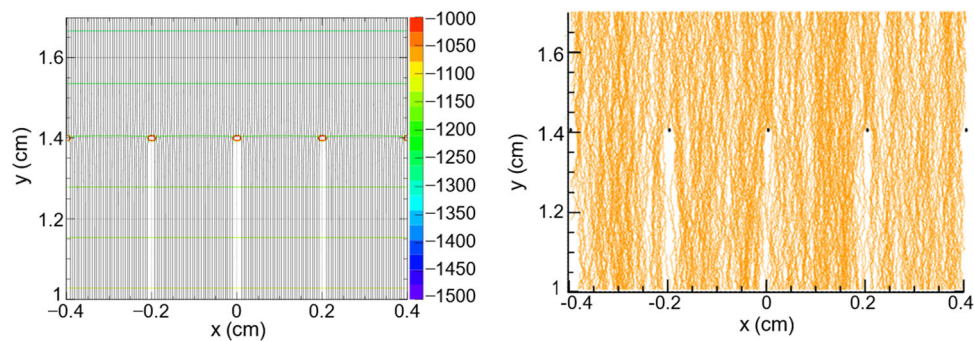


Fig. 2 (left) Simulation of the equipotential surfaces of different potentials and the electric field lines in the field cage when the gate is set at its open state. The GEM, gating grid wires, and mesh plane (bottom of the field cage) are located at $y = 0.4$ cm, 1.4 cm, and 1.7 cm, respectively. The horizontal lines of different colors represent the equipotential sur-

faces at electric potentials (in the unit of V), coded with the color map shown on the right side of the figure. The vertical lines represent the electric field lines. (right) Simulation of the trajectories of the electrons. The black points represent the cross-section of the gating grid, and the orange lines represent the electron trajectories

digital control board and a high-voltage board, respectively. The main function of the digital control unit is to receive the external trigger signal and transmit control signals T1 and T2, TTL-level logic signals, to the high-voltage switch unit. The high-voltage switch unit receives the control signals from the digital control unit and starts the corresponding fast high-voltage transistor switch (HTS) to apply the high voltages $V_{\text{Grid-}} = V_0 - \Delta V$ and $V_{\text{Grid+}} = V_0 + \Delta V$ to the two sets of wires (“Grid–” and “Grid+”) of the gating grid, respectively. The gating grid switches from the closing state to the open

state or vice versa. Figure 6 shows a picture of the gating grid driver.

3.1 Digital control unit

The main architecture of the digital control unit is shown in the lower left unit in Fig. 5. A field-programmable gate array (FPGA) chip, Altera Cyclone-III [17], is adopted to construct the digital control unit. Logic modules (logic firmware) are designed and loaded in it, which serve various functions: receiving the external trigger signal and generating control

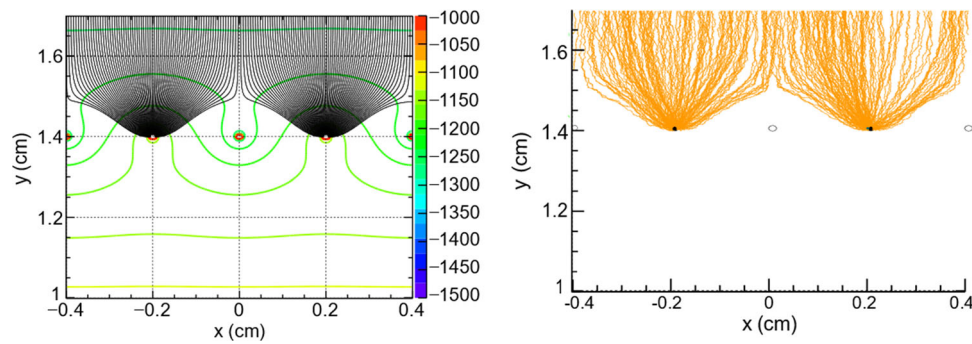


Fig. 3 (left) Same as Fig. 2 but for the closed state of the gating grid. (right) Simulation of the electron trajectories. The hollow and solid circles represent the negative and positive electrode wires, respectively. The electron is eventually absorbed by the gating grid

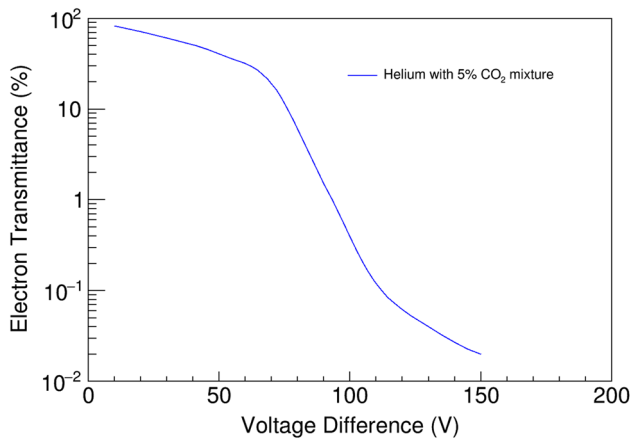


Fig. 4 The variation in electron transmittance with an increasing voltage difference ($2\Delta V$)

signals for opening and closing the gating grid, setting the opening period and closing period of the gating grid, providing the status display, etc. A 50 MHz clock is used for this circuit. The open period of the gating grid can be selected from 1 μ s to 99 ms. The upper limit can be easily extended to

a longer period by changing the firmware of the FPGA. Ten push-buttons are adopted for the setting of the open period of the gating grid. When an external trigger signal, TTL level, is received, two control signals, T1 and T2, will be generated by the digital control unit and sent to the high-voltage switch unit. The opening period of the gating grid is determined by the width of the control signal T1, and the function of T2 is to control the gating grid release, which causes the gating grid to rapidly shift back to the closed state from the open state. Figure 7 shows the timing structure of the main signals of the gating grid driver. To ensure the simultaneity of switch operation, a design with equal length between the driver chip and HTS switches has been implemented.

3.2 High-voltage switch unit

The high-voltage switch unit is the main circuit of the gating grid driver. It is used for applying the two negative high-voltage signals, $V_{\text{Grid-}}$ and $V_{\text{Grid+}}$, to the wires of the gating grid, and implementing the switching of the two states, the open state and closed state. The switches are controlled by the TTL logic signals.

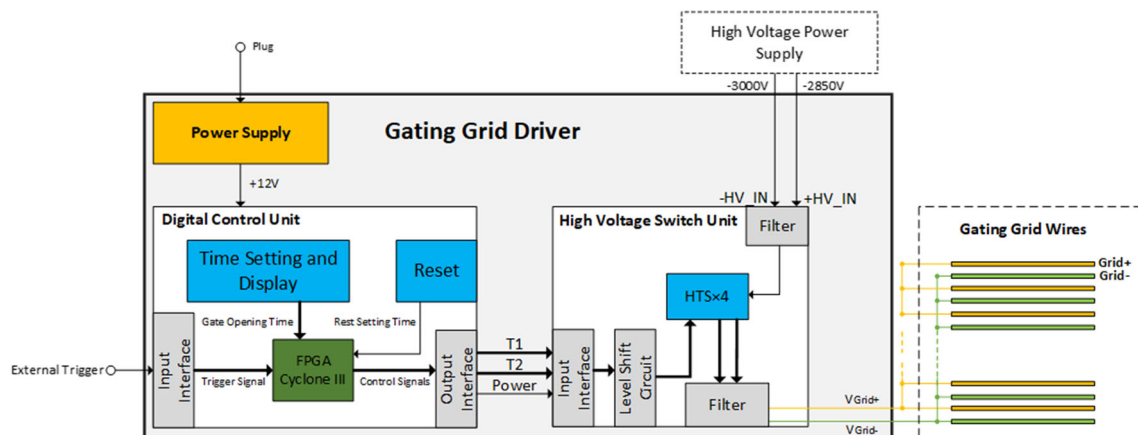


Fig. 5 Schematic diagram of the gating grid driver

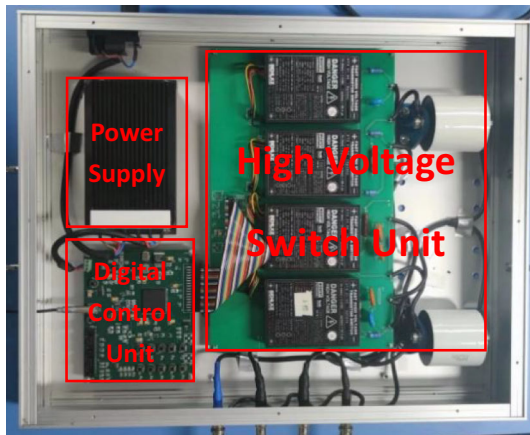


Fig. 6 Picture of the gating grid driver

(1) Circuit of the high-voltage switch unit

As shown in Fig. 8, the high-voltage switch unit mainly consists of HTS switches (S1, S2, S3, S4) and a high-voltage bias circuit, which is also called the high-voltage control board. The HTS 31-06 fast high-voltage transistor switches (HTS) manufactured by Behlke [18] are chosen to construct the main circuit of the high-voltage switch unit. Compared with the traditional metal–oxide–semiconductor (MOS) driving circuit [19,20], the HTS switch has excellent electrical characteristics, such as absolute maximum operating voltage of 3000 VDC, small static on-resistance of 3 ohms, and maximum off-state current of 5 μ A.

The high-voltage switch unit is biased by two negative power supplies, +HV_IN and –HV_IN. Two outputs from this control board, $V_{\text{Grid}+} = V_0 + \Delta V$ and $V_{\text{Grid}-} = V_0 - \Delta V$, are connected to the Grid+ and Grid– wires of the gating grid, respectively. A reference high voltage, HV_avg (V_0), is supplied by the high-voltage bias circuit constructed by R1, R2, R3, R4, and C1, C2. Two large resistors of 1 mega-ohm are used as R2 and R3, ensuring that

a small current is pulled from the power supply. A filtering network constructed with C5, C6, C7, and R11, R12, is connected to the middle point of the high-voltage bias circuit for filtering out voltage fluctuations, which can effectively minimize the small deviation of HV_avg. Compared with the conventional gating grid circuit [21], the circuit structure has been simplified, and there are only two voltages (+HV_IN and –HV_IN) in the system.

(2) Operation of the high-voltage switch unit

Normally, the gating grid driver is closed. All four HTS switches are turned off. The high voltage +HV_IN is added to the Grid+ wires through resistors R4, R6, R7, and R10, and another high voltage –HV_IN is added to the Grid– wires via resistors R1, R5, R8, and R9. The electrons from the drift regions are trapped by the Grid+ wires of the gating grid. When the control signal T1 from the digital control part is received, HTS switches S1 and S3 are turned on simultaneously, and the high voltage HV_avg is sent to Grid+ and Grid– via S3, R10 and S1, R9, respectively. This allows the gating grid to be opened.

There is a delay time from the arrival of the T1 signal to the full opening of the gating grid, which is caused by the voltage transition time of Grid+ and Grid– from the original voltage to intermediate voltage HV_avg. This delay time is called dead time. After the termination of the T1 signal, the voltage on the Grid+ wires will be restored to its original value +HV_IN, and synchronously, the voltage on the Grid– wires will return to its original value –HV_IN. To reduce the recovery time, the control signal T2 (typical width value: 2 μ s) is sent to HTS switches S2 and S4 after a short period (typical value of 1.5 μ s) following the termination of T1 signal. Once S2 and S4 are turned on, the resistors R5 and R6 are bypassed, and the discharge time constant is reduced. As a result, the high-voltage switch unit can be quickly restored to its original state.

Fig. 7 Timing structure of gating grid driver

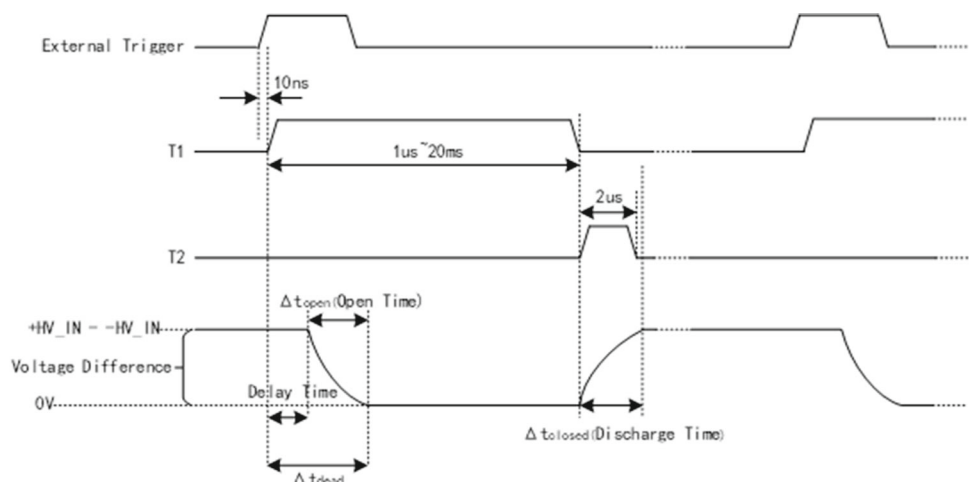
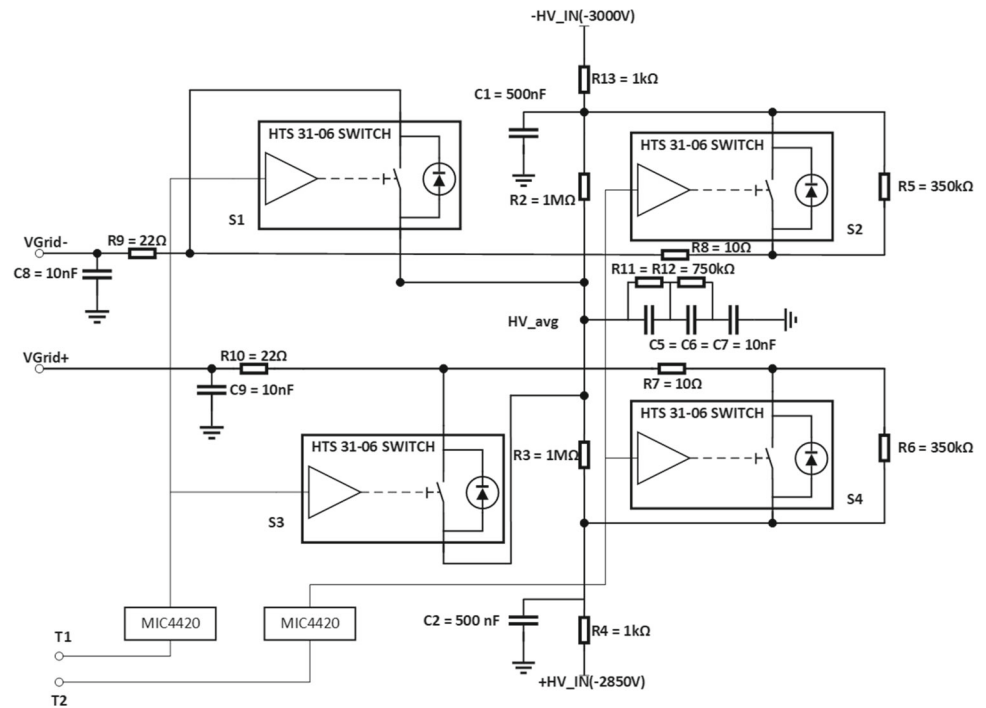


Fig. 8 The schematic of the high-voltage switch unit. The unit mainly consists of HTS switches (S1, S2, S3, S4)



(3) Influence of dead time

As mentioned above, there is a short period from the arrival of T1 to the full opening of the gating grid, which is called dead time. During this period, the drifting electrons cannot fully pass through the gating grid. During the dead time, a small section called a dead region is formed during the drift, and drifting electrons produced in this region will be lost. The length of the dead region can be estimated by the following formula (1):

$$\Delta L_{\text{dead}} = v_{\text{drift}} \cdot \Delta t_{\text{dead}}, \quad (1)$$

where v_{drift} is the drift velocity of the electrons and Δt_{dead} is used to express dead time. The existence of the dead region will lead to loss of track detection. Therefore, it is necessary to minimize the length of the dead region as much as possible. To reduce the dead region, the Δt_{dead} should be reduced. Two main factors affect the Δt_{dead} in our system.

The first factor is the delay time, which means the interval between the arrival of the trigger signal and the beginning of the gating grid voltage change. The delay time is a constant of 288 ns (± 10 ns) according to the tests.

The second factor is the transition time of voltages on Grid+ wires and Grid- wires. The time constant of the RC low-pass filter will produce an effect on the transition time of voltages on Grid+ wires and Grid- wires. In our circuit, there are two RC low-pass filters constructed by R9, C8 and R10, C9, which are located on the line to Grid+ and the line to Grid-, respectively. Although the low-pass filters can minimize the noise and voltage fluctuation on the Grid+ and

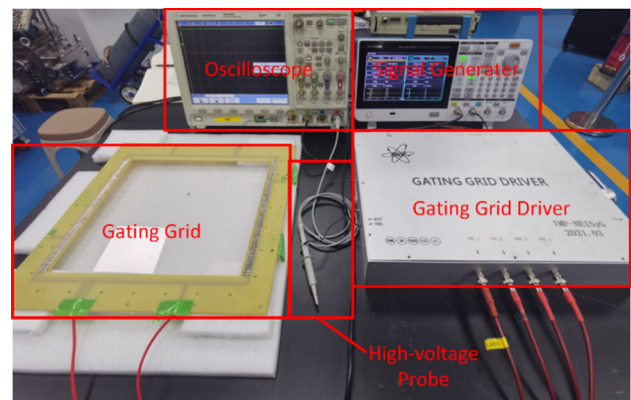


Fig. 9 A picture of the test bench in our laboratory

Grid- wires, the transition time of high voltages is increased. In practice, the transition time of negative bias high voltage on the Grid+ and Grid- wires can be adjusted by changing the time constant of the RC low-pass filter according to the requirement of the experiment. In the current test, it is measured to be less than 400 ns.

4 The test and results

To verify the function of the gating grid driver, a series of tests have been carried out in the laboratory. The setup in the test is shown in Fig. 9. The gating grid driver is powered directly by 220 VAC, and two negative high voltages are supplied by a high-voltage module. An oscilloscope is used to measure

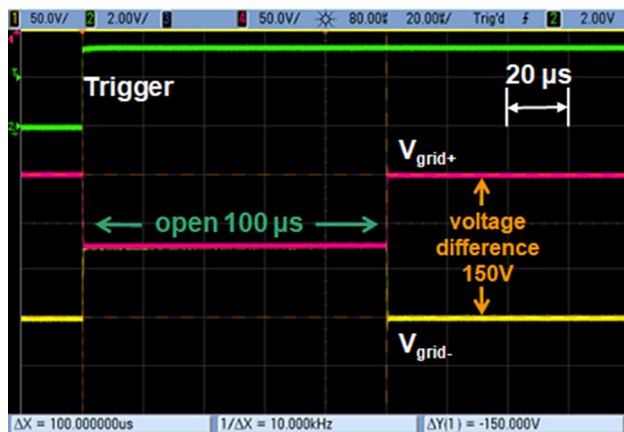


Fig. 10 The test results obtained when $-HV_IN$ is -3000 V and $+HV_IN$ is -2850 V. The green waveform is the external trigger signal, and the red and yellow waveforms are the output voltages (i.e., V_{Grid+} and V_{Grid-})

the output voltage waveforms on V_{Grid+} and V_{Grid-} of the gating grid driver.

First, an evaluation test was performed. The waveforms of the output terminals are shown in Fig. 10, when the negative high voltages supplied to the gating grid driver are -2850 V ($+HV_IN$) and -3000 V ($-HV_IN$), and the gating grid time is set to 100 μ s.

The test result obtained when $-HV_IN$ is -3000 V and $+HV_IN$ is -2850 V. The green waveform is the external trigger signal, and the red and yellow waveforms are the output voltages (i.e., V_{Grid+} and V_{Grid-}).

It can be seen that the time in the open state can be set and maintained by the digital control part of the gating grid driver. Its accuracy is guaranteed, and the amplitude of voltage change ΔV at both ends, V_{Grid+} and V_{Grid-} , is almost the same. The turning-on and turning-off functions of the gating grid can be reliably realized. The switching time, a key performance of the gating grid driver, can be observed in detail in Fig. 11.

The transition times (rise time and fall time) of the voltage signals measured at the port V_{Grid-} and V_{Grid+} . Figure 11 (left) shows the transition from the closing state to the open state. Figure 11 (right) shows the transition from the open state to the closing state.

The rise (fall) time in this work is defined as the required time for the voltage change from 10% to 90% of the desired voltage change. As shown in Fig. 11, oscillations exist in the rising (falling) edges. The voltages (V_{Grid-} and V_{Grid+}) may cross the required thresholds more than once. In this work, we choose the shortest time as the rise (fall) time.

Figure 11 shows that the rise time and fall time of the voltage signal tested at ports V_{Grid-} and V_{Grid+} are both less than 500 ns. For the transition of the closing state to the open state, there is a 200 ns inherent delay for generating

V_{Grid-} and V_{Grid+} after receiving an external trigger signal. Less than 700 ns is obtained to drive the gating grid changing from the closing state to the open state after receiving an external trigger signal under the condition of input negative high voltages of -3000 V ($-HV_IN$) and -2850 V ($+HV_IN$). Therefore, this device is capable of studying any decay process with a half-life of more than 700 ns. Even for decay faster than 700 ns, the TPC is still able to capture this event if the drift time of the primary ionization is longer than 700 ns. However, for a slow gas such as an Ar-based mixture, ΔL_{dead} is around 35 mm at a typical drift velocity of 5 cm/ μ s. In online measurements, the complete track can be measured only when the minimum distance between the particle track and the gating grid is longer than 35 mm. Otherwise, only the portion of the track that is more than 35 mm from the grid can be captured.

The gating grid is also useful for suppressing the positive ions which are generated in the avalanche and travel back to the drift region. In a typical operation of the MATE detector using the He+5%CO₂ mixture at around 200 mbar, the drift time of positive ions from the avalanche region to gating wires is around 100 μ s using a He⁺ ion mobility of 10.2 cm² s⁻¹ V⁻¹ under normal conditions (300 K, one atmosphere). Therefore, the transition time (< 500 ns) of the driver allows the gating grid to return to the closed state before ions go to the drift region, and it can be used in most decay measurements.

A joint test with the gating of the MATE-TPC was performed. The voltage output driven by the gating grid driver was connected to the gating grid of the detector through a pair of high-voltage cables. In the test, different input high voltages with different durations in the open state were tested to investigate their influence on the opening and closing time. Results are shown in Table 1. It was found that with increasing input voltage, the operation accelerates, which means that the performance of the driver improves.

5 Conclusion

A gating grid driver is designed for the MATE-TPC to control the transmittance of electrons and positive ions between the drift region and the amplification region. It consists of two parts: a digital control unit and a high-voltage switch unit. An FPGA chip is adopted to construct the digital control unit for generating the control signals to open or close the gating grid. Four HTS switches, HTS 31-06, are employed as the high-voltage switch unit to generate the required voltages. The gating grid driver features the characteristics of a simple circuit structure, small delay time, and fast transit time of control signals for opening and closing the gating grid. It is powered by two negative high voltages (-2850 V and -3000 V). The highest voltage difference of up to 150 V

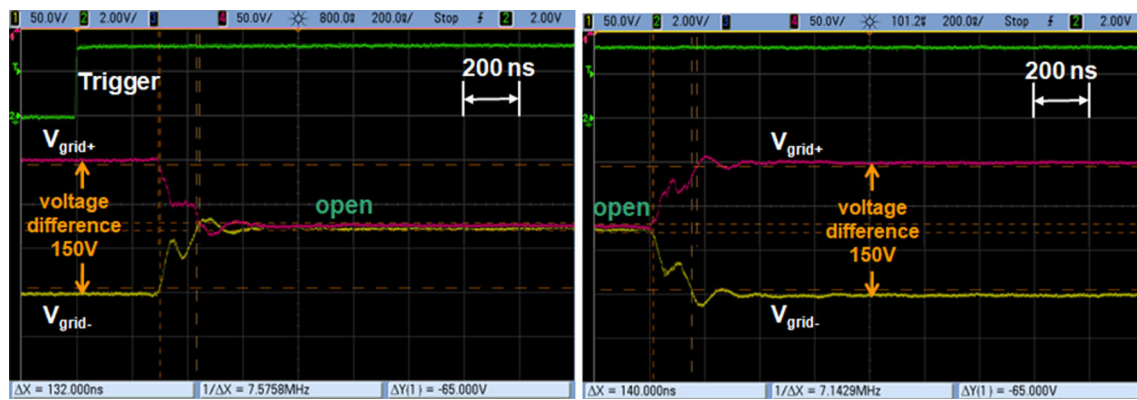


Fig. 11 The transition times (rise time and fall time) of the voltage signals measured at the port $V_{\text{Grid-}}$ and $V_{\text{Grid+}}$. (left) Shows the transition from the closing state to the open state. (right) Shows the transition from the open state to the closing state

Table 1 The variation in opening and discharge time with different +HV_in and -HV_in. The opening time and discharging time is the 10–90% transition time of Vgrid and Verid voltages

	Voltage (V)	Delay time (ns)	Opening time (ns)	Discharge time (ns)
-HV_in	- 1000	288	208	364
+HV_in	- 850	288	212	360
-HV_in	- 2000	288	148	164
+HV_in	- 1850	276	168	184
-HV_in	- 3000	280	132	140
+HV_in	- 2850	284	148	160

can be added to the adjacent wires of the gating grid. The gating grid can be opened within 500 ns with small termination resistors and closed within 400 ns. The test results show that the performance of the gating grid driver can meet the requirements of experiments.

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Data Availability Statement This manuscript has no associated data or the data will not be deposited. [Authors' comment: The results of this article may not require specific data, because the test results and performance of gating grid driver have been shown in Table 1.]

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