FERMILAB-CONF-25-0564-STUDENT

Setup and Testing of PSEC5 ASIC Boards

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Date: August 7, 2025

Abstract

The PSEC5 ASIC is a high-speed waveform sampling chip developed for precise measurements. This report presents the design review, test board configurations, and results from functional validation of the PSEC5 device. Key aspects examined include power integrity, voltage-controlled oscillator (VCO) behavior, SPI register functionality, clock division characteristics, readout performance, and analog biasing response. Tests were conducted across two boards under varied voltage conditions and signal configurations. Notable observations include robust VCO output, SPI communication irregularities, and anomalous readout conditions. The findings support design iterations for improved ASIC operability and firmware integration.

Introduction

High-speed analog sampling ASICs such as the PSEC5 are critical components for applications in time-resolved signal detection. These include particle physics, timing detectors, and fast digitization circuits. The PSEC5 chip integrates analog sampling, discrimination, and digital control within a compact footprint. The current testing phase aims to validate the functional blocks and verify performance against design expectations.

Overview of PSEC5 Architecture

The PSEC5 architecture includes analog front-end amplifiers, threshold discriminators, a voltage-controlled oscillator (VCO), clock dividers, and SPI-controlled digital logic. The device requires five supply voltages: AVDD, DVDD, VCOVDD (1.2 V) and AVDD25, DVDD25 (2.5 V). Communication and control are managed via a standard SPI interface.

Experimental Setup

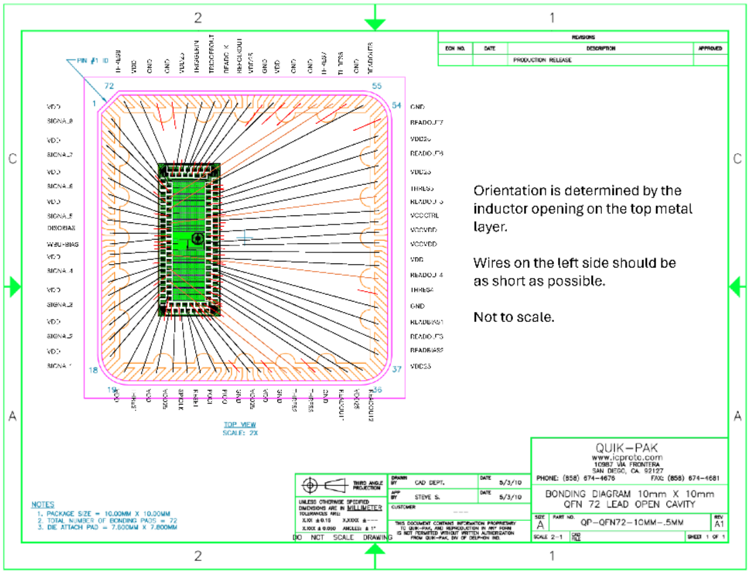
- Two examples of the chip were fabricated for testing.
- Waveform inputs were provided via a EDU33212A.
- Several Oscilloscopes were used but primarily a DPO 4104.
- A PXIe-1062Q with a 4140 and a 4141 was used to provide the power.
- An Arduino Portenta H7 was used to provide the SPI instructions.

Test Procedures

Firstly, wire bonding diagrams were verified and corrected where necessary. Once the board was checked thoroughly, regulated power sources were applied to inputs to check for shorts. Upon first applying all voltages, a frequency was noted on the reference clock output. As such, the following test was to find if varying the VCO control voltage would modify this frequency. At this point, SPI code was developed to send instructions, so operation of the chip could be tested. SPI commands were then issued using an Arduino microcontroller to test individual registers of the chip. This step continued until end of this summer research.

A. Wire bonding:

Wire bonding diagram was compared to connections as described on PCB file and the manufactured chip’s connections as examined under microscope.



Orientation is determined by the inductor opening on the top metal layer.

Wires on the left side should be as short as possible.

Not to scale.

CORRECTIONS on wire bonding

- Pin N3 on the PCB is connected to DVDD and should be connected to DVDD25
- Pin E14 on the bonding diagram has a double connection to READBIAS1 and to GND. The pin is properly connected to BIAS1 on the PCB.
- Pin E17 on the bonding diagram should be wire-bonded to VCODVDD instead of DVDD25.
- Pin N7 on the bonding diagram should be connected to AVDD instead of DVDD.

B. Power test:

B.1. Connect all supply voltages limited to 10mA.

B.2. Verify there is no smoke and the chip is not getting too hot.

B.3. Measure current from all supplies.

B.4. Verify there are no short circuits.

C. Read VCO output

If everything is properly powered, the voltage-controlled oscillator (VCO) should begin oscillating.

C.1. Read the output of the VCO at the following location.

NAME	PCB Name	ASIC Name/Location	Value
Reference clock out	REFCLK	REFCLKOUT / Top side; pin N5	
Read Clock	READ_CLK	READCLK / Top side; pin N8.	Oscillating signal

C.2. Adjust the oscillation frequency of the VCO providing a control voltage at the on the following pin.

NAME	PCB Name	ASIC Name/Location	Value
VCO Control voltage	VCO_CTRL_FILT	VCOCTRL / Right side; pin N23.	0 - 1.2V

C.3. Measure the output of the VCO as stated in 1.3.1 while varying the VCO control voltage.

D. Connect All Bias and Threshold Voltages

D.1. Bias voltages are connected in the following pins.

NAME	PCB Name	ASIC Name/Location	Value
Input Buffer Bias	BUFF BIAS	WBUFFBIAS / Left side; Pin W19	0 - 1.2V
Discriminator bias	DISC BIAS	DISCBIAS / Left side/ pin W17	0 - 1.2V
Spare pin 2	SPR2	Not connected	
Spare pin 1	SPR1	Not connected	
Output read bias 2	BIAS2	READBIAS2 / Right side; Pin E12.	0 - 2.5V
Output read bias 1	BIAS1	READBIAS1 / Right side; Pin E14.	0 - 2.5V

D.2. Adjust the Threshold voltages.

NAME	PCB Name	ASIC Name/Location	Value
Threshold 1	THR _1	THRES1 / Left side; Pin W36	0 - 1.2V
Threshold 2	THR_2	THRES2 / Left side; Pin W32	0 - 1.2V
Threshold 3	THR_3	THRES3 / Left side; Pin W28	0 - 1.2V
Threshold 4	THR_4	THRES4 / Left side; Pin W24	0 - 1.2V
Threshold 5	THR_5	THRES5 / Left side; Pin W14	0 - 1.2V
Threshold 6	THR_6	THRES6 / Left side; Pin W10	0 - 1.2V
Threshold 7	THR_7	THRES7 / Left side; Pin W6	0 - 1.2V
Threshold 8	THR_8	THRES8 / Left side; Pin W2	0 - 1.2V

E. Other Inputs and Outputs

NAME	PCB Name	ASIC Name / Location	Value

Trigger In	TRIG IN	TRIGERIN / Top side; Pin N9	?
Trigger Out	TRIG OUT	TRIGEROUT / Top side; Pin N7	?

F. Connect SPI pins

NAME	PCB Name	ASIC Name / Location	Value
SPI clock	SCLK	SPICLK / Bottom side; pin S5	2.5 Digital
SPI Reset	SRST	RESET / Bottom side; pin S6	2.5V Digital
Peripheral out / Controller in	POCI	POCI / Bottom side; pin S7	2.5 V Digital
Peripheral in / Controller out	PICO	PICO / Bottom side; pin S9	2.5 VDigital

F.1. Send a Writing Command

F.2. Send a Reading Command

G. Connect ideal signals to the inputs

NAME	PCB Name	ASIC Name / Location	Value
Input signal channel 1	CH 1 / Rounded side of PCB	SIGNAL 1 / Left side; Pin W37	0-1.2V
Input signal channel 2	CH 2 / Rounded side of PCB	SIGNAL 2 / Left side; Pin W33	0-1.2V
Input signal channel 3	CH 3 / Rounded side of PCB	SIGNAL 3 / Left side; Pin W29	0-1.2V
Input signal channel 4	CH 4 / Rounded side of PCB	SIGNAL 4 / Left side; Pin W25	0-1.2V
Input signal channel 5	CH 5 / Rounded side of PCB	SIGNAL 5 / Left side; Pin W15	0-1.2V
Input signal channel 6	CH 6 / Rounded side of PCB	SIGNAL 6 / Left side; Pin W11	0-1.2V
Input signal channel 7	CH 7 / Rounded side of PCB	SIGNAL 7 / Left side; Pin W7	0-1.2V
Input signal channel 8	CH 8 / Rounded side of PCB	SIGNAL 8 / Left side; Pin W3	0-1.2V

H. Read the outputs

NAME	PCB Name	ASIC Name / Location	Value
Output readout 1	CH 1 / right side of PCB	READOUT1 / Right side; pin E3	0-2.5V
Output readout 2	CH 2 / Right side of PCB	READOUT2 / Right side; pin E7	0-2.5V

Output readout 3	CH 3 / Right side of PCB	READOUT3 / Right side; pin E11	0-2.5V
Output readout 4	CH 4 / Right side of PCB	READOUT4 / Right side; pin E15	0-2.5V
Output readout 5	CH 5 / Right side of PCB	READOUT5 / Right side; pin E27	0-2.5V
Output readout 6	CH 6 / Right side of PCB	READOUT6 / Right side; pin E31	0-2.5V
Output readout 7	CH 7 / Right side of PCB	READOUT7 / Right side; pin E35	0-2.5V
Output readout 8	CH 8 / Right side of PCB	READOUT8 / Right side; pin E39	0-2.5V

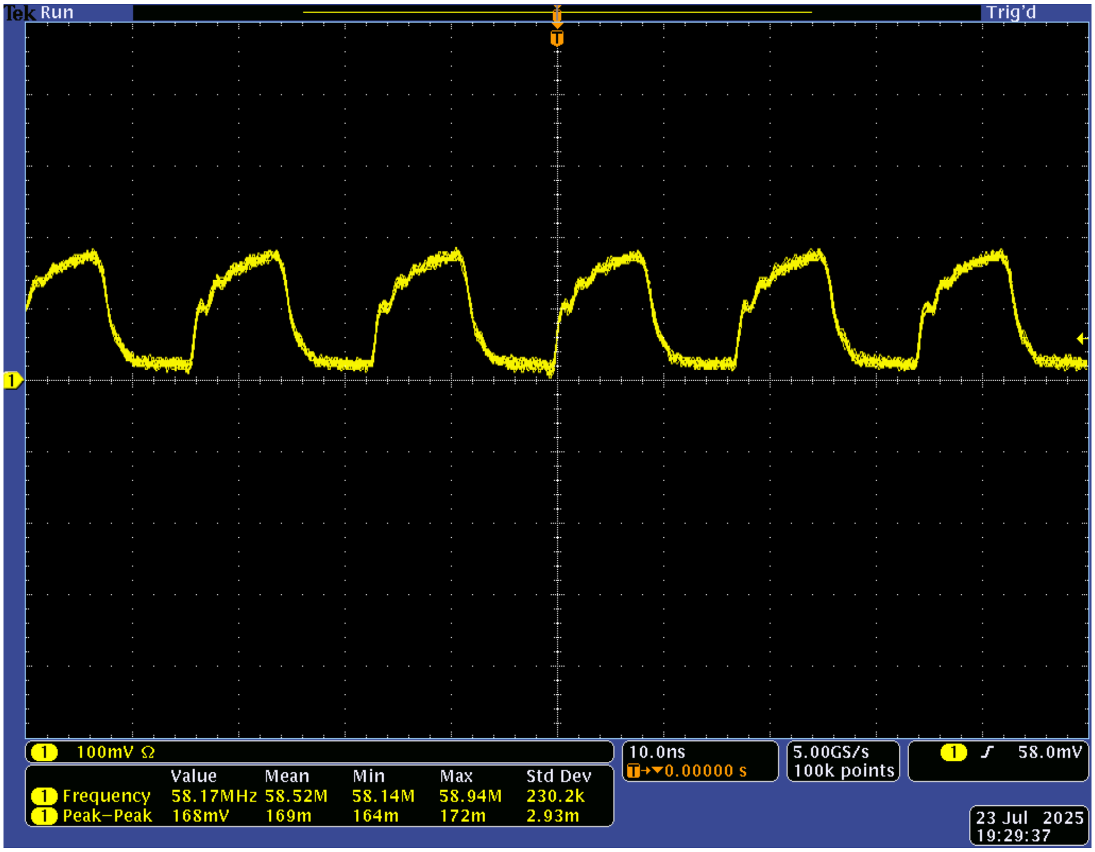
I. Power test:

The chip was powered, and it did not burn. There are some shorts between AVDD, VCOVDD, and DVDD that do not cause a major issue since all of them are 1.2V. When VCOVDD and DVDD are turned on, the total added current drawn from both is ~8mA. From DVDD25 the current drawn is ~4mA.

For the second chip, these observations are roughly the same. VCOVDD and DVDD combined is ~7.8mA. VCOVDD is ~4.6mA. DVDD is ~3.2 mA. DVDD2.5 is ~3.8mA.

J. VCO Test:

The PSEC5 chip requires VCOVDD, DVDD and DVDD25 supply voltages to be on in order to read the divided clock generated by the VCO. Figure 1 shows the output of the VCO that exhibits a frequency of ~58.17MHz. If VCO output was divided by 64, this would mean that the VCO is oscillating at a frequency of ~3.712GHz.



1 100mV Ω

	Value	Mean	Min	Max	Std Dev
1 Frequency	58.17MHz	58.52M	58.14M	58.94M	230.2k
1 Peak−Peak	168mV	169m	164m	172m	2.93m

10.0ns
T→▼0.00000 s

5.00GS/s
100k points

1 ⨍ 58.0mV

23 Jul 2025
19:29:37

Figure 1: Divided VCO output.

The output of the VCO is robust to DVDD and DVDD25 variation. As expected the VCO supply voltage (VCOVDD) affects the frequency of the oscillation. Lowering the supply by 10% increases the oscillation by roughly 1%. Figure 2 depicts the behaviour of the output frequency due to supply variations.

The VCO_ctrl voltage, as expected, has a significant effect on the control of the VCO oscillation frequency. As shown in Figure 3, a frequency variation of ~4.3MHz for a 0-1.2V variation on the control voltage, approximately 7%.

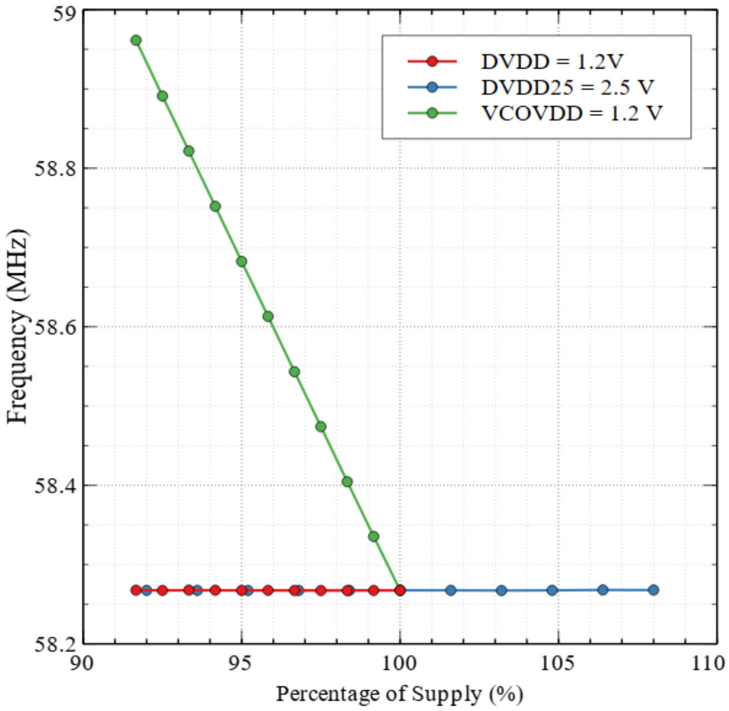


Figure 2: Supply voltages variations.

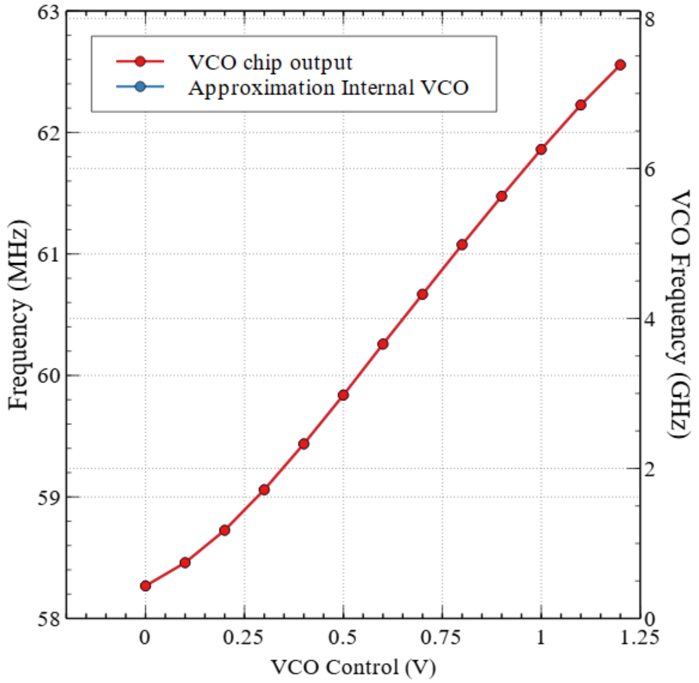


Figure 3: Frequency Variation due to VCO voltage control.

The jitter was approximated by measuring the variation of the rising edge of one clock cycle compared to an n-clock cycle after it. Figure 4 shows the range of the variation calculated by the oscilloscope as the difference between maximum minus minimum and the standard deviation over several thousand measurements. The period of the clock was T=~17.24ns and the measurements were taken for the 1, 2, 4, 8,...1024 that represent the time T, 2T, 4T,..., 1024T with a fixed value VCOCtrl=0V.

The range includes the negative (under the expected value) and positive (above the expected value) variations of the expected value. Figure 5 shows the graphical representation of the variation of half the range, either negative or positive.

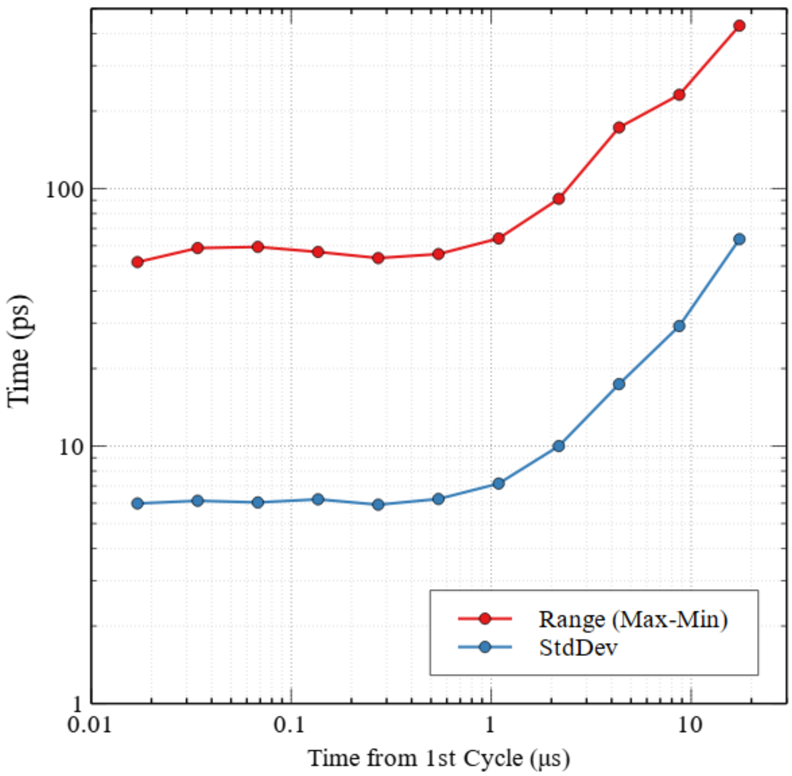


Figure 4: Range variation and standard deviation for rising edge of two different clock cycles with VCOCtrl=0V.

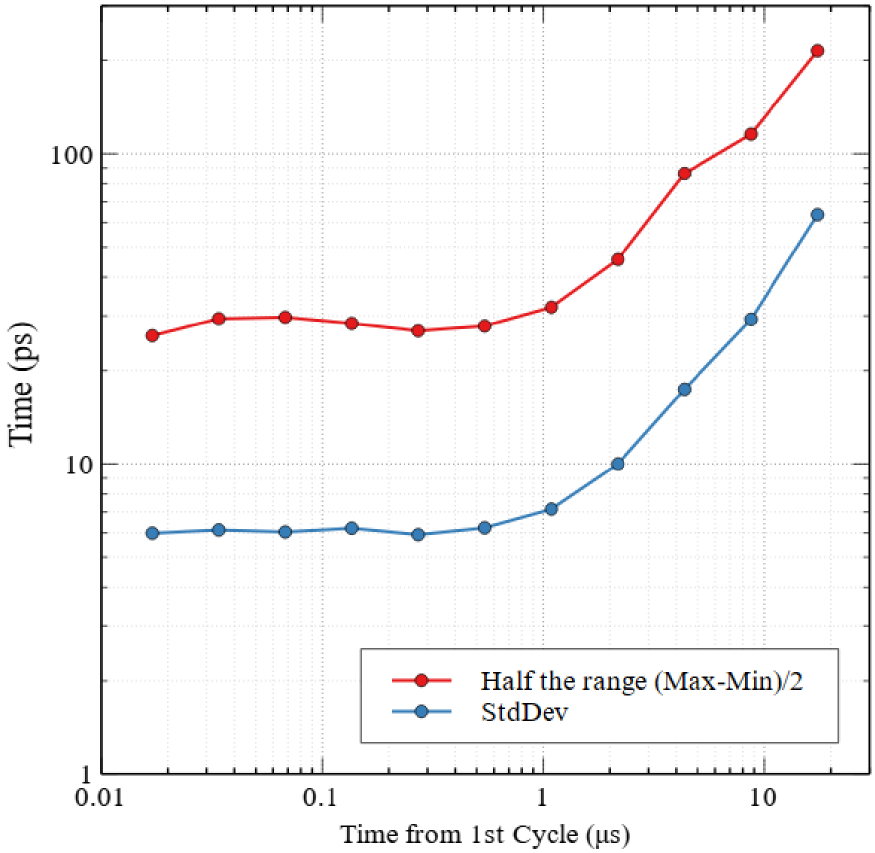


Figure 5: Variation of half the range and standard deviation for rising edge of two different clock cycles with VCOCtrl=0V.

K. SPI Test:

- VCO Digital Band register of SPI seems nonfunctional
- PLL Division Ratio register provides different frequency divisions of internal clock, if differently than the peripheral guide
- Known division ratios (256, 128(40MHz), 64, 32, 16) indicate that pre-division frequency is 1.6GHz
- Correction after switching SPI mode: VCO Digital Band register changes frequency within a roughly +0% to +20% range

In addition to the setup from section 6.1, an Arduino controller is then attached to the SCLK, SRST, PICO, and POCI pins. All other external pins were floating. From here, the SPI periphery's ability to receive instructions can be tested. If a signal that causes a frequency change is sent, the result will be unreliable unless an external reset has overwritten the initial state of the REFCLK just before sending the instruction. As such, a reset signal will be sent before trying to change the clock. The REFCLK can be asynchronously reset back to a low value (20mV) by sending a high input on SRST.

Correction after switching SPI mode to zero: In addition to the setup from section 6.1, an Arduino controller is then attached to the SCLK, SRST, PICO, and POCI pins while all other external pins are left floating. From here, the SPI periphery's ability to receive instructions can be tested.

K.1. VCO Digital Band Test

- VCO Digital Band (reg-62) only reliable response was to force reference clock low.

Firstly, the VCO Digital Band (r-62) was tested. After powering the chip, single bytes were sent to the register to see if there would be any result. Regardless of which command was sent, the result was a logic low. The same result was seen whether the REFCLK pin was initially some given frequency or a logic low. Then, to see if there were any instructions that would see different results, Arduino code was made to rapidly cycle through every possible instruction. Temporary logic highs were seen while cycling quickly but when checked thoroughly, these temporary highs could not be reliably reproduced by sending the instructions that caused it during the cycling. Clearly, the operation of the VCO Digital Band did not work, let alone remotely close to how it should, so it was decided that moving on to testing a different register was appropriate. Repeating this test for the second board saw the exact same behavior.

K.2. Clock Divider Control Test

- Division Ratio (reg-63) can be used to change the frequency shown on the REFCLK

- Last 5 bits of byte data sent to register 63 control which signal results by 1 of those 5 bits being high.

- The Division ratio can produce 5 different clock signals (6.3, 12.6, 25.3, 50.6, 101MHz) which indicates that the undivided clock speed is 1.6GHz

To test the division ratio register, the same procedure as described in 6.3 was used. Before any new instruction was sent to the register, an external reset was sent to the peripheral. The results of that testing can be seen in Table 1.

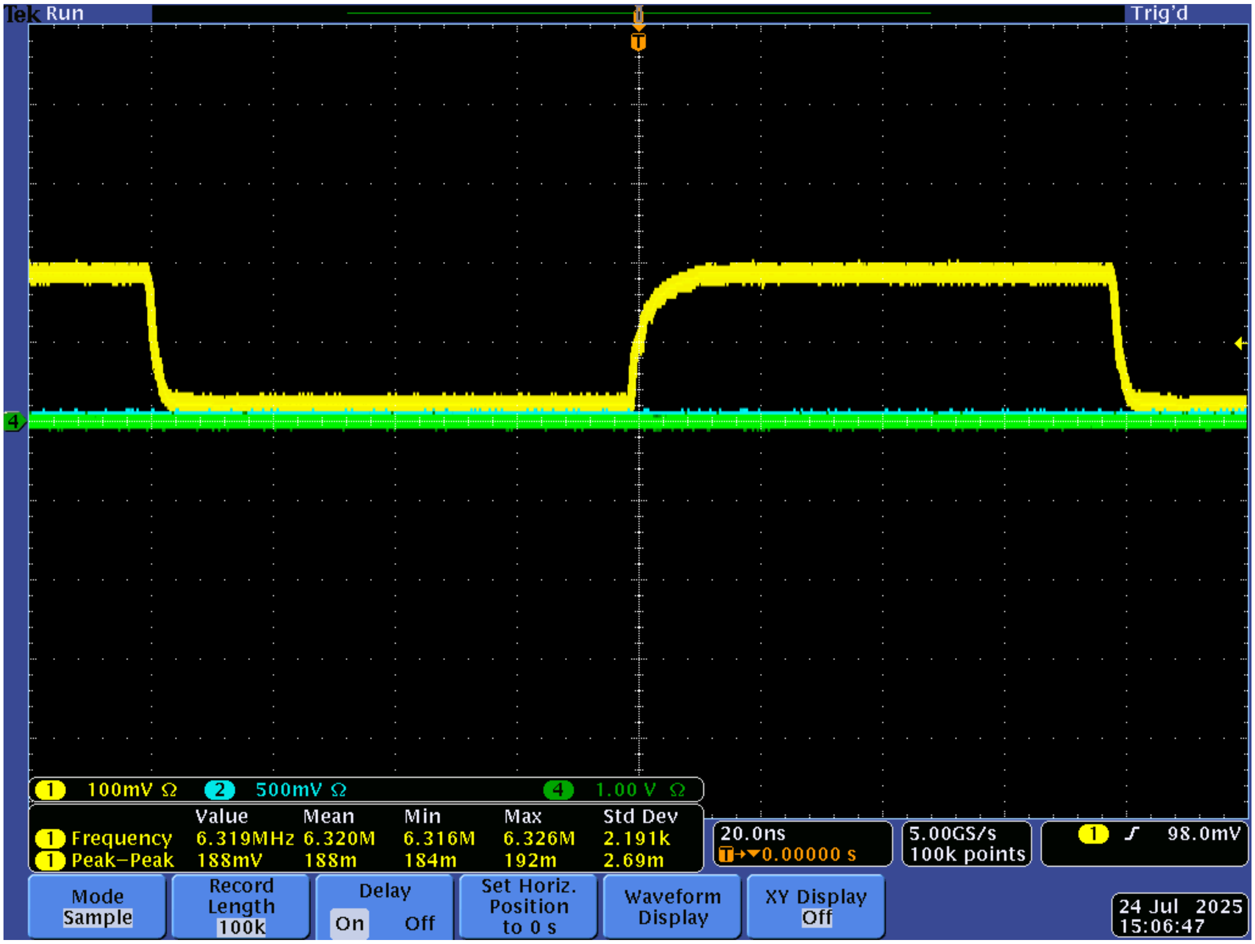
According to the peripheral document, the second byte of data should be sent in such that the first five bits (most significant to least) are irrelevant and the combination of the last 3 bits will determine the level of division with five different levels of division possible (256, 128(~40MHz), 64, 32, 16). However, this is not how the PLL division ratio seems to work after testing. As seen in Table 1, the first three bits are irrelevant to operation and then if only one of the following five is high then one of the five divisions will be shown. If more than one is high, the division will either be determined by the MSB or simply force the clock signal into a logic high. If none of those five bits stored in register 63 are high, then the clock signal will become a logic low; in this case all output transmission gates are disabled.

Specifically, the least significant bit of the five will cause the largest division ratio while moving the single high to more significant bits will cause smaller division ratios as seen in Table 1. Notably, the division ratios given in the SPI peripheral guide combined with these results mean that the undivided clock speed is 1.6GHz. Images of the high and low frequency edge cases can be seen in Figure 7 and Figure 8.

Varying instruction to PLL Division Ratio Register				
			Board 1	Board 2
Hexadecimal	Binary	Decimal	REFCLK Frequency (in MHz)	REFCLK Frequency (in MHz)

Varying instruction to PLL Division Ratio Register				
3F00	0000 0000	16128	LOW	LOW
3F01	0000 0001	16129	6.325	6.533
3F02	0000 0010	16130	12.65	13.09
3F03	0000 0011	16131	HIGH	HIGH
3F04	0000 0100	16132	25.35	26.16
3F05	0000 0101	16133	25.25	26.18
3F06	0000 0110	16134	HIGH	HIGH
3F07	0000 0111	16135	HIGH	HIGH
3F08	0000 1000	16136	50.55	52.26
3F09	0000 1001	16137	50.61	52.48
3F0A	0000 1010	16138	HIGH	52.35
3F0B	0000 1011	16139	50.58	52.38
3F0C	0000 1100	16140	HIGH	HIGH
3F0D	0000 1101	16141	HIGH	HIGH
3F0E	0000 1110	16142	HIGH	HIGH
3F0F	0000 1111	16143	HIGH	HIGH
3F10	0001 0000	16144	101.1	104.8
3F11	0001 0001	16145	101.0	104.7
3F12	0001 0010	16146	101.2	HIGH
3F13	0001 0011	16147	101.1	104.8
3F14	0001 0100	16148	100.9	104.7
3F15	0001 0101	16149	101.5	105.0
3F16	0001 0110	16150	101.2	HIGH
3F17	0001 0111	16150	101.1	HIGH

Table 1: Clock Divider Test of Division Ratio register 63 (3F) with the bit values that cause all 5 divisions



Tek Run

Trig'd

1 100mV Ω 2 500mV Ω 4 1.00 V Ω

	Value	Mean	Min	Max	Std Dev
1 Frequency	6.319MHz	6.320M	6.316M	6.326M	2.191k
1 Peak−Peak	188mV	188m	184m	192m	2.69m

20.0ns
T→▼0.00000 s

5.00GS/s
100k points

1 ʃ 98.0mV

Mode Sample

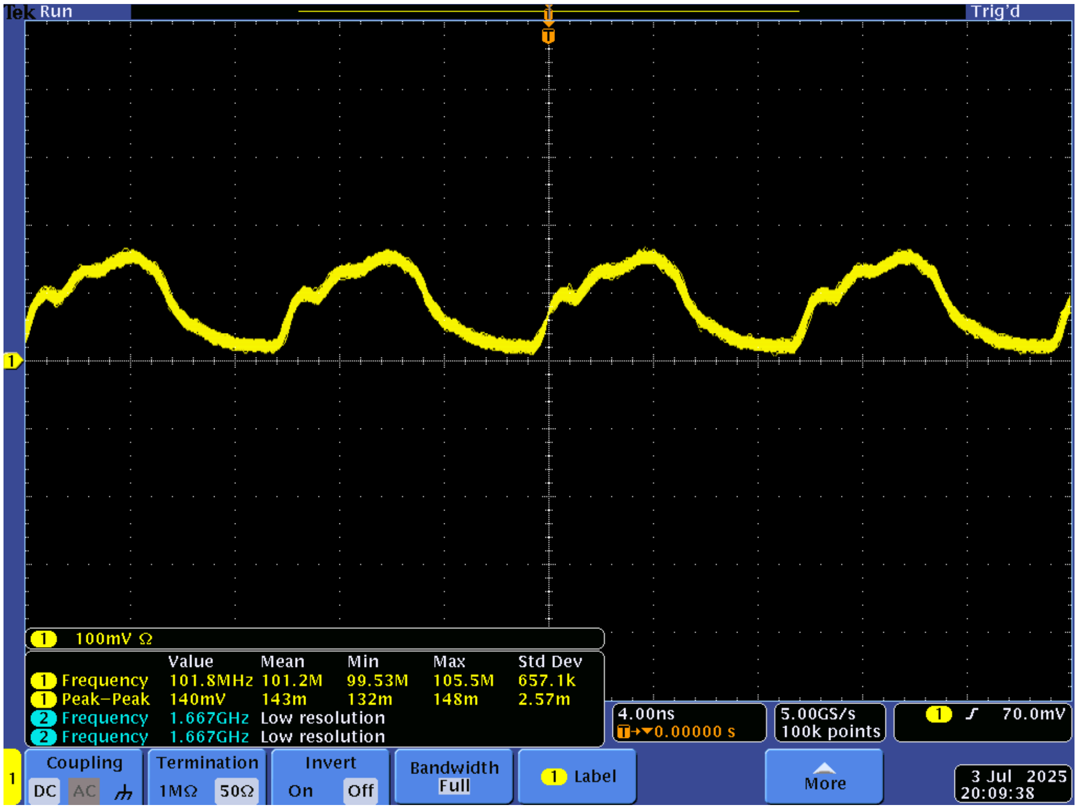
Record Length 100k

Delay On Off

XY Display Off

24 Jul 2025
15:06:47

Figure 6: Result of sending hex01 to the division ratio register



```
1  100mV Ω
             Value     Mean    Min     Max     Std Dev
1 Frequency  101.8MHz  101.2M  99.53M  105.5M  657.1k
1 Peak-Peak  140mV     143m    132m    148m    2.57m
2 Frequency  1.667GHz  Low resolution
2 Frequency  1.667GHz  Low resolution

4.00ns          5.00GS/s      1  ʃ  70.0mV
T→▼0.00000 s    100k points

3 Jul  2025
20:09:38
```

Figure 7: Result of sending hex10 to the division ratio register

K.3. POCI Test

All power supplies are ON.

The test was to write to Reg 63 (clock division ration control) twice. When writing the value 0x08, the second time writing to it, it will read 0x04. The experiment was repeated with the value 0x10 and the value read was 0x08.

Taking the setup with the arduino connected in 6.3, the AVDD and AVDD25 pins were also connected. This means AVDD, DVDD, VCOVDD, DVDD25, AVDD25, VCO_CTRL, and the spi pins were all connected with the first 3 at 1.2 V, the next 2 at 2.5 V, VCO_CTRL at 0V, and the SPI pins using a logic high of 2.5 V.

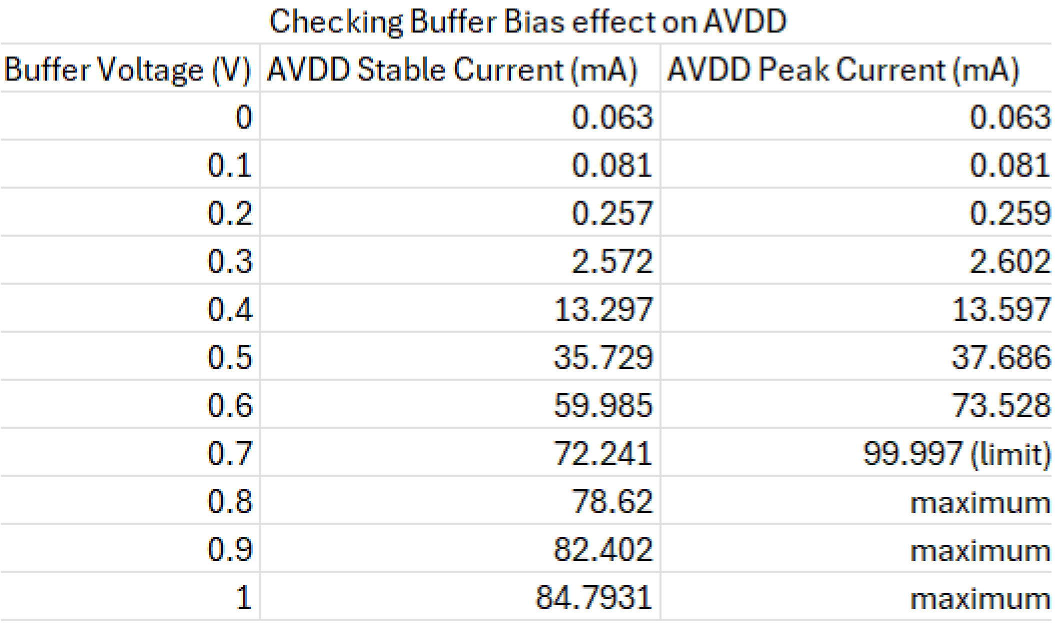
To test the POCI output, several instructions were sent to the Trigger Channel Mask. hex0100 (and hex01FF) was sent to the SPI to test if any data was sent back along the peripheral output. However, there was no logic response recorded. The only result noted was that the peripheral output would increase slightly in voltage (from ~20mV to ~170mV - double check this value later) when the command is first sent after a reset but nowhere near large enough to cause a logic change.

Observations: With additional testing it seemed like the slight voltage rise occurred after sending two instructions following the reset regardless of what the two instructions were or the register they were sent to. This happened to be the case for the testing procedure because we sent a reset, then the first instruction after was the mask values and the second was the start instruction. I saw the same result when sending in any two commands like sending the mask values twice or just sending the start command twice.

For the second board, the slight voltage rise of POCI also occurred but the circumstances were slightly different. The voltage increased from roughly 0 V to 0.7 V upon sending the hex01FF a second time without an external reset. This held true even if there was another instruction between them.

K.3.1. Power Bias Test

At that point, the powering of buffer bias caused a high current on AVDD - well in excess of the 10-20mA being used - which caused concerns over a possible short. To check whether this was caused by a short, the current draw change was measured with various voltages of buffer bias and recorded in Table 2. It was concluded that this high current draw was just the proper operation of the buffer bias rather than a short.



Checking Buffer Bias effect on AVDD

Buffer Voltage (V)	AVDD Stable Current (mA)	AVDD Peak Current (mA)
0	0.063	0.063
0.1	0.081	0.081
0.2	0.257	0.259
0.3	2.572	2.602
0.4	13.297	13.597
0.5	35.729	37.686
0.6	59.985	73.528
0.7	72.241	99.997 (limit)
0.8	78.62	maximum
0.9	82.402	maximum
1	84.7931	maximum

Table 2: Testing how voltage across Buffer Bias effects AVDD current draw

Conclusion

The testing and characterization of the PSEC5 ASIC board revealed several important issues and behaviors critical to its application in high-speed waveform digitization. The VCO demonstrated reliable oscillation near 3.712 GHz, with frequency tunability influenced by both supply voltage and control input. While initial attempts to interface with the registers showed anomalous behavior, switching to the correct SPI mode resolved many issues and restored expected functionality.

Observations from the POCI response and threshold inputs suggest that there are some internal transistor issues that require further investigation. The significant current draw from buffer bias voltage, once mistaken for a short, was shown to be normal operational behavior,

Overall, the board design and power sequencing strategy proved robust, with no fatal shorts or damage upon repeated testing. These results validate the PSEC5 as a viable candidate for further development, while also providing critical insights for future iterations in both hardware and software control systems.

Acknowledgements

a. This manuscript has been authored by FermiForward Discovery Group, LLC under Contract No. 89243024CSC000002 with the U.S. Department of Energy, Office of Science, Office of High Energy Physics.

b. This work was supported in part by the U.S. Department of Energy, Office of Science, Office of Workforce Development for Teachers and Scientists (WDTS) under the Visiting Faculty Program (VFP).