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The ALPIDE pixel sensor chip for the upgrade of the ALICE Inner Tracking System

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ABSTRACT

The ALPIDE chip is a CMOS Monolithic Active Pixel Sensor being developed for the Upgrade of the ITS of the ALICE experiment at the CERN Large Hadron Collider. The ALPIDE chip is implemented with a 180 nm CMOS Imaging Process and fabricated on substrates with a high-resistivity epitaxial layer. It measures 15 mm × 30 mm and contains a matrix of 512 × 1024 pixels with in-pixel amplification, shaping, discrimination and multi-event buffering. The readout of the sensitive matrix is hit driven. There is no signaling activity over the matrix if there are no hits to read out and power consumption is proportional to the occupancy. The sensor meets the experimental requirements of detection efficiency above 99%, fake-hit probability below 10^{-5} and a spatial resolution of 5 μm. The capability to read out Pb–Pb interactions at 100 kHz is provided. The power density of the ALPIDE chip is projected to be less than 35 mW/cm^2 for the application in the Inner Barrel Layers and below 20 mW/cm^2 for the Outer Barrel Layers, where the occupancy is lower. This contribution describes the architecture and the main features of the final ALPIDE chip, planned for submission at the beginning of 2016. Early results from the experimental qualification of full scale prototype predecessors are also reported.

1. Introduction

The ALPIDE chip is a CMOS Monolithic Active Pixel Sensor (MAPS) that is being developed for a major upgrade of the Inner Tracking System (ITS) of the ALICE experiment at the CERN Large Hadron Collider [1]. The existing ALICE ITS will be replaced during the second Long Shutdown of the LHC (2019–2020) with a new detector entirely based on CMOS MAPS [2]. ALICE is the first experiment at LHC implementing a large silicon tracker with this technology.

The ITS Upgrade pursues four major objectives: (a) the impact parameter resolution will be improved by a factor of three combining the reduction of the radial distance of the innermost layer from the interaction point (from 39 mm down to 22 mm), an improvement of single point resolution due to a smaller pixel size, and a reduction of the material budget of the innermost layers (from 1.14%X_0 to 0.3%X_0); (b) the finer granularity and the addition of one detection layer (7 layers in place of the current 6) will improve tracking efficiency and transverse momentum resolution in the low p_t range; (c) the readout rate capability with Pb-Pb interactions shall reach 100 kHz, a factor of 100 improvement over the present readout capability; (d) it will be possible to remove and re-install the full detector for maintenance during the planned yearly shutdown.

The new ITS detector will consist of seven cylindrical sensing layers with radial coverage from 22 mm to 400 mm and z-lengths ranging from 27 cm to 1.5 m. The three innermost layers will constitute the Inner Barrel, while the other four will make the Outer Barrel. The total sensitive area is above 10 m^2 and will be equipped with ~24,000 pixel sensor chips for more than 12.5 billion pixels in total. The requirements on the new ITS pixel chip are summarized in Table 1.

2. The ALPIDE chip

The ALPIDE chip is implemented in a 180 nm CMOS Imaging Process provided by TowerJazz [3]. The circuits can be fabricated on substrates with a high-resistivity (> 1 kΩ cm) epitaxial layer on p-type substrate. Typical values for the thickness of the epitaxial layer are in the range between 18 and 30 μm. A charged particle crossing the sensor liberates free charge carriers in the material by ionization. The electrons released in the epitaxial layer can diffuse laterally while they remain vertically confined by potential barriers at the interfaces with the overlying p-wells and the underlying p-type substrate. The signal sensing elements are n-well diodes (~2 μm diameter). Their area is typically 100 times smaller than the pixel cell area. The electrons that reach the depletion volume of a diode (or carriers that are released directly inside it)

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Table 1
General requirements for the pixel sensor chip for the Upgrade of the ALICE Inner Tracking System. In parentheses: ALPIDE performance figure where above requirements.

Parameter	Inner barrel	Outer barrel
Chip dimensions (mm × mm)	15 × 30	
Silicon thickness (μm)	50	100
Spatial resolution (μm)	5	10 (5)
Detection efficiency	>99%	
Fake hit probability (evt^{-1} $pixel^{-1}$)	$<10^{-5}$ ($<<10^{-5}$)	
Integration time (μs)	<30(10)	
Power density (mW/cm^2)	<300(~ 35)	<100(~ 20)
TID radiation hardness[a] (krad)	2700	100
NIEL radiation hardness[a] (1 MeV n_{eq}/cm^2)	1.7×10^{13}	1×10^{12}
Readout rate, Pb–Pb interactions (kHz)	100	

[a] 10 × the radiation load integrated over the approved program (6 years of operation).

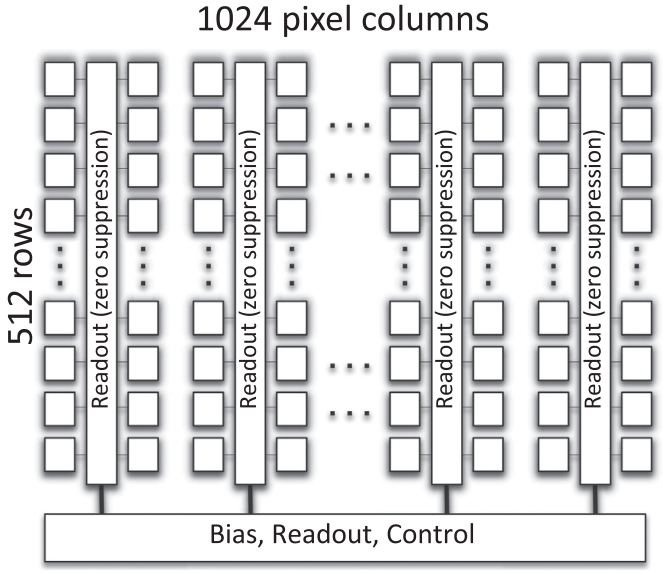

Fig. 1. Architecture of the ALPIDE chip.

induce a current signal at the input of the pixel front-end. The manufacturing process also provides a deep p-well layer that can be used to shield the epitaxial layer from the n-wells of the pmos transistors. These would otherwise compete with the sensing diodes in collecting the electrons, strongly impairing the charge collection. This feature permits the use of full CMOS circuits, including pmos transistors, in the active area. A reverse bias voltage can be applied to the substrate. This increases the depletion volume around the n-well collection diodes and reduces their capacitance. Both processes contribute to increase the S/N ratio.

The ALPIDE chip measures 15 mm by 30 mm and includes a matrix of 512 × 1024 pixel cells, each one measuring 29.24 μm × 26.88 μm ($z \times r\Phi$). Analog biasing, control, readout and interfacing functionalities are implemented in a peripheral region of 1.2 × 30 mm^2 (Fig. 1).

Each pixel cell contains a sensing diode, a front-end amplifier and shaping stage, a discriminator and a digital section (Fig. 2). In every pixel there is a pulse injection capacitor for injection of test charge in the input of the front-end. The digital section includes three hit storage registers (Multi-Event Buffer) and a pixel mask register.

The front-end and the discriminator are continuously active. They feature a non-linear response and their transistors are biased in weak inversion. Their total power consumption is 40 nW. The small signal gain of the front-end is 4 mV/e, the Equivalent Noise Charge is 3.9 *e*, the minimum threshold is below 100 *e*. The typical value of the capacitance of the sensing diode is 2.5 fF. The input capacitance of the front-end is below 2 fF. The output of the front-end has a peaking time of the order of 2 μs, while the discriminated pulse has a typical duration of 10 μs. The front-end and the discriminator act as an analogue delay line. The delay is longer than the latency of the first level trigger in ALICE and enables operating the chip in triggered mode.

A common threshold level is applied to all the pixels. The latching of the discriminated hits in the storage registers is controlled by a global strobe signal. On assertion of the strobe, an event frame is saved in one of the three frame storage slices.

The readout of the frame data from the matrix is zero-suppressed and is executed by circuits named Priority Encoders. There are 512 instances of this circuit, one every two pixel columns. The Priority Encoder provides to the periphery the address of the first pixel with a hit in its double column. Subsequently the storage element of the pixel is reset. This cycle is repeated until the addresses of all pixels initially presenting a valid hit at the inputs of a Priority Encoder have been transferred to the periphery. Each Priority Encoder is a fully combinatorial circuit and it is steered by sequential logic in the periphery during the readout of a matrix frame. It is implemented in a very narrow region between the pixels, extending vertically over the full height of the columns. There is no free running clock distributed in the matrix and there is no signaling activity if there are no hits to read out. The average energy needed to encode the address of a hit pixel is of the order of 100 pJ. Power is consumed proportionally to the readout rate and to the hit occupancy. The readout of the matrix consumes around 3 mW for nominal design values. The Priority Encoders also implement the buffering and distribution of readout and configuration signals to the pixels.

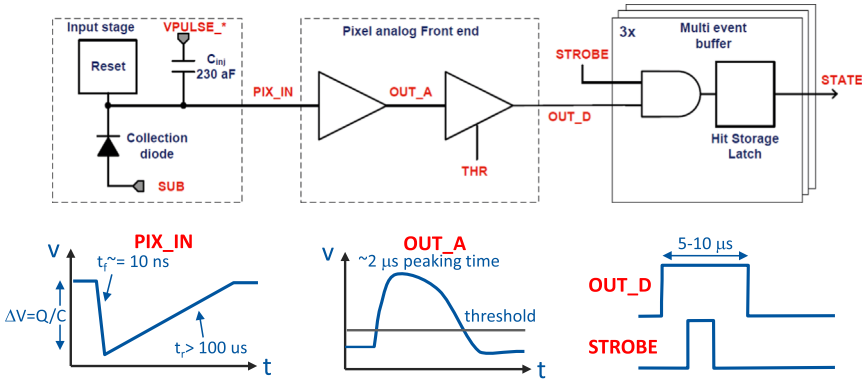

Fig. 2. Block diagram of the ALPIDE pixel cell.

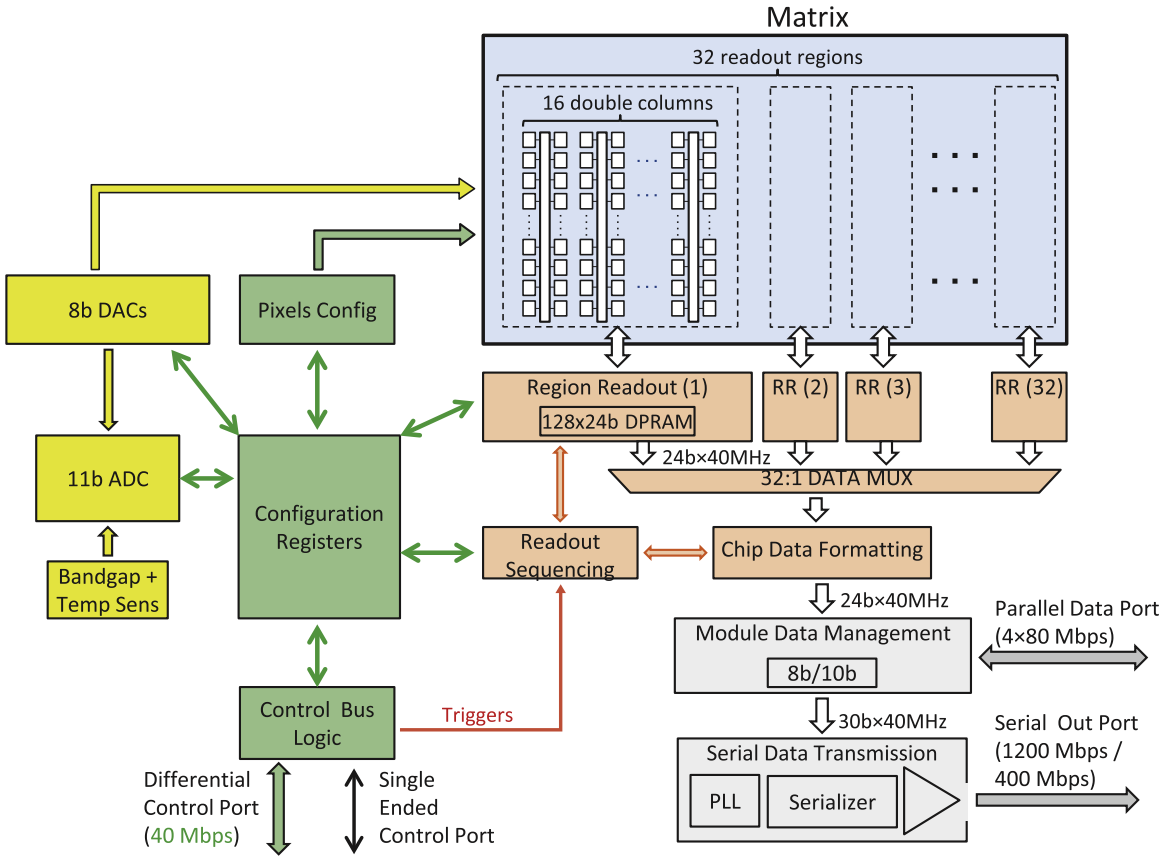

Fig. 3. Block diagram of the ALPIDE chip.

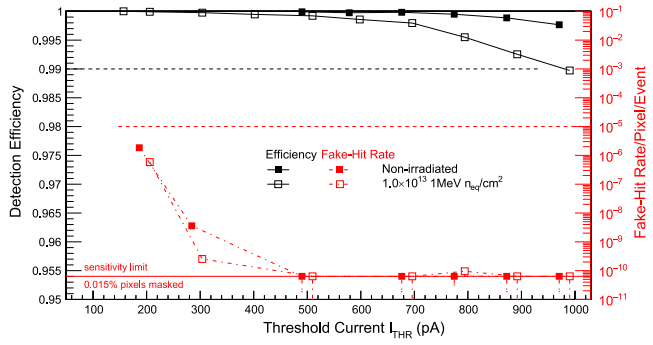

Fig. 4. Experimental results with the pALPIDE-2 full scale prototype chip. Detection efficiency (left axis) and fake-hit rate (right axis) vs. threshold setting. Beam tests at CERN PS with 6 GeV π^-. High resistivity epitaxial layer thickness: 25 μm. Substrate reverse bias: −6 V. Spacing between collection diode and surrounding wells: 2 μm.

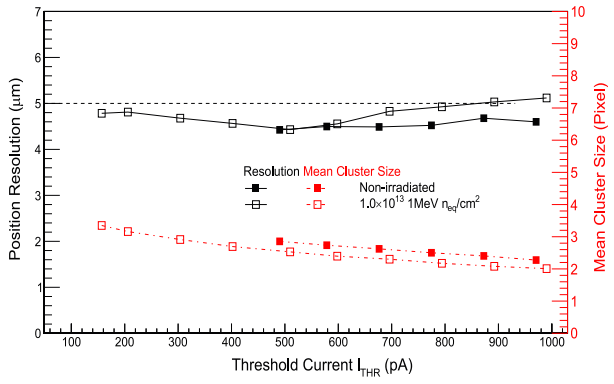

Fig. 5. Experimental results with the pALPIDE-2 full scale prototype chip. Position resolution (left axis) and mean cluster size (right axis) vs. threshold setting. Beam tests at CERN PS with 6 GeV π^-. High resistivity epitaxial layer thickness: 25 μm. Substrate reverse bias: −6 V. Spacing between collection diode and surrounding wells: 2 μm.

The 512 Double Columns and the corresponding Priority Encoders are functionally grouped in 32 submatrices (Fig. 3). There are 32 corresponding region readout modules in the chip periphery, each one executing the readout of a submatrix. The 16 Double Columns inside each region are read out sequentially, while the 32 submatrices are read out in parallel.

The region readout modules include de-randomizing memories and perform additional data reduction and formatting. Two major readout modes are supported, one in which the strobing and readout are triggered externally and a second one in which frames are continuously integrated and read out, with programmable duration of the strobe assertion interval.

Data can be transmitted on two different readout ports. A 1.2 Gb/s serial output port with differential signaling is intended to be the largest capacity data readout interface. A bidirectional parallel data port with single-ended signaling is also present, with a capacity of 320 Mb/s.

The ALPIDE chip has custom designed control interfaces. There is a differential control port supporting bi-directional (half duplex) serial signaling at 40 Mb/s on differential links. A second single ended control line is also available. The control features enable the interconnection of multiple chips on a multi-point control bus with a hierarchical topology. The control bus is also used to distribute broadcast commands to the chips, most notably the trigger messages.

The periphery of the chip contains fourteen 8b analog DACs for

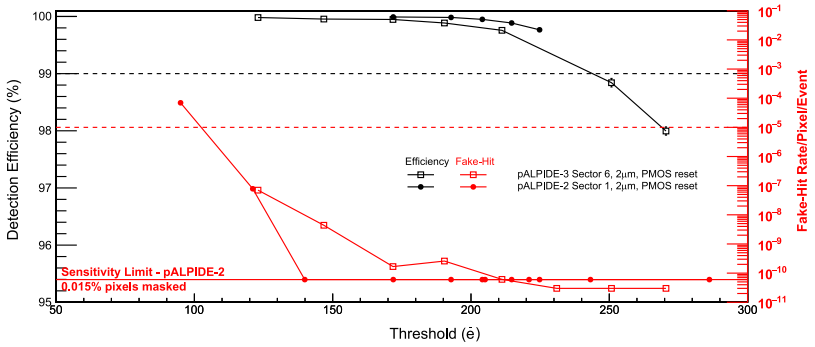

Fig. 6. Preliminary experimental results with the pALPIDE-3 full scale prototype chip. Detection efficiency (left axis) and fake-hit rate (right axis) vs. threshold setting. Comparison with the measurements with pixels of similar characteristics of pALPIDE-2. Beam tests at CERN PS with 6 GeV π^-. High resistivity epitaxial layer thickness: 25 μm. Substrate reverse bias: −6 V. Spacing between collection diode and surrounding wells: 2 μm.

the biasing of the pixel front-ends. An ADC with 11 bit resolution is available for monitoring and testing purposes. The analog section of the periphery also contains a bandgap reference and a temperature sensing circuit.

The digital circuits of the periphery are implemented with mitigation techniques against Single Event Upsets and Transient effects induced by radiation. The minimization of the power consumption of the digital periphery was pursued employing systematically clock gating techniques.

The ALPIDE chip has specific features designed to simplify the integration of multi-chip modules. The ITS Inner Barrel Module will include nine chips. They will share a common differential control bus and a clock distribution bus. Each chip will transmit its own data off-detector at maximum capacity (1200 Mbps) on the high speed data output port.

The ITS Outer Barrel Module will contain 14 chips, arranged in two rows of seven. One chip in each row will play the role of Master. Only the Master chips communicate electrically with the external world. Each of the two Master chips connects to six neighbor chips (Slaves), forwards them the main clock and bridges the control transactions. The Slave chips use a shared parallel local bus to send their data to the Master acting as data collector. The Master transmits the assembled data packets off-detector on its serial output, driving dedicated point-to-point links. In this scenario, a lower bit rate is used (400 Mb/s). Grouping of data of neighboring chips is feasible in the four Outer Barrel layers where the occupancy is lower. This scheme achieves a reduction in the total number of control and data links, and a reduction in the power consumption.

The analog power consumption of the ALPIDE chip is typically 25 mW. The digital periphery and the readout of the matrix consume power in proportion to the frame readout rate and to the occupancy. For nominal design values, the consumption of the periphery of a chip on the innermost layer is expected to reach 54 mW. In the case of chips on the Outer Barrel layers, it is expected to reach a maximum of 44 mW. The output serial link is driven by a Data Transmission Unit including a PLL, Serializer and a Line Driver stage. The expected power consumption of this block alone reaches 68 mW. However, in the case of Slave chips it is disabled. Based on the previous estimates, the power consumption density is expected to be less than 35 mW/cm^2 for the ITS Inner Barrel Modules and below 18.5 mW/cm^2 for the Outer Barrel Modules.

3. Experimental results with prototypes

Small scale chips (< 20 mm^2) were developed in 2012 and 2013 to characterize the technology and to perform initial R&D. Three full scale (30×15 mm^2) prototypes of the ALPIDE chip have then been implemented: pALPIDE-1 (2014), pALPIDE-2 (April 2015) and pALPIDE-3 (October 2015). These chips included variants of the pixel cell and an increasingly larger subset of all the required features. With respect to the ancestor pALPIDE-2, the pALPIDE-3 chip includes the three stages Multi Event Buffer in the pixels and the high speed serial Data Transmission Unit in the periphery.

The characterization of pALPIDE-2 chips with beam tests has demonstrated that a detection efficiency above 99% is maintained over a large range of threshold settings (Fig. 4). At the same time, the fake-hit probability remains orders of magnitude smaller than the requirement ($\lambda_{\text{fake}} << 10^{-5}$). The spatial resolution is better than 5 μm and the average cluster size is between 2 and 3 pixels (Fig. 5). These performance figures are maintained after irradiating the sensors with a non-ionizing dose of 1.7×10^{13} (1 MeV n_{eq}/cm^2).

Systematic characterization and beam tests campaigns with the pALPIDE-3 chip are ongoing as of February 2016. Twenty-five chips out of 29 were found to be fully functional after wire bonding them on carriers. The new Multi-Event Buffer circuits are functional. Tests of the Data Transmission Unit on a test chip and on the pALPIDE-3 chip have shown that this new block is functional. However, an excess of jitter is observed on the pALPIDE-3 chip. This is correlated with the switching of large fan-out global signals and is caused by coupling of digital supply noise. Corrections of this hiccup are planned for the final design iteration and will consist of the reduction of the sensitivity of the block and of the separation of the on-chip power domains.

The pALPIDE-3 includes variants of the pixel cell very similar to variants that were already prototyped in pALPIDE-2. Preliminary results from the beam tests with pALPIDE-3 are available and allow a comparison of the performance of pixels with similar characteristics. An example of this comparison is shown in Fig. 6. The pixels in pALPIDE-3 show detection and noise performances matching those of the corresponding pixels in pALPIDE-2, without any observable degradation. These preliminary results already indicate that the key requirements of detection efficiency, spatial resolution and fake-hit rate are also met by pALPIDE-3.

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