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Cryo-CMOS Bias-Voltage Generation and Demultiplexing at mK Temperatures for Large-Scale Arrays of Quantum Devices

JOB VAN STAVEREN[1,2], LUC ENTHOVEN[1,2], PETER LUKA BAVDAZ[1,3,6], MARCEL MEYER[1,3,7], CORENTIN DÉPREZ[1,3], VILLE NUUTINEN[4], RUSSELL LAKE[4], DAVIDE DEGLI ESPOSTI[1,3], CORNELIUS CARLSSON[1,3,8], ALBERTO TOSATO[1,3], JIANG GONG[1,2,9], BAGAS PRABOWO[1,2] (Graduate Student Member, IEEE), MASOUD BABAIE[1,2,5] (Senior Member, IEEE), CARMEN G. ALMUDEVER[1,2,10] (Member, IEEE), MENNO VELDHORST[1,3], GIORDANO SCAPPUCCI[1,3], AND FABIO SEBASTIANO[1,2] (Senior Member, IEEE)

[1]QuTech, Delft University of Technology, 2628 CJ Delft, The Netherlands
[2]Department of Quantum and Computer Engineering, Delft University of Technology, 2628 CD Delft, The Netherlands
[3]Kavli Institute of Nanoscience Delft, Delft University of Technology, 2628 CJ Delft, The Netherlands
[4]BlueFors Oy, 00370 Helsinki, Finland
[5]Department of Microelectronics, Delft University of Technology, 2628 CJ Delft, The Netherlands
[6]Intel Corporation, Technology Research Group, Hillsboro, OR 97124 USA
[7]Universität Innsbruck, Institut für Experimentalphysik, 6020 Innsbruck, Austria
[8]Department of Engineering Science, University of Oxford, OX1 3PJ Oxford, U.K.
[9]Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China, Shenzhen 518060, China
[10]Departamento de Informática de Sistemas y Computadores, Universitat Politècnica de València, 46022 Valencia, Spain

Corresponding authors: Job van Staveren; Fabio Sebastiano (e-mail: j.vanstaveren@tudelft.nl; f.sebastiano@tudelft.nl).

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ABSTRACT The rapidly growing number of qubits in semiconductor quantum computers requires a scalable control interface, including the efficient generation of dc bias voltages for gate electrodes. To avoid unrealistically complex wiring between any room-temperature electronics and the cryogenic qubits, this article presents an integrated cryogenic solution for the bias-voltage generation and distribution for large-scale semiconductor spin-qubit quantum processors. A dedicated cryogenic CMOS (cryo-CMOS) demultiplexer and a cryo-CMOS dc digital-to-analog converter (DAC) have been developed in a 22-nm fin field-effect transistor process to control a codeveloped 2-D array designed with 648 single-hole transistors. Thanks to the dissipation below 120 μW, the whole system operates at temperatures below 70 mK in a custom-built electrical/mechanical infrastructure embedded in a standard single-pulse-tube dilution refrigerator. The bias voltages generated by the cryo-CMOS DAC are demultiplexed to sample-and-hold structures, allowing to store 96 unique bias voltages over a 3 V range with a voltage drift between 60 μV/s and 18 mV/s. This work demonstrates a tight integration at mK temperatures of cryo-CMOS bias generation and distribution with a dedicated large-scale quantum device. This showcases how this approach simplifies the wiring to the electronics, thus facilitating the scaling up of quantum processors toward the large number of qubits required for a practical quantum computer.

INDEX TERMS Fin field-effect transistor (FinFET), chip-to-chip bonding, crossbar, cryogenic, cryogenic CMOS (cryo-CMOS), demultiplexing, digital-to-analog converter (DAC), dilution refrigerator, quantum computing, scaling, single-hole-transistor (SHT).

I. INTRODUCTION

On the road toward fault-tolerant quantum computing, significant steps are being made in developing high-quality quantum bits (qubits) as the fundamental computational elements. Unlike classical bits, solid-state qubits typically need to be operated at temperatures below 1 K. Due to the physical size of the refrigerator, the cabling that carries the control signals to the qubits is commonly >2 m. At the same time, a quantum computer capable of solving problems untractable by classical computers should comprise thousands or even millions of qubits. The cryogenic operation combined with such a large number of qubits demands enormous amounts of wiring. In addition, unlike classical computer architectures, each qubit requires individual readout and control lines that are typically supplied from room temperature. However, several factors, such as the limited space in the cryostat, the wiring heat load consuming a significant fraction of the available cooling power at the lowest temperature stages, and the limits in wiring reliability, represent significant challenges in the scaling of quantum computers toward a practical application.

Whereas multiplexing strategies can provide some reduction in the amount of wiring, the generally accepted direction for overcoming these bottlenecks lies in placing the control electronics at cryogenic temperatures next to the qubits. Thanks to its maturity, excellent scaling properties, high reliability, extremely large scale of integration, high performance, and wide operating temperature range, CMOS technology is one of the most promising enablers for the cryogenic control of qubits [2], [3]. In addition, various industrial CMOS technologies [4], [5], [6], [7] have been shown to be suitable for the development of semiconductor spin qubits, providing a promising path toward the monolithic integration of control electronics and qubits in CMOS as the ultimate solution for scalability. Most of the work on cryogenic CMOS (cryo-CMOS) control electronics addresses microwave-signal generation and qubit readout [8], [9], [10], [11], [12], [13], [14], [15]. However, the mW-power consumption typically associated with microwave electronics is significantly higher than the cooling power at the mK stage of a typical commercial dilution refrigerator (e.g., 400 μW at 100 mK for a BlueFors LD400 system [16]). As a result, microwave electronics must be placed at higher temperature stages, where the dilution refrigerator has a larger cooling power (e.g., at the 4 K stage). Due to these strict requirements on power consumption at the mK stage, prior work on control electronics for mK temperatures is scarcer [17], [18], [19], [20], [21], [22]. However, with quantum processors quickly approaching the scale of 1000 qubits per chip [21], [23], [24], [25], [26], [27], the wiring bottleneck at the mK stage may soon become a roadblock. For example, an increasing number of semiconductor spin qubits inherently requires a larger number of dc bias voltages. When going from individual control in a linear array to shared control in a 2-D array, the requirement on the number of bias voltages can be alleviated. Nevertheless, some form of individual control may still be required to compensate for variations in uniformity. As recently reported in [21], [27], and [28], a variation in gate voltage of several tens of millivolts up to multiple volts can be expected. A sufficient amount of independent bias voltages covering the range of variation is thus required. Full shared control may therefore still need improvements in device uniformity, and hence, some form of individual control is likely still required to compensate for these variations. In addition, having more control over the dc potential could potentially relax the radio frequency (RF) control requirements. Consequently, hundreds of bias voltages would still be required for thousands of qubits, thus creating a need for a scalable biasing solution.

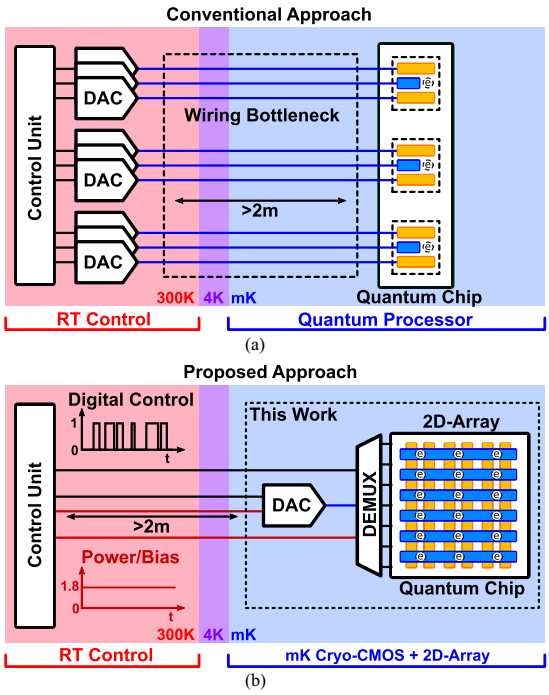

FIGURE 1. Simplified overview of the biasing strategy for a semiconductor spin-based quantum computing system employing the (a) conventional approach and the (b) proposed approach. Sensitive analog signals are indicated in blue, while the more robust digital and supply/bias lines are in black and red, respectively.

The conventional dc biasing approach for small-scale semiconductor spin processors is schematically depicted in Fig. 1(a) for a 1-D array of qubits, where each qubit is electrostatically defined by three gate electrodes. Each of the highly sensitive dc bias voltages is generated by a dedicated digital-to-analog converter (DAC) at room temperature and routed to the device using a dedicated >2 m long cable. Although this approach is extremely flexible and suitable for developing small-scale quantum processors, it is not intrinsically scalable, as in such architectures the number of independent control terminals and signals linearly scales with the number of qubits.

To circumvent that limitation, discrete CMOS demultiplexers using off-the-shelf commercial components

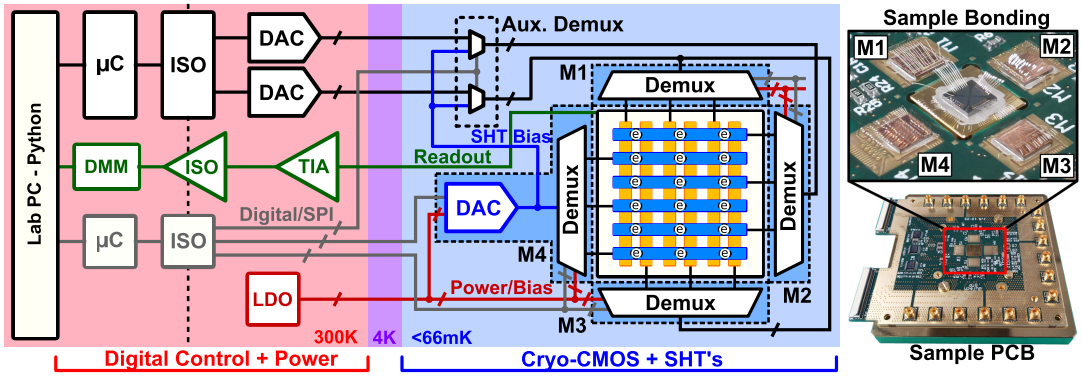

FIGURE 2. (a) Extended electrical overview from the proposed system. The plunger gates (blue) of the 2-D array are biased by M2 and M4, whereas the barrier gates (yellow) are biased by M1 and M3. For visibility, a simplified version of the 2-D array is shown in this figure. In the measurements, an array with 36 plunger gates and 18 pairs of barrier gates is used. (b) Photograph from the main sample PCB, highlighting the location and bonding from the cryo-CMOS chips to the quantum devices.

operating at mK temperatures have been demonstrated [29], [30]. Although useful for speeding up the characterization of large arrays of quantum devices, discrete demultiplexers are too bulky to support the scalability of quantum processors. Demultiplexers integrated in application-specific integrated circuits (ASIC) have overcome this limitation by demonstrating both RF-signal demultiplexing [20], [21], [22], [31] and dc-signal demultiplexing [18], [32], [33], [34], [35], [36], [37], either on a separate chip [18], [22], [34] or even on the chip that hosts the quantum devices [20], [21], [31], [32], [33], [35], [36], [37]. The demultiplexer has also been combined with a sample-and-hold (S/H) circuit, allowing to store the bias voltage on a hold capacitor and enabling time-multiplexed operation as well [17]. However, the bias voltage itself was still generated at room temperature, making synchronization between bias generation and demultiplexing more challenging, and thereby still posing limits to the system integration.

To generate the dc bias at cryogenic temperatures, cryo-CMOS DACs have been proposed for both 4 K [38] and mK temperatures [39] and have been tested in combination with an S/H circuit to operate only a single quantum device [18], [40]. Whereas Schreckenberg et al. [18] showed a scalable integration of a dc DAC, demultiplexer, and quantum device, the scale of the demonstration is currently limited to less than ten channels. In spite of all those recent advances, an integrated electronic system, including bias generation and demultiplexing at mK temperatures and capable of supporting a large array of quantum devices, has not yet been experimentally demonstrated.

To bridge this gap, this article presents a dc biasing approach using fully integrated dc bias generation and distribution on the same temperature stage as the quantum devices, as depicted in Fig. 1(b). By placing the cryo-CMOS demultiplexer and dc DAC at the mK stage of a dilution refrigerator next to the quantum devices and by using an S/H approach, the wiring can be significantly simplified, thus facilitating the scaling to a large number of quantum devices. Moreover, only digital signals and a few static supply/reference voltages are required from room temperature, which reduces the number of sensitive signals compared to the conventional approach, thus improving reliability, integration, and signal purity. To demonstrate the potential of this approach, a dedicated quantum sample was developed, consisting of a 2-D array of 648 single hole transistors (SHTs), controlled via shared gates and arranged in a crossbar architecture, thus providing an additional benefit in terms of scaling [30] compared to a 1-D array. This work demonstrates a scalable, large-scale system integration of a cryo-CMOS DAC, cryo-CMOS demultiplexer, and crossbar array, all at the same mK stage.

The rest of this article is organized as follows. Section II presents the design and implementation of the proposed approach, including the design of the 2-D array, demultiplexer, and dc DAC, followed by the verification and measurements in Section III. Future perspectives will be presented in Section IV. Finally, Section V concludes this article.

II. SYSTEM DESIGN

A simplified overview of the proposed system is presented in Fig. 2(a). It comprises a cryo-CMOS core placed at the mixing chamber (MXC) in the dilution refrigerator and operated at 66 mK and the support measurement/control setup at room temperature. No passive or active components at 4.2 K are used in this system. The heart of the system includes five ASICs: a quantum chip with 648 germanium SHTs arranged in a 2-D crossbar array fabricated within an academic cleanroom environment [41], three demultiplexer chips fabricated in a 22-nm fin field-effect transistor (FinFET) process (M1–M3), and fabricated in the same process, also a dc DAC integrated with a demultiplexer (M4). The outputs from all four demultiplexers are directly bonded to the quantum chip [see Fig. 2(b)]. The DAC output is both connected to M4's on-chip demultiplexer and also brought off-chip and distributed to the inputs of M1–M3, allowing the

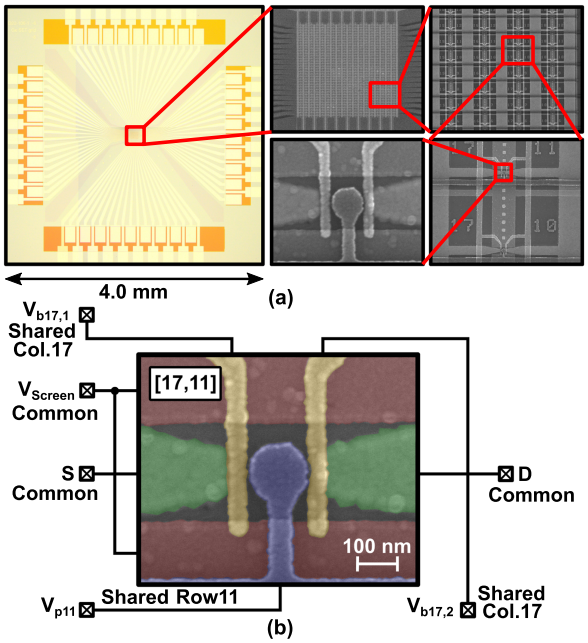

FIGURE 3. Overview of the 2-D array, showing (a) chip micrograph with SEM images as insets and (b) a false-colored SEM image showing the SHT unit cell, highlighting the plunger gate (blue), barrier gates (yellow), ohmics (green), and screening gate (red).

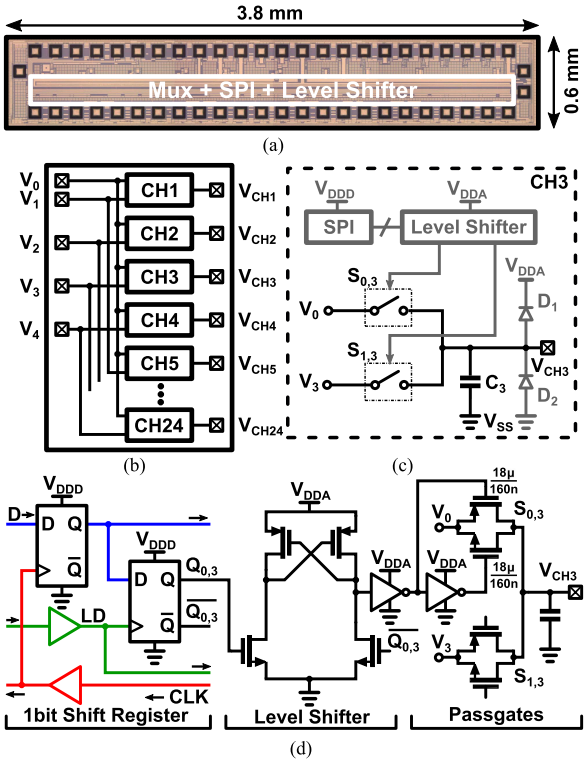

FIGURE 4. Overview of the design of the demultiplexer used for M1–M3, showing (a) the chip micrograph, (b) channel configuration, (c) functional schematic of a typical channel, and (d) a transistor-level schematic of a single channel, where only the control logic for $S_{0,3}$ is shown.

DAC output to be demultiplexed via all four demultiplexers. While the four demultiplexers and the DAC could have been cointegrated on the same chip, a multiple-chip solution has been chosen to simplify the bonding to the quantum chip and the routing to the pads within the quantum chip, which is restricted by the absence of vias and the deposition of only two layers of metals for the electrodes. To compare the performance of the cryo-CMOS DAC with the performance of the room-temperature DAC, auxiliary (commercial discrete) demultiplexers have been placed at the mK stage as well to switch the demultiplexer inputs from M1–M3 between the room-temperature DAC and the cryo-CMOS DAC. The inputs from demultiplexer M4 are always connected to the output from the cryo-CMOS DAC.

A. QUANTUM DEVICE ARRAY DESIGN

The quantum devices have been fabricated on a strained Ge/SiGe heterostructure [42], [43]. The design is a modified version of the SiMOS array presented in [30], and drew inspiration from the crossbar architecture in [44]. The layout has been designed specifically to demonstrate the scaling properties of the proposed biasing approach. Fig. 3(a) shows a micrograph together with several scanning electron microscope (SEM) images of the array. The array consists of 648 unit cells, from which each unit cell contains one SHT defined by a pair of (vertical) barrier gates and one (horizontal) plunger gate. The barriers have a width of 45 nm and the gate has a diameter of 150 nm. The source and drain can be seen as the reservoirs. The current is flowing underneath the plunger gate and the two barrier gates from the source to the drain. Depending on the bias applied from source to drain, Coulomb-blockade effects may become visible, caused by the discrete energy levels in the device [45]. A screening gate prevents the formation of spurious channels and unintended charge accumulation in the device, avoiding any unwanted current paths. The unit cells are indexed by $[x,y]$, where unit cell [1,1] is at the bottom left, and [18,36] at the top right. An SEM image of the unit cell is shown in Fig. 3(b). The source (S), drain (D), and screening gate are common to all SHT unit cells, i.e., there is only one source, one drain, and one screening gate on the chip.

Referring to Fig. 2(a), plunger gates $V_{p\{1,3,\ldots,35\}}$ ($V_{p\{2,4,\ldots,36\}}$) are connected to the bondpads on the left-hand (right-hand) side and then bonded to M4 (M2), respectively. The barrier gates $V_{b\{1,2,\ldots,18\},1}$ ($V_{b\{1,2,\ldots,18\},2}$) are routed to the bond pads on the top (bottom) and bonded to M1 (M3), respectively. Thus, for each SHT unit cell, the left barrier is defined by M1, the right barrier by M3, and the plunger gate by either M2 (even rows) or M4 (odd rows).

B. DEMULTIPLEXER DESIGN

Fig. 4(a) shows a micrograph of the demultiplexer chip (M1–M3 in Fig. 2) fabricated in a 22-nm FinFET process [8], [9], [19], indicating the dimensions and the location of the demultiplexer and the digital control circuits. The analog and digital inputs are on the north side, and the analog outputs are on the south side, whereas the bondpads on the west/east side are unused. As depicted in Fig. 4(b) and (c),

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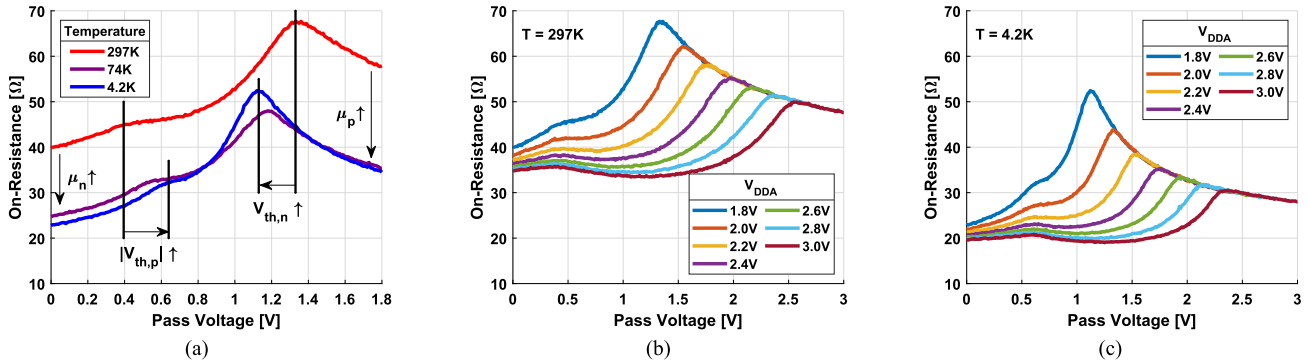

FIGURE 5. Measured ON-resistance from a typical switch in the demultiplexer as a function of the pass voltage, for different (a) temperatures (with nominal $V_{DDA} = 1.8$ V), and for different V_{DDA} at (b) 297 K and (c) 4.2 K.

the demultiplexer architecture consists of 24 channels, each containing two single-pole-single-throw switches, with the outputs from the switches connected together. Channel n ($n \in \{1, 2, \ldots, 24\}$) has one input V_0 common to all channels, and one input equal to V_{i+1}, with $i = (n-1) \mod 4$. Four unique voltages were chosen to ensure reverse compatibility with a previously used measurement setup. The common input V_0 is connected to 0 V, which can be used to disable devices in the 2-D array. An on-chip hold capacitor $C_n = 15$ pF (with an area of $60 \times 60\ \mu m^2$) is added to each output to allow for sampling and storing dc bias voltages that can be applied to the gate electrodes from the 2-D array. The capacitor size has been selected as a tradeoff between area occupation on the test chip and robustness against unforeseen leakage currents. It is envisioned that after further investigation and optimization of the leakage currents, the capacitor size can be reduced in future designs. Each demultiplexer channel occupies a silicon area of $80 \times 65\ \mu m^2$. By periodically refreshing the sampled dc bias voltages, only V_1–V_4 are sufficient to define 24 unique output voltages, providing a significant advantage in terms of required wiring. In order to optimize the ON-resistance of the switches and to maximize the pass voltage range, the switches are implemented as minimum length, thick-oxide pass-gates [see Fig. 6(d)]. Because they can handle a larger gate voltage range (1.8 V) than thin-oxide devices, thick-oxide passgates are less susceptible to the increase in ON-resistance at cryogenic temperatures that follow from the increased threshold voltage, which can be more detrimental in low-voltage (thin-oxide) switches [46]. Due to the larger possible overdrive voltage, thick-oxide devices therefore provide a more reliable implementation than thin-oxide devices. The negative MOS (NMOS) and positive MOS (PMOS) transistors are sized to have an expected ON-resistance (20–40 Ω) in the same order as the on-chip interconnect resistance. Although further reducing this resistance can be done by increasing the switch size at relatively low cost (as the switch is small compared to the hold capacitor), having a too large switch may result in excessive charge injection effects. In addition, no gain in terms of time constant is achieved, as the resistance is now dominated by the interconnect resistance. Each switch

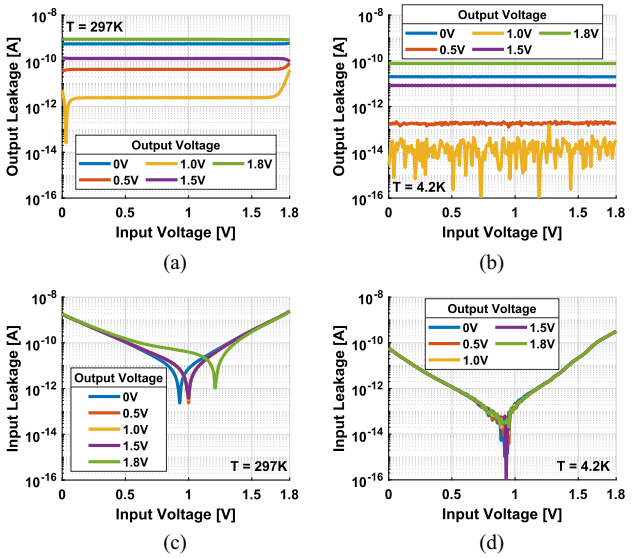

FIGURE 6. Measured leakage current (absolute value) from a switch in the demultiplexer from (a) and (b) the output side and (c) and (d) the input side at both 297 K and 4.2 K, as a function of the input voltage, for different output voltages.

can be individually controlled from a corresponding unique configuration bit in the shift register. Consequently, the demultiplexer channel can be configured to pass V_0, V_{i+1}, or to create a high-Z node such that the output voltage is defined by C_n. A level shifter allows to modify the gate voltage applied to the switches to above 1.8 V (in case the ON-resistance is higher than expected), while still being able to keep the shift register at the nominal 1.8 V supply. In order to minimize the number of transistor flavors, the shift register was also implemented with thick-oxide devices. As there are two switches in each channel, the shift register has a length of 48 bits.

In order to verify the functionality of the demultiplexer, a characterization was performed at 4.2 K using a dipstick in another measurement setup. Resistance and leakage were measured with Keithley 2636B source-measure units and using triaxial cables. A 7- mV differential voltage was applied to the switches for measuring the resistance. Using a four-wire connection, resistance from the measurement

setup (except for on-chip interconnect resistance) could be calibrated for. Fig. 5(a) shows the measured ON-resistance of a switch as used in the demultiplexer, as a function of the pass voltage [V_3 in Fig. 4(c)] when cooling down to 4.2 K. For pass voltages close to either 0 V or 1.8 V, it can be observed that the on-resistance is decreasing at cryogenic temperatures. In these regions, the overdrive on the transistors is maximized, resulting in lower ON-resistance due to increased mobility at cryogenic temperatures [47], [48]. In the region between approximately 1.1 V and 1.3 V, the ON-resistance first drops (when going to 74 K), but starts increasing again toward 4.2 K. As the threshold voltage increases at lower temperatures and the subthreshold slope becomes steeper [47], [48], the resulting reduction in overdrive voltage starts to outweigh the increasing mobility, resulting in a net increase in ON-resistance. Moreover, it can be seen that the knee points move toward mid-supply, caused by the increasing threshold voltage. When considering only 297 and 4.2 K, the ON-resistance reduces between 1.1 and 1.75 times when going to 4.2 K.

Fig. 5(b) and (c) shows the measured ON-resistance at 297 and 4.2 K as a function of the pass voltage for different supply voltages above the nominal 1.8 V. As expected, increasing the supply voltage implies an increase in overdrive, and, therefore, a reduction in ON-resistance, which is clearly observed at both temperatures. For the following measurements, $V_{DDA} = 1.8$ V is used as the resistance obtained for that setting is already sufficiently low.

A characterization of the leakage currents associated with an open switch in the demultiplexer is shown in Fig. 6. Leakage was measured while using V_3 as input and V_{CH3} as output; all other inputs and outputs are left physically floating. All 48 switches on the chip are in the open (high-Z) state during this measurement. As the measurement was done at dc, no capacitive effects are expected to play a role. All leakage currents were observed to be time invariant. Looking at the output leakage at room temperature, as presented in Fig. 6(a), it can be observed that the leakage hardly depends on the input voltage, implying that the leakage due to finite OFF-resistance is below the floor set by other leakage sources. It is expected that the leakage is dominated by the leakage from electrostatic discharge (ESD) diodes. Referring to Fig. 4(c), diode D1 is connected between V_{DDA} and V_{CH3}, and diode D2 between V_{CH3} and V_{SS}. The net leakage from node V_{CH3} is minimized when the currents through both diodes are equal ($I_{D1} = I_{D2}$). Assuming both diodes are equal, this happens when also the voltage across the diodes is equal ($V_{D1} = V_{D2}$). This condition is satisfied when $V_{CH3} = V_{SS} + (V_{DDA} - V_{SS})/2$, i.e., the output voltage is at mid-supply. The measurement in Fig. 6(a) confirms this expectation, as the leakage is minimized for an output voltage of 1.0 V (yellow curve), which is the closest to mid-supply from the measured curves. At this biasing point, leakage mechanisms associated with the switch itself can become visible, which most likely is happening for input voltages close to 0 or 1.8 V. However, when going to cryogenic temperatures [see Fig. 6(b)], the steeper subthreshold slope and increased threshold voltage reduce the leakage currents associated with the switch by orders of magnitude, also making any leakage due to finite OFF-resistance negligible. Consequently, the leakage at the output side of the switch (which is the relevant leakage quantity when using the S/H-structures) is not influenced by the voltage on the input side anymore at 4.2 K. Furthermore, also the dominant leakage from the ESD diodes reduces by multiple orders of magnitude [49]. However, as the leakage is still minimized around mid-supply, it is expected that the ESD diodes are still dominating the leakage at 4.2 K.

Fig. 6(c) and (d) shows the measured leakage from the input side as a function of the input voltage. The leakage on the input node has a strong dependence on the input voltage, both at 297 and 4.2 K, which is now attributed to the ESD diodes on the input side of the demultiplexer [connected to V_{0-4} in Fig. 4(b)]. When the input is around mid-supply, the ESD leakage currents cancel out, resulting in a dip in the measured leakage current. At 297 K in Fig. 6(c), there is a dependence on the output voltage, visible from the shift of the dip. This shift has disappeared when going to 4.2 K in Fig. 6(d) due to the reduced leakage associated with the switch itself. Consequently, there is no dependence on the output voltage anymore at 4.2K. Note that in Fig. 6(d), the minimum is very close to mid-supply.

C. DC DAC DESIGN

The dc DAC [see Fig. 7(a)], together with a demultiplexer, has been fabricated in the same 22-nm FinFET process as the chip in Fig. 4. Compared to M1–M3, the demultiplexer in M4 has a slightly different switching configuration. As shown in Fig. 7(b) and (c), all channels still have one common input V_0 (again connected to 0 V), but the channel-specific input has been replaced by a second common input, the DAC output V_{DAC}. Moreover, V_{DAC} is also brought off-chip, such that it can serve as the input for the other three demultiplexers. For characterization purposes, V_{DAC} also has a direct connection to the room-temperature equipment.

The DAC used for this work is based on the integrating DAC architecture proposed in [38]. As the development was done for a quantum device similar as in [30], the DAC can cover an output voltage range of up to 3 V with a 57 μV resolution at 4.2 K, and can drive a load capacitance up to 500 pF, allowing to drive the parasitic capacitance in a spin qubit processor up to 10 000 gate electrodes. An integrator-based architecture was chosen for the inherent monotonicity and the buffered output from the integrator, allowing to drive large capacitive loads. Because the thin-film resistors in this technology are expected to become superconducting at mK temperatures (similar to [50]), the DAC has been redesigned to avoid any resistors. Since the use of resistors was restricted to biasing networks, no major differences in performance compared to [38] are therefore expected. The DAC bias current generation (left part of Fig. 4 in [38]) was removed and replaced with an external bias current source. The generation of $V_{\mathrm{DAC},H}$ and $V_{\mathrm{DAC},L}$ (middle and right part of Fig. 4 in [38]) was removed as well, and also replaced with external bias

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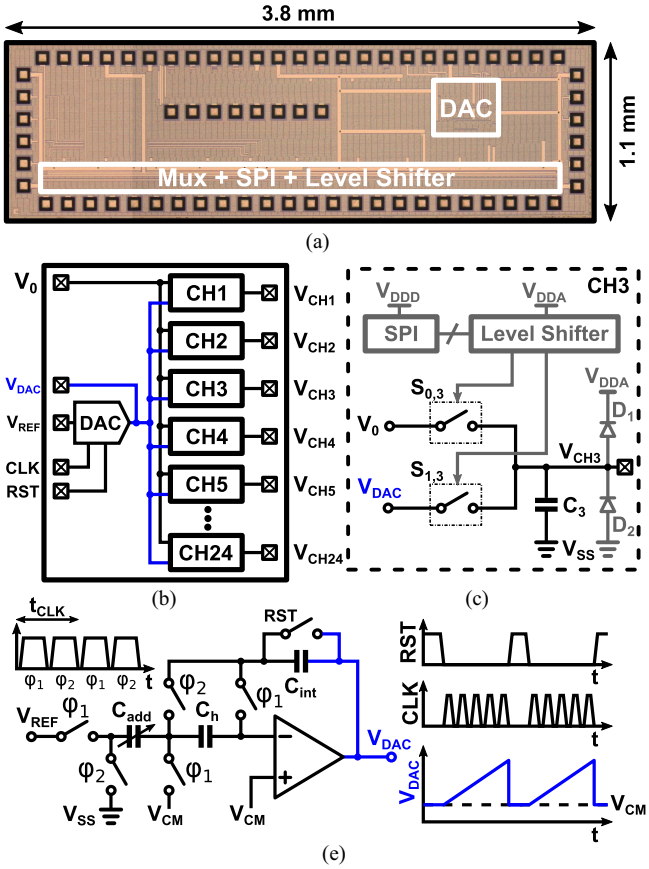

FIGURE 7. Overview of the design used for M4, containing the demultiplexer integrated with a dc DAC, showing (a) the chip micrograph, (b) channel configuration, (c) functional schematic of a typical channel, (d) simplified schematic of the dc DAC core, and (e) simplified waveforms associated with the DAC operation.

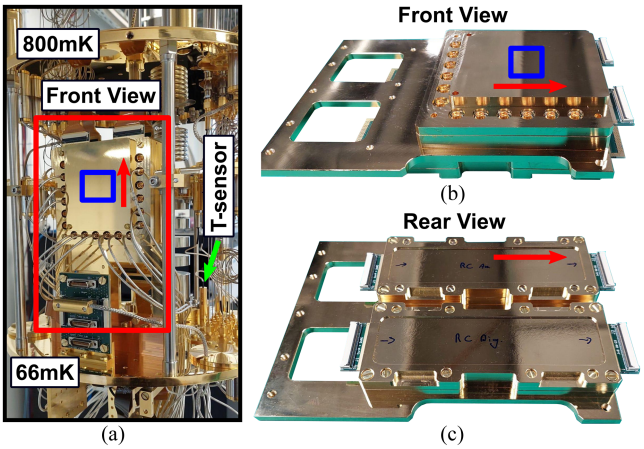

FIGURE 8. Photograph of the cold finger (a) mounted on the MXC plate of a dilution refrigerator (the temperature sensor is mounted on the MXC plate itself), (b) front view, and (c) rear view. The blue square indicates the rough location of the chips and the red arrows indicates the orientation of the cold finger.

voltages, which are shifted (on-chip) with a diode voltage to track the threshold voltage shift.

As shown in Fig. 7(d) and (e), the DAC operates by integrating a reference voltage V_{REF} for a predefined number of integration/clock cycles. First, the reset (RST) signal is set high to discharge the integration capacitor C_{int}. At this point, the output voltage is equal to the operational amplifier's (opamp) common mode voltage V_{CM}. In phase 1 (ϕ_1), V_{REF} is sampled on C_{add}. In phase 2 (ϕ_2), the charge on C_{add} is transferred to the integration capacitor $C_{\mathrm{int}} = 37\mathrm{pF}$. After one clock cycle, the output voltage has increased by a step equal to $V_{\mathrm{REF}} \cdot C_{\mathrm{add}}/C_{\mathrm{int}}$. The capacitor C_{add} is implemented as an 8-bit tunable capacitor, with the LSB equal to ~870 aF, and hence can be used to modify the stepsize of the DAC. The capacitor $C_h = 1.8\,\mathrm{pF}$ serves as an offset-compensation capacitor by sampling the offset in the first phase and then subtracting it in the second phase [51]. While integrating, the output of the DAC behaves as a ramp, as illustrated in Fig. 7(e). When the predefined amount of integration cycles is reached and thus the targeted output voltage is obtained, the clock stops, the integrator can be reset, and the sequence can be repeated. To control the switches in the integrator, the two (nonoverlapping) control signals ϕ_1 and ϕ_2 are derived from the main clock signal. For operating the DAC, only two signals are therefore required: a clock and a reset signal.

D. DILUTION REFRIGERATOR INTEGRATION

In order to mount the sample printed circuit board (PCB) that carries the full system with the 2-D array, demultiplexers, and dc DAC [see Fig. 2(b)] in a dilution refrigerator, a set of enclosures and mounting brackets (cold finger) was developed. Fig. 8(a) shows how the cold finger is mounted in a BlueFors LD400 dilution refrigerator system. As the cold finger from another experiment is mounted on the bottom side of the MXC plate, the cold finger for this work is mounted on top of the MXC plate. The cold finger consists of a backplate with the enclosure for the sample PCB on the front [see Fig. 8(b)] and the PCBs containing *RC*-filters on the back [see Fig. 8(c)].

In general, semiconductor spin qubits can be operated with higher fidelity at lower temperatures [45], implying the qubits and cryo-CMOS electronics must be properly thermalized. Consequently, no packaging was used for the chips. Instead, by making a small cutout in the sample PCB, the 2-D array is glued (with conducting silver paste glue) directly to the copper surface of the cold finger [see Fig. 2(b)], providing a better thermal contact with the cold finger compared to conventional packaging. Ideally, M1–M4 should also be thermally anchored to the cold finger. However, as the charge carriers in the SHTs are holes, negative gate voltages are required to be supplied to the 2-D array via the demultiplexer. For improving thermalization and preventing reliability concerns related to the startup transients of the system, it was decided to keep the reference potential (V_{SS}) of the SHTs at ground level, as SHTs are considered more fragile and more sensitive to temperature variations than the CMOS devices.

To avoid large currents flowing through the ESD diodes from the demultiplexers, M1–M4 are placed on a PCB, electrically isolated from the fridge chassis, allowing a negative V_{SS} to be applied to M1–M4. As a drawback, using a V_{SS} below the ground limits the thermal anchoring to the fridge chassis, as the fridge chassis is inherently grounded. The input signals for M1–M4 are all bonded directly from the PCB. The outputs are bonded chip-to-chip from the demultiplexers directly to the 2-D array. For verification purposes, all four demultiplexers also have one unused channel bonded to the PCB, allowing for directly measuring back these outputs at room temperature. Because the 2-D array only has one source, one drain, and one screening gate, these signals are directly bonded from the PCB to the 2-D array without any form of demultiplexing. Next to the cryo-CMOS chips, also three MAX4619 discrete demultiplexers are placed on the PCB. These demultiplexers have already been verified to be functional at mK temperatures [29] and allow for reconfiguration of the sample PCB without having to physically change the setup. As shown in Fig. 2(a), they can be used to connect the inputs from M1–M3 to either the DACs at room temperature or to the cryo-CMOS DAC. In turn, this allows the measurement of the cryo-CMOS DAC without the need for a thermal cycle, which would otherwise change the *IV* curve of the SHTs.

When integrating the cryo-CMOS electronics in a dilution refrigerator, special care needs to be given to wiring, as otherwise undesired coupling between analog and digital may occur. The digital transition (edge)-sensitive signals are routed via unattenuated coaxial CuNi wiring. As the digital signals are not sensitive to noise, no performance degradation is expected when the attenuators for the digital signals are removed. Thermalization from this type of wiring is obtained in the same way as for dc wiring. Nontransition-sensitive signals are routed via regular dc wiring. However, this entire bundle of wiring has a ground shield. Analog signals are routed via another (physically separated) bundle of dc wiring. For both bundles of dc wiring, there is a separate enclosure containing a filter PCB, which allows for applying a dedicated two-stage discrete RC-filter to each signal [see Fig. 8(c)]. For the digital signals, a 100 Ω resistor is placed in series for reducing reflections/ringing. For analog signals, the filtering generally has a cutoff frequency between 15 and 350 kHz, which is both for thermalization as well as for avoiding excessive power reaching the quantum devices, which would increase their electron temperature. Supply voltages are also routed through the dc wires, which have a 20–30 Ω series resistance. No filtering is applied to supply voltages. Standard 100 nF NP0/C0G capacitors are used for decoupling the supply voltages. The filtered outputs are then connected to the main sample PCB using flex cables and flexible flat cable connectors. The coaxial wiring is connected directly to the sample PCB through the holes in the lid of the enclosure [see Fig. 8(a)]. The filtering for this set of signals is applied on the sample PCB itself.

E. ROOM-TEMPERATURE CONTROL ARCHITECTURE

In order to minimize errors from ground loops and interferers, all room-temperature electronics directly connected to the cryo-CMOS electronics or 2-D array are isolated from the computer ground and powered from batteries. For the DACs at room temperatures, an in-house developed D5a DAC module [52] in an SPI-rack setup has been used. The readout of the current through the 2-D array is done using a transimpedance amplifier [53] followed by an isolation amplifier (both at room temperature), from which the output is digitized using a Keithley 6500 digital multimeter. The digital waveforms required for communicating with M1–M4 and the auxiliary demultiplexers are generated using microcontrollers, followed by optocouplers for isolation. Due to the relatively high output impedance (550 Ω) from the D5a DAC modules, battery-powered [linear and low-dropout (LDO)] voltage regulators were used to generate the supply voltages for M1–M4. As only a limited number of D5a channels were available, the static bias voltages are also generated using LDOs.

III. MEASUREMENT RESULTS

As a first step in demonstrating the performance of the proposed system, the demultiplexer functionalities will be demonstrated. After these measurements, the bias generation functionalities of the cryo-CMOS DAC will also be demonstrated. The analog and digital supply voltage magnitudes [$V_{\mathrm{DDA}} - V_{SS}$ and $V_{\mathrm{DDD}} - V_{SS}$ in Fig. 4(c) and (d)] are both equal to 1.8 V. The value for V_{SS} is provided in each figure. All SHT-measurements are performed using a $-50\,\mu$V drain-to-source voltage, where the source from the 2-D array is connected to ground (i.e., 0 V). For visual purposes, all presented SHT-measurements have an inverted sign for the drain current I_d.

A. QUANTUM DEVICE CHARACTERIZATION

For each demultiplexer, one dedicated channel, which is not connected to the 2-D array, is routed back to room temperature. Verification measurements of these channels showed results consistent with expectations, i.e., the output voltage is correct and the results are repeatable. Given the excellent yield and reliability of this FinFET process, it can be assumed that all other channels are also working as expected. After turning on the demultiplexers, the MXC temperature increase is below the intrinsic temperature fluctuations at the MXC, and the temperature remains below 9 mK. Configuring the switches with a clock speed of ∼500 Hz did not result in noticeable temperature increase. Based on measurements in a dipstick at 4.2 K, it is expected that the static (leakage) current consumption from the multiplexers will be in the order of 28 nA (12 nA from the digital and 16 nA from the level shifters). Fig. 9 shows a turn-ON characterization of the even-numbered SHTs in the first column of the 2-D array, i.e., SHT [1,{2,4, . . . ,36}]. The odd-numbered SHTs are not reported as their plunger gate (biased by M3) can only be biased by the cryo-CMOS DAC, which is not yet enabled

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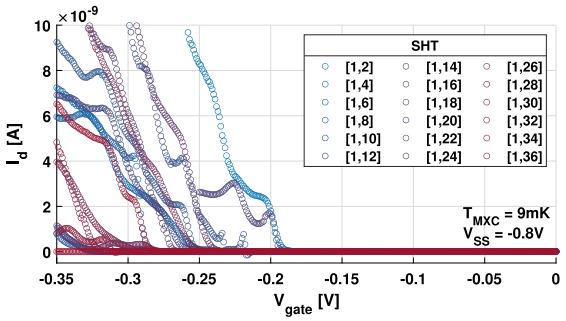

FIGURE 9. Measured forward turn-ON curves from the even-numbered SHTs in the first column from the 2-D array using the cryo-CMOS demultiplexer.

in this measurement. The demultiplexer is first configured to select the desired SHT unit cell in the 2-D array (by using the digital communication interface), after which a turn-ON measurement was performed by simultaneously sweeping the plunger- and two barrier gates corresponding to the unit cell. Except for one unit cell, a nonzero turn-ON current was measured for each selected unit cell. The observed variation in the measurements is comparable with the observed variation in similar devices [28]. Further measurements show that the barrier gates in this particular 2-D array sample are not able to pinch off the current (while keeping the barrier voltage ≤ 0V). As the plunger gate [blue gate in Fig. 2(a)] is shared with 18 SHT unit cells in the same row, measuring turn-ON of a single unit cell essentially results in measuring all 18 unit cells in parallel, from which 17 have barrier gates grounded. The measured turn-ON voltage is then effectively determined by the unit cell in the row with the lowest turn-ON voltage. Due to the variation in turn-ON voltages between devices, the measured ensemble is likely dominated by only a fraction of 18 devices in the row, although it is difficult to predict which exact devices. Even though the device is not fully behaving as desired, these results do already highlight the large-scale biasing potential of this approach.

B. FLOATING GATE BIASING

The capacitor C_3 shown in Fig. 4(c) can be used to define the gate voltage in a floating gate configuration. Assuming that $S_{0,3}$ is open and $S_{1,3}$ is closed, a voltage V_{CH3} can be defined on C_3 via V_3, which is sampled on C_3 at the moment that also $S_{1,3}$ is opened. Any leakage seen from node V_{CH3} will cause the capacitor to slowly discharge, requiring to refresh the capacitor charge after a certain time.

Fig. 10 shows the measurements for quantifying this leakage. By restricting the current flow, and remeasuring the reference turn-ON curve before each floating gate measurement, the effects of drifting device parameters on the measurements are reduced. In Fig. 10(a), the forward *IV* curves for sweeping V_{p18} for device [1,18] are shown. The two corresponding barriers $V_{b1,1}$ and $V_{b1,2}$ are kept grounded. As the barriers are not pinching off the current, sweeping only V_{p18} is sufficient

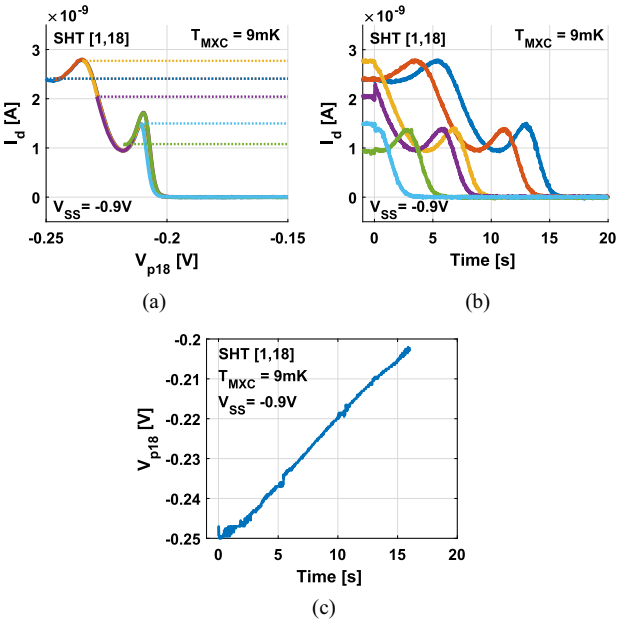

FIGURE 10. Measured (a) forward *IV* curve and (b) corresponding time trace for floating gate biasing of device [1,18]. (c) Plunger voltage V_{p18} vs. time.

to observe turn-ON. Six sweeps of V_{p18} were performed. Each sweep starts at 0 and ends at a different value of V_{p18}, corresponding to either a local minimum or maximum in the *IV* curve, or a local minimum in the derivative of the *IV* curve. When the forward sweep reaches the predefined point, V_{p18} is kept fixed, after which the switch in the demultiplexer corresponding to V_{p18} is opened, creating a floating gate structure. Fig. 10(b) shows the time evolution of the current: For $t < 0$, the switch is closed and the voltage V_{p18} is defined by the DAC; at $t = 0$, the switch opens, and for $t > 0$, V_{p18} is defined by the hold capacitor. When looking at Fig. 10(b), the current follows the *IV* curve in Fig. 10(a) in reverse direction, where the minima and maxima are still clearly visible. Using the dark blue *IV* curve (V_{p18} set to -0.25 V by the DAC) and corresponding time trace, an average leakage from the hold capacitor of 50 fA can be extracted, corresponding to 3.1 mV/s. For the other curves, a leakage between 2.4 and 3.4 mV/s can be found. This is consistent with Fig. 6(b), where a leakage of 10–100 fA is observed for the setting ($V_{SS} = 0$ V and $V_{p18} = 0.65$ V), which for the leakage is equivalent to the setting ($V_{SS} = -0.9$ V and $V_{p18} = -0.25$ V) in Fig. 10. Fig. 10(c) shows a mapping from the blue curve in Fig. 10(b) onto the turn-ON curve from Fig. 10(a). The resulting estimated plunger voltage shows a linear decay from -0.25 V to just below -0.2 V.

1) OPTIMIZING THE HOLD TIME

Based on the leakage measurements presented earlier (see Fig. 6), the dominant source of leakage is expected to be the reverse bias leakage of ESD diodes. Although the leakage can be reduced by fully removing the ESD diodes, from a

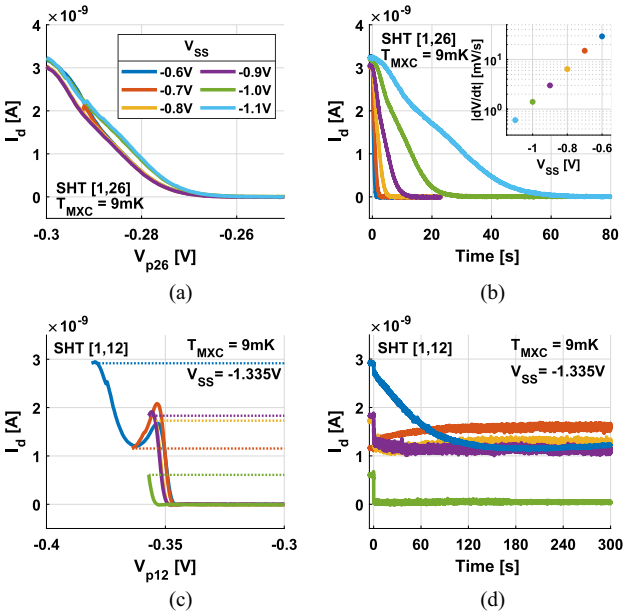

FIGURE 11. Measured (a) forward *IV* curve and (b) corresponding time trace for floating gate biasing of device [1,26], for different values of V_{SS}. Measured (c) forward *IV* curve and (d) corresponding time trace for floating gate biasing of device [1,12], for an optimized value of V_{SS}.

reliability and CMOS design-rule point of view, this may not be desirable. Still, some optimization can be applied by tuning V_{SS}, provided the ESD diodes remain reverse-biased. As derived in Section II, for a given bias point and supply voltage magnitude, the optimum V_{SS} equals $V_{SS,opt} \approx V_{CH3} - (V_{\mathrm{DDA}} - V_{SS})/2$.

To experimentally assess this optimization, floating gate measurements similar to Fig. 10 were performed for different values of V_{SS}. Fig. 11(a) shows the corresponding forward *IV* curves. To ease the visual comparison, a device with a large monotonic region in the *IV* curve was chosen for this measurement. All six *IV* curves are measured down to a plunger voltage V_{p26} equal to -0.3 V. After reaching a plunger voltage equal to -0.3 V, the corresponding switch in the demultiplexer is opened, and the time traces in Fig. 11(b) were measured. As shown in the inset in Fig. 11(b), the leakage is significantly lower when V_{SS} is closer to $V_{SS,opt}$. For example, when changing V_{SS} from -0.6 to -1.1 V, the leakage rate exponentially improves from 29 mV/s to 600 μV/s, caused by the exponential dependence of the leakage current on output voltage (see Fig. 6).

To demonstrate the floating gate biasing for a fully optimized V_{SS}, a full optimization was performed on V_{SS}. For this measurement and the further measurements, device [1,12] will be used as the main DUT. Fig. 11(c) shows five forward *IV* curves when sweeping V_{p12}. Due to drift and charge jumps during the measurements, not all five curves are exactly the same. The corresponding time traces during S/H are depicted in Fig. 11(d). Charge jumps that were observed during the measurement are removed in postprocessing. The jumps at $t = 0$ are caused by charge injection, and therefore cannot be removed. In this experiment, the empirical V_{SS} that optimizes the hold time equals -1.335 V, for which the hold times after opening the switch are now significantly longer. Except for the purple and green curves (which are affected by charge jumps), all curves slowly drift toward a current corresponding to a plunger voltage V_{p12} of about -0.36 V. Given that the output leakage is not dependent on the input voltage of the switch [see Fig. 6(b)], it is not expected that this voltage is influenced by the input voltage of the switch. Because the dark blue curve starts relatively far away (in terms of gate voltage) from -0.36 V, the leakage rate after opening the switch is initially rather high. However, it saturates after roughly 1.5 min when the (floating) gate voltage approaches -0.36 V. These measurements show a theoretical $V_{SS,\mathrm{opt}} = -1.26$V, which is 75 mV away from the empirical value found earlier. However, given the very low currents associated with the output node, any gate leakage from the 2-D array or mismatch between D1 and D2 can easily shift this optimum V_{SS}. Nevertheless, performing a global optimization of V_{SS} can yield significant improvements in terms of hold times and can thus reduce the required refresh rate.

2) CHARGE INJECTION AND CLOCK FEEDTHROUGH

Inherent to CMOS switches is the associated charge injection and clock feedthrough. When opening the switch, the charge carriers forming the transistor conductive channel are injected into the switch output and input node. Although the charge injection from the parallel NMOS and PMOS partially cancels each other, a nonzero net charge injection will appear due to sizing/biasing-induced mismatch in the PMOS and NMOS charge injection. Moreover, depending on the impedance seen at the switch input/output, the charge may not split equally. Clock feedthrough, due to the capacitive coupling of the control signal on the transistor gate to the output, also causes an error in the voltage stored on the hold capacitor. Because these effects cannot easily be distinguished, they will therefore be analyzed together. As can be seen in Fig. 11(d), a jump in the current is observed when opening the switch at $t = 0$. The charge injection effectively adds some charge on the hold capacitor, thus causing a shift in the bias point of the SHT.

To quantify the effective charge injection associated with the demultiplexer, the change in capacitor voltage and charge just after $t = 0$ has been derived. As the current change in the SHT depends on the derivative of the *IV* curve, measurements are performed at two different bias points: at a maximum-derivative point (steep slope in the *IV* curve), see Fig. 12(a) and (b), and at a zero-derivative point (local minimum in the *IV* curve), see Fig. 12(c) and (d). In Fig. 12(d), the device showed a number of charge jumps causing the current to fall back to zero. However, the charge difference for the hold capacitor could still be determined as the charge jumps only happen after 4 s. When taking the measured current just after opening the switch and using the *IV* curve to find

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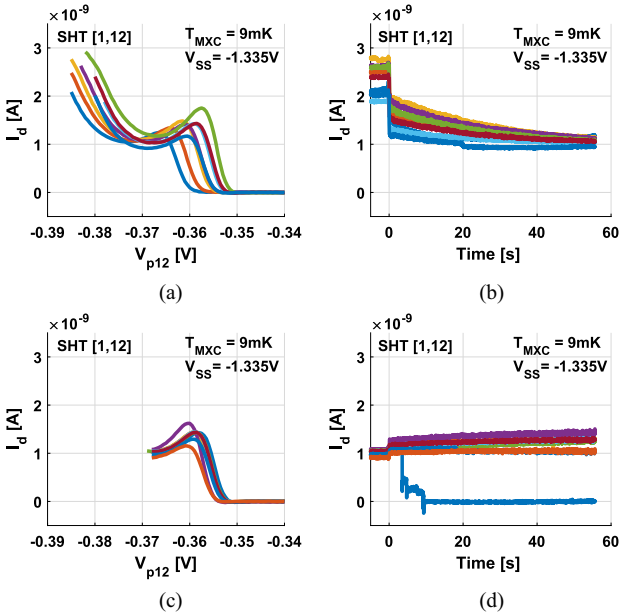

FIGURE 12. Statistical measurements used to quantify charge injection. (a) *IV* curve and (b) corresponding time trace after opening the switch at a steep slope on the *IV* curve, and (c) turn-ON curve with (d) corresponding time trace after opening the switch at a flat region in the turnon curve.

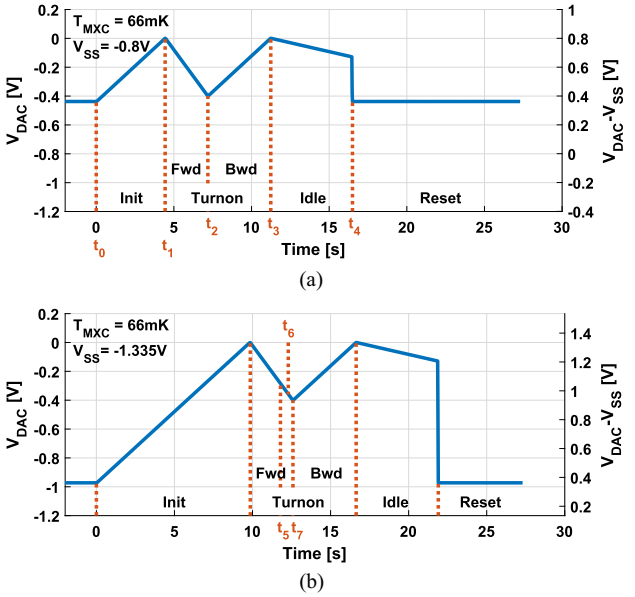

FIGURE 13. Measured output voltage from the cryo-CMOS DC DAC at 66 mK when operating the DAC with (a) $V_{SS} = -0.8$V and (b) $V_{SS} = -1.335$V. The left axis shows $V_{DAC}(t)$ referred to ground (same reference as the 2-D array) and the right axis shows $V_{DAC}(t)$ referred to V_{SS}.

the corresponding plunger voltage, an average (systematic) change in capacitor charge of 59 fC [see Fig. 12(b)] and 66 fC [see Fig. 12(d)] is found for a capacitance equal to 15 pF. Although the injected charge is highly depending on the operating point and surrounding circuits, the results do indicate that charge injection is an important consideration when using demultiplexers in a scaled system, although a significant part of the charge injection could be canceled by calibration. Note that the derivative of the *IV* curve causes the change in current in Fig. 12(b) to be significantly larger than in Fig. 12(d), even for a similar amount of injected charge.

C. BIAS GENERATION AT MK-TEMPERATURES

When enabling the demultiplexers M1 to M4, including the dc DAC integrated in M4, the MXC temperature increases to 66 mK. Due to limitations in the test setup (related to operating two qubit measurement setups at the same time in the same dilution refrigerator), it was not possible to measure the supply current directly. By comparing the increase in MXC temperature with the temperature increase obtained by activating the built-in MXC heater, the power consumption of all cryo-CMOS electronics together is estimated to be around 120 μW. Since the MXC heater is located at a different location from M1–M4, closer to the temperature sensor, it is expected that in reality, the power consumption will be slightly higher. While running the DAC during the experiments, no further temperature increase was observed. Consequently, it is expected that the power consumption is dominated by the static bias currents. A 3.6 V supply, referred to V_{SS}, is used to power the high-voltage output stage from the DAC. The reference voltage V_{REF}, also referred to V_{SS}, equals 1.8 V and is constant for all measurements.

1) DAC WAVEFORM

Fig. 13(a) shows the measured output voltage from the cryo-CMOS DAC for $V_{SS} = -0.8$V (used for the device characterization measurements). As the readout chain is digitized by a benchtop multimeter, a clock frequency of 121 Hz (the lowest clock frequency compatible with the DAC control software) and a positive integration step size of 800 μV were used. For $t < t_0$, the DAC is in the reset state. $V_{\mathrm{DAC}}(t)$ is then equal to the common-mode voltage from the opamp, V_{CM}. The demultiplexers also start in the reset state, where all outputs are connected to $V_0 = 0$ for $t < t_0$, such that the 2-D array is reset as well. At t_0, the DAC starts integrating until $V_{\mathrm{DAC}}(t)$ reaches 0 V at t_1. As $V_{\mathrm{DAC}}(t_1) = 0 = V_0$, the demultiplexer is reconfigured to now pass $V_{\mathrm{DAC}}(t)$ instead of V_0 to the selected gates. In addition, at t_1, the DAC is reconfigured to change the sign of the integration. For $t_1 < t < t_2$, the DAC is integrating from 0 to -0.4 V, which effectively performs a forward sweep on the connected gates. After reaching -0.4 V at t_2, the sign of the integration is flipped. For $t_2 < t < t_3$ the DAC now integrates from -0.4 V back to 0, corresponding to a backward sweep. At t_3, the output voltage from the DAC is 0 again, and the demultiplexer is reset (so it passes $V_0 = 0$ again to the 2-D array). For $t_3 < t < t_4$, the DAC is in the idle mode. Due to the leakage from the integration capacitor, the output voltage tends to slowly drift away in the idle mode. This effect also causes the positive and negative integrations to be slightly skewed, i.e., with the same nominal step size setting, the effective step size in the negative integration direction is larger than in the

positive integration direction. However, this error can easily be compensated for by performing a one-time calibration of the step size. Finally, the DAC is reset at t_4. Fig. 13(b) shows the measured waveform in case of $V_{SS} = -1.335$V (used for the floating gate biasing). Due to the dependence in $V_{\mathrm{DAC}}(t)$ from V_{SS}, a different number of integration steps was required in the initialization mode to bring the DAC output to 0 V. Except for this change, the turn-ON and idle states are equal. Therefore, for a given step size in the positive direction, only the number of integration cycles in the initialization phase needs to be adapted when changing V_{SS}.

2) BENCHMARKING

The auxiliary demultiplexers depicted in Fig. 2(a) allow the inputs from M1–M3 to be supplied from either the DAC at room temperature or the cryo-CMOS DAC. Since the same device can now be subsequently measured by both DACs in the same cooldown, a benchmarking experiment was performed on two devices: [1,12] and [1,18]. Fig. 14(a) and (c) shows the measured (forward and backward) *IV* curve for both devices, measured using the DAC at room temperature. Again, only the plunger is being swept, and the barriers are kept grounded. Both devices exhibit a slight amount of hysteresis, i.e., the direction of the sweep influences the behavior. This was observed for nearly all measured devices and is in line with expectations [54].

The cryo-CMOS DAC is then used to generate and apply the waveform in Fig. 13(a) to the quantum devices. By reconfiguring the auxiliary demultiplexer, the output from the cryo-CMOS DAC is routed to the inputs from all demultiplexers. During the turn-ON phase ($t_1 < t < t_3$), $V_{\mathrm{DAC}}(t)$ is applied to the plunger gate, which yields the curves in Fig. 14(b) and (d). The measurement routine was repeated three times to assess the reproducibility; hence, three curves were also shown. For $t_1 < t < t_3$, $V_{\mathrm{DAC}}(t)$ nominally performs a forward and backward sweep between 0 and -0.4 V, reaching -0.4 V at t_2. After the devices turn ON (just after 6.5 s), the devices show the same characteristic current peaking that was observed with the room temperature DAC, thus demonstrating that the DACs at room temperature can indeed be replaced by the cryo-CMOS DAC. Note that since the waveform generated by the cryo-CMOS DAC has an asymmetric forward and backward sweep, also the measured current from the SHTs has a slight asymmetry around t_2. Fig. 14(e) and (f) shows the time traces from Fig. 14(a) and (c) after mapping them onto the gate voltage [using the waveform from Fig. 13(a)]. When closely looking at turn-ON curves in Fig. 14(e) and (f), the current at a plunger voltage of -0.4 V is larger than what is measured in Fig. 14(a) and (c). Looking at Figs. 11(c) and 14(a), it can be concluded that some form of drift and hysteresis is already present between different measurement runs [54]. Moreover, the thermoelectric voltages [55] (that could be on the order of millivolts over a 300 K range) introduced from the wiring in the dilution refrigerator potentially also play a role, as the curves are measured using DACs at two different temperatures.

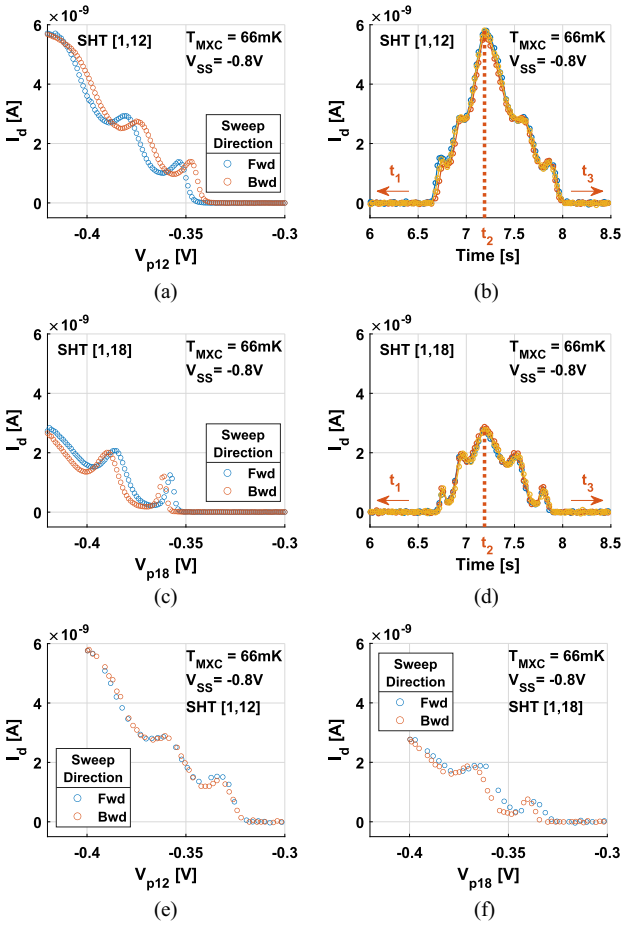

FIGURE 14. Benchmarking experiment for the cryo-CMOS DAC. *IV* curve for (a) device [1,12] and (c) device [1,18] when sweeping the plunger gate using the DAC at room temperature. Measured current versus time when the waveform generated by the cryo-CMOS DAC [Fig. 13(a)] is applied to (b) device [1,12] and (d) device [1,18], and (e) and (f) corresponding mappings of the time traces onto the gate voltage using the cryo-CMOS DAC waveform. Similar to the device characterization measurements in Fig. 9, $V_{SS} = -0.8$V is also used as for the characterization measurements using the cryo-CMOS DAC.

3) FLOATING-GATE BIASING

To fully harness the power of the proposed biasing strategy, the cryo-CMOS DAC can also be used for floating-gate biasing. The starting point for this experiment is again a dc measurement of the *IV* curve from device [1,12]. Fig. 15(a) shows the *IV* curve measured with the DACs at room temperature, for $V_{SS} = -1.335$V.

For performing the floating gate biasing, the cryo-CMOS DAC generates the waveform shown in Fig. 13(b), which is applied to V_{p12} via the demultiplexer. Fig. 15(b) shows the measured time traces, highlighting the time window around the sampling time. In Fig. 15, the same curves are shown, but now for the full time axis. The gate of the device becomes floating by opening the switch to V_{p12} in the demultiplexer at either t_5, t_6, or t_7. At these three instants, the DAC output voltage $V_{\mathrm{DAC}}(t)$ is equal to the voltage required for biasing the device exactly at one of the three peaks in the *IV* curve. Based on Fig. 13(b), t_5, t_6, and t_7, correspond to -347, -371, and -400 mV, respectively. Interestingly, the time traces that

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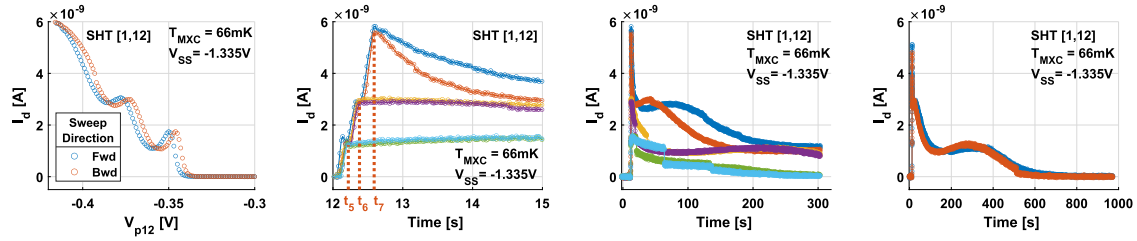

FIGURE 15. Floating gate biasing using the cryo-CMOS DAC. (a) Reference *IV* curve measured using the DAC at room temperature. (b)–(d) Measured current time trace when performing floating gate biasing using the cryo-CMOS DAC. (b) Six measurement runs where the device is biased at the three peaks in (a) (2 runs/peak), corresponding to opening the switch at t_5, t_6, or t_7. (c) Same data as (b), but with an extended time axis. (d) Two measurement runs when biasing the device at the peak at t_7 from (b), measured until the current reduces to 0.

TABLE 1. Performance Comparison With the State of the Art

	This Work	ESSCIRC '23 [18]	Nat.El. '21 [17]	npj QI '22 [30]	VLSI '24 [19]	Nat.El.'22 [20]	Nat.El.'23 [22]	Nat.El.'25 [21]
Temperature	66 mK	45 mK	100 mK	1.7 K	17 mK	50 mK	15 mK	600 mK
Technology	22-nm FinFET	65-nm CMOS	28-nm FDSOI	Discrete	22-nm FinFET	40-nm CMOS	28-nm CMOS	22-nm FDSOI
(De)Mux Type	DC	DC	DC	DC	DC	RF	RF	RF
DC Bias Generation	Yes	Yes	No	No	No	No	No	No
Integrated Control	Shift Registers	I2C + Memory	SPI + FSM	Shift Register	4K-Controller mK-Decoder	Word/Dataline Decoding	Decoder	Decoder
Type of Quantum Device	2D Crossbar Array Ge SHT's	1D Array Si/SiGe QD's	1D Array QD + QPC	2D Crossbar Array SiMOS SET's	Linear Array Si qubits	2D Farm Si NMOS	Super-conducting	2D Farm Si QDs
Nominal # of Quantum Devices	648	3	2	648	12	9	1	1024
Voltage Range	3 V	1 V	1.8 V	4 V	1.8 V	N.A.	0.7	0.8
Leakage Rate	0.06-18 mV/s	0.96 µV/s	0.4 µV/s	N.A.	65-572 µV/s	N.A.	N.A.	N.A.
Total # of Channels (Actually Used)	96 (72)	8 (7)	32 (5)	72 (72)	64 (28)	9 (9)	4 (2)	1024 (1024)
(De)Mux Ratio	1:96	1:8	1:32	7:72	1:64	1:9	1:4	1:1024
Power/Channel	1.2 µW/Ch	2.5 µW/Ch	18 nW/Ch	N.A.	187.5 nW/Ch	N.A.	0.18 µW/Ch	3.9 nW/Ch

start from the same biasing point are not necessarily equal. A combination of hysteresis effects and charge jumps could potentially explain this behavior. However, as this is out of the scope of this experiment, no further investigation into hysteresis effects and charge jumps as commonly observed, e.g., in [54], [56], and [57], was performed. As can be observed from Fig. 15(b), the curves seem to be less affected by charge injection than in Fig. 12. As only the DAC at the input of the switch has been changed, it is expected that this caused the impedance at this node to be reduced, resulting in more charge being absorbed by the cryo-CMOS DAC, and less charge ending up on the hold capacitor. Two measurements over an extended time window are depicted in Fig. 15(d). The device is biased at the third peak (switch opened at t_7), after which a ∼15 min-long time trace was measured. After about 800 s (blue curve), the current has drifted back to 0. In the first 2 s after opening the switch, the leakage equals around 18 mV/s, whereas the leakage has reduced to 60 μV/s after 200 s. For a given V_{SS} and supply voltage, there is a value of V_{p12} at which the leakage is at a minimum. When the plunger voltage comes closer to this value, the leakage rate will reduce. Consequently, it can be seen that initially (when biased at the third peak) the leakage rate is rather high, but that it quickly reduces when it comes closer to the optimum. When taking the minimum leakage of 60 μV/s, and assuming a maximum allowable error of 15 μV (1 LSB from the conventional D5a DAC module [52]), a refresh rate of 4 Hz for a single channel is required.

IV. DISCUSSION AND FUTURE PERSPECTIVES

Table 1 presents a performance comparison with state-of-the-art (de)multiplexer-based systems. This work has shown, for the first time, the experimental demonstration of the integration of four cryo-CMOS chips and a quantum-device chip at mK-temperatures. The cryo-CMOS circuitry consists of a dc DAC, codeveloped with a demultiplexer, allowing for demultiplexing up to 96 channels. Despite the quantum chip not working as expected, the proposed system can nominally support up to 648 SHTs. Although the total power consumption is higher than for the DAC presented in [18], the proposed DAC was sized to drive a 500 pF load, and is expected to be able to drive a few thousand gate electrodes [38]. To define the bias for this amount of electrodes, a slow ramp can be generated by the DAC [see Fig. 7(e)], which can be sampled on the hold capacitors present in the demultiplexer channels. The required bias voltage for a specific electrode then determines the clock cycle when the DAC output voltage ramp needs to be sampled. Using the concept of gear shifting as demonstrated in [38], i.e., dynamically modifying the step size, can bring advantages in terms of noise and efficiency. As the bias voltages do not need to be refreshed simultaneously, the effective load capacitance seen by the DAC is significantly smaller than the sum of all the hold capacitors, thus allowing the DAC to be used in systems with several thousands of demultiplexed channels. The leakage rates in the system now determine how often the voltage on the capacitor needs to be refreshed.

The measured leakage is higher than in prior work [17], [18], but can be improved in future redesigns by removing (part of) the ESD diodes. Depending on the exact CMOS process, this may raise challenges in terms of design rules and/or reliability. Based on the required bias voltages for the quantum devices, globally balancing the leakage currents by tuning V_{SS} may also provide some improvement, but this would only be effective if the required bias voltages are relatively similar. As the leakage is highly dependent on the supply voltage, lowering the supply could also improve hold times, although the minimum supply is eventually limited by the DAC.

In order to make the prototype system agile against unforeseen effects while testing mK temperatures, the measurement setup was made flexible by generating the digital control signals (for the shift registers in M1–M4) at room temperature. However, for future design iterations, a large part of this control architecture could be integrated into M1–M4. Also, while in the current experiment, synchronization could still be done manually via the control software, such an approach would not be viable when sampling at many different time instances. The system would benefit from an integrated controller, allowing to implement a more reliable and scalable way of synchronization between the DAC and demultiplexers. For instance, the control signals for the demultiplexer could be generated from a central digital controller, similar to [17]. In addition, this would also significantly ease the synchronization of the cryo-CMOS DAC and the demultiplexers. Whereas in experiments using a limited number of control signals, directly supplying all digital control signals from room temperature is still possible (see [20], [21], and[22]), this may become more challenging when additional functionality is included in the cryo-CMOS electronics. It is envisioned that more complex digital control will be required. For example, an I2C interface combined with on-chip memory [39] and a finite state machine (FSM) [17] have been reported. Although highly dependent on operating frequency and exact functionality, both [17] and [39] report current consumption from the controller in the order of 20 μW. Taking 100 mK as an upper boundary for the operating temperature, there is a reasonable amount of power available for the implementation of a more comprehensive controller than the currently used shift registers in this work. Finally, a higher level of integration can be achieved by also integrating the voltage reference for the DAC, which is possible thanks to the μW-power consumption and recent developments in cryogenic voltage references [58], [59], thus further reducing the system complexity.

V. CONCLUSION

A quantum computer that can outperform a classical computer will likely require millions of qubits operating at sub-1-K temperatures. As this would result in an enormous number of control lines, the required wiring would pose significant challenges in terms of system integration. To explore the potential of cryo-CMOS operating at mK temperatures as an alternative solution, a cryo-CMOS demultiplexer and cryo-CMOS DC DAC fabricated in a commercial 22-nm FinFET process have been experimentally demonstrated at a temperature below 70 mK, only consuming 120 μW while providing the voltage biasing for up to 96 channels. The proposed biasing approach was successfully tested using a custom-made germanium 2-D crossbar array containing 648 SHTs. These results show the potential of integrating cryo-CMOS electronics at mK temperatures together with quantum devices, in turn supporting the scaling of future quantum computers.

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Job van Staveren received the B.Sc. degree in electrical engineering and the M.Sc. degree in electrical engineering, with a specialization in microelectronics, in 2016 and 2018, respectively, from the Delft University of Technology, Delft, The Netherlands, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include analog/mixed-signal design with a particular focus on design for the cryogenic temperature range as well as measurement of CMOS-electronics at cryogenic temperatures.

Luc Enthoven received the B.Sc. and M.Sc. degrees in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 2018 and 2020, respectively. He is currently working toward the Ph.D. degree in the field of cryo-CMOS circuits for scalable quantum computing in the group of Fabio Sebastiano at QuTech, Delft University of Technology.

During his Ph.D., he has presented his work at conferences, such as ISSCC and VLSI. During his studies, he was an Intern with the Analog Devices BMS group, Munich, Germany. His research interests include analog and mixed-signal circuit design, as well as low-power cryo-CMOS circuits and systems.

Peter Luka Bavdaz received the B.Sc. and M.Sc. degrees in applied physics with a specialization in quantum mechanics from the Delft University of Technology, Delft, The Netherlands, in 2015 and 2017, respectively.

After completing his Ph.D. research in Delft, he continued his research into experimental semiconductor quantum computing with Intel, Hillsboro, TX, USA, in 2024. His professional interests include designing and measuring quantum devices to support high-throughput characterization and feedback cycles, enabling scalability through statistical analysis and automation.

Marcel Meyer received the B.Sc. degree in physics and the M.Sc. degree in experimental condensed matter physics from RWTH Aachen University, Aachen, Germany, in 2016 and 2019, respectively, and the Ph.D. degree in physics from the Delft University of Technology, Delft, The Netherlands, in 2024.

Since 2024, he has been a Postdoctoral Researcher with the University of Innsbruck specializing in trapped-ion quantum computing. His research with QuTech focused on 2-D spin qubit arrays and the development of novel techniques for electrically controlling their uniformity. His research interests include quantum error correction, quantum characterization, verification, and validation, leveraging current trapped-ion systems to explore new quantum algorithm ideas.

Corentin Déprez received the Ph.D. degree in condensed matter and radiation physics from Institut Néel, Grenoble, France, in 2021.

He is a Postdoctoral Researcher with QuTech/TU Delft, Delft, The Netherlands, in the group of Menno Veldhorst. He worked on quantum hall physics and electron interferometry in graphene heterostructures. His current research focusses on hole spin qubits in planar germanium heterostructures and developing new strategies for the operation of spin qubit arrays.

Ville Nuutinen received the vocational degree in micromechanics from The Finnish School of Watchmaking, Espoo, Finland. He is currently working toward the bachelor's degree in automation technology with the Metropolia University of Applied Sciences, Helsinki, Finland.

Since 2016, he has been employed by Bluefors, working on cryogenic wiring, system design, and more recently, mechanical designs related to quantum science products. His research interests include electronic device packaging and its implementation in cryogenic systems.

Russell E. Lake received the Ph.D. degree in physics from Clemson University, Clemson, SC, USA, in 2012.

His thesis work was conducted with the National Institute of Standards and Technology (NIST), Gaithersburg, MD, USA. In 2012, he joined the Department of Applied Physics, Aalto University, Espoo, Finland. In 2016, he worked as an Affiliate with Lawrence Berkeley National Laboratory, Berkeley, CA, USA. From 2016 to 2019, he researched superconducting qubits with NIST, Boulder, CO, USA, and held the NRC Postdoctoral Fellowship from 2017 to 2019. Since 2019, he has been with Bluefors Oy, Helsinki, Finland, where he initially held the position of Senior Scientist and currently the Director of Quantum Applications. His research focuses on the advancement of quantum technologies through innovative measurements.

Dr. Lake was the recipient of the Academy of Finland Postdoctoral Fellowship to research superconducting nanoelectronic devices at millikelvin temperatures. He is a member of the American Physical Society.

Davide Degli Esposti received the B.Sc. degree in physics and the M.Sc. degree in physics, with a specialization in condensed matter physics from Pisa University, Pisa, Italy, in 2017 and 2020, respectively. He is currently working toward the Ph.D. degree in applied physics with QuTech, TU Delft, Delft, The Netherlands, in the group led by Giordano Scappucci.

His research interests include the growth and characterization of Si/SiGe heterostructures for hosting single electron spin qubits.

Cornelius Carlsson received the M.Eng. degree in materials science and engineering from Imperial College London, London, U.K., in 2021, and the M.Sc. degree in applied physics from the Delft University of Technology, Delft, The Netherlands, in 2023. He is currently working toward the D.Phil. degree in engineering science with the University of Oxford, Oxford, U.K., focusing on the automated tuning of scalable spin qubit architectures using machine learning.

Previously, in 2023, he joined IBM Research as a Visiting Researcher, Zürich, Switzerland, and completed internships in the two years prior with Quantware, Delft, and with the Max Planck Institute of Quantum Optics, Munich, Germany.

Alberto Tosato received the B.Sc. degree in chemical and material engineering from the University of Padova, Padova, Italy, and the M.Sc. degree in material science from Augsburg University, Minneapolis, MN, USA. He is currently working toward the Ph.D. degree in physics with the Delft University of Technology, Delft, The Netherlands.

His research interests include quantum transport and spin qubits in planar germanium.

Jiang Gong received the B.Sc. degree in electrical and electronic engineering with distinction from Jilin University, Changchun, China, in 2015, and the M.Sc. (cum laude) and Ph.D. degrees from the Delft University of Technology, Delft, the Netherlands, in 2017, and 2022, respectively.

From 2022 to 2024, he was with SiTime Netherlands as a senior analog/mixed-signal integrated circuit Designer, focusing on phase-locked loop design for precision timing applications. From January 2024 to November 2024, he was with ETH Zurich as a Postdoctoral Researcher. Since December 2024, he has been a Full Professor with the University of Electronic Science and Technology of China, Chengdu, China. His current research includes high-spectral-purity and wide-tuning-range frequency synthesizers, high-speed data converters, and high-precision analog design for wireless, wireline, and quantum computing applications.

Dr. Gong is a Reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, and IEEE SOLID-STATE CIRCUITS LETTERS. He was the recipient of the IEEE Solid-State Circuits Society Predoctoral Achievement Award for 2021–2022, the Chinese Government Award for Outstanding Self-Financed (non-government sponsored) Students Abroad, and the Best Student Paper Award at IMS-2023 (second place).

Bagas Prabowo (Graduate Student Member, IEEE) received the B.Sc. degree in electrical engineering from the University of Twente, Enschede, The Netherlands, in 2018, and the M.Sc. degree in electrical engineering, in 2020, from the Delft University of Technology, Delft, The Netherlands, where he is currently working toward the Ph.D. degree in electrical engineering with QuTech, Delft.

His research interests include cryogenic RF integrated circuits for quantum computer applications with a focus on qubit readout, cryogenic electronics, cryogenic RF characterization, and wireless receivers.

Dr. Prabowo is currently a Reviewer for the IEEE SOLID-STATE CIRCUITS LETTERS and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I.

Masoud Babaie (Senior Member, IEEE) received the B.Sc. degree (Hons.) in electrical engineering from the Amirkabir University of Technology, Tehran, Iran, in 2004, the M.Sc. degree in electrical engineering from the Sharif University of Technology, Tehran, in 2006, and the Ph.D. degree (*cum laude*) in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 2016.

From 2006 to 2011, he was with the Kavoshcom Research and Development Group, Tehran, where he was involved in designing wireless communication systems. From 2014 to 2015, he was a Visiting Scholar Researcher with Berkeley Wireless Research Center, Berkeley, CA, USA. In 2016, he joined the Delft University of Technology, where he is currently an Associate Professor. He has authored or coauthored one book, three book chapters, 11 patents, and more than 100 peer-reviewed technical articles. His research interests include RF/millimeter-wave integrated circuits and systems for wireless communications and cryogenic electronics for quantum computation. Dr. Babaie was a co-recipient of the 2015–2016 IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award, the 2019 IEEE ISSCC Demonstration Session Certificate of Recognition, the 2020 IEEE ISSCC Jan Van Vessem Award for Outstanding European Paper, the 2022 IEEE CICC Best Paper Award, and the 2023 IEEE IMS Best Student Paper Award (second place).

Dr. Babaie was the recipient of the Veni Award from the Netherlands Organization for Scientific Research in 2019. He is currently on the Technical Program Committee of the IEEE International Solid-State Circuits Conference. He is the Co-Chair for the Emerging Computing Devices and Circuits Subcommittee of the IEEE European Solid-State Electronics Research Conference. He is also an Associate Editor for IEEE SOLID-STATE CIRCUITS LETTERS.

Carmen G. Almudever (Member, IEEE) received the Ph.D. degree in electronic engineering from the Universitat Politècnica de Catalunya (UPC BarcelonaTech), Barcelona, Spain, in 2014.

From 2014 to beginning 2021, she was an Assistant Professor with the Quantum and Computer Engineering Department and Group Leader with the Quantum Computing division, QuTech, Delft University of Technology, Delft, The Netherlands, where she worked on the definition and implementation of scalable quantum computer architectures. In February 2021, she joined the Computer Engineering Department, Universitat Politècnica de València, Valencia, Spain, as a Distinguished Researcher (Beatriz Galindo program for attracting talented researchers). She has authored or coauthored one book chapter and more than 60 peer-reviewed technical publications. Her research interests include different aspects full-stack quantum computing systems, including quantum programming languages and compilers, quantum error correction, fault-tolerant quantum computation, mapping of quantum algorithms, and benchmarking and sclalability of (modular) quantum computers.

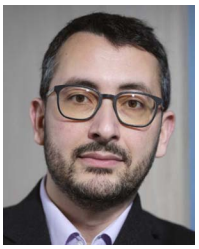
Dr. Almudever is currently an Associate Editor for the *ACM Transactions on Quantum Computing*. She was the Technical Program Co-Chair of the Computing Frontiers Conference 2021 and the Program Track Co-chair (Quantum Systems Software) of QCE22. She was the recipient of several awards that include the 2017 MICRO Best paper Award, three HiPEAC awards (2017, 2023), the Intel Doctoral Student Honor Programme Award (2012), and Beatriz Galindo Grant from the Spanish Ministry of Universities in 2020. She is the Coordinator of an EiC Pathfinder Open project on scalable multicore quantum computer architectures.

Menno Veldhorst is a Group Leader with QuTech, Delft university of Technology, Delft, The Netherlands, and he is a Pioneer in silicon and germanium semiconductor quantum technology. His group demonstrated the first single hole qubit, the first universal quantum gate set in germanium, and a four-qubit quantum processor in germanium. His scientific contributions has been acknowledged as one of top ten physics breakthroughs in 2015.

Dr. Veldhorst was the recipient of the Nicholas Kurti Science prize. He has been included as a visionary by MIT technology review list 35 innovators under 35. Since 2025, he is a Founding Advisor of Groove Quantum.

Giordano Scappucci received the M.Sc. degree from the Universita' La Sapienza Roma, Rome, Italy, in 2000, and the Ph.D. degree from the Universita' Roma TRE, Rome, in 2004.

From 2005, he was a Researcher with the Centre for Quantum Computing Technology, University of New South Wales, Sydney, NSW, Australia, and from 2015, a Group Leader with QuTech, Delft University of Technology, Delft, The Netherlands, where he leads the development of semiconductor materials for quantum computing. The silicon–germanium quantum materials developed by the Scappucci Lab enabled landmark experiments in the field of quantum information and are used by researchers globally for the development of quantum technologies. He has authored or coauthored more than 100 journal articles (for example in Nature, Science, Nature Review Materials) and has given more than 50 invited talks at international conferences, universities, research institutes, and industry.



Fabio Sebastiano (Senior Member, IEEE) received the B.Sc. (cum laude) and M.Sc. (cum laude) degrees in electrical engineering from University of Pisa, Pisa, Italy, in 2003 and 2005, respectively, the M.Sc. degree (cum laude) from the Sant'Anna School of Advanced Studies, Pisa, in 2006, and the Ph.D. degree from the Delft University of Technology, Delft, The Netherlands, in 2011.

From 2006 to 2013, he was with NXP Semiconductors Research, Eindhoven, The Netherlands, where he conducted research on fully integrated CMOS frequency references, nanometer temperature sensors, and area-efficient interfaces for magnetic sensors. In 2013, he joined the Delft University of Technology, where he is currently an Associate Professor. He has authored or coauthored one book, 11 patents, and more than 100 technical publications. His main research interests include cryogenic electronics, quantum computing, sensor read-outs, and fully integrated frequency references.

Dr. Sebastiano is on the Technical Program Committee of the ISSCC and the IEEE RFIC Symposium, and has been on the program committee of IMS. He is currently an Associate Editor of IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION and JSSC, and was also a Guest Editor of the JSSC. He was the recipient of several awards, including the 2008 ISCAS Best Student Paper Award, the 2017 DATE best IP award, the ISSCC 2020 Jan van Vessem Award for Outstanding European Paper, and the 2022 IEEE CICC Best Paper Award. He was a Distinguished Lecturer of the IEEE Solid-State Circuit Society.