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Technologies for Scaling Silicon-MOS Quantum Processors

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Technologies for Scaling Silicon-MOS Quantum Processors

William James Gilbert

A thesis in fulfilment of the requirements for the degree of

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School of Electrical Engineering & Telecommunications

Faculty of Engineering

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Abstract

Gate-defined quantum dots have been identified as a promising platform for quantum information processing thanks to low error rates, and the possibility for large-scale integration with industrial semiconductor manufacturing processes. With multiple recent demonstrations in semiconductor-based material stacks showing high-performance single- and two-qubit gates, the focus turns to how to scale-up these technologies.

In this thesis, three advancements are presented in-depth for the scale-up of Silicon-MOS based quantum dot devices for quantum computation.

Firstly, a passive filter/combiner is developed that behaves as a DC-coupled bias tee. This allows for linear combination of DC-bias voltages with broadband pulses (DC - 500 MHz) from an Arbitrary Waveform Generator (AWG), without AC-coupling the AWG line. These combiners are then optimised for low-power and integrated into the cryostat at the 4 K stage to reduce electrical noise.

Secondly, we investigate devices based on Fully-Depleted Silicon-On-Insulator (FDSOI) technology manufactured in a full-scale 300mm wafer process as a platform for quantum dot based quantum processors. A double-nanowire device is configured such that a 2x2 array of quantum dots is formed in one nanowire, with a Single Electron Transistor (SET) formed in the other nanowire which is used as a charge sensor. The SET sensitivity is improved by the addition of floating gates between the nanowires, which increases capacitive coupling. The tunnel coupling between adjacent quantum dots is modelled, motivating modifications to the device design, and delineating a pathway towards adoption of CMOS industry processes for scalable manufacture.

Finally, we demonstrate a technique that enables fully electrical control of electron spins by enhancing the intrinsic spin-orbit coupling (SOC), which is naturally weak for electrons in silicon. The SOC is enhanced by manipulating the energy quantisation spectrum of the quantum dot to create a level degeneracy. This can be achieved with pulses on gate electrodes, so that the SOC can be enhanced on-demand, allowing for a switchability between ON and OFF control modes. Microwave electrical control of quantum dots in the ON mode shows Rabi oscillation frequencies up to 81 MHz, and single qubit gate fidelities above 99.9%. The effect is reproducible across multiple devices and charge configurations. This technique could alleviate the need to integrate antennas or micromagnets on-chip.

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> Chapter 2 is partially comprised of a manuscript in preparation.
> Chapter 3 is partially comprised of a paper published in Nano Letters 2020.
> Chapter 4 is partially comprised of a manuscript currently under review at Nature Nanotechnology.
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Publications

Peer reviewed journal articles

R. Zhao, T. Tanttu, K. Y. Tan, B. Hensen, K. W. Chan, J. C. C. Hwang, R. C. C. Leon, C. H. Yang, **W. Gilbert**, F. E. Hudson, K. M. Itoh, A. A. Kiselev, T. D. Ladd, A. Morello, A. Laucht, A. S. Dzurak."Single-spin qubits in isotopically enriched silicon at low magnetic field". Nature Communications vol. 10, no. 5500 (2019).

W. Gilbert, A. Saraiva, W. H. Lim, C. H. Yang, A. Laucht, B. Bertrand, N. Rambal, L. Hutin, C. C. Escott, M. Vinet, A. S Dzurak. "Single-electron operation of a silicon-CMOS 2 $\times$ 2 quantum dot array with integrated charge sensing". Nano Letters, vol. 20, p. 7882-7888.

J. Yoneda, W. Huang, M. Feng, C. H. Yang, K. W. Chan, T. Tanttu, **W. Gilbert**, R. C. C. Leon, F. E. Hudson, K. M. Itoh, A. Morello, S. D. Bartlett, A. Laucht, A. Saraiva, A. S. Dzurak. "Coherent spin qubit transport in silicon". Nature Communications, vol. 12, no. 4114 (2021).

Articles submitted for publication

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M. Feng, J. Yoneda, W. Huang, Y. Su, T. Tanttu, C. H. Yang, J. D. Cifuentes, K. W. Chan, **W. Gilbert**, R. C. C. Leon, F. E. Hudson, K. M. Itoh, A. Laucht, A. S. Dzurak, A. Saraiva. "Control of dephasing in spin qubits during coherent transport in silicon". *arXiv:2207.11865*, (2022).

Z. Wang, M. Feng, S. Serrano, **W. Gilbert**, R. C. C. Leon, T. Tanttu, P. Mai, D. Liang, J. Y. Huang, Y. Su, W. H. Lim, F. E. Hudson, C. C. Escott, A. Morello, C. H. Yang, A. S. Dzurak, A. Saraiva, A. Laucht. "Jellybean quantum dots in silicon for qubit coupling and on-chip quantum chemistry". *arXiv:2208.04724*, (2022).

Article in preparation

W. Gilbert, C. H. Yang, T. Tanttu, B. Hensen, A. Laucht, A. S. Dzurak. "A Linear Alternative to Bias-Tees for Spin Qubit Control". To be submitted to Review of Scientific Instruments.

Conference presentations

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- 2021 IEEE Quantum Week QCE21, USA (Virtual talk)
- 2022 APS March Meeting, Chicago, USA (Virtual talk)
- 2022 CQC2T Annual Workshop, Hobart, Australia (Poster)

W. Gilbert, A. Saraiva, W. H. Lim, C. H. Yang, A. Laucht, B. Bertrand, N. Rambal, L. Hutin, C. C. Escott, M. Vinet, A. S Dzurak. "Single-electron operation of a silicon-CMOS 2×2 quantum dot array with integrated charge sensing". Presented at:
- 2019 CEA-Leti internal workshop, Grenoble, France (Talk)
- 2020 SQA Student Mini-Conference, Sydney, Australia (Talk)

W. Gilbert, C. H. Yang, T. Tanttu, B. Hensen, A. Laucht, A. S. Dzurak. "Progress in Linear Alternatives to Bias-Tees for Quantum Dot Control". Presented at:
- 2018 Silicon Quantum Electronics Workshop, Sydney, Australia (Poster)
- 2019 Silicon Quantum Electronics Workshop, San Sebastian, Spain (Poster)
- 2020 CQC2T Annual Workshop, Kingscliff, Australia (Poster)

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Chapter 1

Introduction

The development of computers and digital information systems over the course of the 20th and 21st centuries has driven technological and social change that has profoundly revolutionised human civilisation. Modern technologies such as portable talking navigation assistants, wireless earbuds, and virtual reality only existed in science fiction until very recently as progress continues at full speed more than 60 years after the invention of transistors, and almost a century after the birth of the field of computer science.

Today, thanks to the incredible scaling of silicon CMOS technology, computers can solve a huge set of problems. However, there are some problems that are too complex for today's computers, and will remain intractable for the foreseeable future within classical information systems, and some of these problems would be immensely valuable to solve. Computers based on quantum mechanics and quantum information theory are predicted to be capable of solving some of these problems in fields such as material science, medicine, and cryptography.

This thesis investigates technologies for developing and scaling such a computer based on quantum dots in silicon.

1.1 Quantum Computation

A quantum computer is one that harnesses the unique nature of quantum mechanical interactions in order to perform computations. Specifically, superposition and entanglement are key to the quantum algorithms that promise to revolutionise our computing capability [1–3]. The task then is to create a system in which superposition and entanglement can be reliably created on demand, controlled, and read out. The system then has to be scaled, much like classical computers have been, in order to be able to tackle problems of value [4–6].

1.1.1 Qubits and DiVincenzo's Criteria

The fundamental building block of a quantum computer is the quantum bit, or qubit [7]. The classical bit of information acts as a binary switch, representing the states 0 and 1, whereas a qubit can be represented as a unit vector in three-dimensional space which we can visualise as a point on the Bloch sphere (Figure 1.1). The qubit state $|\Psi\rangle$ then contains information equivalent to two phases θ and φ. When the qubit state is measured, it collapses into one of two basis states with probabilities $cos^2(\theta/2)$ and $sin^2(\theta/2)$ for the respective basis states. By convention we define the measurement operation in the Z direction, with basis state outcomes of $|0\rangle$ and $|1\rangle$.

Prior to measurement, the qubit retains full information as the state vector may point anywhere on the sphere, representing a superposition of the two outcome states. Further to this, with multiple qubits we may create non-classical correlations between output states, known as entanglement. The field of quantum information theory builds on these concepts in the design of algorithms for applications of quantum computers, and is beyond the scope of this thesis.

In order to create a quantum computer that may usefully execute quantum algorithms, the underlying physical qubit technology must meet five criteria set out by David DiVincenzo [9].

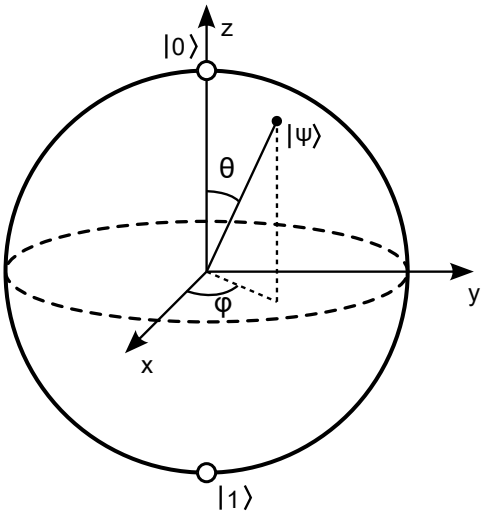


Figure 1.1: Bloch sphere. A qubit can be represented as a unit vector or point on the Bloch sphere. Figure adapted from [8].

1. **A scalable physical system with well characterized qubits.**

   One needs a physical system upon which a qubit can be encoded in a reproducible manner. That is, a well-defined 2-level system with some energy gap. The physical system also needs to be scalable.

2. **The ability to initialise the state of the qubits to a simple fiducial state**

   Computation, both classical and quantum, relies on a known initial state of the system.

3. **Long relevant decoherence times**

   One needs to be able to maintain the state of a qubit for long enough to be able to execute many control operations. More recently this could arguably be extended to incorporate compatibility with error correction protocols [10].

4. **A universal set of quantum gates**

   The set of quantum gates available in the system must be able to access any quantum state of the system.

5. **A qubit-specific measurement capability**

One needs to be able to read out the state of the system with high accuracy, both during and after computation.

1.1.2 Quantum Technologies and Progress

The landscape of technologies for quantum computers that have fulfilled DiVincenzo's criteria has evolved considerably. Now, dedicated commercial efforts are ongoing to build systems using different technologies such as qubits based on superconducting Josephson junctions, trapped ions and neutral atoms, photons, vacancy centres in diamond, and quantum dots and dopants in semiconductors.

The capability of quantum computers has advanced into what is now called the NISQ (Noisy Intermediate Scale Quantum) era [11], after the first demonstrations of quantum computer surpassing classical computers in specific tasks [12–14]. The NISQ era describes a phase where simple quantum algorithms can but run, but where qubit errors limit their effectiveness.

The next phase involves the implementation of error correction protocols which will allow algorithms to run indefinitely, without being affected by noise. To do this, many physical qubits are used to encode a single logical qubit which is protected from errors. One promising encoding, the surface code [10], requires on the order of thousands of physical qubits to encode a single logical qubit. This means that there is significant overhead in the numbers of qubits required to run useful algorithms. Recent studies make estimates on the order of millions of physical qubits required when assuming a 0.1% gate error rate [4–6].

The effectiveness of error correction protocols is very active field of research, with recent demonstrations of reductions in error rates in both trapped ion- [15] and superconducting qubit-based systems [16, 17]. These demonstrations are very encouraging, as they show that with more qubits, and modest reductions in error rates, it seems that it will eventually be possible to build fault tolerant systems.

The importance of scalability in quantum computing can hardly be overstated as studies

indicate the need for millions of qubits for early demonstration of quantum algorithms. The development of classical computing technology provides us with an example of a possible development path, and some salient lessons.

The capability of classical computers advanced rapidly since their inception in the early 20th century. However, critical to this advancement was a fundamental change in their construction that occurred with inventions of the bipolar junction transistor (BJT) in 1947 and the metal oxide semiconductor field effect transistor (MOSFET) in 1959. Prior to this, computers were built from vacuum tubes - a large, hot, and unreliable equivalent to today's JFET. Scaling such a system proved impractical due to the bulkiness, power requirement, and unreliability of vacuum tubes. Only with the advent of transistors and then integrated circuits in the 1960's computers started to get smaller. As transistors were miniaturised, the processing power of computer systems advanced further and further, as more transistors could be integrated into a single system. Today, state-of-the-art chips contain tens of billions of transistors.

Just as semiconductor technologies gave classical computers a way to achieve extraordinary scale, it may again provide a way for quantum computers to scale to the millions, and even billions of qubits.

1.2 Quantum Dot Spin Qubits

The quantum dot spin qubit proposed in 1998 by Loss and DiVincenzo [18] has the potential to be a scalable technology platform quantum computers. Spin states of electrons (or holes) in a quantum dot can behave as well-defined two-level systems which can then can be used to form qubits. Spin is a quantum mechanical property that results from the intrinsic magnetic moment of the electron, and can be polarised with the application of an external magnetic field, with an energy gap caused by the Zeeman effect equal to

$$E_z = g\mu_B B \tag{1.1}$$

where g is the Lande g-factor, μ_B is the Bohr magneton, and B is the magnetic field strength. This results in spin states parallel and anti-parallel to the applied magnetic field, which we denote $|\downarrow\rangle$ and $|\uparrow\rangle$, respectively.

A number of material platforms for quantum dot qubits have been demonstrated, such as GaAs/AlGaAs heterostructures [19, 20], Si/SiGe heterostructures [21–24], Ge/SiGe heterostructures [25], planer silicon MOS [26,27], silicon MOS nanowires and FinFets [28–30], nanowires made from Ge [31], Ge/Si [32], and InAs [33], graphene [34], and even solid neon [35]. Dopant based qubits in semiconductors are a promising technological pathway for quantum computers because of the long coherence times and gate fidelities of nuclear spins, with active development on two manufacturing technologies - One using ion implantation [36–38], and the other using STM lithography [39].

The silicon MOS, Si:P, and Si/SiGe material stacks have already demonstrated high-fidelity one- and two-qubit gate operations [22–24, 27, 37, 38, 40, 41]. Silicon MOS in particular has great potential to leverage the existing manufacturing capability of the CMOS industry, with multiple demonstrations of qubits in devices manufactured in full-scale 300 mm wafer process lines [28–30, 42].

1.2.1 Silicon MOS

Silicon MOS quantum dots leverage the same manufacturing technology that is used to fabricate the chips used in today's classical computers. This consists of a bulk-Si substrate, an insulating oxide layer, and metallic gate electrodes which are used to apply electrostatic biases to form a quantum well within the bulk-Si active area, as shown in Figure 1.2. An insulating layer may also be placed between the active Si region and bulk, which will be investigated in Chapter 3.

Quantum dots can be formed in structures akin to traditional MOS transistor device. We form a accumulate a layer of mobile electrons at the interface between Si and SiO_2 by applying a positive bias voltage to a metal gate electrode (gate ST in Figure 1.2a). We

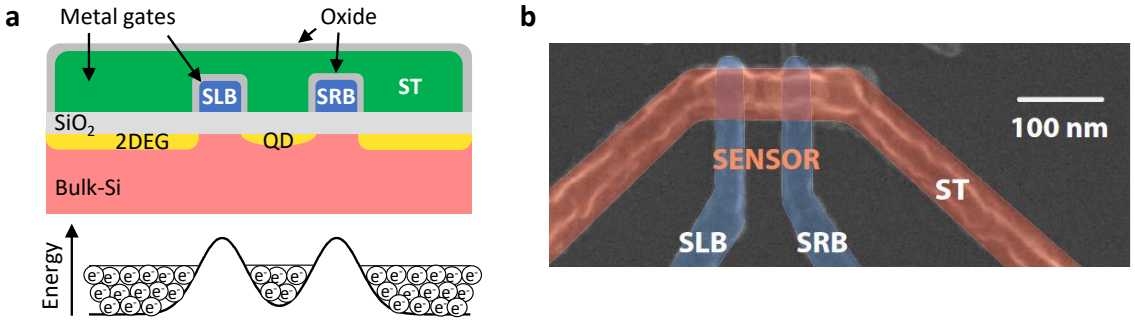


Figure 1.2: Silicon MOS device structure. **a**, schematic cross-section of a MOS quantum dot device structure, consisting of a bulk-Si active layer, an insulating SiO_2 layer, and patterned gate electrodes which are used to shape the chemical potential and accumulate and isolate quantum dots. **b**, Top-down SEM image of the same design as in **a**. This gate layout can be used to form a single electron transistor (SET). Figure **b** adapted from [43].

call this electron layer a 2-dimensional electron gas (2DEG). To form a quantum dot, additional screening gates SLB and SRB are added to create barriers in the potential, and in-turn, gaps in the 2DEG. When operated at deep cryogenic temperatures of 4 Kelvin and below this structure can now form a single confined quantum dot, along with two leads formed by the conductive 2DEG.

Due to electron-electron repulsion, a finite amount of energy is required to add an electron to the quantum dot, denoted as E_C, which causes a quantisation of the dot charge occupation. The charging energy decreases as the quantum dot becomes larger, reducing the relative electron repulsion. Figure 1.3a shows this trend in charging energies, along with peaks at the addition of the first, fifth, and thirteenth electrons, corresponding to shell structure of the quantum dot. For silicon there are spin, orbital, and valley degrees of freedom, leading to 2D Fock-Darwin states as in Figure 1.3b [44]. n and l correspond to the quantum numbers, and v to the valley state which in silicon is restricted to only z-valleys due to the electrostatic and 2-dimensional confinement. In general, it is desirable to ensure that the energy levels within a dot are well quantised, however an exception to this rule will be investigated in Chapter 4 where a degeneracy between levels is utilised for spin control.

Quantum dots in MOS structures can thus have well-defined two level spin states, and

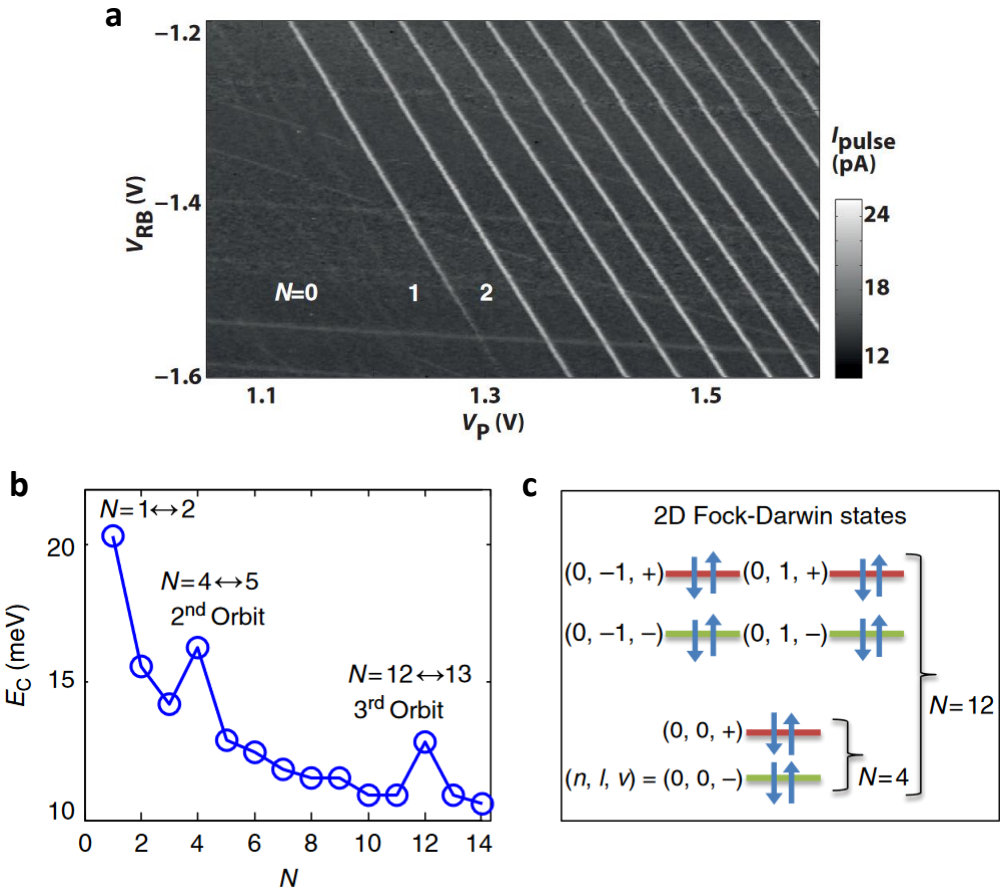


Figure 1.3: Charging energy spectrum of a Si quantum dot. **a**, Discrete charge filling of a quantum dot. Figure adapted from [43]. **b**, Charging energies for the first 14 electrons of a quantum dot in silicon, showing peaks at the addition of the first electron to a new orbital. **c**, 2-dimensional Fock-Darwin states for quantum dots in silicon. n and l are quantum numbers, and v is the valley state. Figures **b** and **c** adapted from [44].

can be reliably produced and scaled with different designs of the control gate electrodes, thus fulfilling the first of DiVincenzo's criteria.

1.2.2 Initialisation

Electron spin qubits in silicon typically have very long T_1 spin relaxation times [44, 45]. Because of this, it is not practical to wait for normal relaxation processes to reset or initialise a qubit, and a range of techniques are used. Two widespread techniques are energy selective loading from a charge reservoir, and splitting of spin singlet states in a double quantum dot. Each of these techniques can be augmented with hotspot relaxation [44]. Readout can also serve as initialisation if it is a non-destructive process.

An example of a device that can utilise reservoir spin loading is shown in Figure 1.4a. The gate LD accumulates a 2DEG connected to ground via an ohmic contact, a charge reservoir which acts a homogeneous spin bath with a Fermi energy, E_F. A quantum dot is formed under the tip of gate P, and its tunnel rate to the reservoir controlled by the barrier gate LB. To load a deterministic spin state, first the electrons are unloaded from the dot by lowering the voltage on P. Next, the potential of the dot is set so that the spin-up and spin-down states straddle the Fermi level set by the reservoir. At this bias point, only a spin-down electron will tunnel into the dot. Finally, the dot is tuned far away from the Fermi level to decouple the spin from the reservoir. Instead of three discrete levels, this process can be replaced by a slow ramp, which is more robust to charge noise as the separation between up and down spin states is typically small ($<$1 mV).

Where a charge reservoir is not available (such as in the middle of an array of quantum dots), spin states may be initialised in a double dot by first creating a singlet state in one dot, then spreading the wavefunction over the two dots. Figure 1.5a shows a device in which this can be done, when quantum dots are formed under the gates G1 and G2, and designated as QD1 and QD2 respectively (Figure 1.5b).

A singlet state is first created in QD2, corresponding to a charge state of (0,2), where

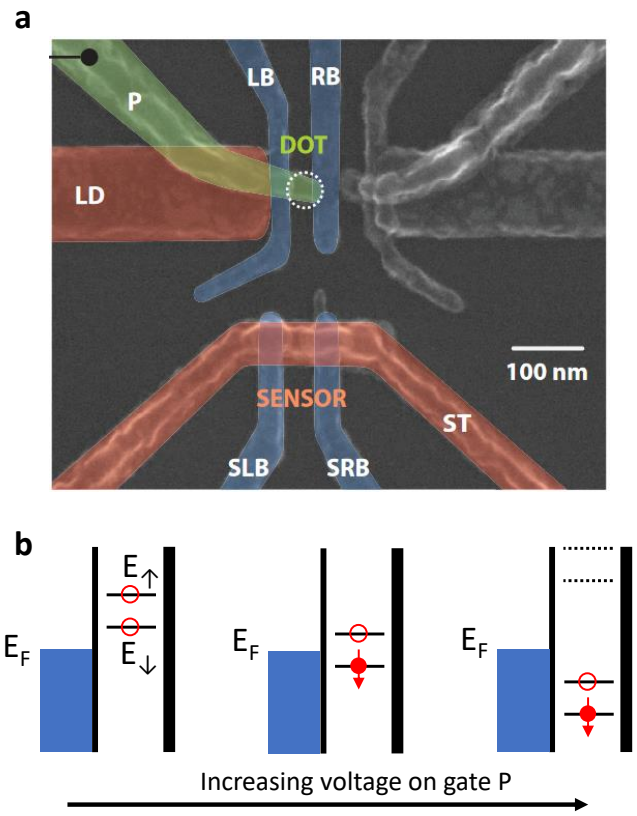


Figure 1.4: Reservoir spin initialisation. **a**, SEM image of a MOS quantum dot device, in which a dot is formed under the tip of gate P. A charge reservoir is accumulated under LD, and connected to ground via a doped lead and ohmic contact. **b**, Initialisation protocol to load a spin down electron from a charge reservoir with a Fermi energy E_F, with a Zeeman splitting of the spin up and spin down states. Firstly, unload the electron from the quantum dot by decreasing the dot gate voltage. Next, set the voltage such that the Fermi energy E_F sits between the two spin levels, so it is favourable for only a spin-down electron to load into the dot. Finally, increase the voltage on P further to decouple the spin from the reservoir. Figure **a** adapted from [43]

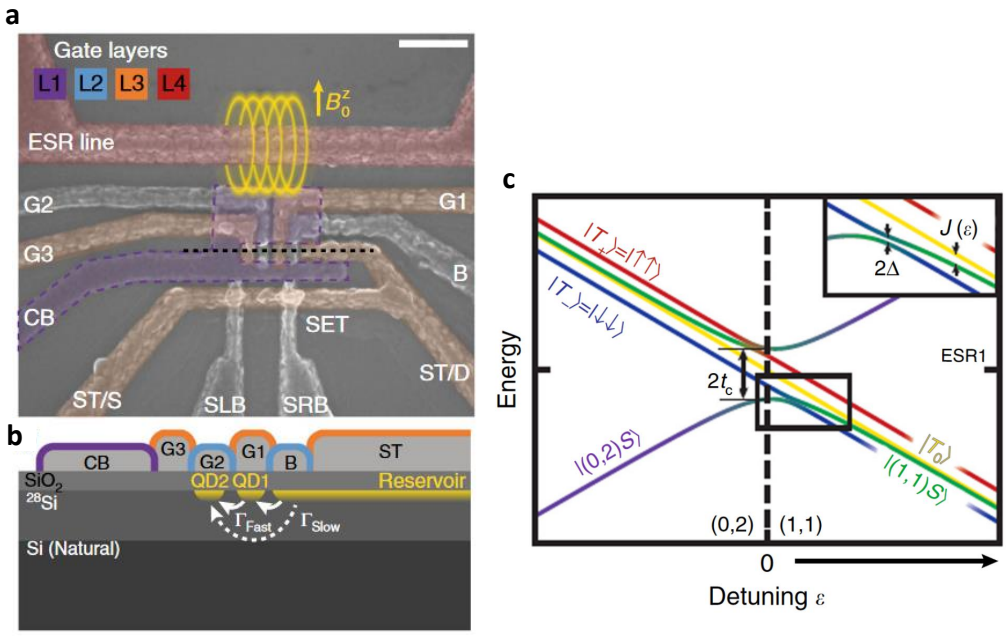


Figure 1.5: Inter-dot spin initialisation. **a**, SEM image of a MOS quantum dot device, in which quantum dots are formed underneath the gates G1 and G2. **b**, Cross-sectional schematic of the device, with quantum dots QD1, QD2, and the charge reservoir indicated in yellow. **c**, Inter-dot level-crossing diagram for the (0,2)-(1,1) charge anti-crossing. A $|(0,2)S\rangle$ two-electron singlet state in QD2 can be split between QD2 and QD1 be ramping the inter-dot detuning across the charge anti-crossing. The ramp rate must be slower than the tunnel coupling t_c to ensure an adiabatic transition. To keep a singlet state, the ramp rate must also be faster than the S to T_- coupling, Δ (shown in inset), when crossing the S to T_- transition. A T_- state can be created by ramping slowly over the S to T_- transition, at a rate slower than Δ. Figure adapted from [46]

(X,Y) denote the charge numbers in dot X and Y. One electron is then moved to QD1 by ramping the detuning voltage between the two quantum dots across the charge anti-crossing, creating a (1,1) charge state. The ramp rate across the anti-crossing must be slower than the inter-dot tunnel rate t_c in order to transfer the electron adiabatically and preserve the singlet state. The ramp rate must also be fast enough to avoid relaxation at the S to T_- transition, shown in the inset to Figure 1.5c. Often this is achieved by tuning the interdot coupling, as it can achieve a larger range of tunability than the ramp rate for practical time scales. After some time the $|(1,1)S\rangle$ state will relax to a mixture of $|\uparrow\downarrow\rangle$ and $|\downarrow\uparrow\rangle$. A high probability of a single one of these states can be achieved with a sufficient Zeeman energy difference (δE_z) between the two dots, and a careful tuning of the ramp rate.

A pure $|\downarrow\downarrow\rangle$ or T_- state can be created by ramping slowly across the $|(1,1)S\rangle$-$|(1,1)T_-\rangle$ transition. It is also possible to use valley or orbital state degeneracies as relaxation hotspots to quickly reset a spin without altering the charge state [44, 47].

A number of techniques then enable quantum dot qubits to meet DiVincenzo's second criteria, of having a reliable fiducial state initialisation.

1.2.3 Control

The spin control strategies for quantum dots primarily involve some form of microwave control, with the microwave frequency matching the spin Larmor frequency which is set by the Zeeman splitting, E_z, with a strong static magnetic field applied. Exchange-only control protocols (which do not require microwave control signals) also show promising progress, with recent demonstrations of single- and two-qubit gates encoded on six quantum dots [41].

Control based on electron spin resonance (ESR) uses a microwave magnetic field to drive the spins [19]. An oscillating field, B_1, is applied in a direction perpendicular to the static field, B_0, an example of which is shown in Figure 1.6a. The specific spin rotation can be

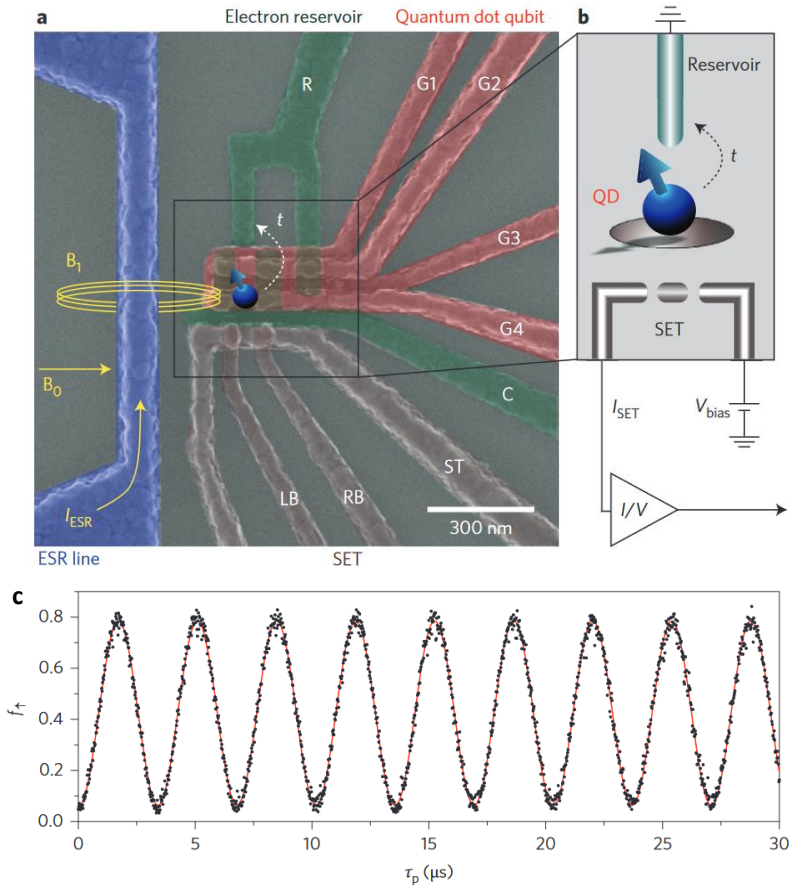


Figure 1.6: Electron spin resonance (ESR). a, Device SEM image with a quantum dot spin qubit situated under the gate electrode G4. The charge state of the dot is sensed with a SET formed under ST. A microwave magnetic field B_1 used to control the qubit is delivered via a micro-antenna, highlighted in blue. A charge reservoir is formed under R. **b**, Simplified schematic of the sensing regime, using the charge reservoir for initialisation and readout. **c**, A Rabi oscillation of an electron spin driven by an applied microwave field. Figure adapted from [48]

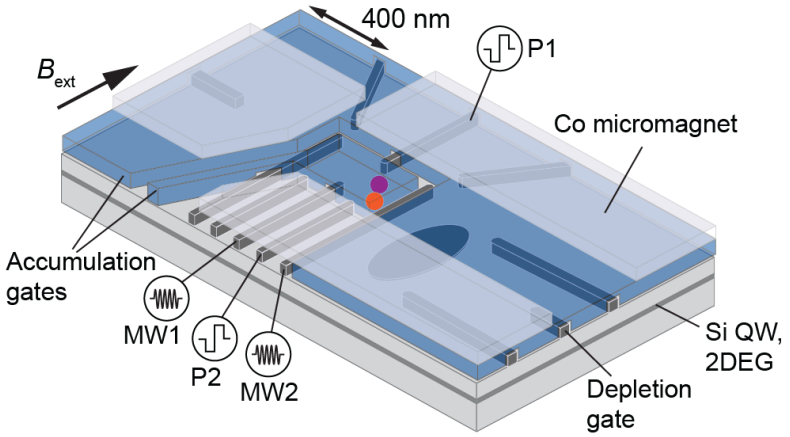


Figure 1.7: Electric dipole spin resonance (EDSR). A device architecture used for electric dipole spin resonance. A micromagnet is fabricated above the qubits which creates a magnetic field gradient. Gate electrodes are then used to deliver a microwave electric field to manipulate the spin via the spin-orbit coupling induced by the magnetic field gradient. Figure adapted from [26]

set by the microwave pulse time, as shown in the Rabi oscillation in Figure 1.6c.

Microwave magnetic fields require large dedicated structures to separate the electric and magnetic field components. It is also challenging to isolate parasitic magnetic fields which can spread far from their source. On the other hand, electric fields can be more targeted, allowing control to be delivered to an individual quantum dot, assuming that microwave control lines are carefully designed with appropriate isolation.

To enable electrical control, one prominent technique is to induce a magnetic field gradient [49], which is commonly done by fabricating a micro-magnet near the qubits [26,50–52]. The gradient that is created in B_0 increases the spin-orbit coupling, which enables the spin to be controlled with electric fields. This technique trades off the large antennae required for magnetic control, in favour of micro-magnets which are still large compared to the quantum dots themselves, but significantly smaller than typical ESR antenna designs. Another advantage of micro-magnets is that the magnetic field gradient gives a large δE_z between nearby qubits, assisting with addressability for small arrays.

In some material stacks, and for hole quantum dots, there is sufficient spin-orbit coupling to drive spins electrically, without the need to add extra structures [28,53,54]. In Chapter 4

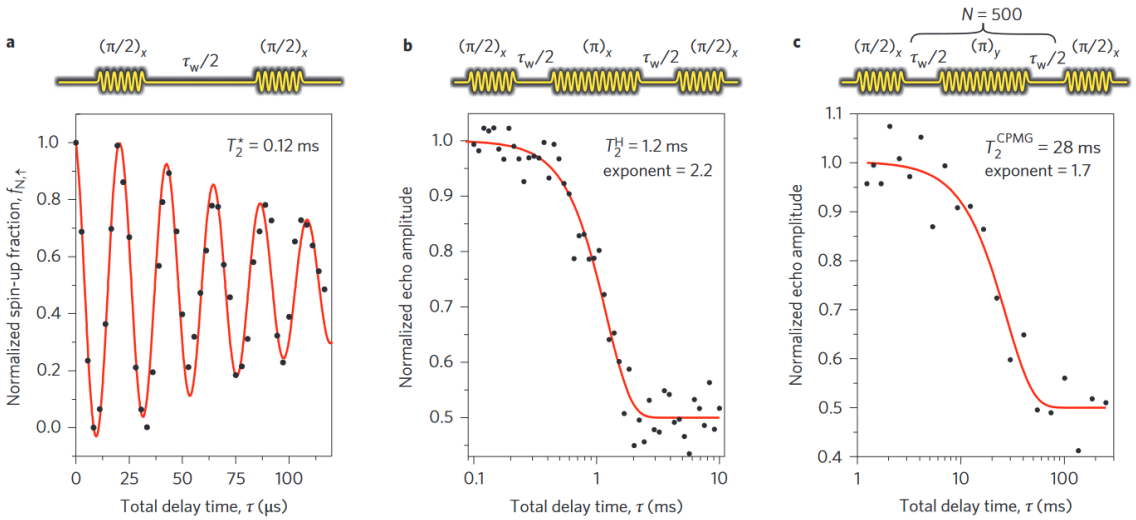


Figure 1.8: Spin coherence times. **a**, Pulse sequence and data for a measurement of the free induction decay time (Ramsey), T_2^*. **b**, Pulse sequence and data for a measurement of the Hahn echo coherence time, T_2^H. **c**, Pulse sequence and data for the CPMG active dynamical decoupling sequence [55], T_2^{CPMG}. Figure adapted from [48]

a technique is investigated to drive electron spins in silicon electrically without a micromagnet.

One of the appeals of electron spin qubits in silicon is their long spin relaxation and coherence times. Spin coherence times typically range between 10-1000 μs with dynamical decoupling, with one such example shown in Figure 1.8, data taken from [48]. When compared to typical gate times with ESR control of 0.1 - 1 μs, high Q-factors can be achieved. The quality factor, Q, is defined as $Q = 2 \times T_2/T_{\mathrm{gate}}$. Multiple recent studies have demonstrated single qubit gate fidelities above 99.9 % [22, 40, 47, 51].

A two qubit gate in quantum dots can be implemented either using the exchange interaction [56,57], or with electric dipole coupling mediated by direct capacitive coupling [58,59], or indirectly via coupling to a cavity [60, 61]. Two-qubit logic gates using exchange have recently surpassed a fidelity of 99 % [22–24, 38], which now shows that quantum dots can implement a universal gate set for multiple qubits with fidelities above error correction thresholds [10].

The demonstration of long coherence times, and high-fidelity universal gate sets mean that

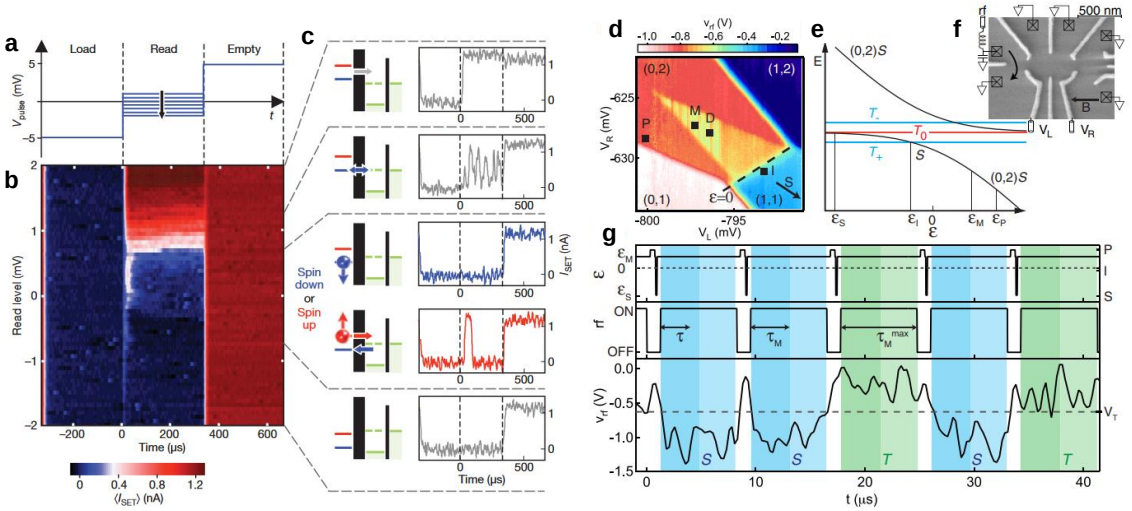


Figure 1.9: Spin to charge conversion. **a-c**, Elzerman readout scheme. A pulse sequence is shown in **a**, and the resulting sensor response shown in **b**. **c** show the current traces that are measured at various read levels. A region with spin-dependent charge tunneling appears between $\approx 0-1$ mV in the read level. **d-g**, Pauli spin blockade readout scheme. A charge stability diagram is shown in **d** at the (1,1)-(0,2) inter-dot charge transition. A triangular region on the (0,2) side of the transition indicates the presence of Pauli blockade. **e**, model energy diagram for the inter-dot transition. **f**, SEM top-view of the test device. **g**, current traces for 5 cycles of the sequence which involves a random initialisation to (1,1) followed by a read phase at the blockade region within (0,2). Blockaded states will remain in the (1,1) charge state, whereas unblockaded states will transition to (0,2). **a-c** adapted from [62]. **d-g** adapted from [63].

quantum dots fulfil DiVincenzo's third and fourth criteria for qubits.

1.2.4 Readout

Readout of quantum dot spin qubits relies on two elements. Firstly a method for spin-to-charge conversion, and secondly a charge sensor to detect the charge state.

A spin can be converted to a charge state either by energy selective tunneling to a charge reservoir, known as Elzerman readout [62, 64], or by utilising Pauli spin blockade (PSB) between two quantum dots [63, 65].

Elzerman readout requires a charge reservoir nearby coupled to the qubit to be read out, and allows for readout of a single spin. Since the charge tunnels out to a reservoir, Elzerman readout is destructive. That is, the qubit is reset as part of the readout.

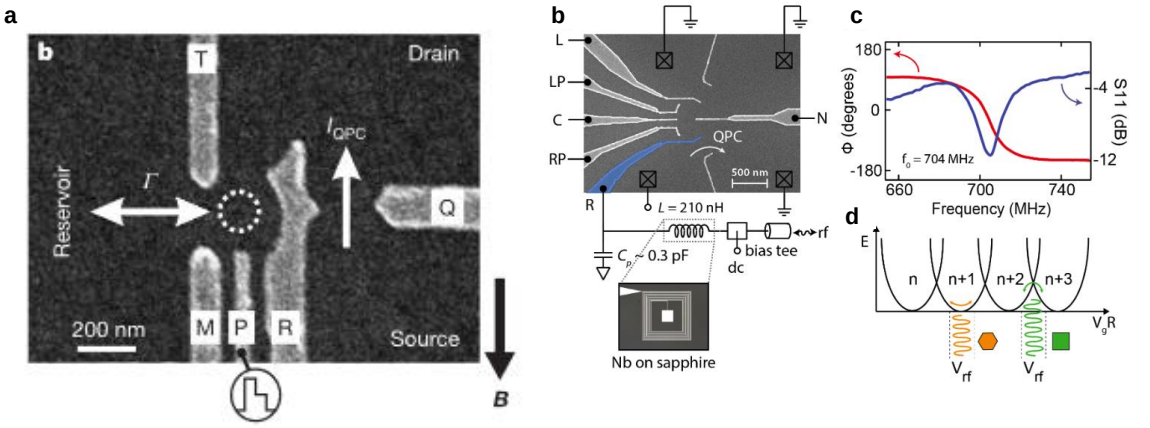


Figure 1.10: Charge sensing techniques. **a**, Quantum point contact (QPC) used to sense charge movements in the adjacent dot. **b**, Gate-based RF sensing, where an LC-tank circuit is connected to the gate R. **c**, Resonance of the LC-tank circuit at 704 MHz. The resonant frequency is influenced by changes in capacitance of the gate R. **d**, Illustrated charging energy spectrum of the quantum dot. A capacitance is added to the circuit when V_{rf} causes a charge movement in the dot. Figure **a** adapted from [64]. Figures **b-d** adapted from [68].

PSB readout does not require a charge reservoir as it uses an inter-dot charge movement. The charge is retained, so this readout type is non-destructive if required. Depending on the timescales of the system, it is possible for PSB to cause blockade in the Singlet-Triplet basis, or in the parity basis [66]. Since PSB readout is performed between two quantum dots, only a single bit of information is gathered for the readout of two spins, but the natural parity check may be useful for some error correcting codes [67].

Two common techniques are used to readout the charge state of qubits during spin-to-charge conversion. The first implements a single electron transistor (SET) or quantum point contact (QPC) which has highly non-linear conductance, making it very sensitive to nearby charge movements [63]. The SET and QPC need to be integrated near the qubits, along with source/drain leads. They can be operated in either DC or RF modes [64, 69]. A second technique is gate-based readout, which senses changes in the capacitance of an electron underneath a gate electrode using an LC-tank circuit [68, 70–73]. This technique has the advantage that it uses the gate electrode that is already required to control the qubit, removing the need to interrupt a qubit array for the integration of an SET. The disadvantage is the requirement for an LC-tank circuit, and the associated RF electronics.

The general technique of using an LC-tank to detect capacitive shifts can also used when an LC-tank is connected to a source/drain contact [74, 75].

In these techniques, quantum dots have a set of viable choices for reliable and high-fidelity qubit readout, meeting DiVincenzo's fifth criteria. With all of the criteria fulfilled, and demonstrated in small-scale devices, we now look to what will be required to create a full-scale quantum computer in silicon, and where this thesis will make contributions.

1.3 The Path to Full-Scale Quantum Computers in Silicon

The pathway towards quantum computers with millions of qubits is likely to take many years. We can make an estimate of this timeline by appropriating Moore's Law from the CMOS industry, which states that the number of transistors in an integrated circuit (IC) will double roughly every two years [76]. With current state of the art systems possessing on the order of 10-100 interacting qubits, it would take approximately 15-20 years to reach the numbers of qubits required for proposed applications [4–6]. Increasing the functional size of quantum computers is however not as simple as increasing the qubit count. It is also necessary to improve the qubit quality and interconnectedness. A system with a million qubits has limited use if the error rate is so high that information cannot be transferred throughout the system without being lost. Both aspects must be addressed to build scalable systems, as shown in Figure 1.11.

Further to this, technologies that can quickly scale to 100 or 1,000 qubits and slow down thereafter will take significantly longer to reach full-scale and complete useful computations. A viable technology must have a pathway to millions of qubits and silicon quantum dots have excellent potential to meet this goal. Various proposals have been made for scalable quantum processor architectures [77–81] which raise important technological considerations and opportunities in future development.

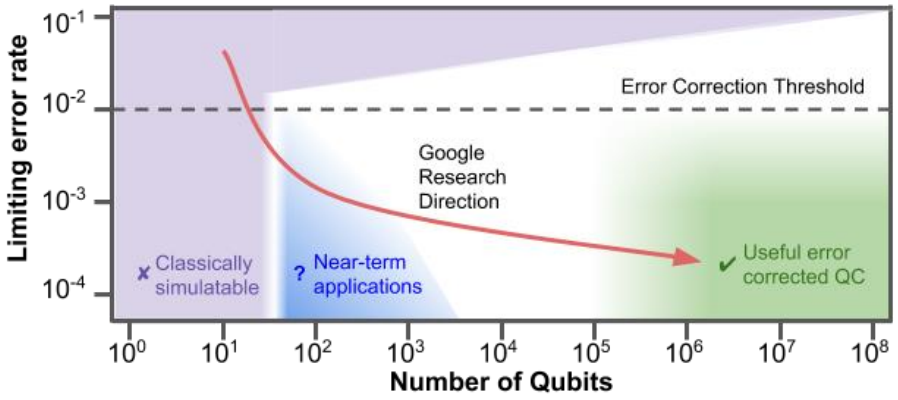


Figure 1.11: Qubit scaling. Figure courtesy of Google Quantum AI, showing the relationship between qubit count and qubit error rate. Useful applications are likely to require millions of qubits with low error rates.

1.3.1 Scalable Manufacturing Processes

An important step towards any scalable system is to have a scalable manufacturing process. Devices in the current state of the art have been (for the most part) manufactured in small-scale research fabrication facilities [22–24, 38, 41, 82, 83]. Whilst the material stacks used in these devices are similar to those used in full-scale commercial foundry processes, the lithography and process control differ significantly.

The devices referenced above all use electron beam lithography (EBL) to etch nano-scale structures in devices, which enables arbitrary structures with critical dimensions down to a scale of 10 nm, and fast design iteration as it does not require a mask as for photo-lithography. To achieve high-yield and throughput, it is necessary to adjust critical dimensions and use photo-lithography for all steps of the fabrication process.

A number of commercial foundries are now involved in the fabrication of quantum dot devices for quantum computing, with notable progress using devices fabricated at Intel [30], CEA [28, 84–87], IBM [29], Hitachi [88], Global Foundries [89], and IMEC [42], among others.

The design and operation of devices manufactured in full-scale foundry processes is a very active area of research with many challenges to be addressed. In particular, techniques

to scale devices in two dimensions are of interest. In Chapter 3 we investigate a device design and operation modes that address this challenge.

1.3.2 Controlling Many Qubits

Quantum processors differ from classical processors in that qubits each need external control signals to implement quantum logic gates, whereas classical bits act as the control signals themselves, and logic gates are implemented as hardware circuits. This has profound implications for the development of full-scale systems.

Firstly, the quality of control signals and the qubit noise environment can directly affect the qubit operation fidelity [40, 90, 91]. For silicon qubits, the wide bandwidth of control signals creates challenges in signal generation and conditioning. In Chapter 2 a signal addition circuit is investigated that allows for simple and low-noise generation of signals with a continuous bandwidth from DC up to 1 GHz.

Secondly, the scaling of interconnect will become increasingly challenging as qubit counts increase. Already, with qubit counts reaching 50 and above, quantum computers fill rooms with the requisite electronics and cabling (see Figure 2.1). It is necessary to develop architectures for the control circuitry that minimise the scaling of the number of control lines required per qubit [92]. It is only practical to have up to roughly one thousand connections to a chip, due to the mechanical and thermal load associated with the wiring needed.

One solution to the wiring problem is to apply some signals to many qubits simultaneously. Crossbar architectures propose that $2 \times N$ control lines may be used to control N^2 qubits if the qubits are arranged in a rectangular grid [79, 93]. These proposals require a very tight tolerance on the variability within the array, which is yet to be demonstrated.

A scheme is being explored for the microwave drive signal, where qubits may be driven continuously within a persistent microwave field [94–97]. Progress has also been made on ways to deliver a single microwave field across an entire chip [98, 99].

These global control strategies make use of the Stark shift to tune the spin Larmor frequency, and in-turn implement quantum logic gates within the driving field. In Chapter 4 a technique will be investigated that enables the qubit resonance to be switched on and off, as well as being driven electrically, which could enable new architectures and control schemes for quantum processors.

1.3.3 Integrated Control Electronics

Another solution to the wiring problem is to implement multiplexing strategies that can allow signals to be shared across many qubits by switching between them in time [100–103].

Alongside multiplexers/demultiplexers, signal generation and digitisation can also be implemented at cryogenic temperatures the wiring bottleneck to room-temperature electronics. It is too early to tell how much signal generation may be implemented on-chip with the qubits, however this is an active field of research with different proposals varying in their approach [78, 80, 89, 104–106].

The primary limiting factor for the integration of control electronics on-chip is the thermal load. Cryostats capable of reaching milliKelvin temperatures typically have a cooling power of of tens of microWatts at base temperature, which would heavily restrict the types of electronic circuits that could be integrated on-chip. Higher temperature stages have much higher cooling power, with tens of milliWatts available at 1 Kelvin, and Watts available at 4 Kelvin. This motivates increasing the temperature of the qubits to allow for more electronics to be integrated on-chip.

1.3.4 High Temperature Operation

Recent studies in silicon MOS systems have shown that electron quantum dot qubits can be operated at a temperature above 1 Kelvin [82, 83]. A study on hole quantum dots in a FinFET even showed qubit operation above 4 Kelvin [29]. In each study, a modest increase in qubit errors is found at increased temperatures. For future architectures this

may need to be traded off against the need to integrate more heat-generating electronics on-chip.

1.3.5 Long-range Quantum Links

An important component of more complicated architectures is the need to transfer quantum information over large distances [78]. The need comes from both the need to integrate control electronics within a qubit array, and also the potential to increase connectivity between qubits within a large array [81].

It is possible to transfer a qubit state within an array using only two-qubit gates between nearest neighbour qubits. However, this may prove to be inefficient over long distances.

One strategy is to physically transport the electron spin across the processor [80,107,108]. The ability to coherently transfer an electron spin between two quantum dots has also been demonstrated in silicon [109] and GaAs [110,111]. A key advantage of this strategy is that it can be implemented using the same quantum dot and gate structure that is required for qubits. Spin transport can also be achieved using surface acoustic waves in piezoelectric material stacks [112–114].

Another strategy is to transfer the spin state via a form of interstitial coupler. Proposals have been made for capacitive coupling [59], but much research has been focused on microwave cavities which couple the spin to a photon [60,61]. This technique could allow for spin information to be transported across millimeter or even centimeter distances quickly and coherently. However, they require large microwave structures to be fabricated on-chip, using superconducting materials.

1.4 Thesis Outline

Chapter 2 introduces the control electronics required for quantum dot qubits in silicon. It then investigates signal combination techniques for addressing the wide bandwidth re-

quired by silicon qubits, before identifying a circuit design that extends control bandwidth to a continuous band from DC to near 1 GHz. The circuit is modified for low power dissipation to be compatible with cryogenic operation, and integrated within a cryostat at the 4 Kelvin stage.

Chapter 3 investigates operation of devices manufactured in a full-scale 300 mm wafer process. Fully-depleted silicon-on-insulator (FD-SOI) devices with one and two silicon nanowires are tested, showing formation of quantum dots. A SET charge sensor is implemented in one nanowire and used to sense quantum dots in an adjacent nanowire remotely. The SET is then used to sense a 2×2 quantum dot array in a remote nanowire. Simulations of inter-dot tunnel couplings show that modest reductions in device critical dimensions are required to achieve tunnel couplings high enough for PSB readout and two-qubit gates.

Chapter 4 introduces the possibility of controlling silicon MOS quantum dot qubits purely electrically, without the need for an antenna or micro-magnet to be fabricated on-chip. Using a degeneracy between ground and excited states of the quantum dot, the spin-orbit effect can be dramatically increased, making the qubit susceptible to electrical control signals. Using electrical drive, Rabi oscillations are observed up to $f_{\mathrm{Rabi}} = 81$ MHz, and single qubit fidelities as high as 99.93 %. The electrical susceptibility can be switched on and off on-demand, with an on-off ratio up to 650, and a switching fidelity of at least 99.35 %. This capability to control the spin electrically without a micro-magnet could enable entirely new quantum processor architectures.

Chapter 5 provides an overview of important results within this thesis. It discusses the potential implications of the work presented, and opportunities for future research and development.

Chapter 2

Instrumentation for High-Fidelity Control of Quantum Dots

The task of engineering many delicate quantum states to act as stable qubits is challenging and requires complicated electrical control signals. For spin qubits in semiconductors, these arbitrary waveforms must span from near-DC up to hundreds of MHz, with low noise and high-resolution. Standard components fail to meet these requirements, with quantum engineers often left with a choice between having high-bandwidth, OR keeping their control lines DC-coupled. We develop a linear-alternative to the bias-tee that utilises both high-impedance and impedance-matched passive circuits to achieve a bandwidth from DC to 760 MHz. The design incorporates DC-line filtering, and has a power dissipation of less than 2 mW, allowing it to be installed within the cryostat.

The work presented in this chapter is included in a manuscript in preparation:

W. Gilbert, C.H. Yang, T. Tanttu, B. Hensen, A. Laucht, and A. S. Dzurak. "A Linear Alternative to Bias-tees for Spin Qubit Control"

The author acknowledges the contributions to this chapter by A. Dickie who assisted with cryogenic integration and testing of the combiners, C.H. Yang who took part in the early cryogenic circuit design, and B. Hensen who assisted with testing of initial prototypes. The author designed, manufactured, and characterised the combiners.

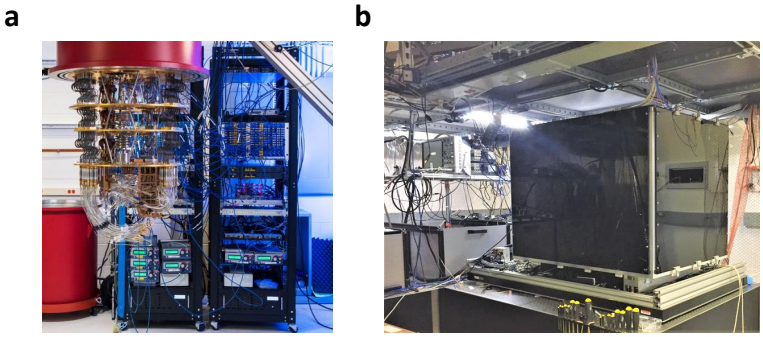


Figure 2.1: Images of state-of-the-art quantum processors. **a**, A 54-qubit quantum processor based on superconducting Josephson junctions at Google AI Quantum. **b**, A 9-qubit quantum processor based on the spins of trapped ions at IonQ.

The challenges of building a quantum computer are well known within the community of companies and research institutes that dedicate their time to it. In fact, Richard Feynman alluded to this at the end of his now famous talk arguing for the simulation of physics with a new type of computer based on quantum mechanics [115] -

> *... if you want to make a simulation of nature, you'd better make it quantum mechanical, and by golly it's a wonderful problem, because it doesn't look so easy.*

Quantum states are inherently fragile. The process of engineering many quantum states to be highly stable and controllable goes against what are arguably the natural tendencies of quantum states of particles, to give in to entropy. To create qubits is then inherently unnatural and challenging, as the physical processes untended cause the engineered quantum states to decay or decohere.

Despite this, at time of writing significant progress has been made in engineering systems with tens to hundreds of qubits working in sync. Looking at two state-of-the-art systems in Figure 2.1 one couldn't fail to notice the complexity of the surrounding control hardware. The reason for this is two-fold. Firstly, extreme environmental conditions are required, such as a high-vacuum and deep cryogenic temperatures, meaning that access to a qubit chip is restricted to compact and low-power solutions. Secondly, qubits are analogue

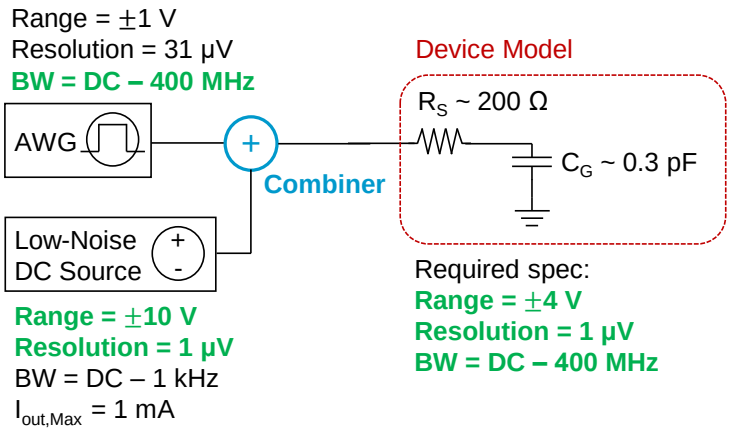


Figure 2.2: High-level schematic. High-level schematic of control setup for quantum dot qubits. The control requirements for quantum dot qubits necessitate the use of multiple instruments, and a method for combining the signals that can pass key specifications.

devices requiring analogue control signals which for semiconductor spin qubits must cover bandwidths from DC up to tens of GHz.

A key challenge in system design is to deliver analogue signals across such a wide bandwidth from room temperature electronics to a chip within a cryostat, without distorting the signals or adding noise.

2.1 Electronics

Spin qubits in semiconductors are inherently analogue devices, requiring a low-noise environment, but also broadband arbitrary waveforms to dynamically control qubit coupling and charge occupation for qubit state initialisation and readout. They are also typically operated at deep cryogenic temperatures below 1 Kelvin.

2.1.1 Electron Control Requirements

A high level schematic is shown in Figure 2.2, including an electrical model of a control gate electrode in a device similar to those in Refs [38, 40, 57]. In the case of quantum

Qubit/Material	Spin relaxation time, T_1	Spin coherence time, T_2^{Hahn}	Two-Qubit coupling, J/h	Ref
SiMOS, Si/SiGe e^- spins	0.001-10 s	0.01-1 ms	1-100 MHz	[22–24, 40]
SiMOS h^+ quantum dots	0.1-10 ms	0.1-10 μs	N/A	[28, 29]
Ge/SiGe h^+ quantum dots	0.1-10 ms	0.1-10 μs	10-1000 MHz	[25, 53]
Si:P, e^- spins	0.001-10 s	0.1-1 ms	1-100 MHz	[37, 39]
Si:P, nuclear spins	>1 min	1-1000 ms	1-1000 MHz	[37, 116]
Si/SiGe exchange-only	0.1-100 ms	1-100 μs	10-1000 MHz	[41]

Table 2.1: Timescales relevant to common spin qubit technologies

dots in a silicon metal-oxide-semiconductor (MOS) structure, a DC bias of 1-2 Volts is applied to accumulate the desired number of electrons (or holes) in the silicon channel. This DC bias should have as low noise and drift as possible, and should have a micro-volt resolution after attenuation. A range of up to ± 4 V can be required for certain device material stacks.

The DC bias is combined with arbitrary pulses with a typical amplitude of 10 - 100 mV, and requiring a resolution of 100 μV of better. The bandwidth requirement of these pulses varies significantly depending on the material stack hosting the qubits. Relevant frequencies for different material stacks are listed in Table 2.1.1. The upper bandwidth requirement is usually set by the duration of pulses used to switch on exchange coupling between qubits and can be up to 1 GHz [39, 41]. The lower bandwidth requirement is set by the spin relaxation time, T_1, and can extend to 10 seconds, or 0.1 Hz for electron spins in silicon [62]. Dopant atoms in silicon can exhibit a T_1 of hours or days, however it is measured indirectly via an electron spin [36] so doesn't impose a requirement on the electronics.

The T_1 timescale is necessary to reach in some cases during initial calibration of systems, but is not required as part of routine operation of a quantum computer. It is however critical to be able to maintain constant voltage levels for at least the full duration of a

single-shot, which will commonly be some multiple of the coherence time, plus initialisation and readout times. For MOS quantum dots this will be between 0.01 - 10 ms on average.

A requirement for a bandwidth from sub-1 Hz up to GHz on a single line does come up for some devices (such as oscilloscopes), however qubit control adds extra constraints that prevent the use of standard circuits without modification.

- **DC bias/offset** - High bandwidth signals must have a DC offset of up to ±4 V.
- **Resolution** - The resulting signal should have a voltage resolution below 10 μV, ideally 1μV.
- **Power dissipation** - Low cooling power at milliKelvin temperatures means that a 50 Ω termination cannot be used on the device end due to the heat load. Instead, solutions must deliver signals to an open-circuit load and manage the resulting reflections. A 50 Ω load also often causes problems for low-noise DC sources which have limited output current capabilities (<10 mA).

To meet all of these requirements in tandem, one would need an instrument with a 20- to 24-bit resolution, and 1 GHz of bandwidth. In a practical sense, the easiest (and perhaps only) way to do this is with a combination of instruments - A high-resolution DC voltage source combined with a fast AWG. Methods for combining the outputs of these two instruments is investigated next.

2.1.2 Adder Circuits

In Figure 2.3a-c, three design approaches for adder circuits are shown that can be used for combining a DC bias with fast waveforms from an AWG. The circuits in **a,b** are standard and widely used, being a resistive combiner and a bias-tee, respectively. An impedance matched variant of the resistive combiner is also common for RF and microwave applications, but low-noise DC noises typically cannot drive 50 Ω loads, so this design is not suitable for quantum dot control which required a low-noise DC bias.

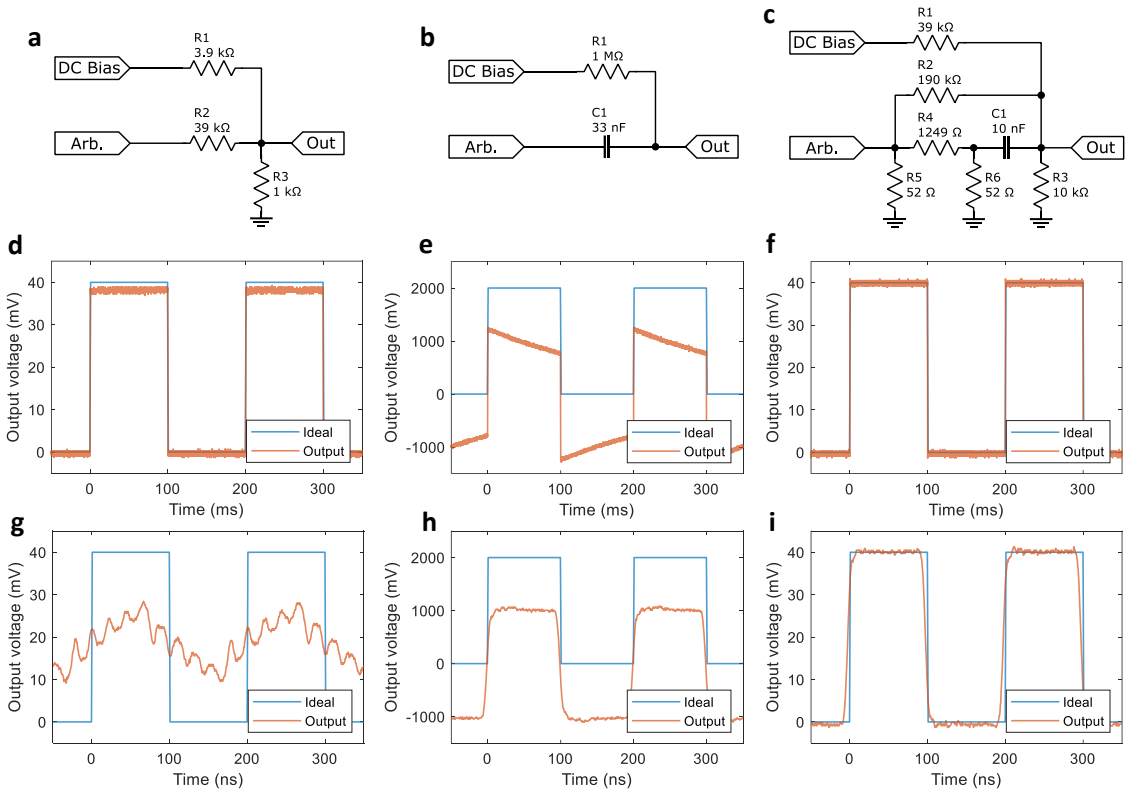


Figure 2.3: Comparison of basic design approaches. **a**, High impedance combination achieves low DC current draw and AWG linearity down to DC, but has limited bandwidth. **b**, Bias-Tees achieve both low DC current draw and high AWG bandwidth, but sacrifice DC coupling of the AWG. **c**, Including both high impedance and 50 Ohm paths for the AWG signal in parallel achieves low DC current draw, and high AWG bandwidth. Additionally, if the division ratio of both paths are matched, then the AWG signal also remains linear down to DC. **d-f**, Output waveforms for test circuits in **a-c**, respectively for a 5 Hz square wave input (100 ms pulse lengths). **g-i**, Output waveforms for test circuits in **a-c**, respectively for a 5 MHz square wave input (100 ns pulse lengths). Rise/fall times may be limited by the signal generator used for testing, which specifies a <9 ns rise/fall time.

The resistive combiner allows for simple addition of voltages without an AC-coupling capacitor, providing linear combination down to DC as seen in Figure 2.3d. However, due to the high impedances required the output is poorly matched to 50 Ω lines so has very limited bandwidth and causes significant reflections and pulse distortion. Early demonstrations of two-qubit gates in silicon used similar circuits [57], however to achieve high-fidelity gate operations more bandwidth is required.

The bias-tee is much more widely used [25, 26, 28]. The author notes a view that bias-tees are used for gate-control of quantum dots in almost all publications in the field, despite their common omission from methods sections and schematics in papers. This design trades off DC-coupling in favour of maintaining an impedance matched line for the AWG signals, allowing for high-bandwidth as seen in Figure 2.3h. As such, long pulses will gradually decay as in Figure 2.3e.

The pulse decay effect can be mitigated with drift compensation strategies where the AWG voltage is gradually increased in order to maintain a steady voltage at the device. This technique has limits in that the AWG voltage cannot be increased indefinitely, and that it requires careful calibration of the filter time-constant.

In a practical sense, dealing with drifting voltages from a low-frequency cut-off adds complication to what are already deep physical systems and where a primary development focus of current research is to improve the accuracy and stability of qubit operations. In order to maintain flexibility and simplicity in pulse waveform generation, the ideal solution is for the pulsing line to be DC-coupled.

Figure 2.3c shows an adder design that achieves both DC-coupling of the AWG line and high-bandwidth, as demonstrated in Figures 2.3f and i, respectively.

2.1.3 Linearised Bias-Tees (Combiners)

The operation principle of the adder circuit in Figure 2.3c (now referred to as a combiner) is that it splits the AWG input into two paths with different impedances but matched

attenuation, such that the line can be driven quickly with a matched impedance, but then held high by a high-impedance path. A 5:1 division ratio is design for the DC bias port, and a 25:1 division ratio for the AWG port.

A first high-impedance path is formed by resistors R1, R2, and R3 and forms a resistive combiner similar to that in Figure 2.3a, with a division ratio of 25:1. A second path consists of an pi-attenuator with a 50 Ω impedance and a 50:1 division ratio (R4, R5, R6), which is then AC-coupled to the output. The attenuation of the 50 Ω path is double that of the high-impedance path due to the voltage doubling effect of signal reflections on an open-circuit load. Fast pulses that are sent through this combiner design will fully reflect off of the gate-electrodes of the test device (Figure 2.2), then propagate back to the combiner output where they will be absorbed by the 50 Ω path in the combiner, resulting in minimal pulse distortion. The pulse level is then held at the doubled value by the high-impedance path, resulting in an effective DC-coupling, as seen in Figure 2.3f.

The attenuation of both paths needs to be well matched in order to achieve acceptable levels of pulse distortion. This is easily achieved with off-the-shelf precision resistors, and is an advantage of constructing the full combiner on a single circuit board. A parallel study utilises the same design principle of splitting the AWG line into two paths, however distributes components between room-temperature and cryogenic stages, making it difficult to achieve good matching [21]. The advantage of such an approach is the ability to apply different filtering to the DC and AWG lines at cryogenic temperatures for reduced noise.

2.1.4 Power Dissipation & Noise

Quantum dot qubits are operated at deep cryogenic temperatures in order to reduce thermal broadening of energy spectra of the quantum dot. Recent demonstrations of qubits in silicon at temperatures above 1 Kelvin are encouraging [29, 82, 83], and may lead to relaxed requirements on temperature. However, currently semiconductor qubits are typically cooled as much as possible in order to realise the highest possible performance.

In order to achieve low effective temperatures for qubits (measured as the effective electron/hole temperature [82]) one must also reduce the effective noise temperature of control signals. A noisy control signal delivered from room temperature to a qubit chip at 20 mK without appropriate filtering will increase the effective electron temperature as noise effectively broadens level transitions of the quantum dots. A common technique for reducing noise is to include both filtering and attenuation on control lines as they are routed down through the thermal stages of the cryostat.

Electrical noise that is transmitted through control lines comes in two primary sources.

- **Instrumental noise** - Generated from instruments such as amplifiers, DACs (Digital-to-Analogue Converter), power supplies, radiated noise, etc.
- **Thermal (Johnson-Nyquist) noise** - Present in all components at a low level that is dependent on circuit impedance, temperature and bandwidth -

$$v_n = \sqrt{4\kappa_B T R \Delta f} \tag{2.1}$$

  where κ_B is Boltzmann's constant, T is temperature, R is the effective resistance of the noise generating component, and Δf is the bandwidth.

We can reduce Δf by filtering lines to only pass the frequencies required, and R by avoiding components with a high output impedance. When bandwidths are high however, it becomes important to also reduce the physical temperature of signal conditioning components to reduce the T component.

Due to the limited cooling power available at cryogenic temperatures, not all components can be placed at the coldest temperature stages. For example, a modern dilution refrigerator will have approximately 1 Watt of cooling power at a 4 K stage, 10 mW at a 1 K stage, and 10-1000 μW at a mK stage, depending on specification and operation point. Dissipative circuits then can rarely be placed on a mK stage, but may be considered for 1 K or 4 K stages. In addition to this, solutions that need to be applied to multiple control lines need to have proportionally lower power dissipation. That is, for 100 lines and 1

Watt of available cooling power, a per-line solution should have less that 1 W / 100 = 10 mW of power dissipation.

In order to benchmark the power dissipation, we assume a maximum pulse amplitude of $200\text{mV}_{\text{p-p}}$, and both static and dynamic inputs (which will be investigated in more detail in Section 2.1.5). Under these conditions the circuit presented in Figure 2.3c dissipates up to 125 mW due to a 50 Ω input impedance and a high division ratio of 25:1, and as such can only be used at room temperature, at least for any significant number of lines. Since the input impedance is 50 Ω across the full bandwidth from DC, there is no difference in dissipation between static and dynamic inputs. We now investigate low-power variations to this base circuit.

2.1.5 Cryogenic Combiners

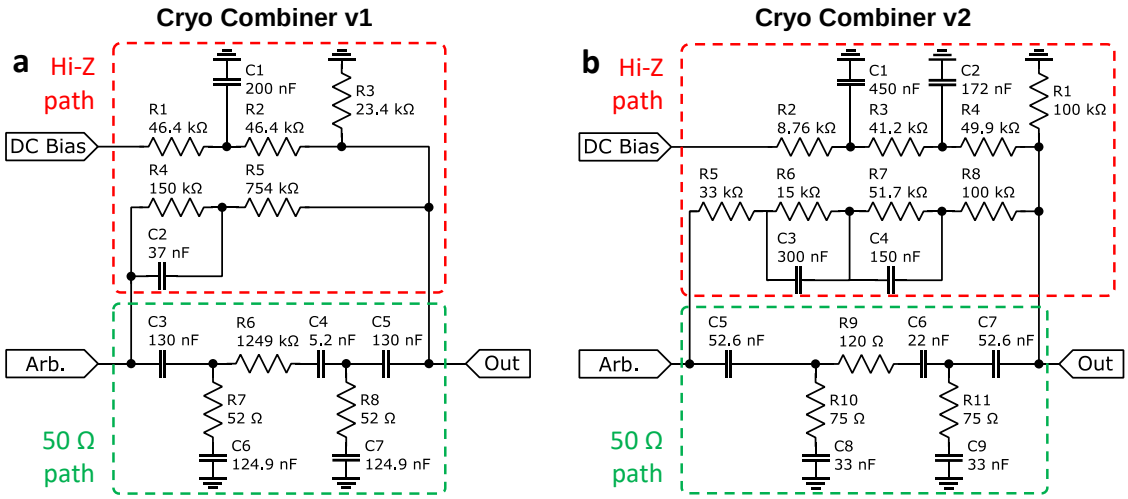
To reduce the power dissipated within the combiner, we make two modifications to the base circuit which are elucidated in two hardware versions shown in Figure 2.4 -

- **Version 1** - Converted the 50 Ω path into an AC-coupled attenuator with zero static power dissipation.
- **Version 2** - Reduced the division-ratios from 5:1 (DC) and 25:1 (AWG) down to 2.5:1 for both ports in order to reduce required input voltages to produce the same output voltage.

A low-pass filter is also added to the DC port path, which is discussed in Section 2.1.6.

The circuits in Figure 2.4 are divided into two paths, a 50 Ω path and a Hi-Z path. Looking firstly at the 50 Ω path we convert from the standard pi-attenuator in Figure 2.3c to a modified AC-coupled version, with capacitors C4, C6, and C7 inserted in series with the resistors of the pi-attenuator. The values of C4, C6, and C7 are chosen to have an impedance ratio equal to that of the resistor network. That is,

$$\frac{||Z_{\text{C4}}||}{||Z_{\text{C6,C7}}||} = \frac{||Z_{\text{R6}}||}{||Z_{\text{R7,R8}}||} \tag{2.2}$$



c **Power dissipation for 200 mV_{p-p} output**

	P_{static}	$P_{dynamic}$
Room Temp Combiner	125 mW	125 mW
Cryo Combiner v1	32.5 uW	125 mW
Cryo Combiner v2	1.5 uW	1.25 mW

Figure 2.4: Cryogenic combiner designs a, Version 1 cryogenic combiner circuit schematic, with a single-pole low-pass filter on the DC port, a 5:1 division ratio on the DC port, and a 25:1 division ratio on the AWG port. **b**, Version 2 cryogenic combiner circuit schematic, with a two-pole low-pass filter on the DC port, and a 2.5:1 division ratio on both ports. **c**, Table of calculated power dissipation for each combiner variant. Power is calculated for a $200mV_{p-p}$ square wave output waveform, and for both the static (DC) and dynamic (fast pulsing) case.

which results in a constant division ratio across all frequencies, equal to that in the original resistive attenuator.

This capacitive attenuator network is sensitive to capacitive loading on the combiner output, which can cause an unbalanced charge/discharge time across attenuator resulting in distortions. To combat this, the value of the smallest capacitor within the circuit is chosen to be an order of magnitude larger than the expected capacitive load at the output. Here we assume capacitive loading equal to 3 metres of coaxial cable, or approximately 300 pF at 100 pF/m, and select 5.2 nF as the smallest capacitor for easy calculation. The values of C3 and C5 are selected to match the capacitance looking into the pi-attenuator. This creates a broadband impedance matching for the capacitive attenuator. The capacitive attenuator has an associated charge/discharge time, which for both versions of the cryogenic combiner is $\approx$ 10 μs.

For the version 2 combiner, the division ratio was significantly decreased for two reasons. Firstly, to reduce the power dissipation within the combiner itself, allowing most of the heat to be taken by upstream components so that the combiner can be placed within the cryostat. Secondly, to give some flexibility in the choice of division ratios as in some cases the maximum amplitude is needed for rough characterisation, whilst in other cases extra attenuation is desired to reduce noise.

2.1.6 Integrated Low-Pass Filter

A low-pass filter (LPF) for the DC bias is integrated into the Hi-Z path to take the place of standard DC line filtering. The high series resistance of typical DC filters has a unpredictable effect on the performance of the combiners since the port impedance must be included in the calculation of the division ratio and resistor values. As such it is much simpler to include the LPF within the combiner circuit for consistency. A single-pole LPF is used in version 1 (components R1, C1), and a double-pole LPF in version 2 (components R2, C1, R3, C2).

The low-pass filter in the DC path adds a capacitive loading to the AWG path. To prevent pulse distortion caused by this loading, a compensating high-pass filter (HPF) is added to the AWG branch of the Hi-Z section (components R4, C2 in version 1, components R6, C3, R7, C4 in version 2). The component values for the HPF are chosen so that, a) the time-constant of both filters are the same, and b) so that the division ratio of the AWG path is the same for both high- and low-frequency signals, cancelling the loading effect of the LPF. The addition of this filter adds some complexity to the design, and necessitates careful tuning of component values.

2.1.7 Distortion & Variability

Distortion is an important and challenging design specification for this combiner with multiple filter time constants and circuit components to match. In particular, the double-pole matched HPF/LPF in the version 2 combiner required careful tuning. A goal of sub-0.5% distortion was set for the design phase in simulation, which required 2-3 days of iteration and tuning. To achieve close to this specification in production, tight tolerances were chosen for the components, with 0.1% tolerance on the resistors, and 1% tolerance on the capacitors (the best that are available off-the-shelf in the required form factor). In production test, waveform distortion was characterised as a proportional overshoot or undershoot, and measured for square wave inputs at decade frequency increments from 5 Hz to 5 MHz. Maximum over/undershoot was found to be sub-2.5% for the version 1 combiner and sub-2% for the version 2 combiner. In most cases, impedance mismatches and reflections will cause distortions much more significant that 2 %. If however additional reductions in maximum distortion are required, they can be achieved with - component screening to reduce component variation, pulse pre-distortion filtering of the AWG waveforms, or reducing the combiner circuit complexity.

An image of a version 2 combiner is shown in Figure 2.5, with SMA connectors and a compact brass enclosure.

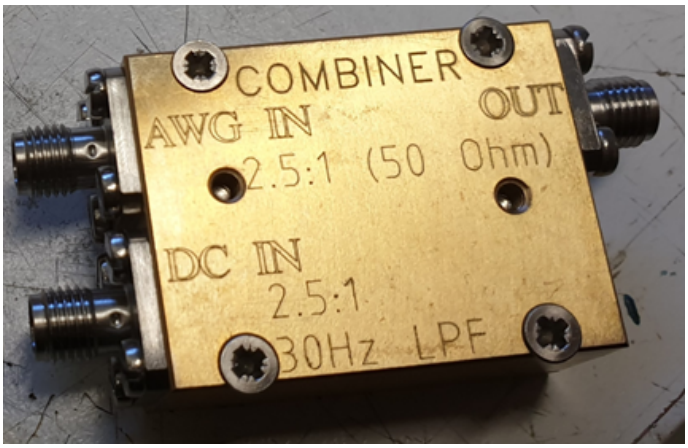


Figure 2.5: Connectorised version 2 cryo-combiner

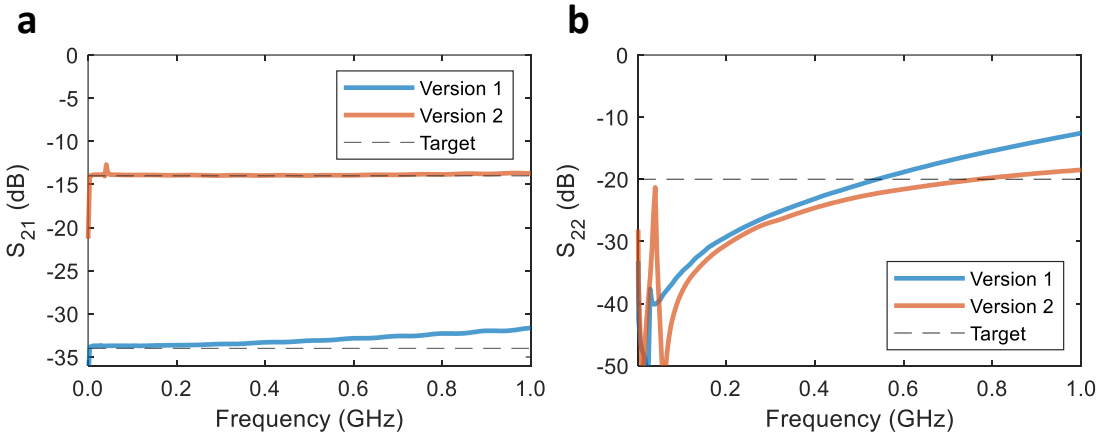


Figure 2.6: Bandwidth measurements a, Insertion loss S21 for the pulsing line of the version 1 cryo-combiner. Target attenuation is 34 dB or a factor of 50:1 when measured with a 50Ω load, double the attenuation that will be seen by a high-impedance load. **b**, Return loss S22 for the output port of the combiner. The target of -20 dB represents a reflected signal amplitude of 10 %.

2.1.8 RF Performance

The RF performance of the combiners was measured with a Keysight N9918B portable network analyser, and is shown in Figure 2.6. The transmission coefficient, S21, for devices with high attenuation will typically rise rather than fall when the bandwidth of the device is exceeded, as signals begin to couple directly from input to output, bypassing dissipative elements. The version 2 combiner is significantly less susceptible to this affect as it has a lower attenuation factor than version 1.

A more important specification for these devices is the return loss, S22, as it determines how well the combiner can absorb signals reflected from control gate electrodes which themselves have a return loss close to 0 dB. The choice of a specification for return loss is arbitrary and depends on what level of distortion one can tolerate at the device. Here we choose a specification of -20 dB, which equates to a reflection amplitude of 10 %. The version 1 combiner achieves a bandwidth of 560 MHz under this specification, with the version 2 combiner improving slightly to 760 MHz. Version 2 exhibits a minor damped resonance at 40 MHz due to the parasitic inductance of a PCB trace.

The bandwidth of these combiners is sufficient to enable sub-10 ns pulses, enough for a majority of semiconductor qubits, whilst still maintaining an effective DC-coupling of the AWG.

2.1.9 Line Losses & Practical Considerations

These combiners are designed for a specific purpose and may produce erroneous results in other settings. The assumptions for the use of these combiners are -

- **Open circuit load** - The combiner is design to connect directly to a control gate electrode with very low leakage current. Any current path to ground at the output will alter the division ratio as it behaves like a resistor in parallel with the shunt resistor of the Hi-Z path. When measuring the output of these circuits using an oscilloscope with 1 $M\Omega$ input impedance, a small decay in output voltage will be seen over a 10 ms timescale. This was calibrated against simulations to build a model for the expected response on an ideal Hi-Z load.

- **Low DC source impedance** - 3-port resistive combiners such as these are sensitive to input impedances, as the impedance of the other two ports must be included in the calculation of the voltage division. To the preserve the division ratio of the Hi-Z path, impedances up to approximately 500 Ω can be tolerated without causing distortion. The DC low-pass filters that are commonly used for quantum dot control

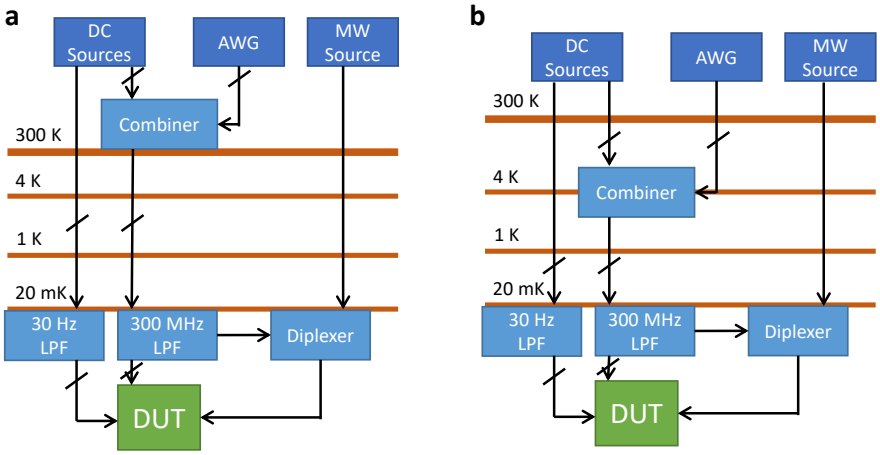


Figure 2.7: Fridge setup a, Simplified schematic of electrical setup using combiners at room temperature. **b**, Simplified schematic for a setup with combiners integrated at the 4 K stage of the cryostat.

typically have a high series impedance, precluding their use, which is the reason for the inclusion of a low-pass filter as part of the cryogenic designs.

- **Impedance matching at AWG input** - A significant impedance mismatch at the AWG input can cause distortions, especially if one cause of the impedance mismatch is a series resistance.

- **50 Ohm input source** - Both cryogenic combiner versions will have a 50 Ω input impedance for fast waveforms, and a Hi-Z input for slow waveforms. For a step pulse input as in Figure 2.3f the input impedance will gradually transition from matched to Hi-Z, which causes a 50 Ω source to gradually output more voltage, increasing to double the nominal value. This behaviour is expected, and will result in the specified division ratio being held for the nominal source voltage. Non-standard 50 Ω sources that do not expect a 50 Ω load (such as with a Hi-Z setting) may generate half the desired voltage.

2.1.10 System integration

The combiner can be integrated into experimental setups either at room temperature, or within the cryostat at the 4 K or 1 K stages, as shown in Figure 2.7. Assuming a thermal

load of 1.25 mW for the version 2 combiner, up to 20 combiners may be integrated at the 1 K stage of a Bluefors XLD-400 cryostat, and up to 800 at the 4 K stage, space allowing.

2.2 Conclusion

The combiner investigated in this chapter enables passive and linear combination of a DC bias with arbitrary waveforms from an AWG, with a continuous bandwidth from DC to over 500 MHz. These combiners are then optimised for low-power and integrated into the cryostat at the 4 K stage to reduce electrical noise. The combiner has now become a standard across the research groups of Prof. Andrew Dzurak, and Prof. Andrea Morello, and a key part of the experimental setup for many influential publications [38, 97, 98, 109, 117, 118], as well as the work of the chapters to follow. Modifications to the design for cryogenic operation have enabled it to be integrated within the cryostat at the 4 K stage for reduced noise, which is a key part of the electrical setup for experiments that are now pushing the limits of silicon MOS qubit fidelities (results unpublished).

Chapter 3

Quantum Dots in CMOS

The advanced nanoscale integration available in CMOS technology motivates its use for spin-based quantum computing applications. Building on a solid foundation of qubit demonstrations in silicon quantum dot devices manufactured in university/prototyping fabrication facilities, this chapter investigates the suitability of an industrial FDSOI CMOS process as a platform to transition to scalable manufacture. A charge sensor is demonstrated in double nanowire devices to be able to sense quantum dots in an adjacent nanowire. Devices augmented with split gates and floating couplers between the nanowires are shown to have increased sensor sensitivity between nanowires, and by applying a relative bias to the nanowires, a 2×2 quantum dot array can be formed in one nanowire and sensed, down to the last electron, by a charge sensor situated in the adjacent nanowire. Interdot tunnel rates are found to be weak in the few electron regime, however valley structure and tunnel rate simulations show that only a modest dimension shrink is required to achieve a workable range.

The work presented in this chapter has been published in:

W. Gilbert, A. Saraiva, W. H. Lim, C. H. Yang, A. Laucht, B. Bertrand, N. Rambal, L. Hutin, C. C. Escott, M. Vinet, and A. S. Dzurak. "Single-electron operation of a silicon-CMOS 2x2 quantum dot array with integrated charge sensing." *Nano Letters* vol. 20 , no. 11, p. 7882–7888, (2020).

The author acknowledges the contributions to this chapter by C. C. Escott who performed electrostatic simulations, and A. Saraiva who performed tunnel rate calculations. The author performed all measurements and analysed the data.

The importance of scalability in computing is hard to overstate. Despite the potential for quantum computing to reduce complexity scaling for some problems, it is not exempt from the reality that practical systems must scale to the millions of qubits or more to have real impact [4–6]. Semiconductor spin qubits hold great potential as a scalable technology platform for quantum computers, firstly due to their small size, typically ranging from 30-100 nm, which would allow many to be fabricated on a single chip. Another advantage is their process compatibility with classical microelectronics, allowing peripheral analogue and digital electronics to be integrated on the same chip, alongside the qubits [78].

At the time of commencement of this study, demonstrations had already been made of high-fidelity single- and two-qubit gates from multiple sources [27, 40, 51, 52, 119]. All of these demonstrations were made in devices manufactured in small-scale fabrication facilities, using manufacturing processes primarily suited to fast turn-arounds and easy adaptability, rather than mass scale and high yield [120]. Few demonstrations had yet been made in which devices were manufactured using full-scale 300 mm wafer process lines [28, 86, 121]. The transition to scalable fabrication processes necessitates changes in device designs and geometries to achieve the expected higher yields, and as such significant work remains to be done to reach parity with the state-of-the-art. This study aims to demonstrate important functionality that is required for operation of small-scale quantum processors using devices manufactured in a 300 mm wafer CMOS process line at CEA-Leti. It occurred alongside other important studies using devices manufactured at CEA-Leti [84,85,122], Intel [30], IMEC [123], Global Foundries [89], Hitachi [88], and IBM [29].

3.1 FD-SOI Quantum Dot Devices

Quantum dot devices based on a traditional MOS process are constructed with metal gate electrodes patterned on top of an insulating layer (such as SiO_2) above a bulk semiconductor substrate [120]. This is based off the traditional planar-MOS transistor design. Recently, Silicon-on-Insulator (SOI), Tri-gate/FinFET, and GAAFET processes have become more popular in state-of-the-art CMOS to achieve high ON/OFF ratios as gate

lengths are aggressively shortened and transistors densities increased [124]. These processes may impose extra complications for the design of 2D quantum dot arrays, however they allow for the adoption of standard CMOS processes with minimal adaptations. There are also some key advantages.

A Fully-Depleted Silicon-on-Insulator (FD-SOI) process allows for quantum dots to be confined on two sides by the edges of a nanowire as shown in Figure 3.1b, rather than requiring dedicated screening gates such as for devices with a bulk active region as in Figure 3.1a. Two added benefits of the FD-SOI process are the ability to apply a voltage bias to the so-called 'back-gate' to tune the threshold voltage, V_{th}, and the ability to apply a bias to the nanowire itself, which will be investigated in section 3.1.

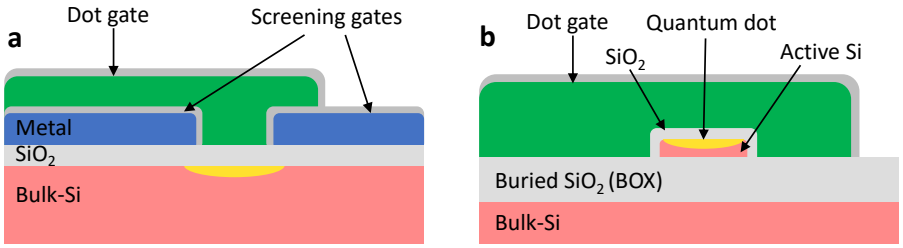


Figure 3.1: Bulk-MOS vs FD-SOI designs a, Schematic cross-section of a typical bulk-MOS based quantum dot device. **b**, Schematic cross-section of an FD-SOI-based quantum dot device.

3.1.1 Dot Formation In Nanowires

In earlier studies of fully-depleted silicon-on-insulator (FD-SOI) devices they have been shown to be a viable platform for hosting quantum dots [28,125,126]. One such study [127] of a device fabricated using FD-SOI technology at CEA-Leti [128] is adapted and shown in Figure 3.2. The studied device consists of a 100 nm wide and 12 nm thick silicon nanowire on-top of a 150 nm thick buried SiO_2 oxide (BOX). The silicon substrate underneath the BOX is also used as a back-gate. The silicon nanowire is encapsulated in a 5 nm SiO_2 layer, upon which two face-to-face gate electrodes are patterned with length L = 60 nm and a face-to-face separation of 70 nm. A 40 nm wide Si_3N_4 spacer is added around the gates to prevent implantation of dopants near the target quantum dot locations.

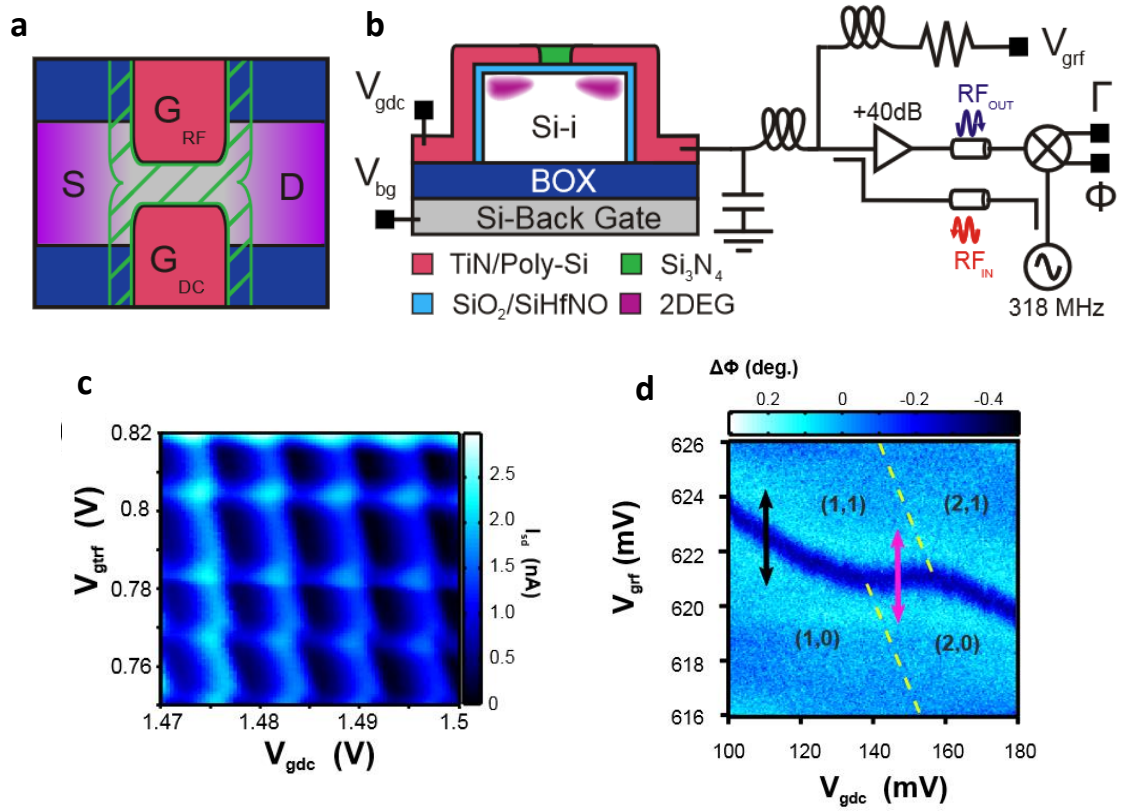


Figure 3.2: Single-nanowire device & dot formation. **a**, Top-view schematic of a nanowire device with face-to-face gate electrodes. **b**, Cross-section schematic showing materials and electrical connections. **c**, Transport current through the nanowire, showing non-linear conductance characteristic of quantum dot formation. The honeycomb pattern indicates formation of a double quantum dot. **d**, Interdot charge anticrossing measured dispersively via the gate electrode G_{RF}. This figure is adapted from Betz, et al. Nano Lett. (2015) [127]

The device is connected as shown in Figure 3.2b, such that charge transitions of the dot under G_{RF} can be detected via dispersive sensing [68]. Firstly, the direct transport current through the nanowire is measured under a 3 mV source-drain bias, whilst sweeping the gate voltages V_{GRF} and V_{GDC}. This reveals a non-linear conductance in a honeycomb pattern indicating the formation of a double quantum dot, one under each gate electrode. The dots are determined to form in the corners of the nanowire, based on electrostatic simulations [129]. Operating a device in transport mode allows for detection of quantum dots, however operation of qubits in this mode does not allow for single-shot readout of qubit states. Whilst some studies have demonstrated qubits in this mode [28, 29, 53], it leads to limited readout visibility, and is incompatible with error correction protocols that

require spin readout.

An advancement is made by probing charge movements in the device via reflectometry. This employs one of the dots as a sensor which can be used to detect charge movements in nearby dots. Figure 3.2d shows a charge transition in the dot under G_{DC} detected via a capacitive shift in the G_{RF} dot-reservoir transition. Single-shot spin readout can then be achieved by performing a spin-to-charge conversion and probing the charge state [130].

Dispersive sensing in this manner requires the placement of an ancillary sensor dot nearby the qubits, in this case on the opposite side of a nanowire. In the case of nanowire based platforms in which it is easiest to form quantum dots as edge states at the corner of the nanowire, this placement of a sensor dot within the nanowire would interrupt the formation of 2xN arrays of qubits. Fully gate-based sensing as in Refs. [70,71] can alleviate this problem by using only interdot charge movements as long as sufficient signal-to-noise ratios can be achieved.

Our study investigates an alternative approach which is to place the sensor in a second adjacent nanowire and will be discussed for the remainder of this chapter.

3.1.2 Double Nanowire Devices

The first device investigated in our study is shown in Figure 3.3a and consists of two parallel 70 nm wide silicon nanowires separated by 120 nm, fabricated using fully-depleted silicon-on-insulator (FD-SOI) technology at CEA-Leti [128]. The nanowires are 7 nm thick and have an effective oxide thickness of 6 nm. The gate electrodes L1, L2, R1, R2, made out of a stack of titanium nitride and polysilicon, wrap over the edges of the nanowires. Silicon nitride spacers are used to self-align the n-type doped source (SR/SL) and drain (DR/DL) leads to the gates.

The device is connected as in Figure 3.3b, with a small source-drain bias V_{SDR} applied to the right-side nanowire, along with a 100 μV excitation at 23 kHz for lock-in amplification. Gate voltages V_{R1} and V_{R2} are swept in Figure 3.3c revealing regular Coulomb oscillations,

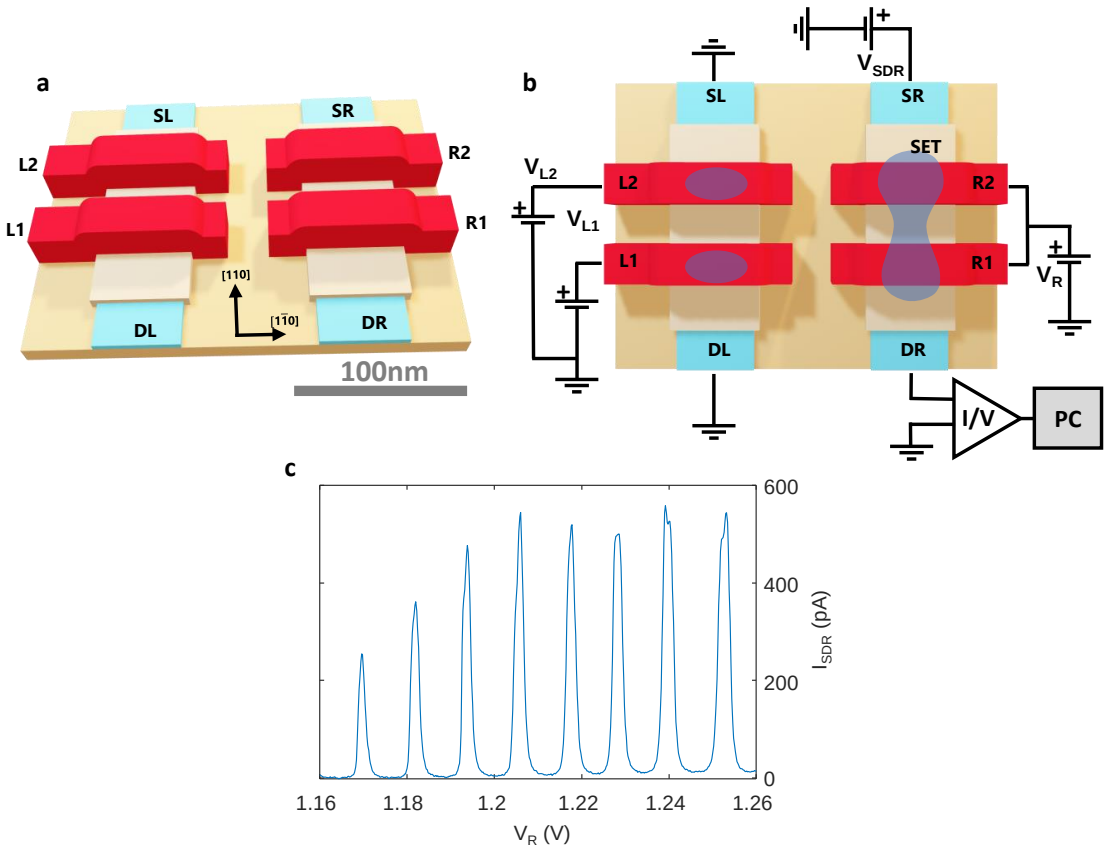


Figure 3.3: Double-nanowire device & dot formation. **a**, Three-dimensional schematic layout of a FD-SOI device with two nanowires and wrap-around gates. **b**, Top-down schematic layout showing electrical connections. Gates L1 and L2 are individually biased from V_{L1} and V_{L2}, whilst gates R1 and R2 are biased together from V_{R}. Approximate quantum dot locations are shown in transparent blue. A source drain bias, V_{SDR}, is applied to SR, and the resulting current through right nanowire measured from DR using lock-in amplification. **c**, Coulomb oscillations in the right-side nanowire.

indicative of the formation of a quantum dot under the gates R1 and R2. Coupling to the source and drain leads is weak in these device designs, resulting in the transport current being too small to measure until the gate-accumulated quantum dots reach the many electron regime, and a single large quantum dot is formed spanning both gates R1 and R2. The right-side nanowire is then configured as a Single Electron Transistor (SET) charge sensor, by biasing it to a point of high dI/dV_{R} on the flank of a Coulomb blockade peak to be sensitive to nearby charge fluctuations [131].

3.1.3 Charge Sensing From a Remote Nanowire

A second excitation of 3 mV at 213 Hz is now applied to the gates L1 and L2 for a second lock-in amplification to measure charge movements sensitive to the voltages V_{L1} and V_{L2}. The DC biases on the left-side nanowire gates L1 and L2 are now individually swept to measure accumulation of quantum dots under each gate, as shown in Figure 3.4 for the few electron regime in Figure 3.4a and the multi-electron regime in Figure Figure 3.4b. Dark lines indicate charge transitions between dots under L1 and L2, and the source/drain leads. The signal is significantly stronger in the many electron regime than in the few electron regime. We determine this to be due to the screening effect of the gates L1 and L2, preventing capacitive coupling from the dots to the SET in the right-side nanowire. This screening becomes less effective as more electrons are added to the dots, causing the wave functions to grow and bleed out from underneath the wrap-around gates, which in-turn increases the capacitive coupling to the SET.

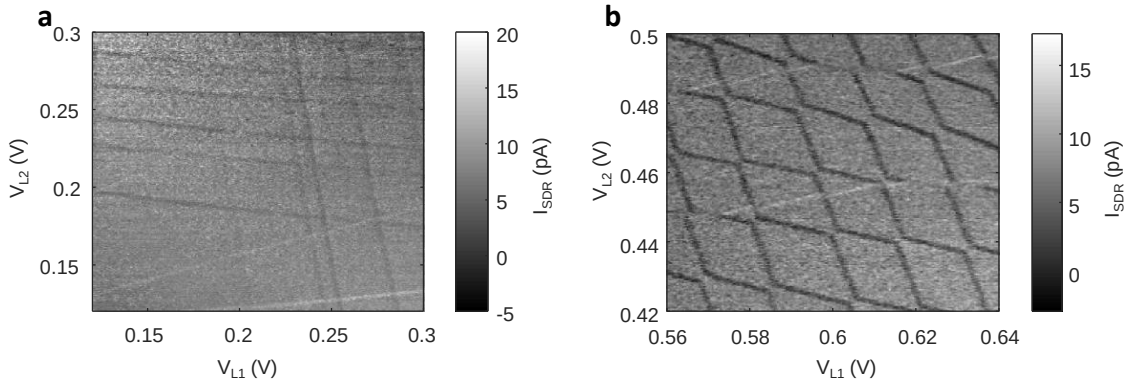


Figure 3.4: Charge sensing in a double-nanowire device. a, Dot-reservoir charge transitions in the left nanowire in the few electron regime. **b**, Dot-reservoir charge transitions in the left nanowire in the many electron regime.

An irregular spacing of the charge transitions in the few-electron regime (Figure 3.4a) may indicate that the first few electrons form multiple separate quantum dots under the same gate, most likely at the corners of the nanowire [129]. The transition spacings become much more regular for many electrons, indicating that eventually the multiple dots merge into one.

3.2 Floating Couplers Between Adjacent Nanowires

In this section we test a new device design in which a cut is made in the polysilicon gates over the nanowires, shown in Figure 3.5a. This leaves gates L1, L2, R1, and R2 only overlapping the edge of the nanowire, and additional gates C1 and C2 which are un-contacted, and therefore floating. C1 and C2 then serve as capacitive couplers between the nanowires. The device is connected as in Figure 3.5b.

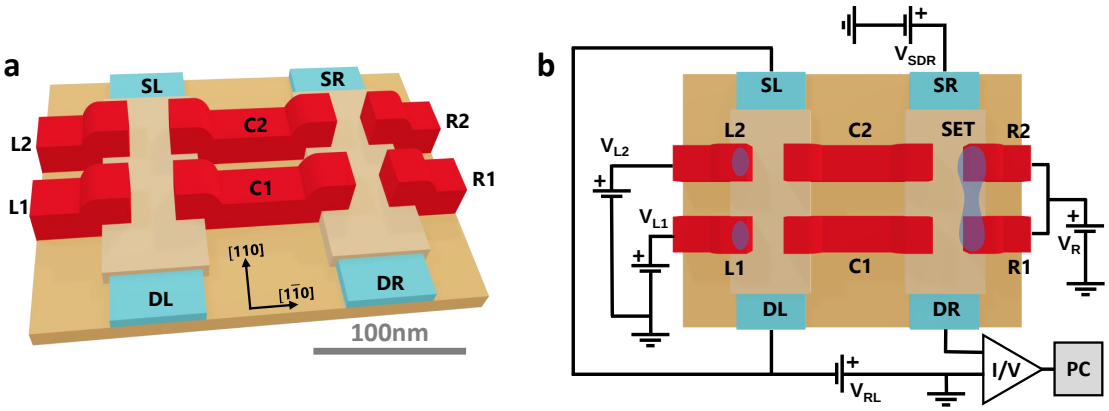


Figure 3.5: Split-gate device schematics. **a**, Three-dimensional schematic layout of a FD-SOI device with two nanowires, split gates, and floating couplers. **b**, Top-down schematic layout showing electrical connections. Gates L1 and L2 are individually biased from V_{L1} and V_{L2}, whilst gates R1 and R2 are biased together from V_R. Floating couplers C1 and C2 are uncontacted. Approximate quantum dot locations are shown in transparent blue. A source drain bias, V_{SDR}, is applied to SR, and the resulting current through right nanowire measured from DR using lock-in amplification. V_{RL} is used to apply a differential bias between the left- and right-side nanowires.

The left-side nanowire gates L1 and L2 were individually biased to accumulate one quantum dot under each gate. This two-dot system was first characterised via current (transport) measurements [132] as a function of bias voltages V_{L1} and V_{L2}, shown in Figure 3.6a. The honeycomb pattern associated with two coupled quantum dots can be resolved only for a high number of electrons in each dot (large V_{L1} and V_{L2}). Again, for low electron occupancies, the smaller electronic wavefunctions result in reduced tunnel rates and immeasurably low currents for this measurement set-up.

The right-side nanowire was then operated as an SET charge sensor by biasing the (electrically shorted) R1 and R2 gates to accumulate one quantum dot, which serves as the SET

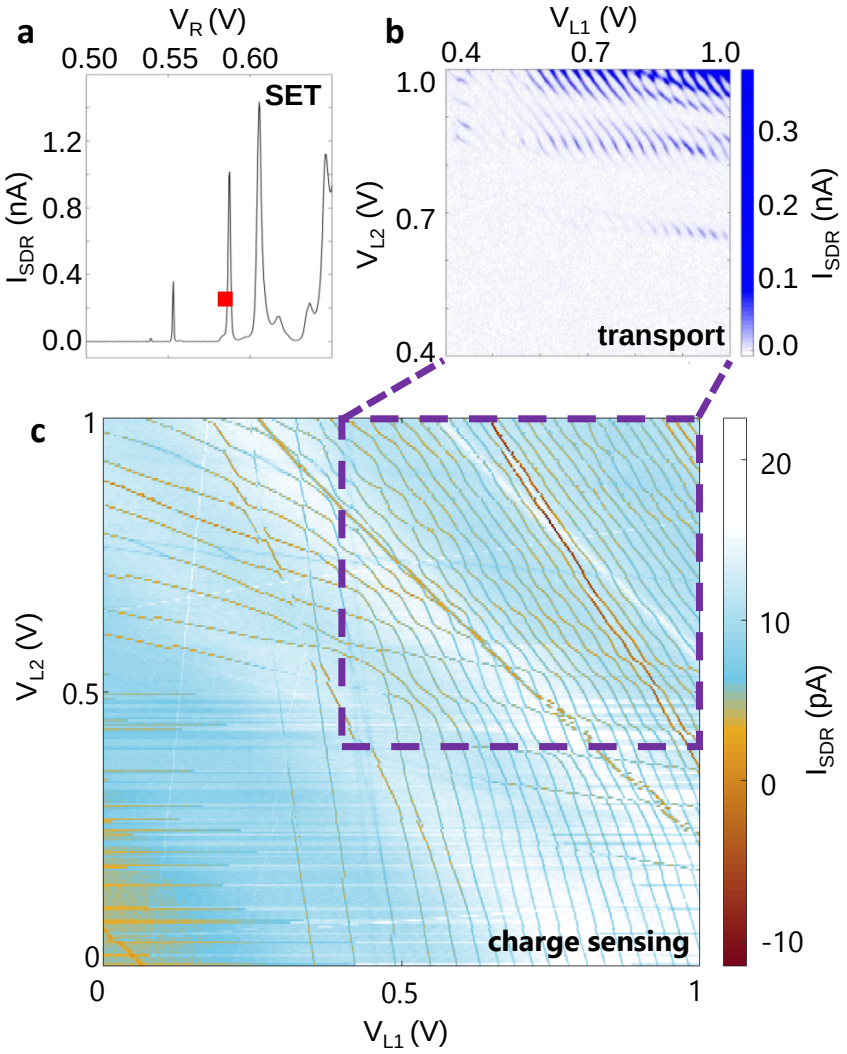


Figure 3.6: Split-gate transport and charge sensing. a, b, Charge transport measured with a single lock-in amplifier applying 100 μV at 23 kHz to the S-D bias for the respective nanowire. **a** Transport through the left nanowire, **b** Transport through the right nanowire, which is then configured as a charge sensor by biasing it to the high sensitivity point shown by the red marker. **c**, Charge sensing performed in a double lock-in amplifier setup, with 100 μV at 23 kHz applied to the sensor V_{SDR}, and 3 mV at 213 Hz applied to the dot gates L1 and L2.

island, coupled to heavily-doped source and drain regions SR and DR. Large amplitude Coulomb blockade oscillations in the sensor nanowire current are observed (Figure 3.6b). The irregular Coulomb blockade oscillations observed in this device can be corrected with independent control of R1 and R2 bias (see Figure 3.3c). The SET is biased to the point marked by the square symbol in Figure 3.6b for maximum sensitivity.

In this device, the charge sensitivity is also increased by the floating electrostatic couplers C1 and C2, providing charge transition sensitivity down to the last electron for the quantum dots under L1 and L2, as can be seen in Figure 3.6c. As the charge occupancy of the dots is increased with more positive bias V_{L1} and V_{L2}, the inter-dot coupling increases as indicated by the emergence of a traditional honeycomb pattern [132]. At higher gate biases the transitions eventually become diagonal lines, corresponding to a completely merged large dot. Decreased visibility of the charge transitions for the last few electrons in each dot is seen where the tunnel rate between the quantum dots and the reservoir becomes slower than the lock-in probe frequency [133] (213 Hz in this case).

Additional spurious transition lines seen in Figure 3.6c may correspond to disorder or randomly positioned dopants in cases where their slope and/or contrast does not match a repeatable feature. Dashed lines mark the full window in which the transport measurements were taken for Figure 3.6a and reinforce the advantage of charge-sensing arrangements for the observation of charge transitions in few-electron quantum dot systems [134].

The electrostatic coupling between the sensor nanowire and the quantum dots is enhanced by the presence of the floating gates C1 and C2 [135], and the floating gates remain well isolated from their surroundings, with no significant charging effect observed during experiments. We expect that device designs incorporating similar couplers may enjoy extra freedom in where sensors can be placed, relative to quantum dots that need to be read out.

3.3 A 2x2 Array of Quantum Dots

The dimensionality of qubit arrangements plays an important role in the propagation of errors, as well as in the fidelity thresholds of quantum error correcting codes [10]. A non-trivial topology for quantum dot networks is therefore a key development towards full scale silicon quantum computers. Even though the device design investigated here does not allow for an extended two-dimensional arrangement of qubits, we take a first step

towards this goal by developing a technique to accumulate and characterise a 2×2 array of dots within a single nanowire.

The strong electrostatic coupling between the floating gates (C1 and C2) and each nanowire allows the creation of additional quantum dots underneath the floating gates by using a differential bias between the nanowires. The left-side (dot) nanowire was biased negatively relative to the right-side (sensor) nanowire, such that the floating couplers C1 and C2 act as gates to induce two additional quantum dots, shown schematically in Figure 3.7a.

Measurements with this configuration are shown in Figure 3.7b. Charge transitions in C1 and C2 dots are distinguishable from L1 and L2 quantum dot transitions on the V_{L1} vs V_{L2} charge stability diagram by nature of their relative coupling strengths to the gates L1 and L2. The L1 and L2 quantum dots have strong coupling to the biased gates and therefore exhibit transitions nearly perpendicular to their respective axes. The quantum dots under C1 and C2 have larger cross capacitance to the opposite dot gate (i.e., L2 and L1, respectively), leading to transitions that are inclined with respect to the axes. Secondly, the C1 and C2 quantum dots couple more strongly to the sensor compared to L1 and L2 dots, owing to their proximity to the floating couplers, and hence their transitions can be distinguished by the larger influence on the SET current (see Figure 3.7b).

This arrangement of quantum dots provides increased connectivity and dimensionality while also providing a configuration favourable for single-shot readout of inter-dot transitions, which is a requirement for qubit readout based on Pauli spin blockade. We note that similar 2×2 quantum dot arrays were formed in devices fabricated with the same foundry technology, but which contain a single nanowire and all the split gates are directly biased (no floating coupler gate) [84, 85]. In contrast to that strategy, our method enables an SET to be positioned remotely to the quantum dot array, while maintaining a high sensitivity to interdot charge movements. Transitions between L1 and C1, and L2 and C2, respectively, can be seen in Figure 3.7b as white lines. Transitions between L1 and L2 have less signal since the charge movement occurs parallel to the SET nanowire. We focus now on a double dot configuration with electrons under L1 and C1, as schematically depicted in Figure 3.7c. The corresponding charge transition diagram in Figure 3.7d shows

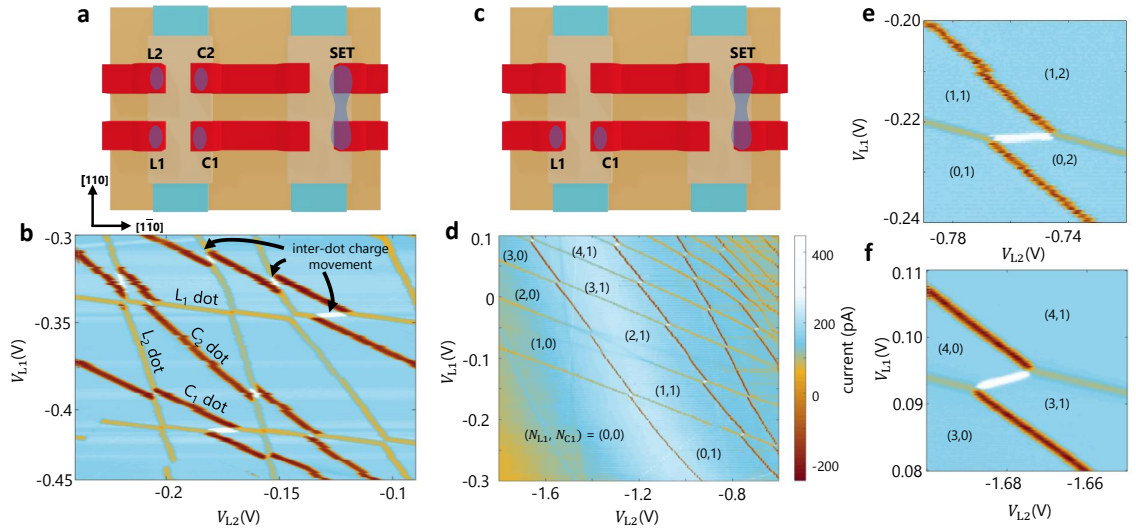


Figure 3.7: 2x2 quantum dot array in CMOS. **a**, Schematic top-view of quantum dot configuration for the charge sensing shown in **b**. **c**, Quantum dot configuration for charge sensing measurements **d, e** and **f**. Quantum dot locations are shown in transparent blue in **a,b** The colour scale is shared across panels **b,d,e,f**.

operation in the few electron regime.

For quantum computation, the quantum level the electron occupies in either dot should be energetically well separated from excited states. If this is not the case, then only a small region in voltage space will exhibit Pauli spin blockade, and avoiding the creation of spin-triplet states during the readout pulse becomes challenging. Due to the low symmetry of these corner dots, a detailed analysis of the electron filling and assigning quantum numbers to the different dot occupations is a challenging task which is beyond the scope of the present work. Instead, we focus on the charge configurations in which the electrons occupy either the ground valley-orbital state (e.g., (1,1)-(0,2) charge transition as in Figure 3.7e); or the configuration in which two electrons could form a closed shell in the ground valley-orbital state and a third electron occupies an excited valley state (e.g., (3,1)-(4,0) charge transition as in Figure 3.7f). The interdot charge transition shown in Figure 3.7e has little dependence on V_{L2}, possibly due to the coupling factors of the L2 gate to the L1 and C1 dots being roughly equal in this configuration [122]. In what follows, all charge occupation values (N_{L1}, N_{C1}) refer to the configuration with N_{L1} electrons under the L1 dot and N_{C1} electrons under the C1 dot.

3.4 Valley Structure and Tunnel Rates

3.4.1 Tunnel Rate Measurements

All possible spin-based quantum processor architectures ultimately rely on a high-fidelity method to read out the spin of each qubit. For spin readout via spin-to-charge conversion, either the energy dependent tunnelling rate to a reservoir [64], or between two dots for Pauli spin blockade [65, 136], should significantly exceed the spin relaxation rates. Preliminary measurements indicate that the tunnel rates in this device are too low for spin readout [56]. In the simplest configuration, the transition rate between (1,0) and (0,1) is measured to be 2.0 ± 0.2 Hz, by observing real-time tunnel events at the anti-crossing (see Figure 3.8a). Increasing the electron population so that the electronic wavefunctions for each dot overlap more strongly, shows an increase in the transition rate to 40 ± 4 Hz for the (2,0)-(1,1) charge transition (Figure 3.8b). We note that transition rates of this magnitude are strongly impacted by stochastic charge movement caused by phonons or high-amplitude low-frequency electric noise.

An additional device that incorporates a metal layer (M1) approximately 270 nm above the active silicon nanowire region was also tested, with results shown in Figure 3.8c-e. By applying a large bias voltage V_{M1} to this 'global' top gate, the tunnel coupling between dots can be tuned. Due to the global influence of this top gate, in particular most strongly through the floating couplers to the C1 and C2 dots, a compensating bias is applied to the other gates, and the charge stability diagram is recalibrated. Initial measurements testing this mode of operation were undertaken by applying an AC lock-in excitation in-phase to L1 and L2, with the device tuned such that the excitation drives a charge movement across the target anti-crossing. The lock-in frequency is swept to measure at which point the SET signal from this charge movement decreases, indicating that the charge is no-longer tunneling across the anti-crossing due to the lock-in frequency exceeding the inter-dot tunnel rate. For the (1,0)-(0,1) transition with $V_{M1} = 9$ V, the tunnel rate was measured to be 8.5 kHz, which is considered still insufficient for spin readout.

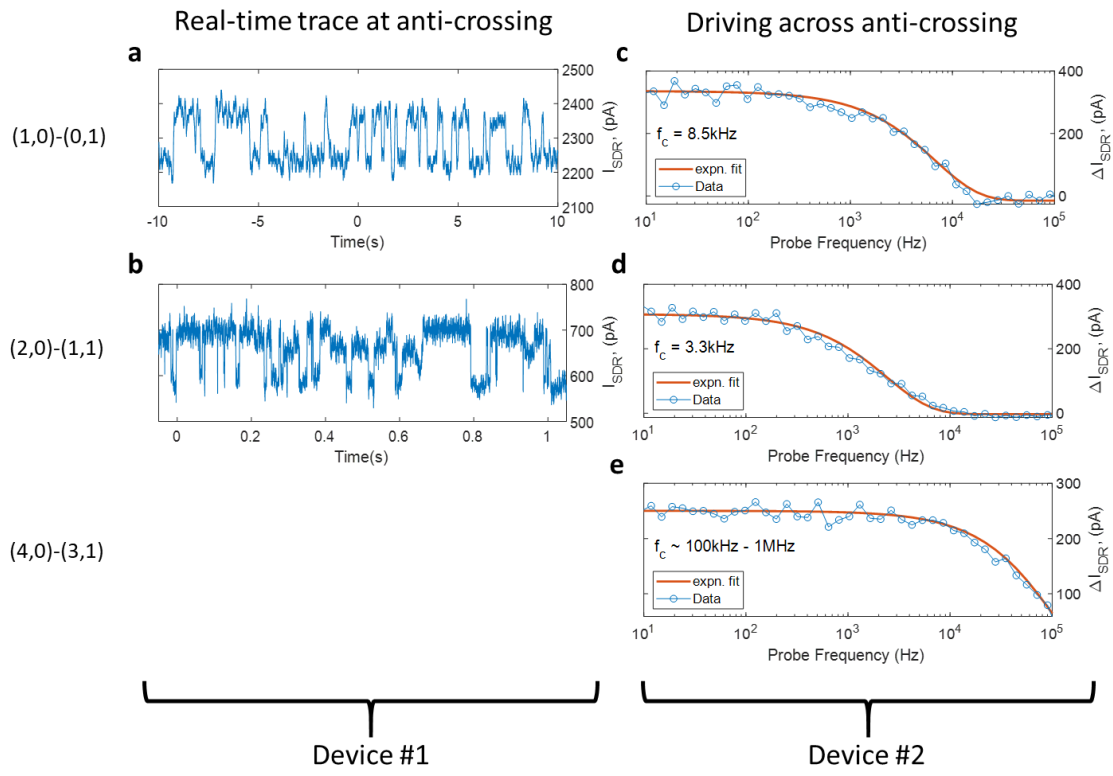


Figure 3.8: Measurement of interdot tunnel rates. a,b, Real-time traces of interdot charge movements between L1 and C1 dots, biased at the (1,0)-(0,1) and (2,0)-(1,1) charge transitions respectively. **c,d,e**, Driven tunnel rate measurements in which an alternate device with a similar design is biased to the (1,0)-(0,1), (2,0)-(1,1), and (4,0)-(3,1) interdot charge transitions respectively, with a detuning excitation applied at the probe frequency. A positive current indicates that a charge is moving in phase with the probe. In this device an additional bias is applied to a line in the Metal-1 layer, 270 nm above the active region, to increase tunnel coupling.

Tunnel rates increase substantially for higher dot charge occupancies due to the increased size of the dot wavefunction, as seen in the (4,0)-(3,1) charge transition in Figure 3.8e, and exceed the bandwidth of the measurement apparatus. A decrease in the tunnel rate for the (2,0)-(1,1) transition could be due to a Pauli blockade effect as only a subset of states populated in the (1,1) charge configuration can tunnel to (2,0).

3.4.2 Tunnel Rate Simulations

In order to design devices with tunnel rates that can enable the spin readout fidelities required for quantum computation, we model the electronic structure of nanowires of dif-

ferent transverse dimensions within the effective mass approximation (see also Ref. [129]). Electrons in silicon possess an anisotropic effective mass. In order to determine the effective mass of the electrons in the direction of the tunnelling movement between dots, it is necessary to determine which silicon conduction-band valley state is the ground state for these quantum dots. The nanowire is fabricated along the [110] direction on a (001) wafer, however the valley states are aligned along [100] (x), [010] (y) and [001] (z) directions. For the geometry of the device studied here, strain and electrostatic confinement have comparable effects in determining the valley ground state (see insets in Figure 3.9). On one hand, the corner electric field confines the electron slightly more strongly against the upper (001) oxide interface, which energetically favours a ground state formed by the z valley states. On the other hand, strain due to the different thermal contractions of the material stack [137] may alter the energy ordering between valley states [138].

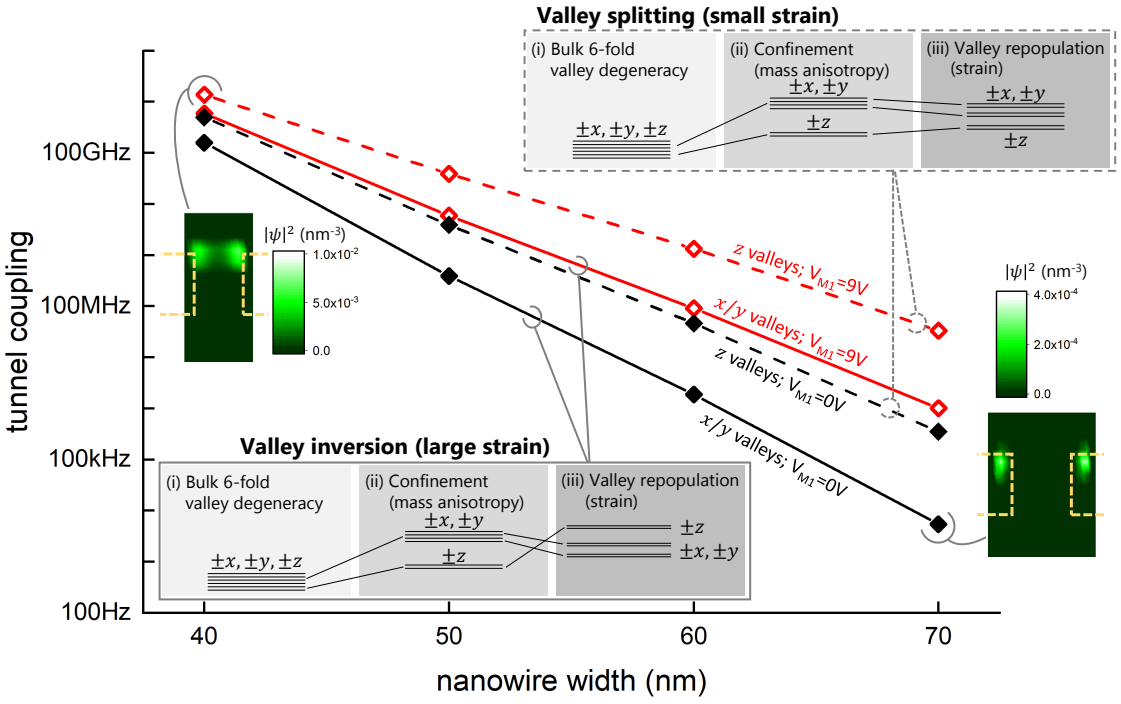


Figure 3.9: Simulation of valley structure and tunnel rates. Simulation of electron wavefunctions and the resulting predicted interdot tunnel coupling versus nanowire width. Inset: energy band diagrams show the modelled quantum dot band structures.

Simulations show that both effects can be quantitatively comparable for all nanowire sizes. The angle of the corner electric field leads to a splitting between z valleys and x or y valleys

induced by quantum confinement of $\Delta_{\text{conf}} \approx 19-22$ meV, favouring a doubly degenerate z ground state (see also Ref. [125]). Valley-orbit coupling could lift the remaining degeneracy between $\pm z$ valleys, but it is not included in the simulations presented here. The impact of strain on the valley structure is hard to predict with precision in nanometric devices, which may be affected by process-induced strains, crystal defects, variability and non-idealities in their geometries. A strain anisotropy of 0.2% would be sufficient to generate a relative energy shift between valleys that is comparable to Δ_{conf} [138, 139]. For this reason, we study the tunnel rates both with and without valley inversion.

With valley inversion, the mass along the direction connecting both L1 and C1 dots $[1\bar{1}0]$ is a combination of the longitudinal and transversal masses and the effective mass tensor becomes non-diagonal. As a result, the electronic wavefunctions are not symmetric and the tunnel rates are smaller than in the case of a z valley state (see Figure 3.9). The calculations shown in Figure 3.9 indicate tunnel rates in this device become more suitable for quantum computing applications for a modest decrease in the transverse nanowire dimension to below 60 nm. The range of tunability expected from biasing the M1 global top gate is also shown (Figure 3.9 red open symbols).

3.5 Conclusion

In general, forms of orbital or valley degeneracy are detrimental for quantum computing, leading to fast spin relaxation and undermining exchange coupling between spins, however this is not always the case and will be investigated in depth in Chapter 4. In the context of spin qubit readout, the added degree of freedom from an additional nearby energy level may hinder spin blockade. In order to guarantee a priori that no undesirable degeneracy is present, it is necessary to know the electronic structure of the dot, which can be a challenging issue for many-electron qubits. In specific examples of very small, highly symmetric quantum dots [50], it is possible to recognise the shell structure of the dot and consider electronic interactions as a small perturbation, similarly to what is done in atomic physics. In a more general case such as the corner dots in a nanowire, the

electronic structure and excitation spectrum may not bear an easily recognisable labelling in terms of quantum numbers. In these conditions, it is desirable to operate at low electron occupancies.

The charge sensor measurements described here enable the identification of quantum dot transitions down to the last electron. High sensitivity charge sensing is a key ingredient used to perform single-shot readout of single spin qubits [140], and we note a parallel study on nanowire devices with floating gates that closely examines the electrostatic couplings [122]. Nevertheless, the device studied here does not allow for spin readout due to the limited tunnel rates between dots, a constraint that may be alleviated with a modest dimension reduction, or with an extra layer of interleaved gates for control of interdot coupling [141, 142]. Our study provides a pathway for future device designs that could reach the tunnel rate regime required for spin readout based on Pauli spin blockade.

In the years following this study, demonstrations have been made of tunable tunnel rates in devices manufactured in full-scale 300mm wafer foundries, in FinFET [30], FD-SOI [87], and planer SiMOS [42] material stacks.

The demonstration of enhanced capacitive coupling between remote quantum dots is also encouraging. Similar structures may also enable long-range spin coupling, as proposed in [59].

Chapter 4

On-Demand Electrical Control of Spin Qubits

Once called a "classically non-describable two-valuedness" by Pauli [143], the electron spin is a natural resource for long-lived quantum information since it is mostly impervious to electric fluctuations and can be replicated in large qubit arrays in silicon, offering high-fidelity control [22–24, 30, 38, 40]. Paradoxically, one of the most convenient control strategies is the integration of nanoscale magnets to artificially enhance the coupling between spins and electric fields [51,144,145], which in turn hampers the spin's noise immunity [146] and adds architectural complexity [80]. Here we demonstrate a technique that enables a ***switchable*** interaction between spins and orbital motion of electrons in silicon quantum dots, without the presence of a micromagnet. The naturally weak effects of the relativistic spin-orbit interaction in silicon are enhanced, leading to a speed-up in Rabi frequency by a factor of more than 650 by controlling the energy quantisation of electrons in the nanostructure, enhancing the orbital motion. Fast electrical control is demonstrated in multiple devices and electronic configurations, highlighting the utility of the technique. Using the electrical drive we achieve a coherence time $\boldsymbol{T_{2,\mathrm{Hahn}} \approx 50}$ µs, fast single-qubit gates with $\boldsymbol{T_{\pi/2} = 3}$ ns, and gate fidelities of 99.93% probed by randomised benchmarking. The higher gate speeds and better compatibility with CMOS manufacturing, enabled by on-demand electric control, improve the prospects for realising scalable silicon quantum processors.

The work presented in this chapter has been presented in:

W. Gilbert, T. Tanttu, W. H. Lim, M. Feng, J. Y. Huang, J. D. Cifuentes, S. Serrano, P. Y. Mai, R. C. C. Leon,

C. C. Escott, K. M. Itoh, N. V. Abrosimov, H-J. Pohl, M. L. W. Thewalt, F. E. Hudson, A. Morello, A. Laucht, C. H. Yang, A. Saraiva, and A. S. Dzurak. "On-demand electric control of spin qubits." *arXiv:2201.06679*, (2022).

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The density of quantum dots in an array is set by the size of the electron wave functions and the consequent size and pitch of gate electrodes [147], but individualised high-fidelity control of electron spin qubits in silicon typically requires on-chip integration of much larger devices, such as micromagnets [50, 145] or stripline antennae [19]. Other spin qubit implementations, such as electrons in InAs nanowires [148] and holes in silicon [28] and germanium [31, 149, 150], have sufficient intrinsic spin-orbit coupling to enable localised, all-electrical control employing only the gate electrodes that are already used to define the quantum dots. The possibility to induce spin-orbit effects by leveraging an orbital quasi-degeneracy has been investigated in a few circumstances [150–154]. However, the same spin-orbit coupling that enables direct electrical control also exposes the qubits to decoherence from electrical noise [146]. Furthermore, while some semiconductor fabrication plants have the capability to integrate non-silicon materials, electrostatic quantum dots using silicon CMOS technology offer the strongest prospect of leveraging the full potential for integration and miniaturisation of the most advanced transistor fabrication nodes [124].

4.1 A Controllable Quantum Dot Energy Spectrum

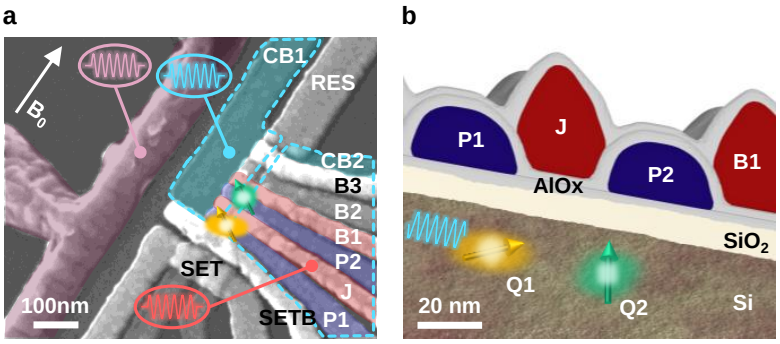

Figure 4.1: Device design a, Scanning electron micrograph of a quantum dot device nominally identical to all four devices investigated here. **b**, Simulated cross section of the device geometry overlaid with a schematic of the electron wavefunctions and spins.

Spin-orbit effects for electrons in silicon quantum dots are typically small resulting from the weak contributions of both Rashba and Dresselhaus spin-orbit couplings. This means that

direct electric driving is weak without a synthetic enhancement. However, these effects can become significant if the electron is allowed to move between orbital configurations, either within the quantum dot [150, 155], or by moving between two quantum dots [153]. To date, there is yet to be a demonstration in silicon that harnesses the effect in a manner that is both controllable, and maintains high-fidelity quantum operations.

Orbital configurations are generally immutable due to the well quantised orbital energies of few-electron quantum dots. However, a dense arrangement of electrodes such as in Figure 4.1a and b (nominally identical to all devices studied here) gives access to a level of control over the potential landscape that can be used to consistently form quantum dots that possess an energy spectrum with flexible controllability.

We accumulate two quantum dots under gates P_1 and P_2 in a silicon MOS device in which the substrate is purified ^{28}Si containing 800 ppm residual ^{29}Si. Each of the two quantum dots are configured as single spin qubits, and read out using spin-charge conversion based on Pauli spin blockade (PSB) [65], and detected with a nearby SET.

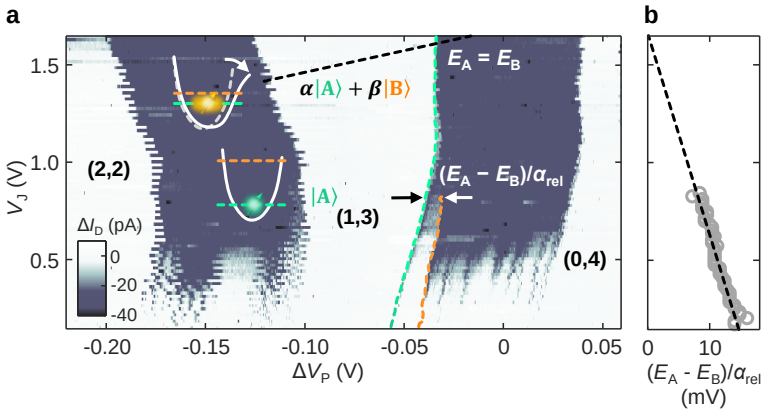

Figure 4.2: Excited state spectroscopy a, Excited state spectroscopy at zero B_0 field of an isolated double quantum dot containing 4 electrons, measured in device A as a function of V_J and the interdot bias ΔV_P (static biases $V_{P1} = 2.08V$, $V_{P2} = 2.4V$), with $f_{probe} = 477$ Hz. Energies E_A (green dashed line) and E_B (orange dashed line) are fitted to step increases in interdot tunnel rate, indicating occurrence of ground and first excited states. **b**, Extrapolation of the $E_A - E_B$ separation reveals a convergence near $V_J = 1.6$ V.

Figure 4.2a shows how excited state spectroscopy may be used to infer the presence within a dot of electronic states that have a differential lever arm α_{rel}, and correspond to different

charge density distributions, which therefore couple differently to the various electrostatic gates due to a non-uniform electric field. In Appendix A we discuss the magnitude of the obtained α_{rel} and how it corroborates our interpretation of the orbital excitation. We denote these orbital configurations A and B, and their energies E_{A} and E_{B}, respectively.

We instigate internal movement of the electron within the dot by biasing the gate voltages to reconfigure the quantum dot to a point where the two states A and B (each with different spin configurations) have approximately the same energy. At this point, the quantum dot becomes highly polarisable, which leads to fast electrically-driven spin resonance (EDSR) [54]. The intrinsic spin-orbit effect is not changing at this point, rather, the coupling to electric fields and the rate of EDSR is enhanced as it is inversely proportional to the energy gap [156]. This quasi-degeneracy point can be found by extracting the excitation energy (separation of fitted orange and green dotted lines in Figure 4.2a), extrapolating its trend against the side gate voltage (J gate) to the point where it reaches zero (Figure 4.2b). At that point, the A and B states hybridize, and the electron enters a superposition state $\alpha|\mathrm{A}\rangle + \beta|\mathrm{B}\rangle$. The exact values of α and β depend on the particular nature of the two states A and B, but they are controllable by exploiting the differential lever arm α_{rel}.

This controllability over the wavefunction hybridization is the key to on-demand exploitation of spin-orbit effects. In Figure 4.3a we present a typical series of control steps, starting from an idling qubit (i) that is set to have minimal spin-orbit effects by setting the quantisation energy to be large ($\alpha \approx 1$ and $\beta \approx 0$). The dot is then deformed to create the hybrid state (ii) for a short amount of time, sufficient for the application of a microwave pulse (iii) that creates the spin rotation. The quantum dot is then reconfigured to the idling mode (iv), which restores the qubit resilience against spurious electric field fluctuations. This strategy allows for idling qubits to be protected for prolonged times while active qubits are being manipulated. The vision of a scalable qubit arrangement presented in Figure 4.3b is based on a dense array of spins in a grid of quantum dots. Individualised control of a subset of the qubits can be performed by reconfiguring the electrostatic potential and applying microwave excitations, both achieved directly by the top gate that defines the

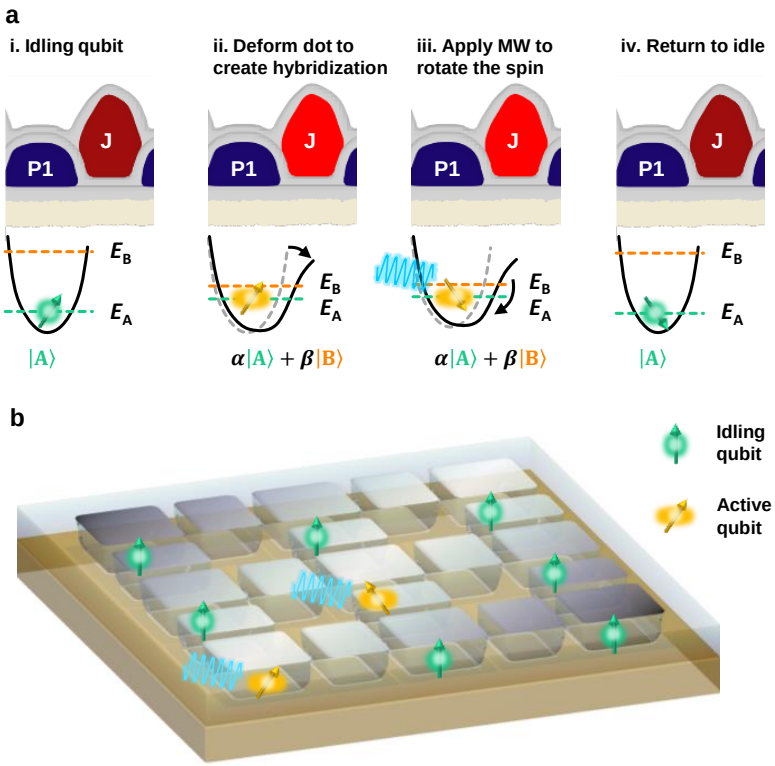

Figure 4.3: Operation protocol for switchable qubits a, Control sequence illustrating how to deform the quantum dot to turn on a controllable orbital degeneracy using the lateral J gate and use it for qubit control. The idling state is purely spin-only, while the control state is a spin-orbit mix. **b**, Rendering of a multi-qubit array with idling qubits set to be in a spin-only state, while some of the qubits are being controlled in a spin-orbit mixed state.

quantum dot. This on-demand activation of spin-orbit effects would significantly simplify the design and operation of large scale quantum processors by removing the need for additional complex nanomagnet or antennae arrays [79, 80].

4.2 Pulsed Electron Spin-Orbit Spectroscopy

While the orbital spectroscopy technique presented in Figure 4.2a is useful in narrowing the search range for a degeneracy point, ultimately it is the change in spin dynamics that will be the most reliable signature of the successful formation of a hybrid wavefunction. We show as a dashed black line in Figure 4.2a the trend of points that are identified as having maximum spin-orbit driving. This identification is obtained by a technique we call

pulsed electron spin-orbital spectroscopy (PESOS). It consists of applying a microwave pulse of fixed duration and power and measuring its effect on the spins as a function of the microwave frequency and gate voltages. Optimal visibility of the spin resonant frequency is obtained when the pulse duration and amplitude match with the condition for a spin flip.

4.2.1 Enhanced Spin-Orbit Coupling

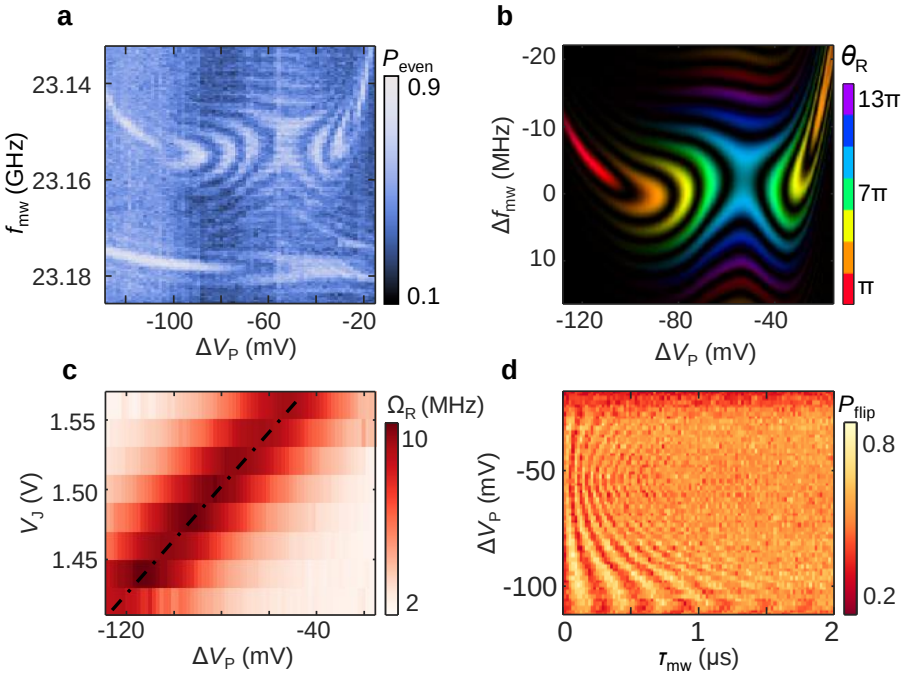

Figure 4.4: Pulsed Electron Spin Orbit Spectroscopy (PESOS) a, PESOS map, consisting of the probability of measuring a spin flip after a burst of microwave of fixed power and duration, while varying the microwave frequency and a gate electrode voltage bias. The power and duration of the burst are roughly calibrated to correspond to a π-rotation for a pure spin state. Fringes appear as a function of gate voltage as the spin-photon coupling becomes more intense, and the spin being rotated by several π. **b**, Simulated PESOS map obtained by modelling the spin-orbit qubit as a two-level system with voltage-dependent Rabi and Larmor frequencies to fit the measured PESOS map (see Appendix A). The colours correspond to the angle of spin rotations. **c**, Rabi frequencies extracted from the fitted simulations. **d**, Measured Rabi oscillations over time as a function of ΔV_P, confirming the interpretation of the Rabi speed-up.

Figure 4.4a shows the results from this experiment. With a fixed microwave pulse time we observe spin-flip oscillations as the interdot detuning bias ΔV_P is swept, indicating an enhancement of the efficiency of the EDSR, which results in multiple spin flips with

the same microwave pulse. Simulations of gate-dependent Rabi and Larmor frequencies, shown for example in Figure 4.4b for the measurement from Figure 4.4a, can be used to extract the magnitude of the speed-up and help interpret the PESOS maps.

By measuring PESOS maps for different biases V_J and ΔV_P, we can extract the bias configuration that provides the largest speed-up in Rabi frequency, as shown in Figure 4.4c. This allows us to completely reconstruct the line in the charge stability diagram in Figure 4.2a that corresponds to a hybrid ground state. Figure 4.4d shows the complete Rabi oscillations of the spin at a fixed drive frequency of 23.154 GHz, confirming our interpretation of the PESOS maps.

4.3 Repeatability Across Multiple Devices & Configurations

In order to assess the suitability of this technique for scalable systems, multiple devices were measured, with different material stacks, charge configurations and B_0-fields. Figure 4.5a and b were taken using different charge configurations in the same device. Figure 4.5c-e are three other devices, with different operation modes, material stacks and microwave excitation strategies, measured in two different cryogenic setups (see Table 4.1 for details). Figures 4.5a-e show examples of PESOS maps generated by double quantum dots in which a single spin is initialised and measured against an ancilla using parity readout [40, 66]. Where two peaks are observed at different frequencies – these correspond to the target spin and the ancilla. All maps have identifiable hybridization points where the probability of a spin flip forms oscillations in at least one of the resonance lines. We note that device D is driven all-electrically by applying a microwave field directly to the CB1 gate (see Figure 4.1a), while devices A to C are driven by the coplanar waveguide antenna, which creates both electric and magnetic fields [157].

We also use this interpretation of the degeneracy enhanced EDSR to guide the experimental search for the degeneracy point shown in Figure 4.5b (see Appendix B). The regularity with which we find these hybridisation points is encouraging for the prospects of scalability

Table 4.1: Device details
Device A was fabricated on an isotopically enriched silicon-28 substrate (50 ppm residual ^{29}Si) [158]. Devices B, C & D were fabricated on an epitaxially grown, isotopically purified ^{28}Si epilayer with a residual ^{29}Si concentration of 800 ppm [159].

Device	A	B	C	D
^{29}Si concentration	50 ppm	800 ppm	800 ppm	800 ppm
Gate materials	TiPd	TiPd	Al	Al
Electron occupancy	(1,3) & (3,1)	(3,1)	(1,3)	(3,1)
B_0-field (T)	0.827	0.55	0.827	0.1 - 1.0
Microwave carrier frequency (GHz)	22.3	15.4	22.3	2.8 - 28
Mode of driving	antenna-based	antenna-based	antenna-based	gate-based

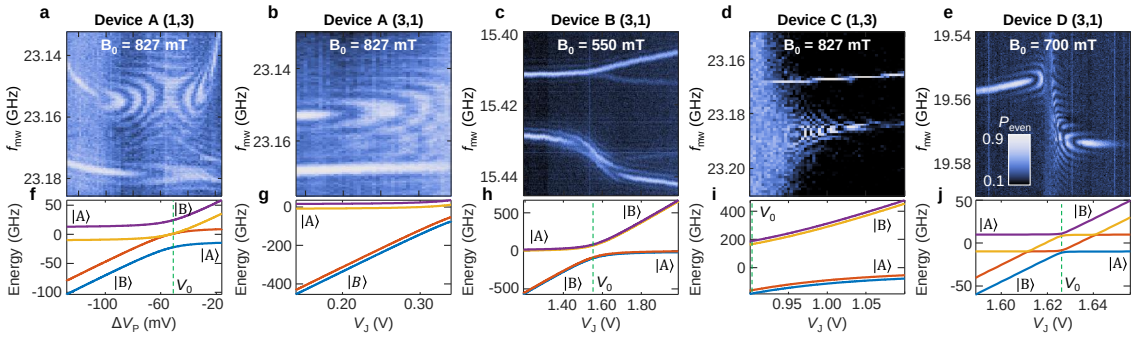

Figure 4.5: Reproducibility across multiple devices a-e, PESOS maps measured in multiple different devices, material stacks, charge configurations, and magnetic fields. See Table 4.1 for details. **f-j**, Four-level models that best reproduce the data from **a-e**, showing the variety of intradot level-crossing regimes and their impact on the spin dynamics.

of this technology. We have been successful in reproducing enhanced EDSR in all devices subject to targeted tests so far.

Across the devices tested, significant variability in the characteristic of level crossings was found. The taxonomy of the spin-orbit effects in Figure 4.5a-e is related to the particularities of the orbital states A and B in each of the devices and dot configurations. The intradot state-hybridization may involve states with different valley configurations (under a rough interface) [86, 160–163], in-plane orbitals [164] or even with interaction-induced charge transitions such as in Wigner molecules [165, 166].

4.3.1 Theoretical Modeling and Fits

We can obtain a description of our system based on the PESOS maps using an effective four-level model, consisting of two spin-$\frac{1}{2}$ systems, A and B. These quantum states can be either valley or orbital states, depending on the specific system, and are represented by $|\mathrm{A}\rangle$ and $|\mathrm{B}\rangle$. The spin states are split by the Zeeman splitting in the presence of a magnetic field, thus forming a total of four non-degenerate states. A full description of the Hamiltonian is contained in Appendix A.

The four-level model is fitted to two different sets of information. One is the qubit frequency f_0, and the other is the Rabi frequency given by f_{Rabi}. To obtain these data from the PESOS maps as shown in Figure 4.5a-e, we extract vertical line traces of P_{even} as a function of the driving frequency f_{mw} at each voltage value. We can then fit these traces to the Rabi equation given by:

$$P_{\mathrm{even}} = \frac{A f_{\mathrm{Rabi}}^2 \left[1 - \cos\left(\tau\sqrt{f_{\mathrm{Rabi}}^2 + (f_{\mathrm{mw}} - f_0)^2}\right)\right]}{f_{\mathrm{Rabi}}^2 + (f_{\mathrm{mw}} - f_0)^2} + \delta A \tag{4.1}$$

where A is the amplitude of the oscillations, f_{Rabi} is the Rabi frequency, f_{mw} is the driving frequency, f_0 is the resonant qubit frequency, τ is the total time of the driving pulse, and δA is amplitude offset of the oscillations. From this fit, we can extract both the Rabi frequency f_{Rabi}, and the qubit frequency, given by f_0, as a function of the gate voltage (either V_{J} or ΔV_{P}). With this information, we are also able to obtain the simulated PESOS maps as shown in Figure 4.4b by plotting the Rabi equation for each voltage value with the fitted parameters.

These extracted values of f_{Rabi} and f_0 as a function of gate voltage will be the target fit values of the four-level model. By varying the parameters of the four-level model Hamiltonian, we perform a non-linear least squares fit of both the Rabi frequencies f_{Rabi} and the qubit frequency f_0 simultaneously, minimizing the difference between the calculated values from the four-level model and target values obtained from fitting to the Rabi equation. The output of this least squares fit are the Hamiltonian parameters describing the system. These fitted parameters will enable us to calculate the eigenenergies of the Hamiltonian

and obtain the energy diagrams as shown in Figure 4.5f-j. More details on the fitting procedure and fitted values are contained in Appendix A.

4.3.2 Tuning a Degeneracy Point

For each of the transitions in Figure 4.5f-j, the hybridization energy gap compares differently to the spin splitting energy, leading to significant qualitative differences as can be seen in the eigenvalues of the fitted four-level models, shown in Figure 4.5f-j. We confirm this interpretation and the ability to recover different regimes by scanning the magnetic field applied to Device D until we obtain the same qualitative features as in Device A (shown in Figure 4.6). Our model indicates that this is possible by setting the spin splitting to be comparable to the orbital splitting. In Device D, this occurs for a magnetic field around $B_0 = 610$ mT.

4.4 Detuning Dependence of the EDSR Drive

We turn our attention to the tunability of the hybridization characteristics, focusing on the device from Figure 4.5e (namely, device D). This is the device with the most marked effects of the orbital degeneracy on spins among the devices studied here. We retake the PESOS map of Figure 4.5e, now focused near the degeneracy point, and with a Gaussian envelope applied to the microwave burst, in order to reduce cross-talk and separately address resonance lines that are close in frequency (shown in Figure 4.7a).

In Figure 4.7b, we characterise the impact of the orbital hybridization on the coherent spin driving. Near the degeneracy point $\Delta V_\mathrm{J} = 0$ V, the Stark shift $\mathrm{d}f/\mathrm{d}V_\mathrm{J}$ becomes large, leading to a faster damping rate of the Rabi oscillations $\Gamma_{2,\mathrm{Rabi}}$. However, the Rabi frequency improvement outpaces the decoherence amplification, resulting in a higher Q-factor $= 2\times f_\mathrm{Rabi}/\Gamma_{2,\mathrm{Rabi}}$ close to the degeneracy point.

It is also apparent that the qubits become somewhat convoluted in this configuration, with

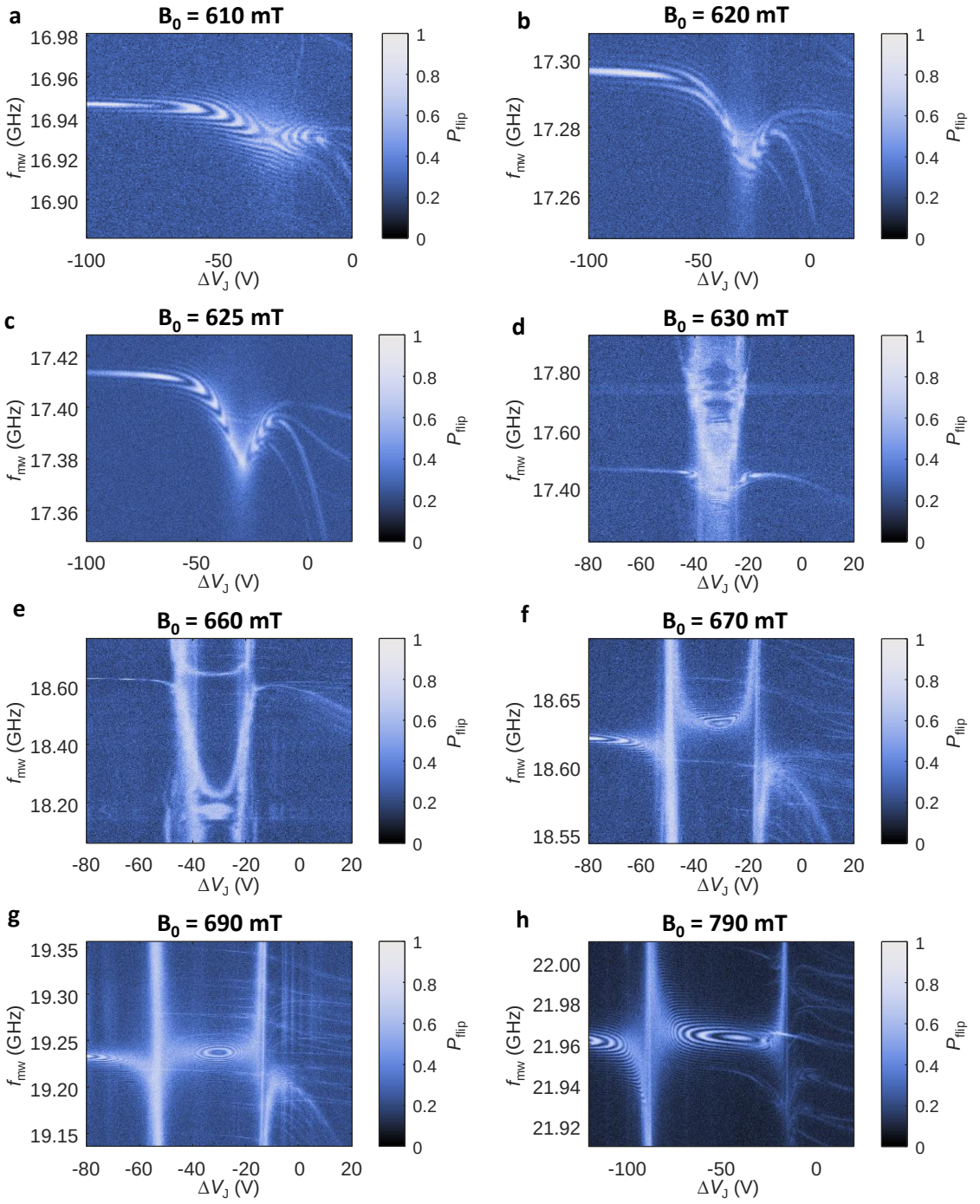

Figure 4.6: Influence of applied magnetic field to degeneracy characteristics a-h, PESOS maps measured in Device D in a (1,1) charge configuration for varying B_0 fields from 610 to 790 mT.

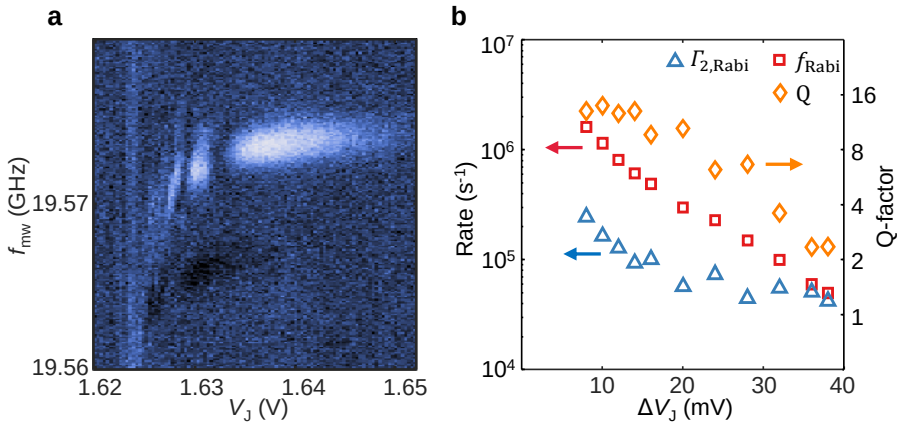

Figure 4.7: Detuning dependence of the Rabi frequency and quality factor a, PESOS map measured in Device D at a B_0-field of 700 mT. A gaussian envelope is used to shape the microwave burst in order to reduce state leakage. **b**, Depending of the Rabi frequency, f_{Rabi}, Rabi decay rate, Γ_2^{Rabi}, and quality factor, Q on the detuning of the J-gate voltage from the degeneracy point, ΔV_{J}.

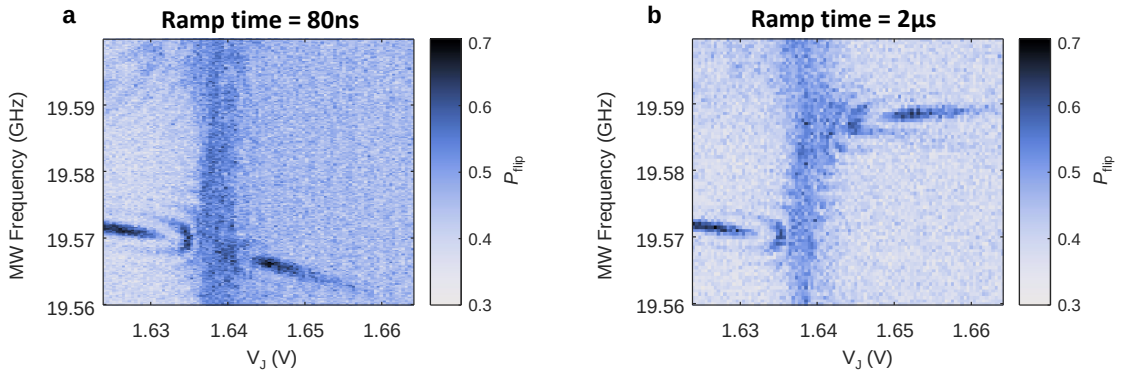

Figure 4.8: Diabatic orbital excitation a, PESOS map in which the ramp time of the J-gate voltage is 80 ns. The resonance frequency continues on a linear trend, indicating that the orbital state is maintained when crossing the point of degeneracy at $V_{\mathrm{J}} = 1.638$ V. **b**, PESOS map in which the J-gate ramp time is increased to 2 μs. The resonance frequency jumps after the degeneracy point, indicating population of a new orbital state via adiabatic passage across the level-crossing.

poorer initialisation fidelity and the appearance of additional transitions, which pollute the two-level nature of the system. Indeed, the small hybridization gap extracted in Figure 4.5j is indicative of susceptibility to the appearance of undesirable diabatic transitions and leakage to the excited orbital as seen in Figure 4.8. However, with careful initialisation strategies and using Gaussian pulses to avoid the leakage of the qubit into undesired excited states, it is possible to achieve PESOS maps with good visibility (Figure 4.7a) and

coherent driving (Figure 4.7b).

4.4.1 Ultra-fast Rabi Oscillations

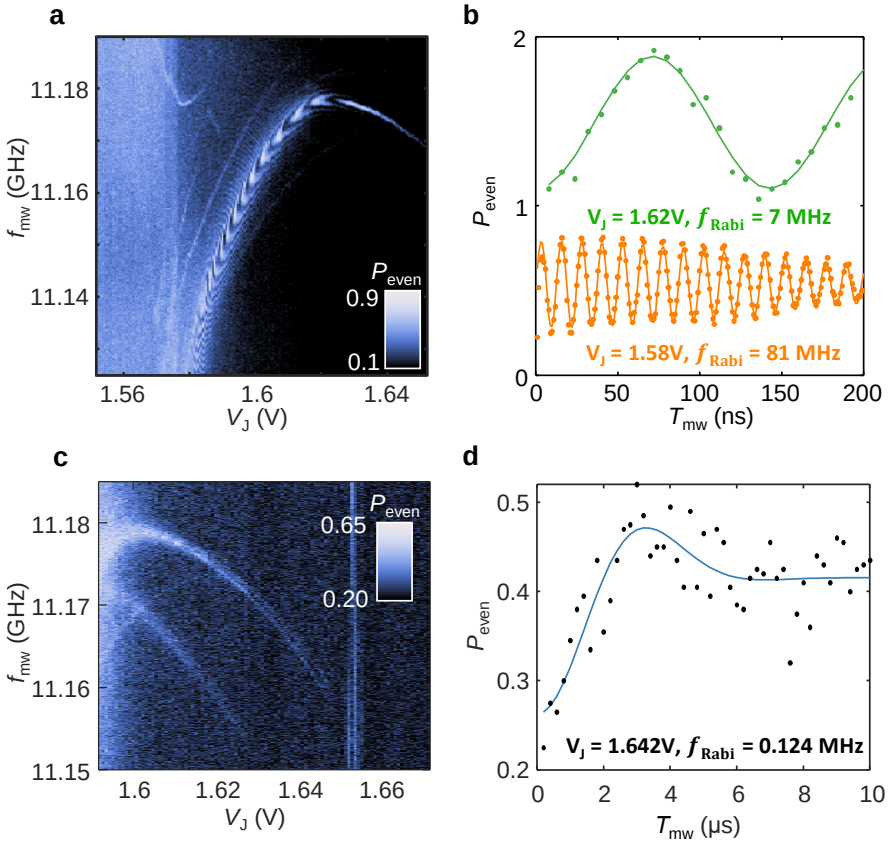

Figure 4.9: Extreme tunability of the Rabi oscillation frequency **a**, PESOS map of device D at an external magnetic field of 400 mT measured with square pulses. At 400 mT the resonance can be tracked until very near the degeneracy point, resulting in an increase in Rabi frequency of almost three orders of magnitude. **b**, Rabi measurements at $V_J = 1.62$ V resulting in 7 MHz oscillations (offset for clarity) and $V_J = 1.58$ V resulting in 81 MHz oscillations. **c**, PESOS map of device D for a larger range in V_J. **d**, Rabi measurement at $V_J = 1.642$ V showing a Rabi frequency of 124 kHz using the same microwave power as for **b**. The Rabi frequency becomes immeasurably low for $V_J > 1.65$ V.

When the B_0-field applied to this device is reduced to $B_0 = 400$ mT we observe an extended range of tunability in the Rabi frequency as seen in the PESOS map in Figure 4.9. Here we observe the largest enhancement in spin-orbit effects and the resulting Rabi frequency across all experiments, reaching $f_{\mathrm{Rabi}} = 81$ MHz close to the degeneracy point, corresponding to a $\pi/2$ qubit rotation in 3 ns (Figure 4.9b, lower curve). The spin-

orbit interaction continues to decrease for increasing V_J, leading to Rabi frequencies $<$ 125 kHz at $V_J > 1.65$ V (Figure 4.9d), recovering the regime of vanishingly small spin-orbit interactions. This translates to an observed on-off ratio for the spin-orbit coupling of ≈ 650. For comparison, we also show the measurement at the point where the Larmor frequency is in first order insensitive to noise in the J gate voltage ($V_J = 1.62$ V), in which the Rabi frequency is $f_{\text{Rabi}} = 7$ MHz (Figure 4.9b, upper curve).

4.4.2 Enhanced Spin Relaxation

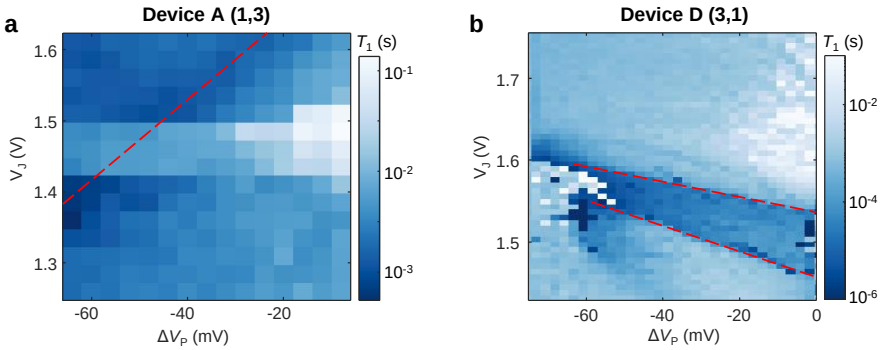

Figure 4.10: Enhanced relaxation rate near level degeneracy The spin relaxation time T_1 measuring across the full target charge configurations for Device A (**a**) and Device D (**b**) in V_J and ΔV_P gate space. The locations of level crossings are indicated as red dashed lines. This shows an enhanced spin relaxation rate near the point of level degeneracy in the respective systems. Interestingly, there are two visible transitions in Device D, between which the spin relaxation is faster than the background, potentially indicating the population of an alternative ground state.

Naturally by enhancing the coupling between ground and excited states of the quantum dot, we also increase the spin relaxation rate, T_1. We characterised this in both devices A and D as shown in Figures 4.10a and b, respectively. Each pixel in these data sets corresponds to a T_1 measurement for that voltage bias configuration. The locations of points with fast relaxation match well with points of enhanced EDSR as in Figure 4.4c and Figure 4.5e. Despite this faster relaxation, it is significantly longer than T_2 and does not limit coherence.

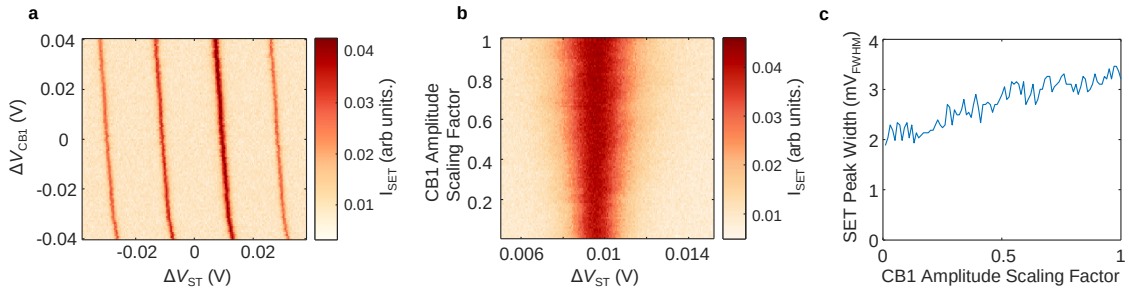

Figure 4.11: Calibration of the microwave excitation amplitude a, Coulomb oscillations of the SET, measured for dependence on the CB1 gate voltage. **b**, SET peak broadening with increasing amplitude of the microwave signal applied to CB1. **c**, Fitted peak widths of the Coulomb peak, using a Full-width-half-maximum threshold.

4.4.3 Microwave Amplitude Calibration

The microwave signal applied to the CB1 gate of Device D is delivered through a transmission line that is poorly characterised for frequencies above 6 GHz. In order to calculate the driving efficiency for the enhanced EDSR, the microwave amplitude is calibrated using a simplified method based on broadening of the conductance peak of the nearby SET.

First, the slope of Coulomb oscillations of the SET are measured relative to the voltages on the sensor top gate and the CB1 gate, which gives a relative lever arm between the two gates of 14.8 (Figure 4.11a). Then, in Figure 4.11b the width of a single Coulomb peak is measured against the microwave amplitude, scaled from a reference level of 0 dBm from the source. The fitted peak width trend in Figure 4.11c gives a maximum amplitude at the CB1 gate of 50 ± 2 mV when multiplied by the relative lever arm. Due to the possibility for a Coulomb peak to also be broadened by local heating effects, or microwave induced charge traps, this calculated amplitude represents an upper bound, and it may be significantly smaller.

4.5 Benchmarking the Fidelity of Electrical Drive

For the remaining experiments of this chapter, we tune device D to an alternative bias point in the (1,3) charge configuration with microwave drive applied to the CB1 gate.

This configuration yields a degeneracy point with strong spin-orbit effect in a region with only a weak voltage dependence on the qubit Larmor and Rabi frequencies (Figure 4.12a), making the qubit substantially more resistant to noise. In Figure 4.12b we take the same PESOS map with microwave drive applied to the J-gate and observe minimal change in resonance characteristic, suggesting minimal angular dependence. In this configuration we measure substantially higher quality factors for Rabi oscillations, in the range of 40-60, with one example in Figure 4.12c which has a Q of 57.

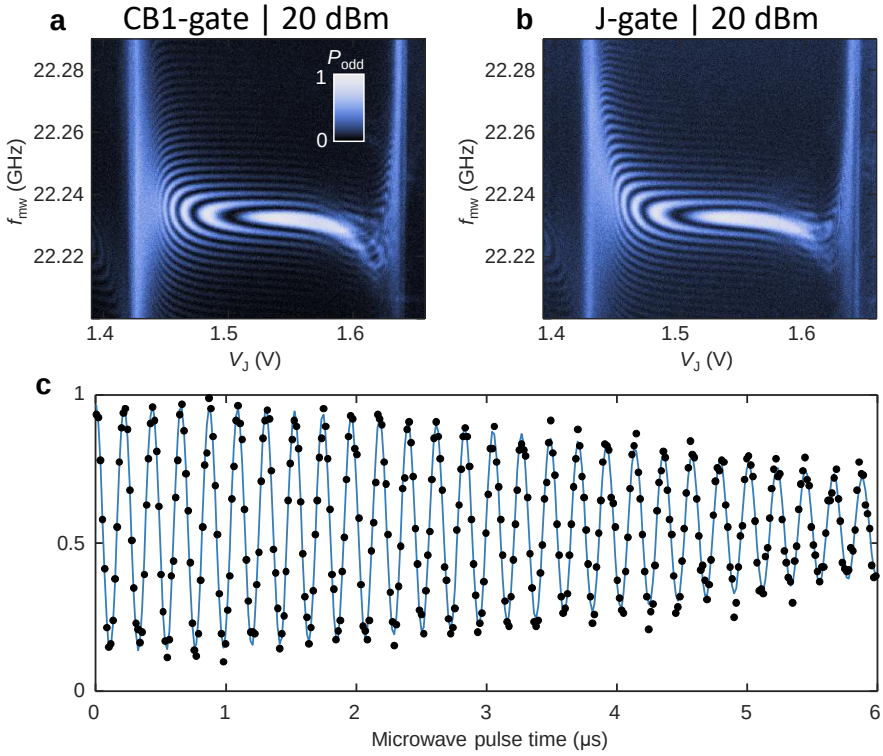

Figure 4.12: PESOS and Rabi oscillations at a high-fidelity point a, PESOS map acquired with microwave drive applied to the CB1 gate. **b**, PESOS map acquired with microwave drive applied to the J-gate. Both **a** and **b** use the same source power of 20 dBm, however variation in line losses due to different electronics may result in differences in electric field amplitude applied to the CB1- and J-gates. **c**, Rabi oscillations driven via the J-gate with an oscillation frequency of $f_{\text{Rabi}} = 4.6$ MHz, and a quality factor of 58.

A unique feature of this driving method is the dependence of the Rabi frequency on the dot potential. Because of this dependence, charge noise can cause variation in the Rabi frequency leading to under or over rotations of the qubit. To combat this we employ a feedback technique that measures the spin flip proportion after a number of $\pi/2$ X pulses.

The effectiveness of this is seen in Figure 4.13a and b, where a discretised Rabi oscillation is noisy and stabilised when the feedback step is implemented or not, respectively.

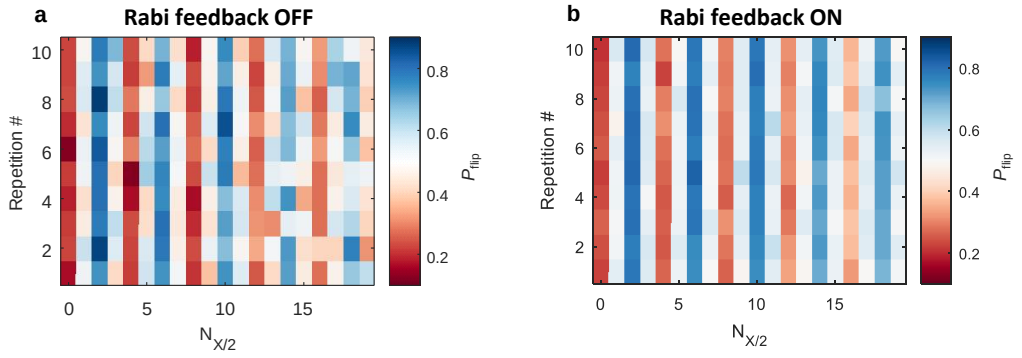

Figure 4.13: Rabi Frequency Compensation. **a** and **b** show Rabi oscillations discretised into $\pi/2$ rotations and repeated 10 times to observe instability, with Rabi frequency feedback on, and off, respectively. The feedback protocol measures P_{flip} for 5, 7, 9, and 11 $\pi/2$ pulses, each of which should result in a 0.5 flip proportion in the ideal case. It then applies a correction to the microwave amplitude of $\delta A_{\text{MW}} = -gain * [P_5 - P_7 + P_9 - P_{11}]$, where P_n is the measured spin flip proportion after n $\pi/2$ rotations.

We then assess the single qubit gate fidelity in this configuration via randomised benchmarking on the Clifford set [167], achieving a 99.93% elementary gate fidelity as shown in Figure 4.14a, well above the threshold for error corrected fault tolerance [10]. Additionally we assess the fidelity of the individual elementary gates using Gate Set Tomography [168] shown in Figure 4.14b resulting in average fidelities of 99.64%, 99.79% and 99.80% for the I, X, and Y gate, respectively.

When benchmarking single qubits, errors from dephasing during idling are minimal thanks to the constant driving and echoing, with idling identity gates consisting of a very small portion of all possible Clifford gates. However, in multi-qubit protocols it is most often necessary for qubits to remain idle for higher proportions of operation time (such as during the readout of ancillas in an error correction protocol), leading to significant dephasing errors [22–24]. Coherence times T_2^{Hahn} and T_2^* for this driving mode are limited by the usual sources of decoherence, such as charge noise coupling through Stark shift, and magnetic noise from nearby ^{29}Si nuclear spin, but also the level of enhanced spin-orbit effect close to a degeneracy point.

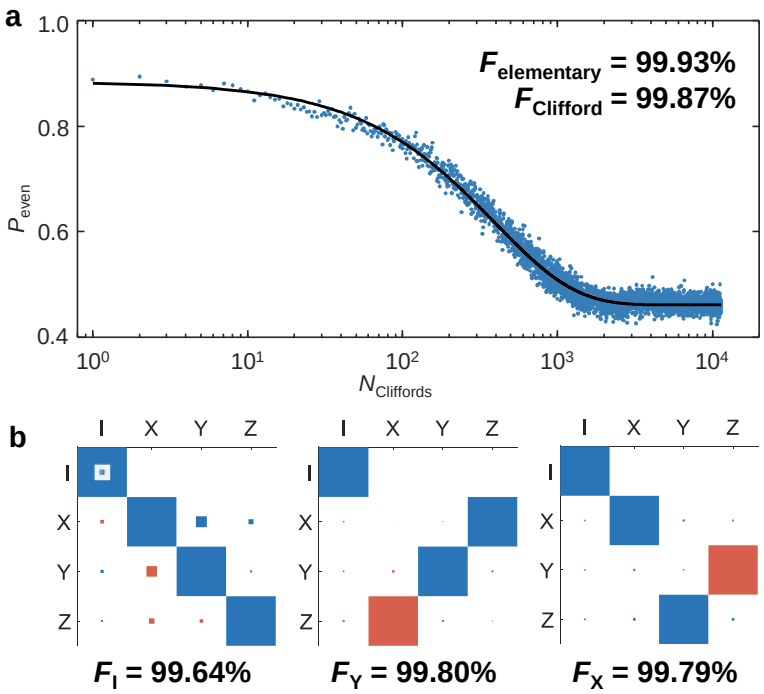

Figure 4.14: Qubit fidelity and errors The device is configured to achieve a high-quality single qubit and benchmarked using standard techniques. **a**, Measurement of single qubit gate fidelity via randomised benchmarking on the Clifford set. The average elementary gate and average Clifford gate have 99.93% and 99.87% fidelity, respectively. **b**, The fidelity and errors associated with the individual elementary gates are characterised with gate set tomography. Projected populations are displayed as areas, with blue and red representing positive and negative polarity. Concentric squares in the top-left position of the first panel represent populations of 1.0, 0.1, 0.01, and 0.001.

The coherence times for different values of ΔV_J are assessed using the pulse sequences in Figures 4.15a and c for T_2^* and T_2^{Hahn}, respectively. In these sequences we always perform X rotations at a fixed control point, but change the bias point during the wait times to assess the decoherence rate. To assist with data processing, a 10 MHz virtual frequency shift is applied to the Ramsey sequence. The raw data for the experiments based on these sequences is plotted in Figures 4.15b and d, and fitted to extract the coherence times, shown in Figure 4.15e.

The coherence times show dependence on detuning from the degeneracy point, as expected, and range from $T_2^{Hahn} = 50$ μs far from the degeneracy to well below 1 μs near the degeneracy. The free induction time T_2^* ranges from 3.5μs to below 100 ns. This encourages the possibility of using the protocol described in Figure 4.3a to extend the qubit lifetime

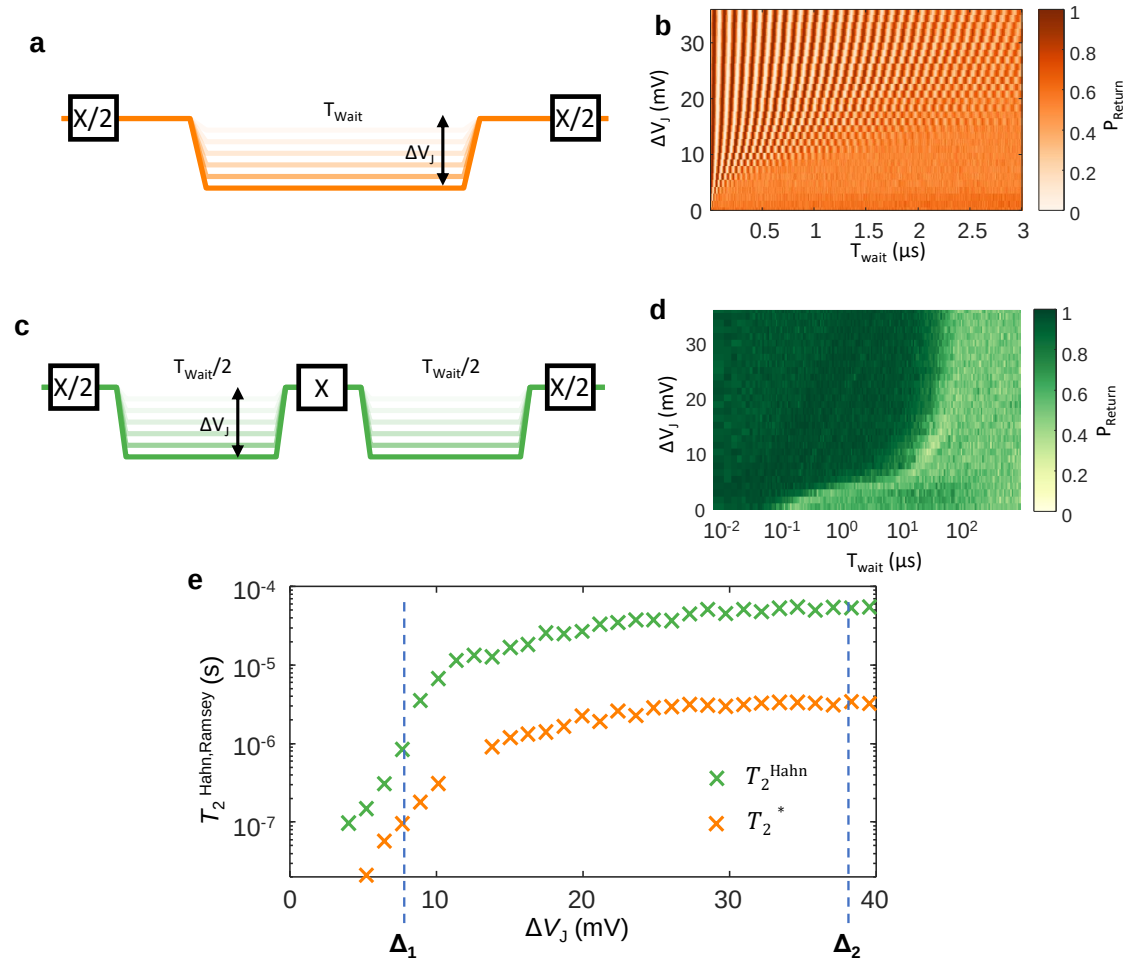

Figure 4.15: Qubit coherence and detuning dependence **a**, Altered Ramsey pulse sequence in which the wait time T_{Wait} is conducted with a bias ΔV_{J} is applied to J. **b**, Coherent Ramsey oscillations for the sequence in **a**. A virtual phase is added to the second X/2 pulse to aid data processing and fitting. **c**, Altered Hahn echo pulse sequence with offset wait times (as in **a**). **d**, Measured data for the pulse sequence in **c**. **e**, Fitted T_2^{Hahn} and T_2^* coherence times with vary detuning in J-gate voltage from the degeneracy point. Δ_1 and Δ_2 show control OFF and ON points respectively, used for switching experiments to follow.

whilst idling. To assess the viability of this we construct benchmarking experiments aimed at measuring the fidelity of a switching operation between points ON- and OFF-points, which we label Δ_1 and Δ_2 and mark as dashed blue lines in Figure 4.15e.

To isolate the error associated with the switching operation, we construct pulse sequences (see Figure 4.16a,b) in which the total sequence time is constant for all values of N_{cycles}, to remove the effect of static decoherence from the result. To do this, a variable wait time,

T_{wait}, is added, which scales down with increasing N_{cycles} to keep total time constant. Here, the duration of each cycle is 80 ns, which is made up of two 20 ns ramps, each followed by 20 ns settling times. For the sequence in Figure 4.16a, all of the added wait time is done at the Δ_2 bias point, far from the degeneracy, whereas for the sequence in Figure 4.16b, the wait time is the same in points Δ_1 and Δ_2. An additional virtual phase is added before the final X/2 pulse and swept to cause oscillations in the result to directly probe the remaining coherence (raw data shown in Figure 4.16c).

We observe an exponential decay in return probability for sequence **a**, corresponding to an average error for a round-trip switching cycle of 0.65%, as shown in Figures 4.16d,e. We expect that the dominant source of error for the switching process is the accelerated decoherence in the ON-state, Δ_1, as the total time spent at this point increases with N_{cycles} for sequence **a**. To test this claim, we run sequence **b**, in which the time spent at the Δ_1 point remains constant. For these tests we see a greatly reduced return probably since it required a long time spent at Δ_1 for all values of N_{cycles}. However, we are able to extract meaningful data, seen in Figure 4.16d. These data exhibit no apparent decay in coherence for increasing N_{cycles}, suggesting that indeed the main source of error is accelerated decoherence near the degeneracy point, rather than any error directly attributed to the bias ramps and consequence dot deformation dynamics.

To integrate such a protocol within a multi-qubit system, a time penalty must be payed to run the ramps associated with each switching cycle. This has to then be weighed up against the potential gain from a reduced decoherence rate for the time a qubit must remain idle. Considering that in this case a switching cycle takes only 80 ns, compared to typical gate times of between 0.1-1 μs for silicon electron spin qubits (during which some qubits must idle) we believe this strategy may provide considerable benefit in most scenarios.

4.6 Outlook

Entering a new realm of ultra-fast single spin control creates new questions regarding the physics of these systems and their application for quantum information processing. For example, the dominant source of control errors for this resonance method are unknown. Pulse engineering for magnetically driven spin qubits in similar devices have led to significant improvements in control fidelity, achieving error rates below 0.05% [40]. However, these strategies can only be translated to the electric driving approach discussed here once the sources of error are well understood and characterised.

Another question left open in our analysis is in regard of the controllability of the hybridization gap. Comparison of the spin-orbit effect in all four devices investigated here creates confidence on the ubiquity of this phenomenon. Hence, its applicability as the main control strategy for qubit devices depends on the regularity of the resulting EDSR speed-up and dependability on being able to shape the orbital hybridization gap in accordance with one's needs.

Switchability of the electrical dependency allows us to tackle one of the most cumbersome aspects of quantum information, which is that the addressability of a qubit often must be traded off against its noise resilience. This allows us to turn on the degeneracy for control and turn it off to harvest the long intrinsic coherence of Si qubits while idling. This prospect comes with the cost of an additional characterisation step for the quantum processor to achieve this degeneracy. Hence, from the scalability perspective it is crucial to further understand how to achieve this degeneracy in a consistent way in a given dot. We believe that the consistency of achieving this degeneracy in four different devices already in this first demonstration gives confidence that a consistent method is achievable and we anticipate more experiments and theoretical work in this direction in future.

We emphasise that enhanced electric driving of the spin is merely one consequence of the ability to controllably create hybridised wavefunctions with coherent spin states. Extensions of this result could lead to strategies to couple spins to photons [60, 169], as well as

lead to long-range two-qubit gates via spin-dependent electric dipolar coupling, similar to strategies such as the Rydberg gates [170, 171] and Mølmer-Sørensen gates [172], previously demonstrated in atomic qubits, or predicted for electron-nuclear flip-flop qubits in silicon [173].

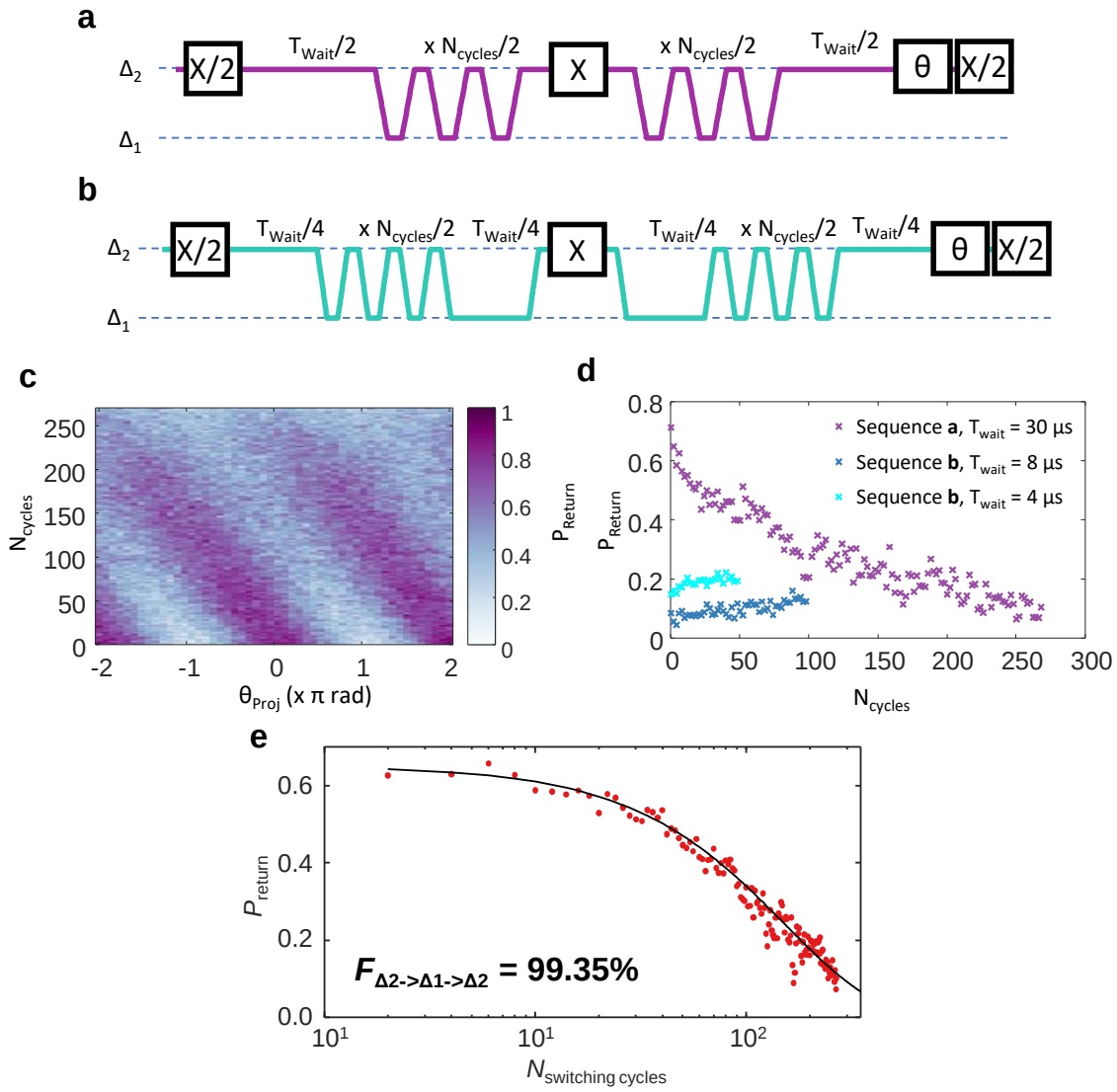

Figure 4.16: Assessment of the switching fidelity for on-demand control a, Coherent switching pulse sequence. The qubit is switched N_{cycles} times between two bias points Δ_1 and Δ_2, being close to and far from the degeneracy point respectively. A virtual Z-phase is added before the final X/2 pulse. In addition to this, a variable time T_{Wait} is added in order to keep the total time between the two X/2 pulses the same for all values of N_{cycles}. The wait time is only added in the off-state, Δ_1. Each switching cycle uses 20 ns on/off ramps, with a 20 ns pulse settling time at each level. **b**, Coherence switching pulse sequence in which the amount of time spent in each of the states Δ_1 and Δ_2 is kept constant in order to cancel out the effect of fast decoherence near the degeneracy from the switching fidelity calculation. **c**, Measured data using the pulse sequence in **a**, with $T_{\text{Wait}} = 30$ μs. This data is used to calculate the return amplitudes for sequence **a** in **d,e** **d**, Measurement of the return amplitudes for varying N_{cycles} for sequences in **a** with $T_{\text{Wait}} = 30$ μs, and **b** with $T_{\text{Wait}} = 4, 8$ μs. We see that for sequence **b** the baseline return amplitude is reduced, due to the short coherence time at the Δ_1 point, however there is no observable coherence decay associated with increasing N_{cycles}. **e**, Switching fidelity assessment using the pulse sequence in **a**. The fitted curve corresponds to a round-trip switching fidelity of 99.35%.

Chapter 5

Conclusion

The work presented in this thesis was conducted with the goal of advancing progress towards creating a useful quantum computer. The studies undertaken, whilst varied in their approach, have each identified new techniques and technologies for scaling silicon quantum dot systems.

In Chapter 2 an alternative to the bias-tee was found that could allow for a continuous control bandwidth from DC to near 1 GHz. This linearised bias-tee (known amongst the team as a combiner) brings ample bandwidth capability, without the need to AC-couple pulse lines and manage the resulting pulse distortion. The combiner has now become a standard across the research groups of Prof. Andrew Dzurak, and Prof. Andrea Morello, and a key part of the experimental setup for several influential publications [38, 97, 98, 109, 117, 118], as well as the work presented in Chapters 3 and 4. Modifications to the design for cryogenic operation have enabled it to be integrated within the cryostat at the 4 K stage for reduced noise. This advancement also serves as a reminder of the importance of electronics in experimental work, and a motivator for further improvements that may enable advancements in quantum computing in the years to come.

In Chapter 3 the possibility to truly leverage the manufacturing capability of the CMOS industry was investigated. A FD-SOI device fabricated in the 300 mm wafer process line

at CEA-Leti was tested and demonstrated the first ever use of a charge sensor situated in a remote nanowire used to sense a quantum dot array. Using this configuration, a 2×2 quantum dot array was formed and depleted down to the last electron in each dot. The operation of this device showed that $2 \times N$ arrays of quantum dots may implemented without being interrupted by charge sensors which could be a critical enabler for quantum processor architectures. Whilst this study did not lead to the creation of qubits due to low inter-dot tunnel couplings, simulations determined that only modest reductions in device dimensions are required to achieve workable coupling strengths.

The study in Chapter 4 started from a discovery of an abnormal speed-up in Rabi oscillations in a particular bias configuration. The results that followed were taken from multiple devices and experimental setups, and supported by an in-depth theoretical study that has allowed us to understand what could be a totally new way to control spins in quantum processors. By deforming the quantum dot shape we were able to manipulate the dot energy spectrum to create a level degeneracy that dramatically strengthens the spin-orbit effect. Using this technique we drove spin qubits with purely electrical microwave signals, alleviating the need to integrate large antennae or micro-magnets on-chip alongside the qubits. The qubit performance was encouraging, with single qubit gates fidelities exceeding 99.9%, and a Rabi frequency that was tuneable up to 81 MHz, the fastest recorded to-date for electron spins. Additionally, because the level degeneracy is controllable using normal pulses on gate electrodes, the electrical controllability could be switched on and off, potentially enabling both fast qubit drive, and long coherence times within the same shot. The ability to tune spin-orbit coupling demonstrated in this study could enable new ways to couple spins to photons, or implement long-range two-qubit gates using the electric dipole interaction.

The path towards full-scale quantum computers is long, and will require countless new developments. The studies in this thesis raise some questions that may motivate research interest in the near term.

The requirement to apply microwave signals to a gate electrode is now common, either for gate-based readout or for EDSR. One challenge with the electrical setup of these config-

urations is the combination of microwave signals with AWG pulses in baseband, without degrading the quality of both signals. The combiner investigated in Chapter 2 allows for a single line to be used for DC and AWG pulses, which enables an easy combination with a microwave line using a diplexer. However, it is currently not yet demonstrated that gate-based readout can be combined with a DC-GHz pulsing bandwidth, and may require further adaptations to line filtering.

The progress on scaling quantum dot devices is inextricably linked to the fabrication capability that can be realised from full-scale foundry processes. The realisation of devices with hundreds of quantum dot qubits or more requires significant progress in design and operation of devices within the constraints of scalable fabrication. As such there is plentiful opportunity in this area to make progress. A particularly interesting result would be the demonstration of high-fidelity qubits within a truly scalable 2D array.

The realisation of fully electrical control of electron spin qubits could open the doors for many new opportunities. Before this capability can be fully exploited, there is a lot of work to do in further understanding how to reproduce the effect in a consistent manner. We created an model with which we can analyse the characteristic of each level degeneracy, and have shown that the degeneracy characteristic can be tuned by sweeping amplitude of the applied magnetic field. We also hope that further tuning of quantum dot potential profiles will yield consistent results, and expect that the viability of this technique may depend on the particular device and gate arrangements that can be fabricated. Contributions from the wider research field will greatly assist advancing this study.

As the reproducibility of orbital degeneracies is investigated, further physical effects remain to be explored. Firstly, the co-integration of orbital degeneracies with two-qubit gates may be challenging. Changes to the orbital state of a quantum dot can dramatically change the dot coupling to neighbouring dots. While changes to the tunnel coupling can be managed easily enough, changes in the exchange coupling may complicate the implementation of two-qubit gates in systems utilising orbital degeneracies. Instead, it may be possible to use the voltage-tuneable spin-orbit effect to enable long-range two qubit gates using electric dipole coupling, in which case variability in the exchange coupling may not be as critical.

Finally, orbital degeneracies could provide a way to couple spins to photons for the creation of long-range quantum links, without the need to integrate micro-magnets.

Appendix A

Origin of spin-orbit parameters and implications for spin driving

In this Appendix, we explain the analysis of the experimental results and the construction of the four-level model that can be used to describe the transition in qubit frequency between orbitals as well as the speed up in Rabi frequency near the degeneracy points. This modeling protocol will finally allow us to obtain the energy diagrams shown in Fig. 4.5f-j in Chapter 4.

The work in this appendix was done by Mengke Feng, and is included as Supplementary Information in **W. Gilbert**, T. Tanttu, W. H. Lim, M. Feng, J. Y. Huang, J. D. Cifuentes, S. Serrano, P. Y. Mai, R. C. C. Leon, C. C. Escott, K. M. Itoh, N. V. Abrosimov, H-J. Pohl, M. L. W. Thewalt, F. E. Hudson, A. Morello, A. Laucht, C. H. Yang, A. Saraiva, and A. S. Dzurak. "On-demand electric control of spin qubits." *arXiv:2201.06679*, (2022).

A.1 Analysis of PESOS maps

We begin by extracting the key quantities from the PESOS maps shown in Fig. 4.5, which are the qubit frequency, denoted as f_0, and the Rabi frequency, denoted as f_{Rabi}.

We firstly identify which qubit is suspected to have an orbital transition by inspecting qualitative signatures in its PESOS map. The qubit of interest will exhibit both a speed-up in Rabi frequency f_{Rabi} indicated by oscillation patterns for fixed pulse time, and a transition in the qubit frequencies f_0 indicated by a non-linear change in the resonance (non-linear Stark shift). The upper transition in the PESOS map shown in Supp Fig. A.1a is an example. We then take line cuts along the frequency axis (f_{mw}) at separate voltage values (ΔV_{P} in this case) with examples indicated in Supp Fig. A.1a. These line traces are also plotted in blue in Supp Figs. A.1(b-e). These traces are oscillations of P_{even} probabilities and we can fit them according to the following equation,

$$P_{\text{even}} = \frac{A f_{\text{Rabi}}^2 \left[1 - \cos\left(\tau\sqrt{f_{\text{Rabi}}^2 + (f_{\text{mw}} - f_0)^2}\right)\right]}{f_{\text{Rabi}}^2 + (f_{\text{mw}} - f_0)^2} + \delta A, \tag{A.1}$$

where A is the amplitude of the oscillations, f_{Rabi} is the Rabi frequency, f_{mw} is the driving frequency from the microwave source, f_0 is the resonant frequency which can be interpreted as the qubit frequency, τ is the total time of the driving microwave pulse, and δA is a constant shift in the amplitude of the probabilities due to SPAM errors. Fitted traces of P_{even} are plotted in red in Supp Figs. A.1(b-e).

The Rabi frequency f_{Rabi} is plotted in Supp Fig. A.1f along with the fitting error bars. In Supp Fig. A.1g, we superimposed the fitted qubit frequencies f_0 onto the PESOS map, indicating that the qubit frequencies correspond to the center of the oscillations, as expected, and also show that this empirical fitting protocol is of satisfactory accuracy.

Finally, as a demonstration of the capabilities of the fitting protocol, we generate a simulated PESOS map colour coded such that the colours represent the number of π rotations (θ_{R}) that the qubit undergoes. As the Rabi frequency speeds up and slows down again with voltage, the same fixed pulse duration causes more or less qubit rotations (with red representing one π rotation and purple representing 13 π rotations).

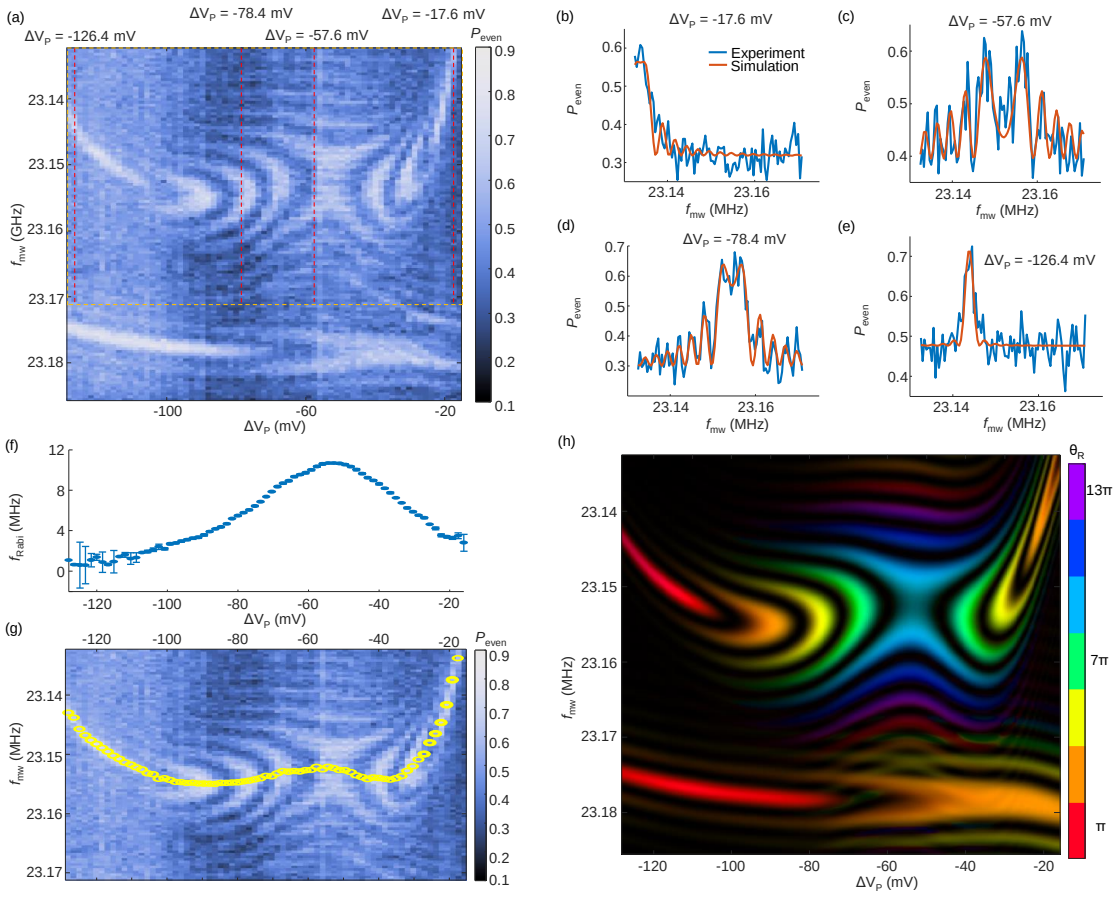

Figure A.1: Rabi frequency fitting. **a**, PESOS map for Device A in the (1,3) configuration. The red dotted lines indicate examples of line cuts. We focus only on the upper transition (outlined by the yellow dotted lines), with a clear speed up in Rabi frequency as well as a transition in qubit frequency. **b-e**, Line cuts of P_{even} oscillations taken at the indicated dotted lines in **a**. Blue traces indicate the experimental data and red traces are the fitted lines based on Eq. A.4. **f**, Extracted Rabi frequency f_{Rabi} as a function of voltage ΔV_{P}. Error bars of the fit are also shown. **g**, Fitted qubit dispersion f_0 superimposed onto a PESOS map. **h**, Simulated PESOS map based on fitted traces shown in **b-e**.

A.2 Four-level model of spin-orbital quasi-degeneracy

We have described how we can obtain a set of parameters for fitting the PESOS maps. From the theoretical point of view, we interpret these parameters based on properties of quasi-degenerate orbitals. Our goal is to find an effective model that captures the qualitative features of the qubit and Rabi frequencies. This will typically involve making conjectures about the degrees of freedom involved in the orbital excitation of a multi-electron state in a quantum dot, estimating the underlying first-principles microscopic Hamiltonian, then extracting the effective two-level system subspace, by a Schrieffer-Wolff transformation for example, that reduces to the phenomenological model.

For this purpose, the simplest model consists of two spin-$\frac{1}{2}$ states with orbital parts designated by A and B, which represent the two different sets of states away from the degeneracy point, *i.e.*, $|A\rangle, |B\rangle$ are the quantum states representing two different valley states, orbital states etc. The use of our model is agnostic to the exact nature of these states and therefore, we will refer to them generally as orbital states for simplicity. We also operate in electronic configurations with a single valence electron, and therefore our system can be described in the basis of $\{|A\rangle, |B\rangle\} \otimes \{|\uparrow\rangle, |\downarrow\rangle\}$. Here, the spin degree of freedom is in general a pseudo-spin due to spin-orbit coupling. The g-factors for both orbitals are typically close to the bulk value in silicon, with small variations of $\approx$0.1% from qubit to qubit and between orbitals due to surface roughness. This implies that the Zeeman splitting $E_{\mathrm{Z}}^{\mathrm{A}}$ will in general be different from $E_{\mathrm{Z}}^{\mathrm{B}}$.

The general form of the desired Hamiltonian is

$$H_0 = \begin{pmatrix} H_{\mathrm{A}} & H_{\mathrm{c}} \\ H_{\mathrm{c}}^{\dagger} & H_{\mathrm{B}} \end{pmatrix} , \tag{A.2}$$

where H_{A} and H_{B} describe quantum subsystems A and B, respectively, far from any degeneracy, and H_{c} describes the coupling between subsystems A and B. Each of these terms (H_{A}, H_{B}, and H_{c}) are 2×2 blocks. For subsystem A,

$$H_{\mathrm{A}} = \left[\frac{1}{2} E_{\mathrm{Z}}^{\mathrm{A}} + \eta_{\mathrm{A}} \left(V_{\mathrm{G}} - V_0\right)\right] \sigma_z ,$$

where $E_{\mathrm{Z}}^{\mathrm{A}}$ is the Zeeman energy of subsystem A and η_{A} is the linear part of its Stark shift (all the non-linearity of the Stark shift in our model stems from the resulting orbital hybridization near the degeneracy point), V_{G} is the gate voltage, and σ_z is the Pauli z operator acting on the spin basis $\{|\uparrow\rangle, |\downarrow\rangle\}$. The definition of the reference voltage V_0 is discussed next. For subsystem B,

$$H_{\mathrm{B}} = \left[\frac{1}{2}E_{\mathrm{Z}}^{\mathrm{B}} + \eta_{\mathrm{B}}\left(V_{\mathrm{G}} - V_0\right)\right]\sigma_z + \alpha_{\mathrm{rel}}\left(V_{\mathrm{G}} - V_0\right)\mathbb{1}\ ,$$

where the Hamiltonian takes on a similar form to that for subsystem A, except with the corresponding parameters for B and the additional term describing the effect of the gate voltage on the energy separation between orbitals.

We model the effect of a gate with voltage V_{G} bringing $|\mathrm{B}\rangle$ into alignment with $|\mathrm{A}\rangle$ by adding the term $\alpha_{\mathrm{rel}}(V_{\mathrm{G}} - V_0)\mathbb{1}$ to H_{B} where α_{rel} is the differential lever arm between $|\mathrm{A}\rangle$ and $|\mathrm{B}\rangle$. Here, the definition of V_0 becomes clear – it is the voltage bias at which the two states A and B would be degenerate (which gets slightly shifted in the presence of a difference in Zeeman splitting). Finally, the last term in Eq. A.2 is one that describes the coupling between $|\mathrm{A}\rangle$ and $|\mathrm{B}\rangle$, which sets the energy gap at the anticrossing,

$$H_{\mathrm{c}} = \begin{pmatrix} \Delta + \Delta_{\mathrm{sd}} & \Delta_{\mathrm{sf}} \\ \Delta_{\mathrm{sf}} & \Delta - \Delta_{\mathrm{sd}} \end{pmatrix}\ ,$$

Here, Δ is the spin-independent coupling rate between $|\mathrm{A}\rangle$ and $|\mathrm{B}\rangle$. The presence of spin-orbit coupling creates a spin-dependent coupling term Δ_{sd}, as well as a spin-flip coupling Δ_{sf}. The existence of both spin-conserving and spin-flip terms stem from the non-alignment of the qubit quantization axis with the crystallographic axes of the device, as well as the reduced symmetry due to interface roughness. This will be shown explicitly in Section A.5. Note that a σ_y term in H_{c} is not necessary for fitting the qubit frequency because it only produces a phase shift in the transverse coupling - but it may be important for fitting Rabi frequencies, as will be explained in section A.5.

Therefore, the full Hamiltonian in the basis of $\{|\mathrm{A}\rangle, |\mathrm{B}\rangle\} \otimes \{|\uparrow\rangle, |\downarrow\rangle\}$ is

$$H_0 = \begin{pmatrix} \frac{1}{2}E_Z^A + \eta_A v & 0 & \Delta + \Delta_{sd} & \Delta_{sf} \\ 0 & -\frac{1}{2}E_Z^A - \eta_A v & \Delta_{sf} & \Delta - \Delta_{sd} \\ \Delta + \Delta_{sd} & \Delta_{sf} & \frac{1}{2}E_Z^B + (\eta_B + \alpha_{rel})\, v & 0 \\ \Delta_{sf} & \Delta - \Delta_{sd} & 0 & -\frac{1}{2}E_Z^B - (\eta_B - \alpha_{rel})\, v \end{pmatrix} \tag{A.3}$$

where $v = (V_G - V_0)$.

As we have described, this model works for arbitrary orbital states $|A\rangle$ and $|B\rangle$, and provides the theoretical basis for predicting both the change in qubit dispersion from one orbital to another, and the speed-up in Rabi frequency f_{Rabi} near the degeneracy point. These are the two key quantities that we will calculate using the model, and fit to the experimental results.

To calculate the qubit dispersion, we first diagonalize the Hamiltonian numerically for a given set of parameters, which outputs the eigenenergies of the system. We then consider the energy difference between the lowest spin up and spin down states ($f_0 = E_\uparrow - E_\downarrow$), which is also the first excitation energy, as the qubit frequency. Generally for a large orbital coupling (for example in the cases of Supp Fig. A.2l-n), the ground and excited orbital energies are well separated and the qubit frequency is also the difference in energy between the two lowest energy levels. In the case where the orbital coupling Δ is smaller than the Zeeman energies E_Z^A and E_Z^B, there are multiple degeneracy points (for example in Supp Fig. A.2o) and there is a need to track the lowest energy spin up state which changes in its ordering with detuning.

The second fitting parameter is the Rabi frequency, which is a function of detuning and is determined by,

$$f_{Rabi} = |\langle e|\, H_{AC}\, |g\rangle| \tag{A.4}$$

where $|g\rangle$ and $|e\rangle$ are respectively the ground and excited states. Again, in the case where the orbital coupling is lesser than the Zeeman energy (Supp Fig. A.2o), it becomes necessary to track the states so that the Rabi frequency is always calculated between spin

up and down states. The driving Hamiltonian, H_{AC}, is defined as

$$H_{\mathrm{AC}} = \Omega_{\mathrm{AC}} \cdot \sigma_x \otimes \sigma_x \ , \tag{A.5}$$

where Ω_{AC} is the magnitude of the spin-flip modulation resulting from the driving microwave pulse on the qubit.

A.3 Fitting Procedure

Now, we have all the ingredients necessary to perform the fit, and we perform a non-linear least-squares fit of both the Rabi frequencies and the qubit dispersion simultaneously. The cost function in this minimization procedure is defined as

$$f_{\mathrm{cost}} = \sum (f_{\mathrm{model}} - f_{\mathrm{PESOS}})^2, \tag{A.6}$$

where f_{model} and f_{PESOS} refer to the quantities obtained from the four-level model and extracted from the PESOS maps respectively. They include both the qubit dispersion f_0 and Rabi frequency quantities f_{Rabi}.

From this point, the fitting procedure works to vary the parameters of the Hamiltonian as defined in Eq. A.3, such that we minimize the cost function as shown in Eq. A.6. We summarize the protocol as follows,

1. Begin with an initial guess of the Hamiltonian parameters. This is an educated guess based on what we know of the system and does not have to be strictly accurate. How we can begin to guess at these quantities will be explained in the following sections.

2. Using the *lsqcurvefit* function in MATLAB, we input the Hamiltonian parameters necessary for calculating f_0 and f_{Rabi} from the model, which will be compared with the target values previously obtained from the fitting to the Rabi equation. We also set upper and lower bounds to the fitting parameters of the Hamiltonian within the orders of magnitude that are expected.

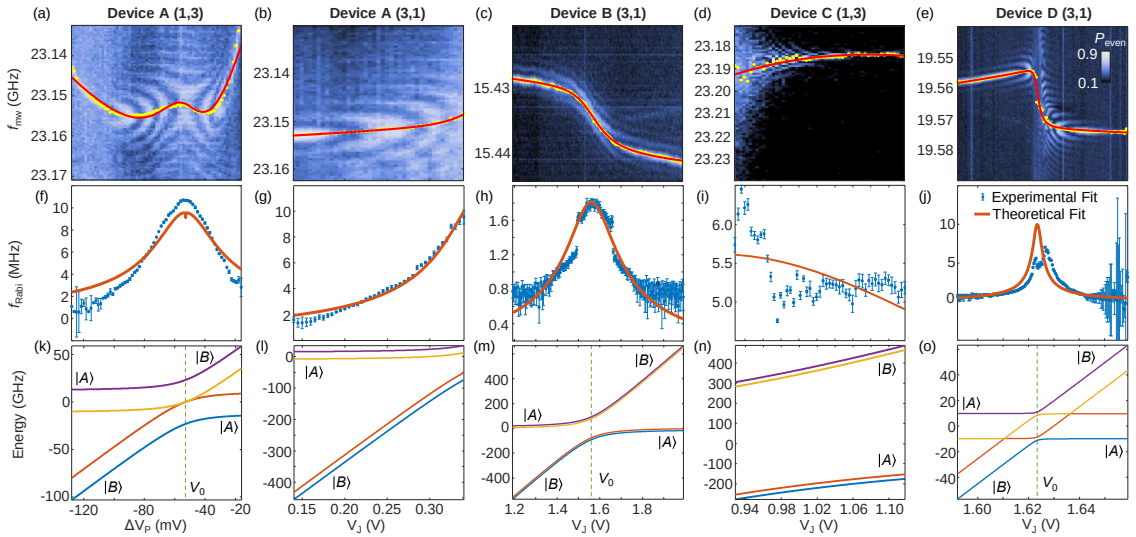

Figure A.2: Four-level model fit. a-e, PESOS maps with both the fitted center frequency f_0 (yellow dots) and the fitted qubit dispersion from the four-level model (red lines). We show here only the relevant qubit of study. **b-j**, The extracted Rabi frequencies f_{Rabi} from the fitting to the PESOS map and the fitted Rabi frequencies from the four-level model. We note that for **j**, the error bars extend below $f_{\text{Rabi}} = -5$ MHz but are not shown here in order to highlight the actual range of Rabi frequencies. Both the positive and negative error bars are of the same magnitude. **k-o**, The resultant four-level energy diagram from the fitted parameters.

3. The output from this fitting procedure are the parameters of the Hamiltonian. The fit results are summarized in Table A.1.

The results from this fitting protocol are summarized in Supp Fig. A.2.

We plot in Supp Figs. A.2a-e the PESOS maps with both the target (yellow dots) and fitted (red line) f_0 superimposed onto the 2D map. We include here only the qubit of concern, more specifically, only the qubit that shows a significant speed-up in Rabi frequency. Similarly, in Supp Figs. A.2f-j, we plot the Rabi frequencies within the same voltage range as the PESOS maps, with the blue dots representing the target values of Rabi frequency which are obtained in the same way as shown in Supp Fig. A.1f, and the red line being the fitted Rabi frequencies from the four-level model. We note that there are large errors in the Rabi frequency fit for extreme values of V_J in Supp Fig. A.2j due to a reduction in the visibility of the Rabi oscillation peaks associated to the reduction in coherence. Finally, using these fitted parameters, we can diagonalize the Hamiltonian

and obtain the eigen-energies as a function of the voltage as shown in Supp Figs. A.2(k-o), similarly to Fig. 4.5. The anticrossing for the transition from one orbital to another is indicated as a green dashed line and labeled by V_0, except in the case of Supp Fig. A.2l,n, where the anticrossing is out of the plotted range. The expected dominant state (either $|\mathrm{A}\rangle$ or $|\mathrm{B}\rangle$) is also labeled, with the energies of $|\mathrm{B}\rangle$ shown to be changing significantly with gate voltage.

In the rest of the section, we will explain in detail the parameters involved in the fitting. There are many parameters involved in the construction of the Hamiltonian as shown in Eq. A.3, and in order for accurate and efficient fitting, it is necessary for us to consider the real system and reduce the number of degrees of freedom that we have to deal with. Of the many parameters that define the Hamiltonian, there are two of them which we fix in all the devices, those are the differential lever arm, α_{rel} and the anticrossing position in voltage, V_0.

The position of the anticrossing can be read directly from the voltage position of the Rabi frequency peak assuming a singular peak, as shown in Supp Figs. A.2f-j, and therefore can be readily confirmed without fitting. Test fits can also be performed to empirically guess the position of the anticrossing in cases where the anticrossing may not be obvious, like in Supp Figs. A.2g,i.

On the other hand, to determine the differential lever arm α_{rel} requires time-consuming additional measurements, for example, excited state magnetospectroscopy (Fig. 4.2), which was only performed for device A in the (1,3) charge configuration. For fitting purposes, we take all the α_{rel} to be on the same order of magnitude as obtained in device A. It is not possible to independently obtain the differential lever arm, α_{rel}, and the inter-orbital coupling, Δ, directly from Supp Figs A.2a-e, only their ratio $\alpha_{\mathrm{rel}}/\Delta$.

The other fitting parameters comprise the inter-orbital coupling Δ, the spin-orbit couplings Δ_{sd} and Δ_{sf}, the constant offset in frequency c, the difference in qubit frequencies between orbitals ΔE_{Z}, the linear Stark shifts of each orbital $\eta_{\mathrm{A/B}}$, and finally the amplitude of the electric driving Ω_{AC}. We note that not all of these parameters will necessarily be used

for fitting. In particular, the Stark shifts are generally only used where we can observe the linear Stark shift regions in the PESOS maps. For example, in the case of device B and D (Figs. A.2c,e), we observe clearly the linear regions of the qubit dispersion and that allows us to fit the linear Stark shift terms well. In the case of the other devices, where we typically observe only one side of the qubit dispersion, we either fit only one of the Stark shift terms for simplicity (in the case of Fig. A.2a,b) or none at all (in the case of Fig. A.2d). In these cases, having the linear Stark shift term $\eta_{\mathrm{A,B}}$ in the model can introduce an additional degree of freedom which negatively impacts the fit result.

Similarly, the amplitude of electric driving Ω_{AC} is in general required as an additional fitting parameter, except in the case of device D, where we experimentally estimate the AC voltage amplitude based on the impact of a microwave pulse on current profile of the device SET (shown in Figure 4.11).

The parameter c is treated as a free parameter to account for any constant offsets in the PESOS maps due to SPAM errors. We also have ΔE_{Z} accounting for differences in Zeeman energies, which is typically on the order of tens of megahertz.

Finally, we have the spin-orbit coupling parameters, which are the spin-dependent and spin-flip coupling terms respectively (Δ_{sd} and Δ_{sf}). While these parameters are in general different, they are expected to be on the same order of magnitude. For the ease of fitting, we have them to be equal in magnitude in our model. The detailed justification for this will be given in the next section.

The primary result from the fits are the energy diagrams. The four-level model provides a reasonable description of the experiments for parameters extending across a few orders of magnitude. Not all parameters are uniquely set by this model due to either large uncertainties or weak dependence of the experimental results on certain parameters. However, the extracted parameters do lie within the expected bounds from either previous independent experiments or first principles calculations in the literature. The extracted magnitude of the electric drive corresponds to the maximum Rabi frequency shown in Figs. A.2(f-j). The difference in qubit frequencies are on the order of tens of megahertz

(Table A.1) as expected for our devices [109, 174–176]. For device C, the larger difference in g factors resulting in a ΔE_{Z} one order of magnitude larger than the rest could be due to the two orbitals having different shapes, such that the surface roughness along the interface impacts them in significantly different ways. The Stark shifts $\eta_{\mathrm{A,B}}$ range from a few MHz/V to hundreds of MHz/V. The lower bound is typical for dots without orbital degeneracy [109, 174], while the higher Stark shifts can be understood in terms of the sudden transition between $|\mathrm{A}\rangle$ and $|\mathrm{B}\rangle$. Confirming the physical significance of the remaining parameters Δ and $\Delta_{\mathrm{sd/sf}}$ requires a model of the orbitals involved, which we develop in the next section.

A.4 Microscopic Origin of Δ

The parameter Δ in our model describes how the orbitals A and B are *coupled* to each other. Examples could include the case where A and B represent the s and p orbitals in an approximately harmonic confinement potential, in which case Δ stems from any small anharmonicity. Another example would see p_x and p_y states coupled through quadrupolar deformation of the dot. Often the two orbitals will also have a different valley composition, which means that the precise estimation of Δ is limited by atomistic disorder that might affect the valley structure of the dot [44, 177–181].

To explore the full capabilities of this formalism, it would require knowledge of the microscopic details of the quantum dot, making this calculation impractical. While it remains possible to infer information about the anti-crossing from Δ, there is in fact a caveat here in this case, that is the interplay between Δ and the differential lever arm α_{rel} means that to draw any meaningful conclusions, an independent measurement of α_{rel} is required as already discussed.

As such, we will only comment on device A in the (1,3) configuration because α_{rel} has been measured independently here. We first note that the measured $\alpha_{\mathrm{rel}} = 1200$ GHz/V $\approx 5/h$ meV/V as shown in Fig. 4.2b. suggests that the observed pair $|\mathrm{A}\rangle, |\mathrm{B}\rangle$ are orbital

states rather than valley states which have a α_{rel} about an order of magnitude smaller ($\alpha_{\text{rel}} \approx 0.6/h$ meV/V in ref. [44]). This accords with the fact that pairs of valley states typically do not differ much in charge distribution [182], whereas different orbital states do.

The extracted $\Delta = 12 \pm 1$ GHz $\approx (50 \pm 4)/h$ μeV, as shown in Table A.1, is quite small and suggests that the avoided crossing is set mostly by valley-orbit coupling. To see this, we first note that we usually observe valley splittings E_{vs} in the order of hundreds of μeV [44]. Under the effective mass approximation (EMA) formalism, the valley-orbit splitting can be written in general as [183]

$$E_{\text{vo}} = 2\left|\langle A| \, e\phi(\mathbf{r}) \, |B\rangle\right| \tag{A.7}$$

Normally for E_{vs} (inter-valley, intra-orbital), A and B have approximately the same envelopes leading to a large overlap. We now apply the same calculation but now taking A and B to have different envelopes as justified earlier. The lower overlap results in a lower valley-orbit coupling (inter-valley, inter-orbital). So it is not unreasonable that Δ is an order of magnitude smaller than E_{vs}. Thus, this analysis suggests that $|\text{A}\rangle, |\text{B}\rangle$ are different orbital states (having different orbital shapes) that occupy different valleys, and the change in gate voltage allows for transitions between the orbital states. This explanation is natural for the case of dots occupied by three electrons if the shell and valley structure of the dot are well preserved across the different occupation numbers.

A.5 Origin of Δ_{sd} and Δ_{sf}

The coupling terms Δ_{sd} and Δ_{sf} arise from spin-orbit coupling. To see this, we start with the spin-orbit coupling Hamiltonian, which reflects the relatively low symmetry of the rough Si/SiO_2 interface [174, 175, 184]

$$H_{\text{SO}} = \alpha \underbrace{\left(\sigma_{\bar{x}} k_{\bar{y}} - \sigma_{\bar{y}} k_{\bar{x}}\right)}_{h_{\text{R}}} + \beta \underbrace{\left(\sigma_{\bar{x}} k_{\bar{x}} - \sigma_{\bar{y}} k_{\bar{y}}\right)}_{h_{\text{D}}} \tag{A.8}$$

where the Rashba and Dresselhaus Hamiltonians (h_{R} and h_{D} respectively) are scaled by the corresponding coefficients α, β. The effect of inter-valley spin-orbit coupling is integrated into these coefficients in our analysis. The operators here $\boldsymbol{\sigma}, \mathbf{k}$ are defined according to the underlying crystallographic axes, which are represented with bars over x, y and z to underscore that they refer to [100], [010] and [001] directions. These directions are not necessarily aligned with either the dot symmetry axes or the external magnetic field, such that both terms may play a role on spin-dependent and spin-flip coupling. In our experiments, for instance, the dots ideally have an approximate mirror symmetry about the [110] direction and an external magnetic field applied along the $[1\bar{1}0]$ direction, which would mean that Rashba and Dresselhaus effects participate equally in Δ_{sd} and Δ_{sf}. In reality this scenario is further complicated by the presence of interface roughness, which in the case of amorphous thermal Si/SiO_2 (001) interfaces has no particular crystallographic structure. This means that A and B orbitals may well have no special symmetry.

Only in fortuitous cases Δ_{sd} and Δ_{sf} would differ by a large factor. In most cases, the approximation $\Delta_{\mathrm{sf}} = \Delta_{\mathrm{sd}}$ is quantitatively acceptable. Qualitatively, this equality might introduce artificial symmetries to the Hamiltonian, such that an analysis of the impact of this approximation is warranted for any predictive analyses.

A.6 Estimating Δ_{sd} from spin-orbit coupling

We now turn to estimating the magnitude of Δ_{sd}. To find the matrix element $\langle \mathrm{A}| k_i |\mathrm{B}\rangle$, we first consider the case where $|\mathrm{A}\rangle, |\mathrm{B}\rangle$ are different orbital states, *i.e.*, s and p (we will consider a mixture of orbital states later). Take p along the most elongated axis in an elliptical dot potential (which is the most common case). Assuming harmonic oscillator states gives an analytical expression

$$\langle s|k|p\rangle = -i\sqrt{\frac{m^*\omega}{2\hbar}}. \tag{A.9}$$

Taking a typical orbital splitting of $\hbar\omega = 3$ meV [43,50], we obtain $\langle s|k|p\rangle = -0.06i$ nm^{-1}.

In general, $|\mathrm{A}\rangle, |\mathrm{B}\rangle$ could have mixed orbital character due to the anharmonicity of the

dot or interface roughness. So, denoting r as the proportion of orbital mixing, we could have $|A\rangle = \sqrt{1-r}\,|s\rangle + \sqrt{r}e^{i\varphi}\,|p\rangle$ and $|B\rangle = -\sqrt{r}e^{-i\varphi}\,|s\rangle + \sqrt{1-r}\,|p\rangle$ with the coefficients chosen to preserve orthonormality. Then the matrix element reads

$$\langle A|\,k\,|B\rangle = (1-r)\,\langle s|\,k\,|p\rangle - re^{-2i\varphi}\,\langle p|\,k\,|s\rangle = \langle s|\,k\,|p\rangle\left[(1-r) - re^{-i(2\varphi+\pi)}\right] \tag{A.10}$$

By symmetry of the states, the absolute value $\overline{|\,\langle \mathrm{A}|\,k\,|\mathrm{B}\rangle\,|}$ is symmetric under $r \to (1-r)$ and it is largest when $r = 0$ or 1, giving $\overline{|\,\langle s|\,k\,|p\rangle\,|}$. The lower bound is given when $r = 0.5$. Averaging over the random phase φ, we find that,

$$\overline{|\langle s|\,k\,|p\rangle|} \geq \overline{|\langle A|\,k\,|B\rangle|} \geq \overline{|\langle s|\,k\,|p\rangle|}\;\overline{|0.5 - 0.5e^{-i(2\varphi+\pi)}|} = \frac{2}{\pi}\overline{|\langle s|\,k\,|p\rangle|} \approx 0.64\overline{|\langle s|\,k\,|p\rangle|} \tag{A.11}$$

which shows that $\overline{|\langle \mathrm{A}|\,k\,|\mathrm{B}\rangle|}$ does not depend strongly on the amount of orbital mixing r and is always roughly the same order of magnitude.

A similar analysis may be performed for the case of p_x and p_y dots, in which case the direct transition induced by the vector $\{k_i\}$ is forbidden, but in second order it is allowable through the virtual coupling to d orbitals.

We should also consider the case when $|\mathrm{A}\rangle, |\mathrm{B}\rangle$ have different valley compositions, which is the most common case for very flat interfaces (energy levels ordered by valley splitting). Within the EMA formalism and only including the Bloch phase factor, the states appear approximately as $\psi_{\mathrm{A/B}}(\mathbf{r}) = F_{\mathrm{A/B}}(\mathbf{r})e^{\pm ik_0 z}$ where $F_{\mathrm{A/B}}$ is the envelope and the valleys occur at $\mathbf{k} = \pm(0,0,k_0)$, with $k_0 = 0.852\pi/a_0$. The matrix element becomes ($j = x, y$)

$$\langle A|\,k_j\,|B\rangle \approx -i\int d\mathbf{r}F^*_{\mathrm{A}}(\mathbf{r})\frac{\partial F_{\mathrm{B}}(\mathbf{r})}{\partial r_j}e^{2ik_0 z} \tag{A.12}$$

We see that the valley phase likely attenuates the integral and we suppose that this attenuation could easily be a factor of $0.1 \sim 0.01$ or even less.

To compare theory with experiment, we note that in general the Dresselhaus contribution to the SOC is larger than the Rashba contribution [174,175,185]. In ref. [174] it was found that $\beta = 178(11) \times 10^{-13}$ eV cm while in ref. [175] it was found that $\alpha - \beta$ is in the range from -300μeV nm to 800μeV nm. We thus estimate $|\alpha + \beta| \approx (100 - (-1000))\mu$eV nm.

If $|\mathrm{A}\rangle, |\mathrm{B}\rangle$ belong to the same valley then we estimate $|\Delta_{\mathrm{sd}}| \approx |\alpha + \beta| \times 0.1 \times |\langle s|k|p\rangle| = 10^{-1} \sim 10^{0}$ GHz as an order of magnitude estimate. For $|\mathrm{A}\rangle, |\mathrm{B}\rangle$ inter-valley this becomes $\Delta_{\mathrm{sd}} \approx 10^{-3} \sim 10^{-1}$ GHz.

We see that the variation of the spin-orbit parameters as well as the valley-orbit character of the states leads to variation of Δ_{sd} among the devices. The estimates compare favorably with the fitted Δ_{sd} which are between $10^{-3} \sim 10^{-2}$ GHz (Table A.1). Our analysis suggests that the states $|\mathrm{A}\rangle, |\mathrm{B}\rangle$ are states that with different valley composition.

For Device A in the (1,3) configuration, this conclusion is consistent with our previous remark - that the $|\mathrm{A}\rangle, |\mathrm{B}\rangle$ here are in different orbital and valley states. In the other charge configuration (3,1), the smaller Δ_{sd} may be due to the different valley character that appears since the confinement potential and the interface that is probed by the different dot wavefunctions would be different here. For the maps in devices B and D, a similar conclusion holds because Δ_{sd} is of a similar magnitude.

For device C, the value of $\Delta_{\mathrm{sd}} = 0.06 \pm 0.08$ GHz $\approx 0.24 \pm 0.32$ μeV is the largest (although the confidence interval is not conclusive). This suggests we may be observing a mostly orbital anticrossing, with the valley composition of either orbital being compatible (valley interference not completely destructive). This is consistent with the large $\Delta \approx 1.2 \pm 0.8$ meV.

Parameters	**Device A (1,3)**	**Device A (3,1)**	**Device B (3,1)**	**Device C (3,1)**	**Device D (3,1)**
V_0 (V)	-0.0528	0.36	1.56	0.91	1.6234
α_{rel} (THz/V)	1.2	1.2	1.5	1.5	1.5
Δ (GHz)	12 ± 1	38 ± 3	85 ± 3	279 ± 200	1.3 ± 0.3
Δ_{sd} or Δ_{sf} (MHz)	-27 ± 5	0 ± 0.002	-7.5 ± 0.2	-60 ± 80	-1.6 ± 0.9
dE_{Z} (MHz)	27 ± 7	-9 ± 9	10.3 ± 0.3	-110 ± 70	19 ± 1
η_{A} (MHz/V)	-238 ± 30	Not Fitted	-2.4 ± 0.4	Not Fitted	64 ± 30
η_{B} (MHz/V)	826 ± 100	5 ± 4	1.7 ± 0.3	Not Fitted	17 ± 20
c (MHz)	21 ± 10	-58 ± 10	25.8 ± 0.3	-60 ± 100	73 ± 1
Ω_{AC} (MHz)	9.5 ± 0.6	11.3 ± 0.5	1.81 ± 0.04	5.6 ± 0.4	Not Fitted

Table A.1: Fitted parameters of the four-level model

Appendix B

Locating & Tuning a Level Degeneracy

We discuss now the protocol for tuning the energy spectrum of a new charge configuration to create a level degeneracy, resulting in a speed-up of the qubit Rabi frequency. The protocol utilises tunnel-rate-based excited state spectroscopy. The interdot detuning ΔV_{P} is swept across an interdot charge transition to observe changes in the interdot tunnel rate associated with the population of excited states [43].

Figure B.1a shows a top-view schematic layout of the device gates. Figure B.1b shows the schematic potential landscapes for increasing ΔV_{P}, progressing from deep in (3,1) to deep in (4,0), where in-between the ground state of the P2 dot crosses the level of multiple states for the 4th electron of the P1 dot. We denote the ground and 1st excited states of the P1 dot as A and B, respectively, and mark these as the two right-most features in Figure B.1g.

To create a level degeneracy, we observe the trend in the separation of states A and B whilst deforming the dots, and tune towards a point of zero separation. In Figure B.1g, V_{P1}, V_{P2}, and V_{J} are varied and denoted as $V_{\mathrm{P,offset}}$, with the expected potential deformation shown in Figure B.1c. The states A & B appear to converge for decreasing $V_{\mathrm{P,offset}}$, so we set

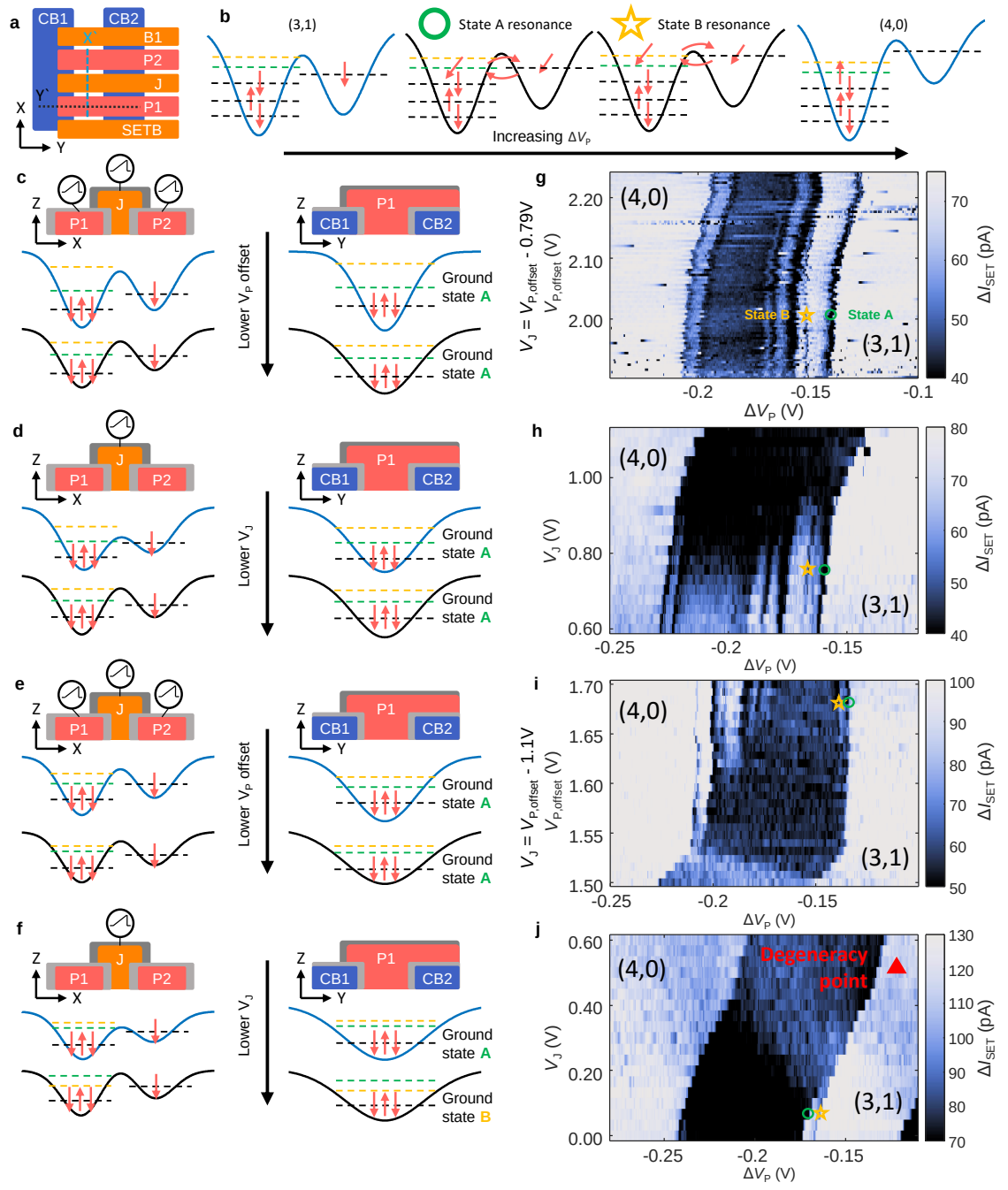

Figure B.1: Process for finding and tuning a degeneracy point

$V_{\mathrm{P,offset}} = 1.7\ V$ and in Figure B.1d & h re-tune V_{J} to achieve desired tunnel rates.

At the lower J value, the excited states can be probed again. In Figure B.1e & i, we further lower $V_{\mathrm{P,offset}}$, and lose the visibility of the excited state due to high tunnel rates.

In Figure B.1f & j we again attempt to re-tune the interdot tunnel rate and again observe the states A & B, here converging for higher V_{J}, potentially a sign that states A & B have already crossed. Now we perform a PESOS map near the red triangle where we anticipate a degeneracy, with results shown in 4.5b in the main text. We note that the first PESOS map we took in the vicinity of the red triangle immediately showed a speed up of the qubit Rabi frequency.

References

[1] B. Bauer, S. Bravyi, M. Motta, and G. K.-L. Chan, "Quantum Algorithms for Quantum Chemistry and Quantum Materials Science," *Chemical Reviews*, vol. 120, no. 22, pp. 12 685–12 717, Nov. 2020.

[2] A. Montanaro, "Quantum algorithms: An overview," *npj Quantum Information*, vol. 2, no. 1, pp. 1–8, Jan. 2016.

[3] P. W. Shor, "Polynomial-Time Algorithms for Prime Factorization and Discrete Logarithms on a Quantum Computer," *SIAM Journal on Computing*, vol. 26, no. 5, pp. 1484–1509, Oct. 1997.

[4] C. Gidney and M. Ekerå, "How to factor 2048 bit RSA integers in 8 hours using 20 million noisy qubits," *Quantum*, vol. 5, p. 433, Apr. 2021.

[5] J. J. Goings, A. White, J. Lee, C. S. Tautermann, M. Degroote, C. Gidney, T. Shiozaki, R. Babbush, and N. C. Rubin, "Reliably assessing the electronic structure of cytochrome P450 on today's classical computers and tomorrow's quantum computers," Feb. 2022.

[6] J. Lee, D. W. Berry, C. Gidney, W. J. Huggins, J. R. McClean, N. Wiebe, and R. Babbush, "Even More Efficient Quantum Computations of Chemistry Through Tensor Hypercontraction," *PRX Quantum*, vol. 2, no. 3, p. 030305, Jul. 2021.

[7] M. A. Nielsen and I. L. Chuang, "Quantum Computation and Quantum Information: 10th Anniversary Edition,"

https://www.cambridge.org/highereducation/books/quantum-computation-and-quantum-information/01E10196D0A682A6AEFFEA52D53BE9AE, Dec. 2010.

[8] Smite-Meister, "Bloch sphere."

[9] D. P. DiVincenzo, "The Physical Implementation of Quantum Computation," *Fortschritte der Physik*, vol. 48, no. 9-11, pp. 771–783, 2000.

[10] A. G. Fowler, M. Mariantoni, J. M. Martinis, and A. N. Cleland, "Surface codes: Towards practical large-scale quantum computation," *Physical Review A*, vol. 86, no. 3, p. 032324, Sep. 2012.

[11] J. Preskill, "Quantum Computing in the NISQ era and beyond," *Quantum*, vol. 2, p. 79, Aug. 2018.

[12] F. Arute, K. Arya, R. Babbush, D. Bacon, J. C. Bardin, R. Barends, R. Biswas, S. Boixo, F. G. S. L. Brandao, D. A. Buell, B. Burkett, Y. Chen, Z. Chen, B. Chiaro, R. Collins, W. Courtney, A. Dunsworth, E. Farhi, B. Foxen, A. Fowler, C. Gidney, M. Giustina, R. Graff, K. Guerin, S. Habegger, M. P. Harrigan, M. J. Hartmann, A. Ho, M. Hoffmann, T. Huang, T. S. Humble, S. V. Isakov, E. Jeffrey, Z. Jiang, D. Kafri, K. Kechedzhi, J. Kelly, P. V. Klimov, S. Knysh, A. Korotkov, F. Kostritsa, D. Landhuis, M. Lindmark, E. Lucero, D. Lyakh, S. Mandrà, J. R. McClean, M. McEwen, A. Megrant, X. Mi, K. Michielsen, M. Mohseni, J. Mutus, O. Naaman, M. Neeley, C. Neill, M. Y. Niu, E. Ostby, A. Petukhov, J. C. Platt, C. Quintana, E. G. Rieffel, P. Roushan, N. C. Rubin, D. Sank, K. J. Satzinger, V. Smelyanskiy, K. J. Sung, M. D. Trevithick, A. Vainsencher, B. Villalonga, T. White, Z. J. Yao, P. Yeh, A. Zalcman, H. Neven, and J. M. Martinis, "Quantum supremacy using a programmable superconducting processor," *Nature*, vol. 574, no. 7779, pp. 505–510, Oct. 2019.

[13] H.-S. Zhong, Y.-H. Deng, J. Qin, H. Wang, M.-C. Chen, L.-C. Peng, Y.-H. Luo, D. Wu, S.-Q. Gong, H. Su, Y. Hu, P. Hu, X.-Y. Yang, W.-J. Zhang, H. Li, Y. Li, X. Jiang, L. Gan, G. Yang, L. You, Z. Wang, L. Li, N.-L. Liu, J. J. Renema, C.-Y. Lu,

and J.-W. Pan, "Phase-Programmable Gaussian Boson Sampling Using Stimulated Squeezed Light," *Physical Review Letters*, vol. 127, no. 18, p. 180502, Oct. 2021.

[14] Y. Wu, W.-S. Bao, S. Cao, F. Chen, M.-C. Chen, X. Chen, T.-H. Chung, H. Deng, Y. Du, D. Fan, M. Gong, C. Guo, C. Guo, S. Guo, L. Han, L. Hong, H.-L. Huang, Y.-H. Huo, L. Li, N. Li, S. Li, Y. Li, F. Liang, C. Lin, J. Lin, H. Qian, D. Qiao, H. Rong, H. Su, L. Sun, L. Wang, S. Wang, D. Wu, Y. Xu, K. Yan, W. Yang, Y. Yang, Y. Ye, J. Yin, C. Ying, J. Yu, C. Zha, C. Zhang, H. Zhang, K. Zhang, Y. Zhang, H. Zhao, Y. Zhao, L. Zhou, Q. Zhu, C.-Y. Lu, C.-Z. Peng, X. Zhu, and J.-W. Pan, "Strong Quantum Computational Advantage Using a Superconducting Quantum Processor," *Physical Review Letters*, vol. 127, no. 18, p. 180501, Oct. 2021.

[15] L. Egan, D. M. Debroy, C. Noel, A. Risinger, D. Zhu, D. Biswas, M. Newman, M. Li, K. R. Brown, M. Cetina, and C. Monroe, "Fault-tolerant control of an error-corrected qubit," *Nature*, vol. 598, no. 7880, pp. 281–286, Oct. 2021.

[16] R. Acharya, I. Aleiner, R. Allen, T. I. Andersen, M. Ansmann, F. Arute, K. Arya, A. Asfaw, J. Atalaya, R. Babbush, D. Bacon, J. C. Bardin, J. Basso, A. Bengtsson, S. Boixo, G. Bortoli, A. Bourassa, J. Bovaird, L. Brill, M. Broughton, B. B. Buckley, D. A. Buell, T. Burger, B. Burkett, N. Bushnell, Y. Chen, Z. Chen, B. Chiaro, J. Cogan, R. Collins, P. Conner, W. Courtney, A. L. Crook, B. Curtin, D. M. Debroy, A. D. T. Barba, S. Demura, A. Dunsworth, D. Eppens, C. Erickson, L. Faoro, E. Farhi, R. Fatemi, L. F. Burgos, E. Forati, A. G. Fowler, B. Foxen, W. Giang, C. Gidney, D. Gilboa, M. Giustina, A. G. Dau, J. A. Gross, S. Habegger, M. C. Hamilton, M. P. Harrigan, S. D. Harrington, O. Higgott, J. Hilton, M. Hoffmann, S. Hong, T. Huang, A. Huff, W. J. Huggins, L. B. Ioffe, S. V. Isakov, J. Iveland, E. Jeffrey, Z. Jiang, C. Jones, P. Juhas, D. Kafri, K. Kechedzhi, J. Kelly, T. Khattar, M. Khezri, M. Kieferová, S. Kim, A. Kitaev, P. V. Klimov, A. R. Klots, A. N. Korotkov, F. Kostritsa, J. M. Kreikebaum, D. Landhuis, P. Laptev, K.-M. Lau, L. Laws, J. Lee, K. Lee, B. J. Lester, A. Lill, W. Liu, A. Locharla, E. Lucero, F. D. Malone, J. Marshall, O. Martin, J. R. McClean, T. Mccourt, M. McEwen, A. Megrant, B. M. Costa, X. Mi, K. C. Miao, M. Mohseni, S. Montazeri, A. Morvan, E. Mount,

W. Mruczkiewicz, O. Naaman, M. Neeley, C. Neill, A. Nersisyan, H. Neven, M. Newman, J. H. Ng, A. Nguyen, M. Nguyen, M. Y. Niu, T. E. O'Brien, A. Opremcak, J. Platt, A. Petukhov, R. Potter, L. P. Pryadko, C. Quintana, P. Roushan, N. C. Rubin, N. Saei, D. Sank, K. Sankaragomathi, K. J. Satzinger, H. F. Schurkus, C. Schuster, M. J. Shearn, A. Shorter, V. Shvarts, J. Skruzny, V. Smelyanskiy, W. C. Smith, G. Sterling, D. Strain, M. Szalay, A. Torres, G. Vidal, B. Villalonga, C. V. Heidweiller, T. White, C. Xing, Z. J. Yao, P. Yeh, J. Yoo, G. Young, A. Zalcman, Y. Zhang, and N. Zhu, "Suppressing quantum errors by scaling a surface code logical qubit," Jul. 2022.

[17] S. Krinner, N. Lacroix, A. Remm, A. Di Paolo, E. Genois, C. Leroux, C. Hellings, S. Lazar, F. Swiadek, J. Herrmann, G. J. Norris, C. K. Andersen, M. Müller, A. Blais, C. Eichler, and A. Wallraff, "Realizing repeated quantum error correction in a distance-three surface code," *Nature*, vol. 605, no. 7911, pp. 669–674, May 2022.

[18] D. Loss and D. P. DiVincenzo, "Quantum computation with quantum dots," *Physical Review A*, vol. 57, no. 1, pp. 120–126, Jan. 1998.

[19] F. H. L. Koppens, C. Buizert, K. J. Tielrooij, I. T. Vink, K. C. Nowack, T. Meunier, L. P. Kouwenhoven, and L. M. K. Vandersypen, "Driven coherent oscillations of a single electron spin in a quantum dot," *Nature*, vol. 442, no. 7104, pp. 766–771, Aug. 2006.

[20] J. R. Petta, A. C. Johnson, J. M. Taylor, E. A. Laird, A. Yacoby, M. D. Lukin, C. M. Marcus, M. P. Hanson, and A. C. Gossard, "Coherent Manipulation of Coupled Electron Spins in Semiconductor Quantum Dots," *Science*, vol. 309, no. 5744, pp. 2180–2184, Sep. 2005.

[21] J. Z. Blumoff, A. S. Pan, T. E. Keating, R. W. Andrews, D. W. Barnes, T. L. Brecht, E. T. Croke, L. E. Euliss, J. A. Fast, C. A. Jackson, A. M. Jones, J. Kerckhoff, R. K. Lanza, K. Raach, B. J. Thomas, R. Velunta, A. J. Weinstein, T. D. Ladd, K. Eng, M. G. Borselli, A. T. Hunter, and M. T. Rakher, "Fast and High-Fidelity

State Preparation and Measurement in Triple-Quantum-Dot Spin Qubits," *PRX Quantum*, vol. 3, no. 1, p. 010352, Mar. 2022.

[22] A. Noiri, K. Takeda, T. Nakajima, T. Kobayashi, A. Sammak, G. Scappucci, and S. Tarucha, "Fast universal quantum gate above the fault-tolerance threshold in silicon," *Nature*, vol. 601, no. 7893, pp. 338–342, Jan. 2022.

[23] A. R. Mills, C. R. Guinn, M. J. Gullans, A. J. Sigillito, M. M. Feldman, E. Nielsen, and J. R. Petta, "Two-qubit silicon quantum processor with operation fidelity exceeding 99%," *Science Advances*, vol. 8, no. 14, p. eabn5130, Apr. 2022.

[24] X. Xue, M. Russ, N. Samkharadze, B. Undseth, A. Sammak, G. Scappucci, and L. M. K. Vandersypen, "Quantum logic with spin qubits crossing the surface code threshold," *Nature*, vol. 601, no. 7893, pp. 343–347, Jan. 2022.

[25] N. W. Hendrickx, W. I. L. Lawrie, M. Russ, F. van Riggelen, S. L. de Snoo, R. N. Schouten, A. Sammak, G. Scappucci, and M. Veldhorst, "A four-qubit germanium quantum processor," *Nature*, vol. 591, no. 7851, pp. 580–585, Mar. 2021.

[26] T. F. Watson, S. G. J. Philips, E. Kawakami, D. R. Ward, P. Scarlino, M. Veldhorst, D. E. Savage, M. G. Lagally, M. Friesen, S. N. Coppersmith, M. A. Eriksson, and L. M. K. Vandersypen, "A programmable two-qubit quantum processor in silicon," *Nature*, vol. 555, no. 7698, pp. 633–637, Mar. 2018.

[27] W. Huang, C. H. Yang, K. W. Chan, T. Tanttu, B. Hensen, R. C. C. Leon, M. A. Fogarty, J. C. C. Hwang, F. E. Hudson, K. M. Itoh, A. Morello, A. Laucht, and A. S. Dzurak, "Fidelity benchmarks for two-qubit gates in silicon," *Nature*, vol. 569, no. 7757, pp. 532–536, May 2019.

[28] R. Maurand, X. Jehl, D. Kotekar-Patil, A. Corna, H. Bohuslavskyi, R. Laviéville, L. Hutin, S. Barraud, M. Vinet, M. Sanquer, and S. De Franceschi, "A CMOS silicon spin qubit," *Nature Communications*, vol. 7, no. 1, p. 13575, Nov. 2016.

[29] L. C. Camenzind, S. Geyer, A. Fuhrer, R. J. Warburton, D. M. Zumbühl, and A. V. Kuhlmann, "A hole spin qubit in a fin field-effect transistor above 4 kelvin," *Nature Electronics*, vol. 5, no. 3, pp. 178–183, Mar. 2022.

[30] A. M. J. Zwerver, T. Krähenmann, T. F. Watson, L. Lampert, H. C. George, R. Pillarisetty, S. A. Bojarski, P. Amin, S. V. Amitonov, J. M. Boter, R. Caudillo, D. Correas-Serrano, J. P. Dehollain, G. Droulers, E. M. Henry, R. Kotlyar, M. Lodari, F. Lüthi, D. J. Michalak, B. K. Mueller, S. Neyens, J. Roberts, N. Samkharadze, G. Zheng, O. K. Zietz, G. Scappucci, M. Veldhorst, L. M. K. Vandersypen, and J. S. Clarke, "Qubits made by advanced semiconductor manufacturing," *Nature Electronics*, vol. 5, no. 3, pp. 184–190, Mar. 2022.

[31] H. Watzinger, J. Kukučka, L. Vukušić, F. Gao, T. Wang, F. Schäffler, J.-J. Zhang, and G. Katsaros, "A germanium hole spin qubit," *Nature Communications*, vol. 9, no. 1, p. 3902, Sep. 2018.

[32] A. P. Higginbotham, T. W. Larsen, J. Yao, H. Yan, C. M. Lieber, C. M. Marcus, and F. Kuemmeth, "Hole Spin Coherence in a Ge/Si Heterostructure Nanowire," *Nano Letters*, vol. 14, no. 6, pp. 3582–3586, Jun. 2014.

[33] S. Dorsch, B. Dalelkhan, S. Fahlvik, and A. M. Burke, "Side-gated, enhancement mode, InAs nanowire double quantum dot devices—toward controlling transverse electric fields in spin-transport measurements," *Nanotechnology*, vol. 30, no. 14, p. 144002, Feb. 2019.

[34] L. M. Gächter, R. Garreis, J. D. Gerber, M. J. Ruckriegel, C. Tong, B. Kratochwil, F. K. de Vries, A. Kurzmann, K. Watanabe, T. Taniguchi, T. Ihn, K. Ensslin, and W. W. Huang, "Single-Shot Spin Readout in Graphene Quantum Dots," *PRX Quantum*, vol. 3, no. 2, p. 020343, May 2022.

[35] X. Zhou, G. Koolstra, X. Zhang, G. Yang, X. Han, B. Dizdar, X. Li, R. Divan, W. Guo, K. W. Murch, D. I. Schuster, and D. Jin, "Single electrons on solid neon as a solid-state qubit platform," *Nature*, vol. 605, no. 7908, pp. 46–50, May 2022.

[36] J. J. Pla, K. Y. Tan, J. P. Dehollain, W. H. Lim, J. J. L. Morton, F. A. Zwanenburg, D. N. Jamieson, A. S. Dzurak, and A. Morello, "High-fidelity readout and control of a nuclear spin qubit in silicon," *Nature*, vol. 496, no. 7445, pp. 334–338, Apr. 2013.

[37] J. T. Muhonen, J. P. Dehollain, A. Laucht, F. E. Hudson, R. Kalra, T. Sekiguchi, K. M. Itoh, D. N. Jamieson, J. C. McCallum, A. S. Dzurak, and A. Morello, "Storing quantum information for 30 seconds in a nanoelectronic device," *Nature Nanotechnology*, vol. 9, no. 12, pp. 986–991, Dec. 2014.

[38] M. T. Mądzik, S. Asaad, A. Youssry, B. Joecker, K. M. Rudinger, E. Nielsen, K. C. Young, T. J. Proctor, A. D. Baczewski, A. Laucht, V. Schmitt, F. E. Hudson, K. M. Itoh, A. M. Jakob, B. C. Johnson, D. N. Jamieson, A. S. Dzurak, C. Ferrie, R. Blume-Kohout, and A. Morello, "Precision tomography of a three-qubit donor quantum processor in silicon," *Nature*, vol. 601, no. 7893, pp. 348–353, Jan. 2022.

[39] Y. He, S. K. Gorman, D. Keith, L. Kranz, J. G. Keizer, and M. Y. Simmons, "A two-qubit gate between phosphorus donor electrons in silicon," *Nature*, vol. 571, no. 7765, pp. 371–375, Jul. 2019.

[40] C. H. Yang, K. W. Chan, R. Harper, W. Huang, T. Evans, J. C. C. Hwang, B. Hensen, A. Laucht, T. Tanttu, F. E. Hudson, S. T. Flammia, K. M. Itoh, A. Morello, S. D. Bartlett, and A. S. Dzurak, "Silicon qubit fidelities approaching incoherent noise limits via pulse engineering," *Nature Electronics*, vol. 2, no. 4, pp. 151–158, Apr. 2019.

[41] A. J. Weinstein, M. D. Reed, A. M. Jones, R. W. Andrews, D. Barnes, J. Z. Blumoff, L. E. Euliss, K. Eng, B. Fong, S. D. Ha, D. R. Hulbert, C. Jackson, M. Jura, T. E. Keating, J. Kerckhoff, A. A. Kiselev, J. Matten, G. Sabbir, A. Smith, J. Wright, M. T. Rakher, T. D. Ladd, and M. G. Borselli, "Universal logic with encoded spin qubits in silicon," Feb. 2022.

[42] N. I. Dumoulin Stuyck, R. Li, C. Godfrin, A. Elsayed, M. Shehata, G. Simion, Y. Canvel, L. Goux, M. Heyns, B. Govoreanu, and I. P. Radu, "Uniform Spin Qubit

Devices with Tunable Coupling in an All-Silicon 300 mm Integrated Process," in *2021 Symposium on VLSI Circuits*. IEEE, 2021, pp. 1–2.

[43] C. H. Yang, W. H. Lim, N. S. Lai, A. Rossi, A. Morello, and A. S. Dzurak, "Orbital and valley state spectra of a few-electron silicon quantum dot," *Physical Review B*, vol. 86, no. 11, p. 115319, Sep. 2012.

[44] C. H. Yang, A. Rossi, R. Ruskov, N. S. Lai, F. A. Mohiyaddin, S. Lee, C. Tahan, G. Klimeck, A. Morello, and A. S. Dzurak, "Spin-valley lifetimes in a silicon quantum dot with tunable valley splitting," *Nature Communications*, vol. 4, no. 1, p. 2069, Jun. 2013.

[45] V. N. Ciriano-Tejel, M. A. Fogarty, S. Schaal, L. Hutin, B. Bertrand, L. Ibberson, M. F. Gonzalez-Zalba, J. Li, Y.-M. Niquet, M. Vinet, and J. J. Morton, "Spin Readout of a CMOS Quantum Dot by Gate Reflectometry and Spin-Dependent Tunneling," *PRX Quantum*, vol. 2, no. 1, p. 010353, Mar. 2021.

[46] M. A. Fogarty, K. W. Chan, B. Hensen, W. Huang, T. Tanttu, C. H. Yang, A. Laucht, M. Veldhorst, F. E. Hudson, K. M. Itoh, D. Culcer, T. D. Ladd, A. Morello, and A. S. Dzurak, "Integrated silicon qubit platform with single-spin addressability, exchange control and single-shot singlet-triplet readout," *Nature Communications*, vol. 9, no. 1, p. 4370, Oct. 2018.

[47] W. Gilbert, T. Tanttu, W. H. Lim, M. Feng, J. Y. Huang, J. D. Cifuentes, S. Serrano, P. Y. Mai, R. C. C. Leon, C. C. Escott, K. M. Itoh, N. V. Abrosimov, H.-J. Pohl, M. L. W. Thewalt, F. E. Hudson, A. Morello, A. Laucht, C. H. Yang, A. Saraiva, and A. S. Dzurak, "On-demand electrical control of spin qubits," Jan. 2022.

[48] M. Veldhorst, J. C. C. Hwang, C. H. Yang, A. W. Leenstra, B. de Ronde, J. P. Dehollain, J. T. Muhonen, F. E. Hudson, K. M. Itoh, A. Morello, and A. S. Dzurak, "An addressable quantum dot qubit with fault-tolerant control-fidelity," *Nature Nanotechnology*, vol. 9, no. 12, pp. 981–985, Dec. 2014.

[49] Y. Tokura, W. G. van der Wiel, T. Obata, and S. Tarucha, "Coherent Single Electron Spin Control in a Slanting Zeeman Field," *Physical Review Letters*, vol. 96, no. 4, p. 047202, Jan. 2006.

[50] R. C. C. Leon, C. H. Yang, J. C. C. Hwang, J. C. Lemyre, T. Tanttu, W. Huang, K. W. Chan, K. Y. Tan, F. E. Hudson, K. M. Itoh, A. Morello, A. Laucht, M. Pioro-Ladrière, A. Saraiva, and A. S. Dzurak, "Coherent spin control of s-, p-, d- and f-electrons in a silicon quantum dot," *Nature Communications*, vol. 11, no. 1, p. 797, Feb. 2020.

[51] J. Yoneda, K. Takeda, T. Otsuka, T. Nakajima, M. R. Delbecq, G. Allison, T. Honda, T. Kodera, S. Oda, Y. Hoshi, N. Usami, K. M. Itoh, and S. Tarucha, "A quantum-dot spin qubit with coherence limited by charge noise and fidelity higher than 99.9%," *Nature Nanotechnology*, vol. 13, no. 2, pp. 102–106, Feb. 2018.

[52] D. M. Zajac, A. J. Sigillito, M. Russ, F. Borjans, J. M. Taylor, G. Burkard, and J. R. Petta, "Resonantly driven CNOT gate for electron spins," *Science*, vol. 359, no. 6374, pp. 439–442, Jan. 2018.

[53] N. W. Hendrickx, D. P. Franke, A. Sammak, G. Scappucci, and M. Veldhorst, "Fast two-qubit logic with holes in germanium," *Nature*, vol. 577, no. 7791, pp. 487–491, Jan. 2020.

[54] K. C. Nowack, F. H. L. Koppens, Y. V. Nazarov, and L. M. K. Vandersypen, "Coherent Control of a Single Electron Spin with Electric Fields," *Science*, vol. 318, no. 5855, pp. 1430–1433, Nov. 2007.

[55] S. Meiboom and D. Gill, "Modified Spin-Echo Method for Measuring Nuclear Relaxation Times," *Review of Scientific Instruments*, vol. 29, no. 8, pp. 688–691, Aug. 1958.

[56] J. R. Petta, A. C. Johnson, A. Yacoby, C. M. Marcus, M. P. Hanson, and A. C. Gossard, "Pulsed-gate measurements of the singlet-triplet relaxation time in a two-electron double quantum dot," *Physical Review B*, vol. 72, no. 16, p. 161301, Oct. 2005.

[57] M. Veldhorst, C. H. Yang, J. C. C. Hwang, W. Huang, J. P. Dehollain, J. T. Muhonen, S. Simmons, A. Laucht, F. E. Hudson, K. M. Itoh, A. Morello, and A. S. Dzurak, "A two-qubit logic gate in silicon," *Nature*, vol. 526, no. 7573, pp. 410–414, Oct. 2015.

[58] M. D. Shulman, O. E. Dial, S. P. Harvey, H. Bluhm, V. Umansky, and A. Yacoby, "Demonstration of Entanglement of Electrostatically Coupled Singlet-Triplet Qubits," *Science*, vol. 336, no. 6078, pp. 202–205, Apr. 2012.

[59] L. Trifunovic, O. Dial, M. Trif, J. R. Wootton, R. Abebe, A. Yacoby, and D. Loss, "Long-Distance Spin-Spin Coupling via Floating Gates," *Physical Review X*, vol. 2, no. 1, p. 011006, Jan. 2012.

[60] X. Mi, M. Benito, S. Putz, D. M. Zajac, J. M. Taylor, G. Burkard, and J. R. Petta, "A coherent spin–photon interface in silicon," *Nature*, vol. 555, no. 7698, pp. 599–603, Mar. 2018.

[61] P. Harvey-Collard, J. Dijkema, G. Zheng, A. Sammak, G. Scappucci, and L. M. K. Vandersypen, "Coherent Spin-Spin Coupling Mediated by Virtual Microwave Photons," *Physical Review X*, vol. 12, no. 2, p. 021026, May 2022.

[62] A. Morello, J. J. Pla, F. A. Zwanenburg, K. W. Chan, K. Y. Tan, H. Huebl, M. Möttönen, C. D. Nugroho, C. Yang, J. A. van Donkelaar, A. D. C. Alves, D. N. Jamieson, C. C. Escott, L. C. L. Hollenberg, R. G. Clark, and A. S. Dzurak, "Single-shot readout of an electron spin in silicon," *Nature*, vol. 467, no. 7316, pp. 687–691, Oct. 2010.

[63] C. Barthel, D. J. Reilly, C. M. Marcus, M. P. Hanson, and A. C. Gossard, "Rapid Single-Shot Measurement of a Singlet-Triplet Qubit," *Physical Review Letters*, vol. 103, no. 16, p. 160503, Oct. 2009.

[64] J. M. Elzerman, R. Hanson, L. H. Willems van Beveren, B. Witkamp, L. M. K. Vandersypen, and L. P. Kouwenhoven, "Single-shot read-out of an individual electron spin in a quantum dot," *Nature*, vol. 430, no. 6998, pp. 431–435, Jul. 2004.

[65] K. Ono, D. G. Austing, Y. Tokura, and S. Tarucha, "Current Rectification by Pauli Exclusion in a Weakly Coupled Double Quantum Dot System," *Science*, vol. 297, no. 5585, pp. 1313–1317, Aug. 2002.

[66] A. E. Seedhouse, T. Tanttu, R. C. Leon, R. Zhao, K. Y. Tan, B. Hensen, F. E. Hudson, K. M. Itoh, J. Yoneda, C. H. Yang, A. Morello, A. Laucht, S. N. Coppersmith, A. Saraiva, and A. S. Dzurak, "Pauli Blockade in Silicon Quantum Dots with Spin-Orbit Control," *PRX Quantum*, vol. 2, no. 1, p. 010303, Jan. 2021.

[67] C. Jones, M. A. Fogarty, A. Morello, M. F. Gyure, A. S. Dzurak, and T. D. Ladd, "Logical Qubit in a Linear Array of Semiconductor Quantum Dots," *Physical Review X*, vol. 8, no. 2, p. 021058, Jun. 2018.

[68] J. I. Colless, A. C. Mahoney, J. M. Hornibrook, A. C. Doherty, H. Lu, A. C. Gossard, and D. J. Reilly, "Dispersive Readout of a Few-Electron Double Quantum Dot with Fast rf Gate Sensors," *Physical Review Letters*, vol. 110, no. 4, p. 046805, Jan. 2013.

[69] D. J. Reilly, C. M. Marcus, M. P. Hanson, and A. C. Gossard, "Fast single-charge sensing with a rf quantum point contact," *Applied Physics Letters*, vol. 91, no. 16, p. 162101, Oct. 2007.

[70] A. West, B. Hensen, A. Jouan, T. Tanttu, C.-H. Yang, A. Rossi, M. F. Gonzalez-Zalba, F. Hudson, A. Morello, D. J. Reilly, and A. S. Dzurak, "Gate-based single-shot readout of spins in silicon," *Nature Nanotechnology*, vol. 14, no. 5, pp. 437–441, May 2019.

[71] G. Zheng, N. Samkharadze, M. L. Noordam, N. Kalhor, D. Brousse, A. Sammak, G. Scappucci, and L. M. K. Vandersypen, "Rapid gate-based spin read-out in silicon using an on-chip resonator," *Nature Nanotechnology*, vol. 14, no. 8, pp. 742–746, Aug. 2019.

[72] A. Rossi, R. Zhao, A. S. Dzurak, and M. F. Gonzalez-Zalba, "Dispersive readout of a silicon quantum dot with an accumulation-mode gate sensor," *Applied Physics Letters*, vol. 110, no. 21, p. 212101, May 2017.

[73] P. Pakkiam, A. V. Timofeev, M. G. House, M. R. Hogg, T. Kobayashi, M. Koch, S. Rogge, and M. Y. Simmons, "Single-Shot Single-Gate rf Spin Readout in Silicon," *Physical Review X*, vol. 8, no. 4, p. 041032, Nov. 2018.

[74] K. D. Petersson, C. G. Smith, D. Anderson, P. Atkinson, G. A. C. Jones, and D. A. Ritchie, "Charge and Spin State Readout of a Double Quantum Dot Coupled to a Resonator," *Nano Letters*, vol. 10, no. 8, pp. 2789–2793, Aug. 2010.

[75] M. G. House, T. Kobayashi, B. Weber, S. J. Hile, T. F. Watson, J. van der Heijden, S. Rogge, and M. Y. Simmons, "Radio frequency measurements of tunnel couplings and singlet–triplet spin states in Si:P quantum dots," *Nature Communications*, vol. 6, no. 1, p. 8848, Nov. 2015.

[76] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, no. 8, p. 4, 1965.

[77] M. Veldhorst, H. G. J. Eenink, C. H. Yang, and A. S. Dzurak, "Silicon CMOS architecture for a spin-based quantum computer," *Nature Communications*, vol. 8, no. 1, p. 1766, Dec. 2017.

[78] L. M. K. Vandersypen, H. Bluhm, J. S. Clarke, A. S. Dzurak, R. Ishihara, A. Morello, D. J. Reilly, L. R. Schreiber, and M. Veldhorst, "Interfacing spin qubits in quantum dots and donors—hot, dense, and coherent," *npj Quantum Information*, vol. 3, no. 1, pp. 1–10, Sep. 2017.

[79] Li Ruoyu, Petit Luca, Franke David P., Dehollain Juan Pablo, Helsen Jonas, Steudtner Mark, Thomas Nicole K., Yoscovits Zachary R., Singh Kanwal J., Wehner Stephanie, Vandersypen Lieven M. K., Clarke James S., and Veldhorst Menno, "A crossbar network for silicon quantum dot qubits," *Science Advances*, vol. 4, no. 7, p. eaar3960, 2018.

[80] J. M. Boter, J. P. Dehollain, J. P. G. van Dijk, Y. Xu, T. Hensgens, R. Versluis, H. W. L. Naus, J. S. Clarke, M. Veldhorst, F. Sebastiano, and L. M. K. Vandersypen, "The spider-web array–a sparse spin qubit array," Sep. 2021.

[81] Z. Cai, A. Siegel, and S. Benjamin, "Looped Pipelines Enabling Effective 3D Qubit Lattices in a Strictly 2D Device," Mar. 2022.

[82] C. H. Yang, R. C. C. Leon, J. C. C. Hwang, A. Saraiva, T. Tanttu, W. Huang, J. Camirand Lemyre, K. W. Chan, K. Y. Tan, F. E. Hudson, K. M. Itoh, A. Morello, M. Pioro-Ladrière, A. Laucht, and A. S. Dzurak, "Operation of a silicon quantum processor unit cell above one kelvin," *Nature*, vol. 580, no. 7803, pp. 350–354, Apr. 2020.

[83] L. Petit, H. G. J. Eenink, M. Russ, W. I. L. Lawrie, N. W. Hendrickx, S. G. J. Philips, J. S. Clarke, L. M. K. Vandersypen, and M. Veldhorst, "Universal quantum logic in hot silicon qubits," *Nature*, vol. 580, no. 7803, pp. 355–359, Apr. 2020.

[84] E. Chanrion, D. J. Niegemann, B. Bertrand, C. Spence, B. Jadot, J. Li, P.-A. Mortemousque, L. Hutin, R. Maurand, X. Jehl, M. Sanquer, S. De Franceschi, C. Bäuerle, F. Balestro, Y.-M. Niquet, M. Vinet, T. Meunier, and M. Urdampilleta, "Charge Detection in an Array of CMOS Quantum Dots," *Physical Review Applied*, vol. 14, no. 2, p. 024066, Aug. 2020.

[85] F. Ansaloni, A. Chatterjee, H. Bohuslavskyi, B. Bertrand, L. Hutin, M. Vinet, and F. Kuemmeth, "Single-electron operations in a foundry-fabricated array of quantum dots," *Nature Communications*, vol. 11, no. 1, p. 6399, Dec. 2020.

[86] A. Corna, L. Bourdet, R. Maurand, A. Crippa, D. Kotekar-Patil, H. Bohuslavskyi, R. Laviéville, L. Hutin, S. Barraud, X. Jehl, M. Vinet, S. De Franceschi, Y.-M. Niquet, and M. Sanquer, "Electrically driven electron spin resonance mediated by spin–valley–orbit coupling in a silicon quantum dot," *npj Quantum Information*, vol. 4, no. 1, p. 6, Feb. 2018.

[87] T. Bédécarrats, B. C. Paz, B. M. Diaz, H. Niebojewski, B. Bertrand, N. Rambal, C. Comboroure, A. Sarrazin, F. Boulard, E. Guyez, J.-M. Hartmann, Y. Morand, A. Magalhaes-Lucas, E. Nowak, E. Catapano, M. Cassé, M. Urdampilleta, Y.-M. Niquet, F. Gaillard, S. De Franceschi, T. Meunier, and M. Vinet, "A new FDSOI

spin qubit platform with 40nm effective control pitch," in *2021 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2021, pp. 1–4.

[88] N. Lee, R. Tsuchiya, G. Shinkai, Y. Kanno, T. Mine, T. Takahama, R. Mizokuchi, T. Kodera, D. Hisamoto, and H. Mizuno, "Enhancing electrostatic coupling in silicon quantum dot array by dual gate oxide thickness for large-scale integration," *Applied Physics Letters*, vol. 116, no. 16, p. 162106, Apr. 2020.

[89] I. Bashir, E. Blokhina, A. Esmailiyan, D. Leipold, M. Asker, E. Koskin, P. Giounanlis, H. Wang, D. Andrade-Miceli, A. Sokolov, A. Koziol, T. Siriburanon, and R. B. Staszewski, "A Single-Electron Injection Device for CMOS Charge Qubits Implemented in 22-nm FD-SOI," *IEEE Solid-State Circuits Letters*, vol. 3, pp. 206–209, 2020.

[90] K. W. Chan, W. Huang, C. H. Yang, J. C. C. Hwang, B. Hensen, T. Tanttu, F. E. Hudson, K. M. Itoh, A. Laucht, A. Morello, and A. S. Dzurak, "Assessment of a Silicon Quantum Dot Spin Qubit Environment via Noise Spectroscopy," *Physical Review Applied*, vol. 10, no. 4, p. 044017, Oct. 2018.

[91] J. P. Kestner, X. Wang, L. S. Bishop, E. Barnes, and S. Das Sarma, "Noise-Resistant Control for a Spin Qubit Array," *Physical Review Letters*, vol. 110, no. 14, p. 140502, Apr. 2013.

[92] D. P. Franke, J. S. Clarke, L. M. K. Vandersypen, and M. Veldhorst, "Rent's rule and extensibility in quantum computing," *Microprocessors and Microsystems*, vol. 67, pp. 1–7, Jun. 2019.

[93] C. D. Hill, E. Peretz, S. J. Hile, M. G. House, M. Fuechsle, S. Rogge, M. Y. Simmons, and L. C. L. Hollenberg, "A surface code quantum computer in silicon," *Science Advances*, vol. 1, no. 9, p. e1500707, Oct. 2015.

[94] A. Laucht, R. Kalra, S. Simmons, J. P. Dehollain, J. T. Muhonen, F. A. Mohiyaddin, S. Freer, F. E. Hudson, K. M. Itoh, D. N. Jamieson, J. C. McCallum, A. S. Dzurak, and A. Morello, "A dressed spin qubit in silicon," *Nature Nanotechnology*, vol. 12, no. 1, pp. 61–66, Jan. 2017.

[95] A. E. Seedhouse, I. Hansen, A. Laucht, C. H. Yang, A. S. Dzurak, and A. Saraiva, "Quantum computation protocol for dressed spins in a global field," *Physical Review B*, vol. 104, no. 23, p. 235411, Dec. 2021.

[96] I. Hansen, A. E. Seedhouse, A. Saraiva, A. Laucht, A. S. Dzurak, and C. H. Yang, "Pulse engineering of a global field for robust and universal quantum computation," *Physical Review A*, vol. 104, no. 6, p. 062415, Dec. 2021.

[97] I. Hansen, A. E. Seedhouse, K. W. Chan, F. Hudson, K. M. Itoh, A. Laucht, A. Saraiva, C. H. Yang, and A. S. Dzurak, "Implementation of the SMART protocol for global qubit control in silicon," Sep. 2021.

[98] E. Vahapoglu, J. P. Slack-Smith, R. C. C. Leon, W. H. Lim, F. E. Hudson, T. Day, T. Tanttu, C. H. Yang, A. Laucht, A. S. Dzurak, and J. J. Pla, "Single-electron spin resonance in a nanoelectronic device using a global field," *Science Advances*, vol. 7, no. 33, p. eabg9158, Aug. 2021.

[99] E. Vahapoglu, J. P. Slack-Smith, R. C. C. Leon, W. H. Lim, F. E. Hudson, T. Day, J. D. Cifuentes, T. Tanttu, C. H. Yang, A. Saraiva, N. V. Abrosimov, H.-J. Pohl, M. L. W. Thewalt, A. Laucht, A. S. Dzurak, and J. J. Pla, "Coherent control of electron spin qubits in silicon using a global field," Oct. 2021.

[100] S. Pauka, K. Das, J. Hornibrook, G. Gardner, M. Manfra, M. Cassidy, and D. Reilly, "Characterizing Quantum Devices at Scale with Custom Cryo-CMOS," *Physical Review Applied*, vol. 13, no. 5, p. 054072, May 2020.

[101] A. Ruffino, T.-Y. Yang, J. Michniewicz, Y. Peng, E. Charbon, and M. F. Gonzalez-Zalba, "A cryo-CMOS chip that integrates silicon quantum dots and multiplexed dispersive readout electronics," *Nature Electronics*, vol. 5, no. 1, pp. 53–59, Jan. 2022.

[102] S. J. Pauka, K. Das, R. Kalra, A. Moini, Y. Yang, M. Trainer, A. Bousquet, C. Cantaloube, N. Dick, G. C. Gardner, M. J. Manfra, and D. J. Reilly, "A cryogenic CMOS chip for generating control signals for multiple qubits," *Nature Electronics*, vol. 4, no. 1, pp. 64–70, Jan. 2021.

[103] S. Schaal, A. Rossi, V. N. Ciriano-Tejel, T.-Y. Yang, S. Barraud, J. J. L. Morton, and M. F. Gonzalez-Zalba, "A CMOS dynamic random access architecture for radio-frequency readout of quantum devices," *Nature Electronics*, vol. 2, no. 6, pp. 236–242, Jun. 2019.

[104] X. Xue, B. Patra, J. P. G. van Dijk, N. Samkharadze, S. Subramanian, A. Corna, B. Paquelet Wuetz, C. Jeon, F. Sheikh, E. Juarez-Hernandez, B. P. Esparza, H. Rampurawala, B. Carlton, S. Ravikumar, C. Nieva, S. Kim, H.-J. Lee, A. Sammak, G. Scappucci, M. Veldhorst, F. Sebastiano, M. Babaie, S. Pellerano, E. Charbon, and L. M. K. Vandersypen, "CMOS-based cryogenic control of silicon quantum circuits," *Nature*, vol. 593, no. 7858, pp. 205–210, May 2021.

[105] A. Esmailiyan, H. Wang, M. Asker, E. Koskin, D. Leipold, I. Bashir, K. Xu, A. Koziol, E. Blokhina, and R. B. Staszewski, "A Fully Integrated DAC for CMOS Position-Based Charge Qubits with Single-Electron Detector Loopback Testing," *IEEE Solid-State Circuits Letters*, vol. 3, pp. 354–357, 2020.

[106] J. M. Hornibrook, J. I. Colless, I. D. Conway Lamb, S. J. Pauka, H. Lu, A. C. Gossard, J. D. Watson, G. C. Gardner, S. Fallahi, M. J. Manfra, and D. J. Reilly, "Cryogenic Control Architecture for Large-Scale Quantum Computing," *Physical Review Applied*, vol. 3, no. 2, p. 024010, Feb. 2015.

[107] A. R. Mills, D. M. Zajac, M. J. Gullans, F. J. Schupp, T. M. Hazard, and J. R. Petta, "Shuttling a single charge across a one-dimensional array of silicon quantum dots," *Nature Communications*, vol. 10, no. 1, p. 1063, Mar. 2019.

[108] I. Seidler, T. Struck, R. Xue, N. Focke, S. Trellenkamp, H. Bluhm, and L. R. Schreiber, "Conveyor-mode single-electron shuttling in Si/SiGe for a scalable quantum computing architecture," Aug. 2021.

[109] J. Yoneda, W. Huang, M. Feng, C. H. Yang, K. W. Chan, T. Tanttu, W. Gilbert, R. C. C. Leon, F. E. Hudson, K. M. Itoh, A. Morello, S. D. Bartlett, A. Laucht, A. Saraiva, and A. S. Dzurak, "Coherent spin qubit transport in silicon," *Nature Communications*, vol. 12, no. 1, p. 4114, Jul. 2021.

[110] H. Flentje, P.-A. Mortemousque, R. Thalineau, A. Ludwig, A. D. Wieck, C. Bäuerle, and T. Meunier, "Coherent long-distance displacement of individual electron spins," *Nature Communications*, vol. 8, no. 1, p. 501, Sep. 2017.

[111] T. Fujita, T. A. Baart, C. Reichl, W. Wegscheider, and L. M. K. Vandersypen, "Coherent shuttle of electron-spin states," *npj Quantum Information*, vol. 3, no. 1, pp. 1–6, Jun. 2017.

[112] S. Hermelin, S. Takada, M. Yamamoto, S. Tarucha, A. D. Wieck, L. Saminadayar, C. Bäuerle, and T. Meunier, "Electrons surfing on a sound wave as a platform for quantum optics with flying electrons," *Nature*, vol. 477, no. 7365, pp. 435–438, Sep. 2011.

[113] B. Jadot, P.-A. Mortemousque, E. Chanrion, V. Thiney, A. Ludwig, A. D. Wieck, M. Urdampilleta, C. Bäuerle, and T. Meunier, "Distant spin entanglement via fast and coherent electron shuttling," *Nature Nanotechnology*, vol. 16, no. 5, pp. 570–575, May 2021.

[114] J. Wang, S. Ota, H. Edlbauer, B. Jadot, P.-A. Mortemousque, A. Richard, Y. Okazaki, S. Nakamura, A. Ludwig, A. D. Wieck, M. Urdampilleta, T. Meunier, T. Kodera, N.-H. Kaneko, S. Takada, and C. Bäuerle, "Generation of a single-cycle acoustic pulse: A scalable solution for transport in single-electron circuits," Jul. 2022.

[115] R. P. Feynman, "Simulating physics with computers," *International Journal of Theoretical Physics*, vol. 21, no. 6, pp. 467–488, Jun. 1982.

[116] Y. Wang, A. Tankasala, L. C. L. Hollenberg, G. Klimeck, M. Y. Simmons, and R. Rahman, "Highly tunable exchange in donor qubits in silicon," *npj Quantum Information*, vol. 2, no. 1, pp. 1–5, Apr. 2016.

[117] R. Zhao, T. Tanttu, K. Y. Tan, B. Hensen, K. W. Chan, J. C. C. Hwang, R. C. C. Leon, C. H. Yang, W. Gilbert, F. E. Hudson, K. M. Itoh, A. A. Kiselev, T. D. Ladd, A. Morello, A. Laucht, and A. S. Dzurak, "Single-spin qubits in isotopically enriched

silicon at low magnetic field," *Nature Communications*, vol. 10, no. 1, p. 5500, Dec. 2019.

[118] B. Hensen, W. Wei Huang, C.-H. Yang, K. Wai Chan, J. Yoneda, T. Tanttu, F. E. Hudson, A. Laucht, K. M. Itoh, T. D. Ladd, A. Morello, and A. S. Dzurak, "A silicon quantum-dot-coupled nuclear spin qubit," *Nature Nanotechnology*, vol. 15, no. 1, pp. 13–17, Jan. 2020.

[119] X. Xue, T. F. Watson, J. Helsen, D. R. Ward, D. E. Savage, M. G. Lagally, S. N. Coppersmith, M. A. Eriksson, S. Wehner, and L. M. K. Vandersypen, "Benchmarking Gate Fidelities in a $\mathrm{Si}/\mathrm{SiGe}$ Two-Qubit Device," *Physical Review X*, vol. 9, no. 2, p. 021011, Apr. 2019.

[120] W. H. Lim, H. Huebl, L. H. Willems van Beveren, S. Rubanov, P. G. Spizzirri, S. J. Angus, R. G. Clark, and A. S. Dzurak, "Electrostatically defined few-electron double quantum dot in silicon," *Applied Physics Letters*, vol. 94, no. 17, p. 173502, Apr. 2009.

[121] A. C. Betz, M. L. V. Tagliaferri, M. Vinet, M. Broström, M. Sanquer, A. J. Ferguson, and M. F. Gonzalez-Zalba, "Reconfigurable quadruple quantum dots in a silicon nanowire transistor," *Applied Physics Letters*, vol. 108, no. 20, p. 203108, May 2016.

[122] J. Duan, M. A. Fogarty, J. Williams, L. Hutin, M. Vinet, and J. J. L. Morton, "Remote Capacitive Sensing in Two-Dimensional Quantum-Dot Arrays," *Nano Letters*, vol. 20, no. 10, pp. 7123–7128, Oct. 2020.

[123] R. Li, N. I. D. Stuyck, S. Kubicek, J. Jussot, B. T. Chan, F. A. Mohiyaddin, A. Elsayed, M. Shehata, G. Simion, C. Godfrin, Y. Canvel, T. Ivanov, L. Goux, B. Govoreanu, and I. P. Radu, "A flexible 300 mm integrated Si MOS platform for electron- and hole-spin qubits exploration," in *2020 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2020, pp. 38.3.1–38.3.4.

[124] "IEEE International Roadmap for Devices and Systems - IEEE IRDS™," https://irds.ieee.org/.

[125] B. Voisin, V.-H. Nguyen, J. Renard, X. Jehl, S. Barraud, F. Triozon, M. Vinet, I. Duchemin, Y.-M. Niquet, S. de Franceschi, and M. Sanquer, "Few-Electron Edge-State Quantum Dots in a Silicon Nanowire Field-Effect Transistor," *Nano Letters*, vol. 14, no. 4, pp. 2094–2098, Apr. 2014.

[126] B. Roche, B. Voisin, X. Jehl, R. Wacquez, M. Sanquer, M. Vinet, V. Deshpande, and B. Previtali, "A tunable, dual mode field-effect or single electron transistor," *Applied Physics Letters*, vol. 100, no. 3, p. 032107, Jan. 2012.

[127] A. C. Betz, R. Wacquez, M. Vinet, X. Jehl, A. L. Saraiva, M. Sanquer, A. J. Ferguson, and M. F. Gonzalez-Zalba, "Dispersively Detected Pauli Spin-Blockade in a Silicon Nanowire Field-Effect Transistor," *Nano Letters*, vol. 15, no. 7, pp. 4622–4627, Jul. 2015.

[128] L. Hutin, R. Maurand, D. Kotekar-Patil, A. Corna, H. Bohuslavskyi, X. Jehl, S. Barraud, S. De Franceschi, M. Sanquer, and M. Vinet, "Si CMOS platform for quantum information processing," in *2016 IEEE Symposium on VLSI Technology*, Jun. 2016, pp. 1–2.

[129] S. De Franceschi, L. Hutin, R. Maurand, L. Bourdet, H. Bohuslavskyi, A. Corna, D. Kotekar-Patil, S. Barraud, X. Jehl, Y.-M. Niquet, M. Sanquer, and M. Vinet, "SOI technology for quantum information processing," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2016, pp. 13.4.1–13.4.4.

[130] M. Urdampilleta, D. J. Niegemann, E. Chanrion, B. Jadot, C. Spence, P.-A. Mortemousque, C. Bäuerle, L. Hutin, B. Bertrand, S. Barraud, R. Maurand, M. Sanquer, X. Jehl, S. De Franceschi, M. Vinet, and T. Meunier, "Gate-based high fidelity spin readout in a CMOS device," *Nature Nanotechnology*, vol. 14, no. 8, pp. 737–741, Aug. 2019.

[131] G. J. Podd, S. J. Angus, D. A. Williams, and A. J. Ferguson, "Charge sensing in intrinsic silicon quantum dots," *Applied Physics Letters*, vol. 96, no. 8, p. 082104, Feb. 2010.

[132] W. G. van der Wiel, S. De Franceschi, J. M. Elzerman, T. Fujisawa, S. Tarucha, and L. P. Kouwenhoven, "Electron transport through double quantum dots," *Reviews of Modern Physics*, vol. 75, no. 1, pp. 1–22, Dec. 2002.

[133] C. H. Yang, W. H. Lim, F. A. Zwanenburg, and A. S. Dzurak, "Dynamically controlled charge sensing of a few-electron silicon quantum dot," *AIP Advances*, vol. 1, no. 4, p. 042111, Dec. 2011.

[134] E. P. Nordberg, H. L. Stalford, R. Young, G. A. Ten Eyck, K. Eng, L. A. Tracy, K. D. Childs, J. R. Wendt, R. K. Grubbs, J. Stevens, M. P. Lilly, M. A. Eriksson, and M. S. Carroll, "Charge sensing in enhancement mode double-top-gated metal-oxide-semiconductor quantum dots," *Applied Physics Letters*, vol. 95, no. 20, p. 202102, Nov. 2009.

[135] T. M. Buehler, V. Chan, A. J. Ferguson, A. S. Dzurak, F. E. Hudson, D. J. Reilly, A. R. Hamilton, R. G. Clark, D. N. Jamieson, C. Yang, C. I. Pakes, and S. Prawer, "Controlled single electron transfer between Si:P dots," *Applied Physics Letters*, vol. 88, no. 19, p. 192101, May 2006.

[136] A. C. Johnson, J. R. Petta, C. M. Marcus, M. P. Hanson, and A. C. Gossard, "Singlet-triplet spin blockade and charge sensing in a few-electron double quantum dot," *Physical Review B*, vol. 72, no. 16, p. 165308, Oct. 2005.

[137] T. Thorbeck and N. M. Zimmerman, "Formation of strain-induced quantum dots in gated semiconductor nanostructures," *AIP Advances*, vol. 5, no. 8, p. 087107, Aug. 2015.

[138] C. Herring and E. Vogt, "Transport and Deformation-Potential Theory for Many-Valley Semiconductors with Anisotropic Scattering," *Physical Review*, vol. 101, no. 3, pp. 944–961, Feb. 1956.

[139] M. V. Fischetti and S. E. Laux, "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys," *Journal of Applied Physics*, vol. 80, no. 4, pp. 2234–2252, Aug. 1996.

[140] T. Nakajima, M. R. Delbecq, T. Otsuka, P. Stano, S. Amaha, J. Yoneda, A. Noiri, K. Kawasaki, K. Takeda, G. Allison, A. Ludwig, A. D. Wieck, D. Loss, and S. Tarucha, "Robust Single-Shot Spin Measurement with 99.5% Fidelity in a Quantum Dot Array," *Physical Review Letters*, vol. 119, no. 1, p. 017701, Jul. 2017.

[141] D. M. Zajac, T. M. Hazard, X. Mi, E. Nielsen, and J. R. Petta, "Scalable Gate Architecture for a One-Dimensional Array of Semiconductor Spin Qubits," *Physical Review Applied*, vol. 6, no. 5, p. 054013, Nov. 2016.

[142] R. Pillarisetty, H. C. George, T. F. Watson, L. Lampert, N. Thomas, S. Bojarski, P. Amin, R. Caudillo, E. Henry, N. Kashani, P. Keys, R. Kotlyar, F. Luthi, D. Michalak, K. Millard, J. Roberts, J. Torres, O. Zietz, T. Krähenmann, A. M. Zwerver, M. Veldhorst, G. Scappucci, L. M. K. Vandersypen, and J. Clarke, "High Volume Electrical Characterization of Semiconductor Qubits," in *2019 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2019, pp. 31.5.1–31.5.4.

[143] W. Pauli, "Über den Einfluß der Geschwindigkeitsabhängigkeit der Elektronenmasse auf den Zeemaneffekt," *Zeitschrift für Physik*, vol. 31, no. 1, pp. 373–385, Feb. 1925.

[144] V. N. Golovach, M. Borhani, and D. Loss, "Electric-dipole-induced spin resonance in quantum dots," *Physical Review B*, vol. 74, no. 16, p. 165319, Oct. 2006.

[145] M. Pioro-Ladrière, T. Obata, Y. Tokura, Y.-S. Shin, T. Kubo, K. Yoshida, T. Taniyama, and S. Tarucha, "Electrically driven single-electron spin resonance in a slanting Zeeman field," *Nature Physics*, vol. 4, no. 10, pp. 776–779, Oct. 2008.

[146] A. Kha, R. Joynt, and D. Culcer, "Do micromagnets expose spin qubits to charge and Johnson noise?" *Applied Physics Letters*, vol. 107, no. 17, p. 172101, Oct. 2015.

[147] M. F. Gonzalez-Zalba, S. de Franceschi, E. Charbon, T. Meunier, M. Vinet, and A. S. Dzurak, "Scaling silicon-based quantum computing using CMOS technology," *Nature Electronics*, vol. 4, no. 12, pp. 872–884, Dec. 2021.

[148] S. Nadj-Perge, S. M. Frolov, E. P. a. M. Bakkers, and L. P. Kouwenhoven, "Spin–orbit qubit in a semiconductor nanowire," *Nature*, vol. 468, no. 7327, pp. 1084–1087, Dec. 2010.

[149] G. Scappucci, C. Kloeffel, F. A. Zwanenburg, D. Loss, M. Myronov, J.-J. Zhang, S. De Franceschi, G. Katsaros, and M. Veldhorst, "The germanium quantum information route," *Nature Reviews Materials*, vol. 6, no. 10, pp. 926–943, Oct. 2021.

[150] F. N. M. Froning, L. C. Camenzind, O. A. H. van der Molen, A. Li, E. P. A. M. Bakkers, D. M. Zumbühl, and F. R. Braakman, "Ultrafast hole spin qubit with gate-tunable spin–orbit switch functionality," *Nature Nanotechnology*, vol. 16, no. 3, pp. 308–312, Mar. 2021.

[151] D. Kim, D. R. Ward, C. B. Simmons, D. E. Savage, M. G. Lagally, M. Friesen, S. N. Coppersmith, and M. A. Eriksson, "High-fidelity resonant gating of a silicon-based quantum dot hybrid qubit," *npj Quantum Information*, vol. 1, no. 1, pp. 1–6, Oct. 2015.

[152] M. Benito, X. Croot, C. Adelsberger, S. Putz, X. Mi, J. R. Petta, and G. Burkard, "Electric-field control and noise protection of the flopping-mode spin qubit," *Physical Review B*, vol. 100, no. 12, p. 125430, Sep. 2019.

[153] X. Croot, X. Mi, S. Putz, M. Benito, F. Borjans, G. Burkard, and J. R. Petta, "Flopping-mode electric dipole spin resonance," *Physical Review Research*, vol. 2, no. 1, p. 012006, Jan. 2020.

[154] S. Bosco, M. Benito, C. Adelsberger, and D. Loss, "Squeezed hole spin qubits in Ge quantum dots with ultrafast gates at low power," *Physical Review B*, vol. 104, no. 11, p. 115425, Sep. 2021.

[155] R. C. C. Leon, C. H. Yang, J. C. C. Hwang, J. Camirand Lemyre, T. Tanttu, W. Huang, J. Y. Huang, F. E. Hudson, K. M. Itoh, A. Laucht, M. Pioro-Ladrière, A. Saraiva, and A. S. Dzurak, "Bell-state tomography in a silicon many-electron artificial molecule," *Nature Communications*, vol. 12, no. 1, p. 3228, May 2021.

[156] E. I. Rashba and V. I. Sheka, "Electric-Dipole Spin Resonances," Nov. 2018.

[157] J. P. Dehollain, J. J. Pla, E. Siew, K. Y. Tan, A. S. Dzurak, and A. Morello, "Nanoscale broadband transmission lines for spin qubit control," *Nanotechnology*, vol. 24, no. 1, p. 015202, Dec. 2012.

[158] P. Becker, H.-J. Pohl, H. Riemann, and N. Abrosimov, "Enrichment of silicon for a better kilogram," *physica status solidi (a)*, vol. 207, no. 1, pp. 49–66, 2010.

[159] K. M. Itoh and H. Watanabe, "Isotope engineering of silicon and diamond for quantum computing and sensing applications," *MRS Communications*, vol. 4, no. 4, pp. 143–157, Dec. 2014.

[160] X. Hao, R. Ruskov, M. Xiao, C. Tahan, and H. Jiang, "Electron spin resonance and spin–valley physics in a silicon double quantum dot," *Nature Communications*, vol. 5, no. 1, p. 3860, May 2014.

[161] L. Bourdet and Y.-M. Niquet, "All-electrical manipulation of silicon spin qubits with tunable spin-valley mixing," *Physical Review B*, vol. 97, no. 15, p. 155433, Apr. 2018.

[162] W. Huang, M. Veldhorst, N. M. Zimmerman, A. S. Dzurak, and D. Culcer, "Electrically driven spin qubit based on valley mixing," *Physical Review B*, vol. 95, no. 7, p. 075403, Feb. 2017.

[163] P. Huang and X. Hu, "Fast spin-valley-based quantum gates in Si with micromagnets," *npj Quantum Information*, vol. 7, no. 1, pp. 1–8, Nov. 2021.

[164] J. Kyriakidis and G. Burkard, "Universal quantum computing with correlated spin-charge states," *Physical Review B*, vol. 75, no. 11, p. 115324, Mar. 2007.

[165] H. E. Ercan, S. N. Coppersmith, and M. Friesen, "Strong electron-electron interactions in Si/SiGe quantum dots," *Physical Review B*, vol. 104, no. 23, p. 235302, Dec. 2021.

[166] J. C. Abadillo-Uriel, B. Martinez, M. Filippone, and Y.-M. Niquet, "Two-body Wigner molecularization in asymmetric quantum dot spin qubits," *Phys. Rev. B*, vol. 104, no. 19, p. 195305, Nov. 2021.

[167] E. Knill, D. Leibfried, R. Reichle, J. Britton, R. B. Blakestad, J. D. Jost, C. Langer, R. Ozeri, S. Seidelin, and D. J. Wineland, "Randomized benchmarking of quantum gates," *Physical Review A*, vol. 77, no. 1, p. 012307, Jan. 2008.

[168] E. Nielsen, J. K. Gamble, K. Rudinger, T. Scholten, K. Young, and R. Blume-Kohout, "Gate Set Tomography," *Quantum*, vol. 5, p. 557, Oct. 2021.

[169] W. Yao, R.-B. Liu, and L. J. Sham, "Theory of Control of the Spin-Photon Interface for Quantum Networks," *Physical Review Letters*, vol. 95, no. 3, p. 030504, Jul. 2005.

[170] D. Jaksch, J. I. Cirac, P. Zoller, S. L. Rolston, R. Côté, and M. D. Lukin, "Fast Quantum Gates for Neutral Atoms," *Physical Review Letters*, vol. 85, no. 10, pp. 2208–2211, Sep. 2000.

[171] E. Crane, A. Schuckert, N. H. Le, and A. J. Fisher, "Rydberg entangling gates in silicon," *Physical Review Research*, vol. 3, no. 3, p. 033086, Jul. 2021.

[172] A. Sørensen and K. Mølmer, "Quantum Computation with Ions in Thermal Motion," *Phys. Rev. Lett.*, vol. 82, no. 9, pp. 1971–1974, Mar. 1999.

[173] G. Tosi, F. A. Mohiyaddin, V. Schmitt, S. Tenberg, R. Rahman, G. Klimeck, and A. Morello, "Silicon quantum processor with robust long-distance qubit couplings," *Nature Communications*, vol. 8, no. 1, p. 450, Sep. 2017.

[174] T. Tanttu, B. Hensen, K. W. Chan, C. H. Yang, W. W. Huang, M. Fogarty, F. Hudson, K. Itoh, D. Culcer, A. Laucht, A. Morello, and A. Dzurak, "Controlling Spin-Orbit Interactions in Silicon Quantum Dots Using Magnetic Field Direction," *Phys. Rev. X*, vol. 9, no. 2, p. 021028, May 2019.

[175] R. Ruskov, M. Veldhorst, A. S. Dzurak, and C. Tahan, "Electron g-factor of valley states in realistic silicon quantum dots," *Physical Review B*, vol. 98, no. 24, p. 245424, Dec. 2018.

[176] R. Ferdous, K. W. Chan, M. Veldhorst, J. C. C. Hwang, C. H. Yang, H. Sahasrabudhe, G. Klimeck, A. Morello, A. S. Dzurak, and R. Rahman, "Interface-

induced spin-orbit interaction in silicon quantum dots and prospects for scalability," *Physical Review B*, vol. 97, no. 24, p. 241401, Jun. 2018.

[177] A. Hosseinkhani and G. Burkard, "Electromagnetic control of valley splitting in ideal and disordered Si quantum dots," *Physical Review Research*, vol. 2, no. 4, p. 043180, Nov. 2020.

[178] B. Tariq and X. Hu, "Effects of interface steps on the valley-orbit coupling in a Si/SiGe quantum dot," *Physical Review B*, vol. 100, no. 12, p. 125309, Sep. 2019.

[179] P. Boross, G. Széchenyi, D. Culcer, and A. Pályi, "Control of valley dynamics in silicon quantum dots in the presence of an interface step," *Physical Review B*, vol. 94, no. 3, p. 035438, Jul. 2016.

[180] J. K. Gamble, P. Harvey-Collard, N. T. Jacobson, A. D. Baczewski, E. Nielsen, L. Maurer, I. Montaño, M. Rudolph, M. S. Carroll, C. H. Yang, A. Rossi, A. S. Dzurak, and R. P. Muller, "Valley splitting of single-electron Si MOS quantum dots," *Applied Physics Letters*, vol. 109, no. 25, p. 253101, Dec. 2016.

[181] D. Culcer, X. Hu, and S. Das Sarma, "Interface roughness, valley-orbit coupling, and valley manipulation in quantum dots," *Physical Review B*, vol. 82, no. 20, p. 205315, Nov. 2010.

[182] A. Hosseinkhani and G. Burkard, "Relaxation of single-electron spin qubits in silicon in the presence of interface steps," *Physical Review B*, vol. 104, no. 8, p. 085309, Aug. 2021.

[183] A. L. Saraiva, M. J. Calderón, R. B. Capaz, X. Hu, S. Das Sarma, and B. Koiller, "Intervalley coupling for interface-bound electrons in silicon: An effective mass study," *Physical Review B*, vol. 84, no. 15, p. 155320, Oct. 2011.

[184] M. O. Nestoklon, L. E. Golub, and E. L. Ivchenko, "Spin and valley-orbit splittings in SiGe/Si heterostructures," *Physical Review B*, vol. 73, no. 23, p. 235334, Jun. 2006.

[185] M. Veldhorst, R. Ruskov, C. H. Yang, J. C. C. Hwang, F. E. Hudson, M. E. Flatté, C. Tahan, K. M. Itoh, A. Morello, and A. S. Dzurak, "Spin-orbit coupling and operation of multivalley spin qubits," *Physical Review B*, vol. 92, no. 20, p. 201401, Nov. 2015.