Published by IOP Publishing for Sissa Medialab

Received: *November 2, 2024*
Accepted: *March 5, 2025*
Published: *April 10, 2025*

Topical Workshop on Electronics for Particle Physics
University of Glasgow, Scotland, U.K.
30 September–4 October 2024

An ASIC for ToF-PET application with MCP-PMTs

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Abstract: The micro-channel plate photomultiplier tube (MCP-PMT) demonstrates excellent sensitivity to single photoelectrons, with a rise time of less than 100 ps. It offers an exceptionally low transit time spread, around 10 ps for multi-photoelectrons and under 50 ps for single photoelectrons. This performance has the potential to enhance coincidence timing, improving image quality in positron emission tomography (PET) and advancing next-generation physics experiments. To meet the stringent demands of picosecond-level time resolution, we developed a prototype frond-end circuit, the FPMROC, designed to accurately measure the time of arrival from the MCP-PMT with a gain of 10^5. For a target coincidence time resolution of 100 ps, the MCP-PMT contribution is limited to approximately 30 ps, requiring the FPMROC jitter to remain below 10 ps. The FPMROC is implemented using a 55 nm CMOS process and integrates 8 readout channels, a data builder, a high-speed serializer, periphery, and test circuits. Each channel comprises a low-noise preamplifier, discriminator, and time-to-digital

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https://doi.org/10.1088/1748-0221/20/04/C04024

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converter (TDC) for both time of arrival and time-over-threshold measurements. Digital-to-analog converters, a phase-locked loop, and an serial peripheral interface are used for calibration and threshold adjustment, providing low jitter clocks, and slow control, respectively. Additionally, a charge injection circuit is incorporated for testing and calibration. A prototype design was submitted in July 2024, and the following sections present the architecture, key circuits and simulation results.

Keywords: Front-end electronics for detector readout; Gamma camera, SPECT, PET PET/CT, coronary CT angiography (CTA); Photon detectors for UV, visible and IR photons (solid-state) (PIN diodes, APDs, Si-PMTs, G-APDs, CCDs, EBCCDs, EMCCDs, CMOS imagers, etc); Timing detectors

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Contents

1 Introduction

The micro-channel plate photomultiplier tube (MCP-PMT) is a photosensitive device capable of detecting single photons with excellent time resolution, commonly referred to as the Fast-PMT (FPMT) [1]. Its outstanding time resolution makes it widely applicable across various fields, including high-energy physics, high precision medical imaging device [2], biofluorescence detection [3] and nucleic acid detection devices [4]. The transit time spread (TTS) is remarkably low, measuring around 10 ps for multi-photoelectrons and less than 50 ps for single photoelectrons. To meet the demands of picosecond-level time resolution, we have developed a prototype front-end circuit called FPMROC. This circuit is designed to measure the time of arrival from the MCP-PMT with a gain of 10^5 and also records the time-over-threshold (TOT) to enable time-walk correction.

The FPMROC prototype includes 8 complete readout channels, with each channel comprising the following components: a low-noise preamplifier, a discriminator, and a time-to-digital converter (TDC) for both time of arrival (TOA) and time over threshold (TOT) measurements. The event rate of each channel can reach to 100% occupancy with 40 MHz for our system. A data event builder is integrated to manage data flow, along with fast data serialization and data driver for output. The TOT is employed to correct the time walk effect in the TOA measurements [5]. Peripheral circuits include digital-to-analog converters (DACs) for calibration and threshold adjustment, a phase-locked loop (PLL) to generate high-quality clocks, and a serial peripheral interface (SPI) module for slow control. Additionally, the prototype incorporates a charge injection circuit for testing and calibration.

2 Design

Figure 1 presents the block diagram of the FPMROC ASIC (application-specific integrated-circuits). Eight channels collectively utilize a data event builder for buffering, framing, scrambling and encoding parallel data from various channels. The ASIC includes a serializer for off-chip data transmission at a rate of 10.24 Gbps, and a low-jitter LC-based PLL for the generation of 5.12 GHz and 40 MHz clocks for the serializer and TDCs, respectively. Additionally, an SPI is integrated to provide configurations up to 200 bits.

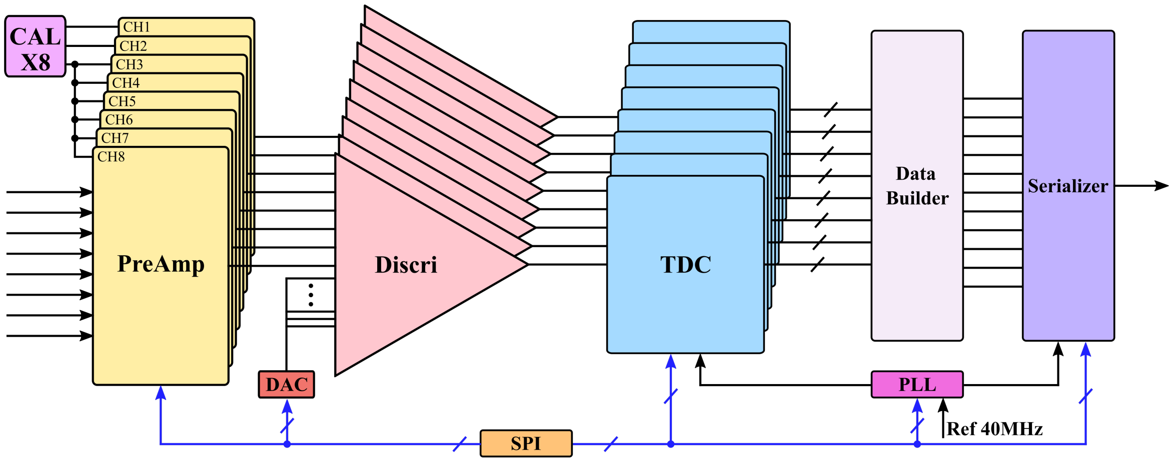

Figure 1. Block diagram of the FPMROC.

2.1 Front-end circuit

Two types of preamplifiers are implemented in the FPMROC. The first design employs a 4-stage amplifier to saturate the signal, where each stage offers high bandwidth but low gain, as illustrated in figure 2(a). The second design incorporates a classic trans-impedance amplifier (TIA) that provides higher gain but operates at a slower speed, as shown in figure 2(b). Both designs maintain an input impedance of approximately 50 Ω to ensure proper impedance matching [6].

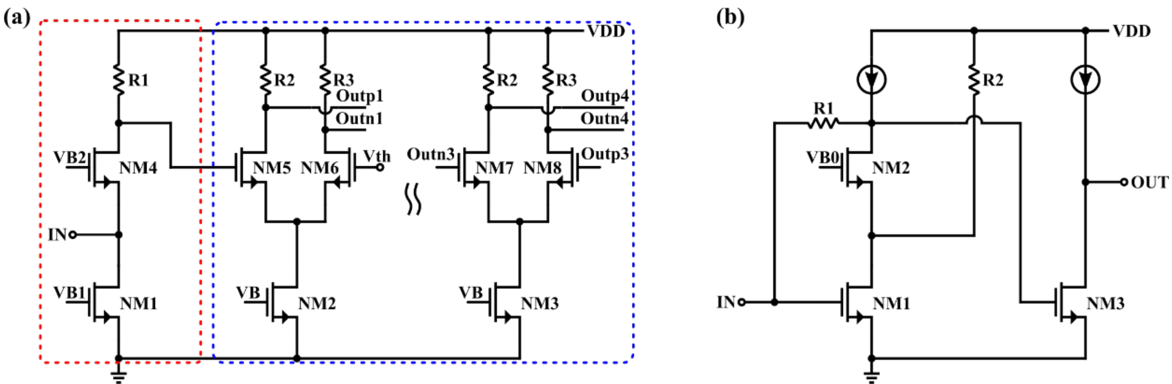

Figure 2. (a) Schematic of the saturated amplifier, (b) Schematic of the trans-impedance amplifier.

The discriminator converts analog pulses from the preamplifier into digital signals. It comprises a four-stage preamplifier and a comparator with programmable hysteresis. The preamplifier stages amplify small input pulses to a level suitable for reliable processing by the comparator. The comparator digitizes the differential input at the crossing point, with the hysteresis providing adjustable noise immunity. The hysteresis helps prevent false triggering near the threshold ensuring robust signal detection.

2.2 Time-to-digital converter

The TDC block utilizes 11 voltage-controlled differential delay cells, which construct a ring oscillator using an interpolator approach, as shown in figure 3. Each delay cell is designed to facilitate precise time measurements by integrating interpolated differential delay cells for fine time resolution, combined

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with two sets of ripple counters for coarse time measurement. To address propagation variations, a self-calibration mechanism is implemented that records timestamps twice. This approach utilizes two recorders, constructed as chains of D-flip-flops (DFFs), to capture snapshots of both fine and coarse time for TOA (TOA_Code[11:0]) and TOT (TOT_Code[7:0]) measurements, as well as for calibration purposes (CAL_Code[10:0]).

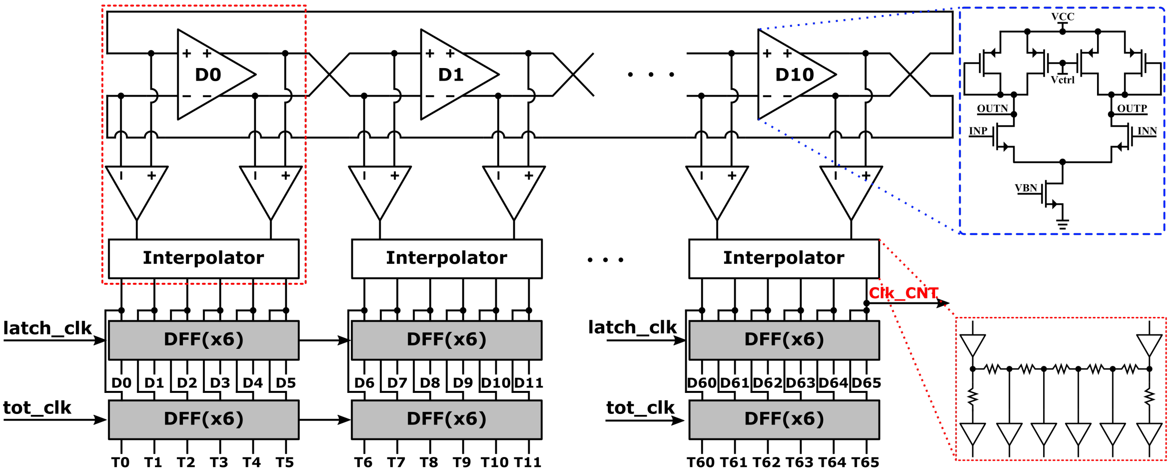

Figure 3. The architecture of the TDC delay line.

The delay cell is a voltage-controlled differential amplifier (VCDA) as shown in blue dashed block of the figure 3. The VCDA has a propagation delay of approximately 55.08 ps. In order to achieve a bin size of around 9.2 ps, a 6-stage passive interpolator is designed to divide the propagation delay accordingly as shown in the red dashed box.

2.3 Event data builder

The event data builder receives data from eight TDC channels, along with a 320 MHz synchronous clock from the serializer, to generate 64-bit parallel data at a rate of 160 Mbps. Figure 4 gives the scheme and data frame architecture. Two-level FIFOs are employed for data storage and aggregation. A frame builder retrieves and combines the data, which is subsequently forwarded to a 64B66B encoder incorporating scrambling algorithms from 10 Gigabit Ethernet to maintain DC balance within the data stream. Ultimately, a gearbox ensures alignment with the data rate and width requirements of the high-speed serializer.

2.4 PLL and serializer

Figure 5 shows the architecture of the PLL and serializer. Both designs have been silicon-proven and modified for this specific application. The PLL mainly comprises a phase-frequency detector (PFD), a charge pump (CP), an LC-based voltage-controlled oscillator (LC-VCO), a low-pass filter (LPF), dividers and buffers [7]. The serializer facilitates the conversion of 64 bits into a pair of differential serial outputs by employing four low-speed CMOS-logic 16:4 subunits, four CMOS-logic 4:1 subunits, and a high-speed current-mode logic (CML) multiplexer paired with a driver. A PRBS15 (pseudorandom binary sequence) generator is also integrated in the serializer for fast self-tests. Figure 6 shows the overall layout, which occupies an area of $2.2 \times 3.4\,\mathrm{mm}^2$.

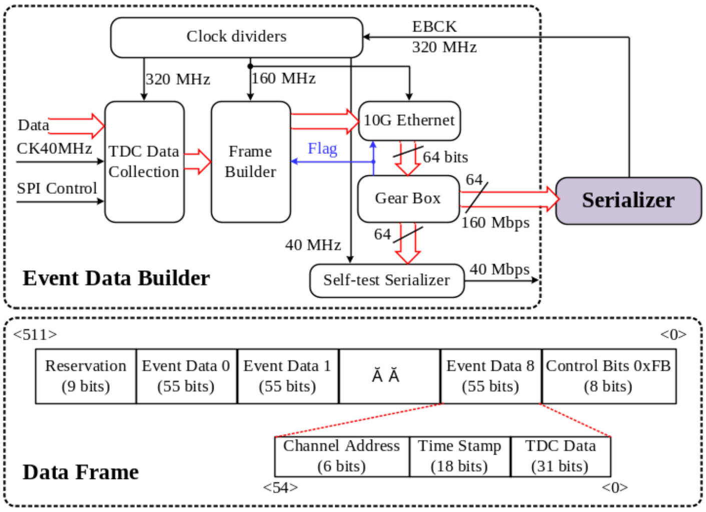

Figure 4. The scheme and data frame of the event data builder.

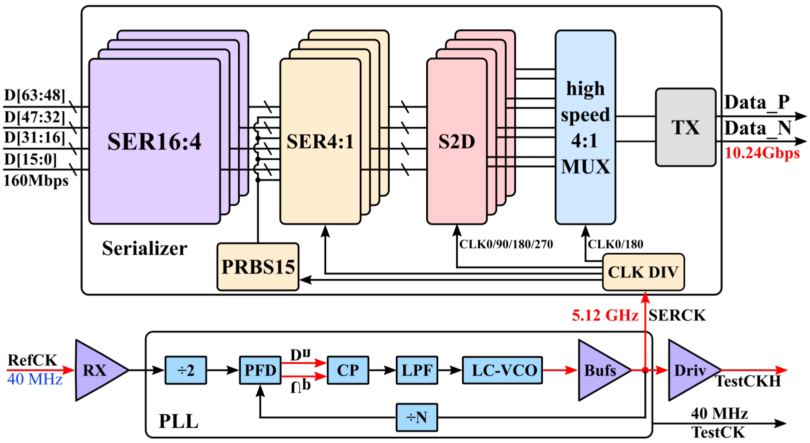

Figure 5. The block diagram of the PLL and serializer.

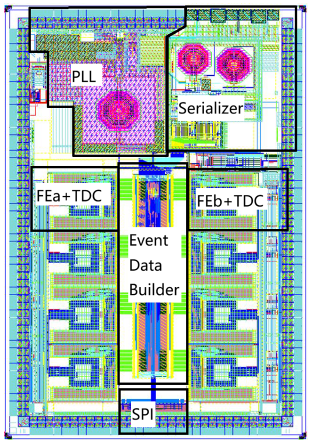

Figure 6. The chip layout.

3 Simulation results

The capacitance *Cs* for the MCP-PMT is estimated to be approximately 4 pF. A stimulus input charge of 16 fC is injected during the simulation, characterized by rise and falls times of 100 ps and a pulse width of 100 ps. A total of 400 transient noise simulations were conducted for both front-end schemes. The total jitter of the discriminator for both schemes is less than 18 ps, as shown in figure 7. For the preamplifier in the first scheme, the root mean square (RMS) noise is 158 µV, with a slop of 67 V/µs. In contrast, the RMS noise for the second scheme is 508 µV, with a slop of 145 V/µs.

The transfer function of the TDC is illustrated in figure 8(a). In the TOA measurement, the TOA denotes the time interval between the rising edge of 40 MHz clock and the rising edge of input pulse. The arrival time of the input pulse increases in fixed steps of 1 ps with each clock cycle. A minimum-square linear fitting of the measured data is also shown in figure 8(a) (dashed blue line). The fitting curve indicates that the TDC achieves a time resolution of 9.18 ps, which means for a signal with a width of 100 ps, the charge resolution is estimated about 10%. The integral nonlinearity (INL) quantifies the deviation of each stair center in the transfer function from the expected time. Figure 8(b)

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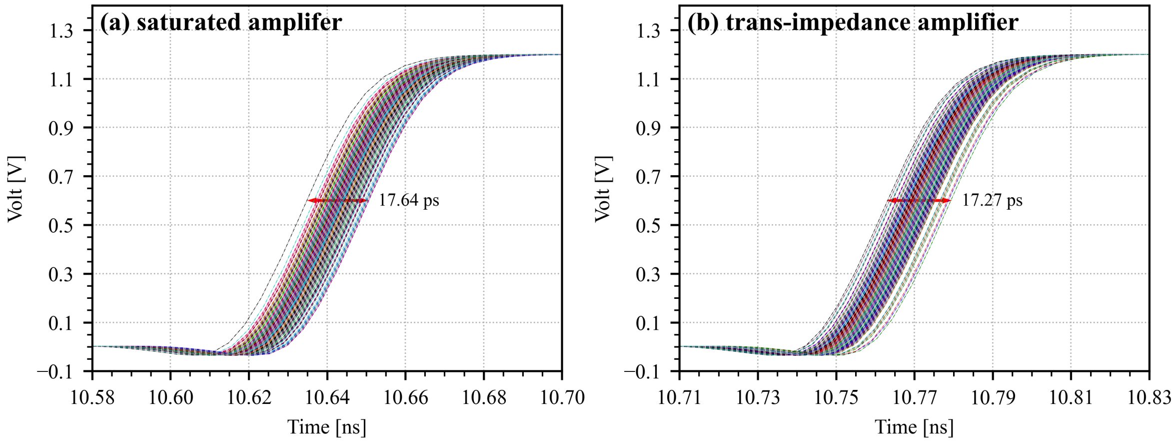

Figure 7. Transient noise simulation for output of preamplifier.

shows the INL and differential nonlinearity (DNL) of the TDC. According to the simulations, the INL of the delay line is less than ±0.6 least significant bit (LSB), and the DNL is less than ±0.7 LSB. Performing Monte Carlo simulations for mismatch of transistor and resistor on the delay line circuit yields a standard deviation of bin size as small as 28.7 fs and a mean value of bin size about 9.26 ps that is very close to the resolution of 9.18 ps as shown in figure 8(a), indicating that the impact of mismatch on INL and DNL is significantly less than 1 LSB.

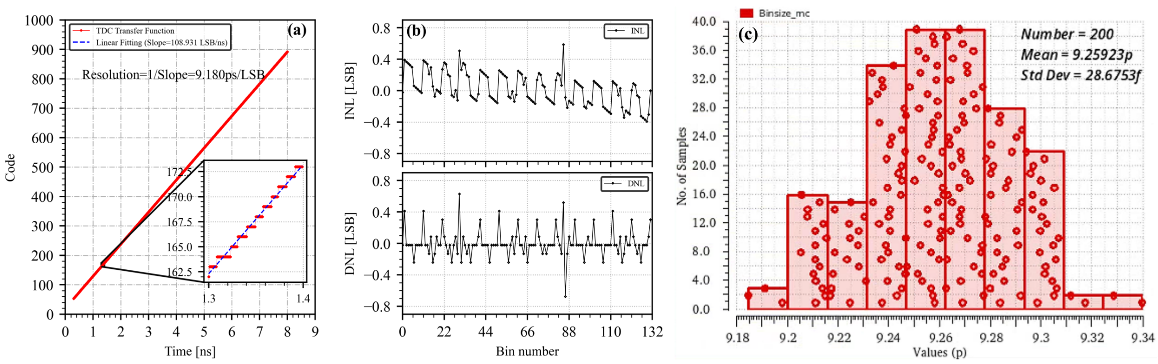

Figure 8. (a) TDC transfer function curve, (b) DNL and INL of the delay line, (c) bin size Monte Carlo simulation.

Since the PLL has been silicon-proven, detailed performance metrics can be found in the reference [7], which indicates a total jitter less than 7.5 ps. Furthermore, a spectrum analyzer (Agilent N9320B) was used to characterize the phase noise performance of the frequency-halved output clock (2.56 GHz), with a corresponding measurement shown in figure 9(a). Figure 9(b) presents a clear eye diagram, simulated at 10.24 Gbps, of the modified serializer, while the earlier design has been verified with a measured total jitter of less than 43 ps.

The power consumption of each block in FPMROC is listed in table 1.

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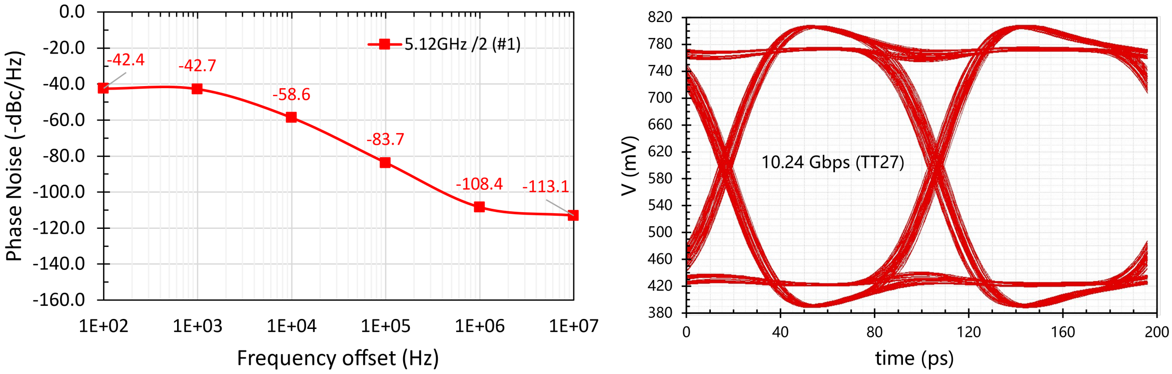

(a) Phase noise measurement of the divide-by-2 output clock

(b) 10.24-Gbps eye diagram

Figure 9. Performance of the PLL and serializer.

Table 1. Power consumption of each block in FPMROC based on post-layout simulation.

Block name	**Power consumption (mW)**	
	1st Scheme	2nd Scheme
Preamplifier	1.8	3.6
Discriminator	2.0	0.6
TDC	21.8	
PLL	28.0	
Event Builder	40.0	
Serializer	194.4	

4 Conclusions

We have developed a prototype chip, designed as FPMROC, for time measurement that features eight channels, making it suitable for ToF-PET and other physics experiment applications. Two schemes of preamplifiers have been implemented. The jitter performance of two scheme is very close because the ratio of noise to slope of signal edge is similar with a capacitance of 4 pF, though the first scheme is faster without Cs. The second scheme is preferred in the final implementation because a larger amplitude of output provides a greater margin for threshold noise. The time-to-digital converter can achieve a nominal bin size of 9.2 ps by using a differential ring oscillator and a passive interpolator. The chip is expected to be delivered by the end of November 2024, and we are currently preparing the test board and test platform.

Acknowledgments

This work was supported by the Research Foundation of the Education Bureau of Hubei province, China (Grant No. Q20231713), and the funding of the independent deployment project of Institute of High Energy Physics, Chinese Academy of Sciences (No. 2023000134). It was also partially funded by the National Natural Science Foundation of China (No. 12005245).

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