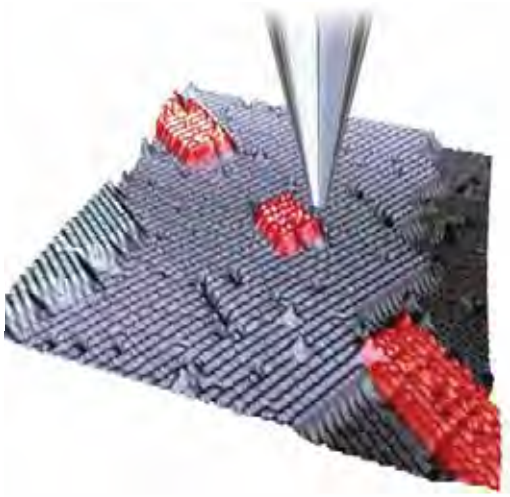
Precision Few-Electron Silicon Quantum Dots



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Certificate of Originality

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Cover art: 3D rendering of a STM image showing a hydrogen terminated silicon surface which has been selectively depassivated to form a few-electron quantum dot with source and drain leads (see chapter 6).

An electronic version of this thesis, including colour figures, is available at:
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Abstract

We demonstrate the successful down-scaling of donor-based silicon quantum dot structures to the single donor limit. These planar devices are realized in ultra high vacuum (UHV) by means of scanning tunneling microscope (STM) based hydrogen lithography which – in combination with a gaseous dopant source and a thermal silicon source – allows for the patterning of highly-doped planar Si:P structures with sub-nm precision encapsulated in a single-crystal environment.

We present advancements of the alignment strategy for patterning *ex-situ* metallic contacts and top gates over the buried dopant devices. Here, we use a hierarchical array of etched registration markers. A key feature of the alignment process is the controlled formation of atomically flat plateaus several hundred nanometers in diameter that allows the active region of the device to be patterned on a single atomic Si(100) plane at a precisely known position.

We present a multiterminal Si:P quantum dot device in the many-electron regime. Coplanar regions of highly doped silicon are used to gate the quantum dot potential resulting in highly stable Coulomb blockade oscillations. We compare the use of these all epitaxial in-plane gates with conventional metallic surface gates and find superior stability of the former. We highlight the challenges of down-scaling within a planar architecture and show how capacitance modeling can be used to optimize the tunability of quantum dot devices. Based on these results, we demonstrate the fabrication of an in-plane gated few-donor quantum dot device which shows highly stable Coulomb blockade oscillations as well as a surprisingly dense excitation spectrum on the scale of 100 μeV. We explain how these low-energy resonances arise from transport through valley-split states of the silicon quantum dot providing extensive effective mass calculations to support our findings.

Finally, we describe how STM H-lithography can be used to incorporate individual impurities at precisely known positions within a gated device and demonstrate transport through a single phosphorus donor. We find a bulk-like charging energy as well as clear indications for bulk-like excited states. We highlight the potential of this technology to realize elementary building blocks for future donor-based quantum computation applications in silicon.

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List of Publications

Journal articles

M. Fuechsle, S. Mahapatra, F. A. Zwanenburg, Mark Friesen, M. A. Eriksson, M. Y. Simmons, Spectroscopy of few-electron single-crystal silicon quantum dots, *Nature Nanotech.* **5**, 505 (2010).

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Abbreviations

1D, 2D, 3D	one-, two-, three-dimensional
2T, 4T	two-, four-terminal
CB	Coulomb blockade
CMOS	complementary metal-oxide-semiconductor
DC	direct current
DOS	density of states
EBL	electron beam lithography
EMT	effective mass theory
FET	field-effect transistor
IVC	inner vacuum chamber
mK	milli-Kelvin
ML	monolayer
MOSFET	metal-oxide-semiconductor field-effect transistor
qubit	quantum bit
RIE	reactive ion etching
RT	room temperature (293 K)
RTS	random telegraph signal
SEM	scanning electron microscope/microscopy
SET	single-electron transistor/tunneling
Si:P	phosphorus doped silicon
SOI	silicon on insulator
STM	scanning tunneling microscope/microscopy
TEM	transmission electron microscope/microscopy
UHV	ultra-high vacuum

Chapter 1

Introduction

Down-scaling has been the leading paradigm of the semiconductor industry ever since the invention of the first transistor in 1947 [1]. Miniaturization of the single most important building block of modern silicon-based electronic devices – the field-effect transistor (FET) – has advanced to a stage where device performance can depend on the number and the discrete distribution of individual dopants [2] with channel lengths approaching the 10nm-scale [3]. Consequently, the ability to control dopant density and distribution on a sub-nm level is a key challenge for further scaling of conventional integrated nanoelectronic devices. The realization that "traditional" miniaturization of conventional silicon devices by geometric scaling will soon reach its ultimate limit (set by the discreteness of matter) has lead to intensified research in alternative approaches to further enhance the computational power of logic devices. One of the most exciting of these emerging technologies is *quantum computation* – a drastically novel concept of computation that goes far beyond digital logic.

Richard Feynman was amongst the first to realize the potential of the peculiar nature of quantum mechanics for computational purposes, suggesting in the early 1980's [4] that a quantum computer may be used to efficiently simulate quantum mechanical systems. The field of quantum computation received wider interest with the development of several quantum algorithms that allow for efficient solutions to problems that are considered computationally hard on a classical computer. Arguably the most famous examples in this regard are Shor's algorithm [5] for prime factorization of large numbers and Grover's algorithm [6] for searching in large databases.

A key element of quantum computation is the concept of *superposition*. Consider a two-level system characterized by the two states $|1\rangle$ and $|0\rangle$. A classical system will always be in one of the two discrete states. By contrast, a quantum two-level system can be in

any superposition, or linear combination $\alpha|1\rangle + \beta|0\rangle$ of these basis states, where α and β are complex numbers and $|\alpha|^2 + |\beta|^2 = 1$. It is these quantum states of a suitable two-level quantum-mechanical system that form the elementary building block of a quantum computer – a quantum bit or *qubit*.

The qubit represents the full quantum-mechanical phase information of the system. However, by measuring the system (by coupling it to a suitable measurement apparatus) the system is forced into one of its eigenstates. Any measurement therefore destroys the superposition in a probabilistic way: while the outcome of a single measurement is non-deterministic, the probability for measuring the eigenstates $|1\rangle$ and $|0\rangle$ are given by $|\alpha|^2$ and $|\beta|^2$, respectively. One of the greatest challenges in realizing a functional quantum computer is thus the need to preserve the coherent state of the superpositions, i.e. the relative phase information defining the qubits. In particular, the corresponding coherence times must be much longer than the typical time needed to perform logical operation on the qubits. This requires the system to be sufficiently isolated from its environment since any unwanted interactions with the external world might cause quantum decoherence.

One of the intriguing features of quantum computation is the fact that the governing quantum mechanics are universal and therefore independent of the physical implementation of a quantum computer. As a result, qubit architectures are being pursued in a wide and diverse variety of systems, such as ion traps [7], quantum-optical systems [8], atoms trapped in photon cavities described by cavity quantum electrodynamics (CQED) [9], or nuclear magnetic resonance (NMR) schemes using molecules in solution [10]. The latter received wide-spread interest in 2001 when a group at IBM Almaden Research Center reported the first successful demonstration of Shor's algorithm [11]. By using NMR techniques on a 7-qubit system (defined by the nuclear spins of a molecule) Vandersypen *et al.* were able to factorize the number 15 into its prime factors 3 and 5.

Alternatively, qubits have also been proposed in several solid-state systems. Considering the stringent need to protect the qubits from decoherence, solid-state qubits may not seem ideal due to the inherent strong coupling to the host material. However, solid-state systems offer the key advantage that scaling of the structures seems feasible. The need for scalability was highlighted in 1998 by Preskill [12] who argued that a "useful" quantum computer required a suitably large number of qubits to exploit its computational advantage over classical computers. Considering a finite (10^{-6}) error rate for each operation, he estimated that 10^6 qubits may be necessary to outperform classical computers on the prime factorization problem. Shortly after, DiVincenzo [13] formulated several essential requirements for a successful quantum computer architecture, again emphasizing the need

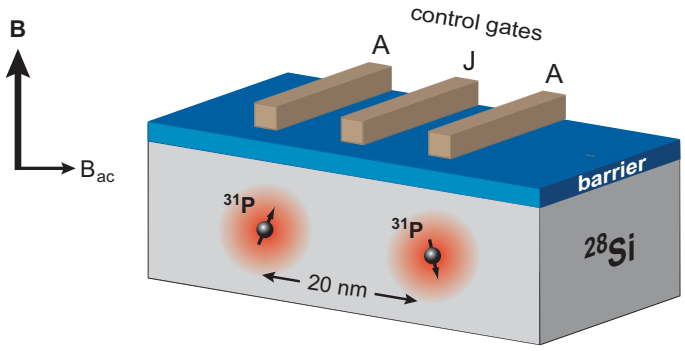

Figure 1.1: Schematic of the Kane quantum computer. Illustration of the elementary building block of a silicon-based quantum computer as proposed by Kane [14]. Information is encoded on the nuclear spin of individual phosphorus donors in a ^{28}Si host. Logic operations are performed using surface gates: The 'J gates' control the electron-mediated coupling between the spins while the 'A gates' control their resonance frequency in an external magnetic field.

for scalability. His five major criteria for the physical implementation of a quantum computer are: (i) A scalable physical system with well-defined qubits. (ii) The ability to initialize these qubits to a simple fiducial state. (iii) Decoherence times that are much longer than the required quantum logical operations. (iv) A universal set of quantum gates. (v) A qubit-specific measurement capability. These so-called *DiVincenzo criteria* have since been seminal in focusing both theoretical and experimental research in different quantum-information processing schemes.

In 1998, Kane [14] proposed using the nuclear spin of phosphorus donors in silicon to realize a scalable solid-state quantum computer. A key advantage of silicon-based systems is their inherent potential for scalability due to the vast existing knowledge and advanced technologies developed by the silicon industry over many decades. A schematic of the Kane architecture is illustrated in Fig. 1.1. Here, the qubits are realized by the nuclear spin of individual ^{31}P donors which are patterned in a regular array (with 20 nm spacing) in an isotopically purified ^{28}Si host crystal. Surface gates ('A' and 'J') are deposited on an oxide barrier over the donor array. Logic operations on the qubits are performed by applying an external oscillating magnetic field B_{ac}. By applying a suitable voltage to the 'A gate' above a donor, its hyperfine interaction can be altered resulting in a change in the resonance frequency of its nucleus. It is therefore possible to address the qubits individually by bringing specific donors into resonance with B_{ac}. By contrast, the 'J gates' control the electron-mediated coupling between adjacent nuclear spins thus enabling two-qubit operations.

Spins in a magnetic field are an inherent two-level system and therefore a natural choice

for the realization of a qubit. For solid-state systems, spins in silicon are a particularly promising candidate due to their resilience against decoherence. This is essentially due to two desirable material properties of silicon [14]: The predominance of spin-zero ^{28}Si nuclei and a small spin-orbit coupling. Indeed, for P donors in bulk silicon at $T = 1.5\,\mathrm{K}$ the electron spin relaxation time has been found to be thousands of seconds, while the ^{31}P nuclear spin relaxation time exceeds 10 hours [15]. As a result, further donor-based quantum computer architectures have been proposed in silicon, using either the donor electron spin [16] or charge [17] to define the qubit. More recently, nuclear spins of ^{31}P in Si have also been shown to serve as suitable quantum memory for spin superposition states [18] with a lifetime exceeding 100 s [19].

Scaling of all donor-based quantum computer schemes relies on vast arrays of individual impurities that are patterned in a host crystal. Indeed, two-dimensional architectures for such donor arrays have been proposed [20] that specifically address the need for quantum error correction and the necessity to "shuttle" qubit states in a realistic system. To avoid spatial oscillations in the exchange coupling between neighboring donor sites arising from the silicon bandstructure [21], these architectures rely on the precise control over the location of each dopant atom within the array. A key challenge in fabricating a functional donor-based qubit is therefore the ability to pattern individual impurities in an epitaxial silicon environment with essentially atomic accuracy.

In this thesis, we demonstrate how scanning tunneling microscopy (STM) based lithography can be used as a viable way to overcome this challenge. STM has previously proven its capability to both image [22] as well as manipulate [23] crystalline matter on the atomic scale. Here, we use STM-based hydrogen lithography – in combination with a gaseous dopant source and a thermal silicon source – to fabricate highly phosphorus doped nanostructures in a silicon single-crystal environment.

Following the goal of realizing a single donor device, we initially fabricate donor-based quantum dots. Here, electrons are confined in all three dimensions resulting in a quantized energy spectrum. Quantum dots have attracted significant research interest over the past 30 years since they allow the effects of an engineered confinement to be studied in structures that are often referred to as "artificial atoms" [24]. We then follow a systematic approach to down-scaling of donor-based quantum dots towards the single donor limit. Finally, we demonstrate the fabrication of a deterministic single donor transport device where precisely one phosphorus dopant atom is patterned between electrical leads with a spatial accuracy of $\pm 6\,\text{Å}$.

Our approach thus enables the placement of individual impurities within a single-crystal

silicon environment with a spatial accuracy comparable to the lattice spacing. The results of this thesis therefore present an important step towards a scalable donor-based quantum computer in silicon.

Overview of this thesis

This thesis is structured as follows:

Chapter 2 gives a summary of the background and theoretical concepts necessary for the understanding of the following chapters. We briefly discuss the relevant material and electronic properties of silicon which serves as a host material for the donor-based devices presented here. We also review some characteristic features of electronic transport in silicon nanostructures. In particular, we introduce effective mass theory as a viable method to calculate the electronic states of strongly confined systems. Furthermore, we discuss the constant interaction model of Coulomb blockade which will be applied in subsequent chapters to interpret experimental results on quantum dots.

The experimental methods used will be described in **chapter 3**. Here, we first give a brief introduction to the basics of scanning tunneling microscopy (STM) and describe the features of our STM system. This is followed by an overview of the fabrication technique used to realize planar dopant-based devices in silicon by means of STM hydrogen lithography. We then explain how the electrical transport properties of these devices are measured at low temperatures in a dilution refrigerator.

The subsequent four chapters then present the key experiments and results of this PhD thesis:

Chapter 4 concerns itself with advances in device fabrication developed during this thesis. We present an improved strategy to align *ex-situ* metallic contacts and top gates to the dopant devices allowing for an overall alignment accuracy of $\sim$100 nm. This method relies on a hierarchical array of alignment markers that is etched into the silicon substrate. A key feature of this new alignment strategy is the controlled formation of step-free areas in the middle of a central etched marker, which allows the active area of a device to be patterned on a single atomic plane. We will highlight the importance of this for donor-based quantum computation architectures. Furthermore, we introduce a new method to form reliable ohmic contact to the overgrown dopant structures by using vertically etched contact vias.

In **chapter 5** we show how STM-lithography can be used to fabricate functional donor-based quantum dot structures in silicon. Here, we present a multiterminal planar quantum

dot in the many-electron regime and demonstrate how donor-based in-plane gates can be used as a viable alternative to metallic top gates to reliably tune the electrochemical of the dot. In particular, we compare the use of such in-plane gates in an epitaxial environment with conventional surface gates and find superior stability of the former. Based on these results, we then describe the particular challenges of down-scaling in a planar dopant-based architecture and discuss strategies to overcome these obstacles.

Successful down-scaling will be demonstrated in **chapter 6**, where we present a donor-based quantum dot in the few-electron regime. Electrical characterization of this device at low temperatures reveals a surprisingly dense excitation spectrum at an energy scale of $\sim$100 μeV. We attribute this spectrum to valley splitting of electronic states in the strongly confined dot. To support our interpretation, we present extensive effective mass calculations for our few-donor structure. These results highlight the importance of the valley degree of freedom in ultra-small silicon quantum devices.

In **chapter 7** we demonstrate how STM-lithography can be used to fabricate a gated single donor transport device in silicon. Here, exactly one phosphorus dopant is placed between source and drain electrodes with a spatial accuracy comparable to the lattice spacing. Low-temperature transport measurements reveal a stability diagram that is consistent with the bound states of a single donor. Furthermore, we observe a charging energy that is in very good agreement with reported values for phosphorus donors in bulk silicon. We also find indications for bulk-like excited states in the co-tunneling spectrum of the device. We attribute the bulk-like properties to the absence of surface gates and nearby interfaces in our planar architecture.

Chapter 8 concludes this thesis and gives an outlook on future experiments.

Chapter 2

Background

2.1 Electronic properties of silicon

Silicon (Si) with atomic number 14 is one of the most abundant elements on earth. It has several isotopes, the most common of which (∼92%) is ^{28}Si which has nuclear spin zero. To this day, silicon remains the most important material in the semiconductor industry where it is used to fabricate transistors, microchips, integrated circuits, and solar cells. As a result, Si is also one of the most extensively studied materials. The following section gives a brief overview of its material properties so far as they are relevant for this thesis. They can be found in any introduction to semiconductor physics, e.g. ref. [25].

In bulk Si, each atom forms covalent bonds to its four neighbors in a tetrahedral configuration, as illustrated in Fig. 2.1. It thus adopts the diamond cubic crystal structure represented by a face-centered cubic (fcc) Bravais lattice with two atoms in each primitive

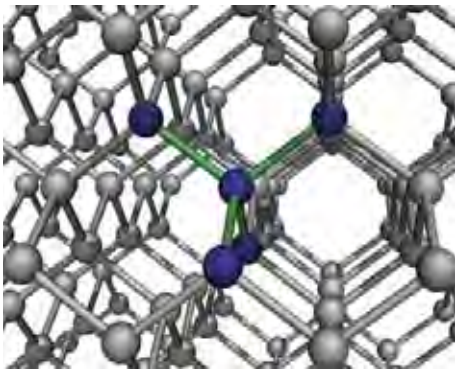

Figure 2.1: Bulk silicon lattice structure. In the diamond cubic crystal structure of bulk Si each atom is covalently bound to 4 tetrahedral neighbors. Reproduced from [26].

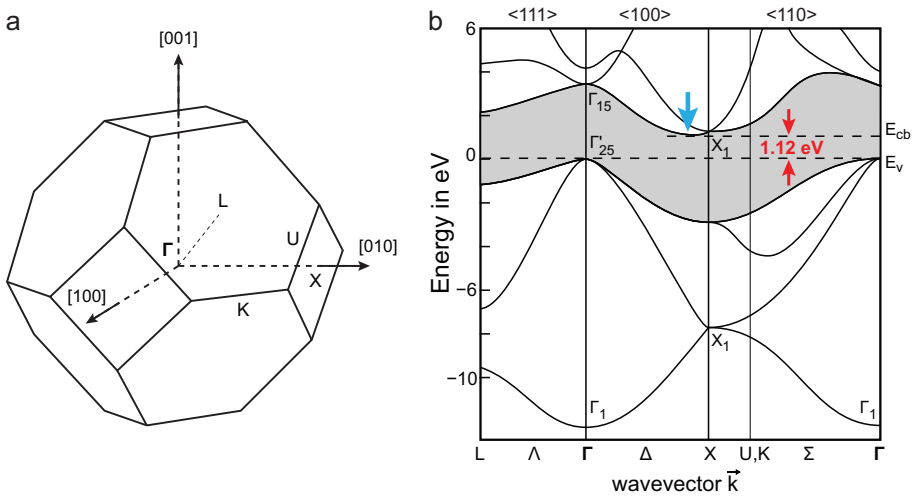

Figure 2.2: Band structure of silicon. a, The 1st Brillouin zone of the fcc lattice showing the labels for high symmetry points. **b**, Simplified band structure (or ϵ-**k** diagram) for bulk silicon. The blue arrow indicates the position of the conduction band minima at $k \approx 0.85\frac{2\pi}{a}$ along $\langle 100 \rangle$ which leads to 6 degenerate "valleys" (see Fig. 2.4 a). Unoccupied states are shaded in gray. Si has an indirect bandgap of 1.12 eV at 300 K. Reproduced from [27].

cell, separated by $a/4$ in each dimension. The lattice spacing a (i.e. the length of the unit cell) is approx. 5.43 Å. The first Brillouin zone of the fcc lattice is depicted in Fig. 2.2 a. Silicon is an elemental group-IV semiconductor with a bandgap of ∼1.12 eV at room temperature. A simplified band structure for bulk Si is shown in Fig. 2.2 b. Silicon has an indirect bandgap, i.e. the maximum energy state of the valence band and the energy minimum of the conduction band occur at different positions in k-space. The conduction band minima are located at $k = 0.85\frac{2\pi}{a}$ along the $\langle 100 \rangle$ directions. Due to the crystal symmetry, this leads to 6 equivalent minima which are degenerate in energy. The presence of these 6 so-called *valleys* (see Fig. 2.4 a) has important implications for electronic transport in silicon systems which will be discussed in the next section.

The Si(100) surface

The crucial part of device fabrication in this thesis was performed on the 2×1 reconstructed Si(100) surface. When a bulk silicon crystal is truncated along a crystallographic (100) plane (see Fig. 2.3 a), every surface atom has two valence electrons that do not participate in a covalent bond (Fig. 2.3 b). The high density of the resulting dangling bonds renders this surface configuration energetically unfavorable resulting in a reconstruction of the surface lattice (Fig. 2.3 c). Here, the formation of dimers (Fig. 2.3 d) between two neighboring Si surface atoms (with a bond length of 2.67 Å) lowers the energy of the

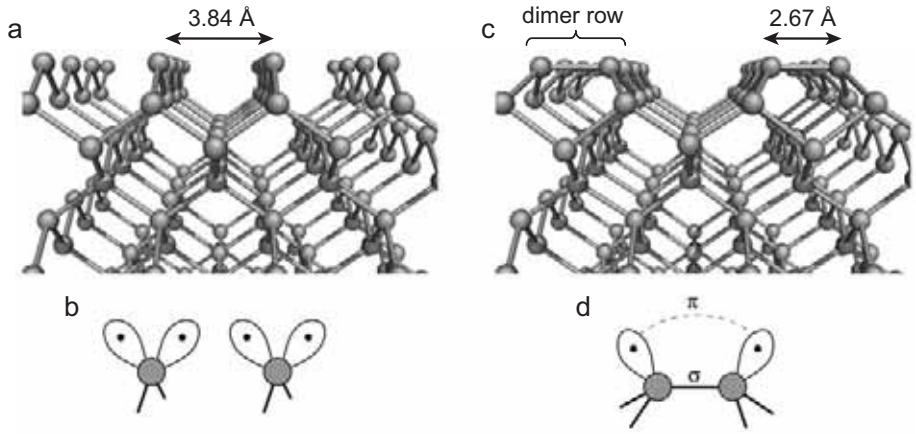

Figure 2.3: Surface reconstruction of Si(100). **a**, Si bulk truncated along the (100) direction yields an energetically unfavorable surface with a 1×1 symmetry, where each Si surface atom has two dangling bonds (**b**). **c**, The formation of dimers lowers the energy of the surface which results in the Si(100)-2×1 reconstruction. These dimers form parallel rows on the surface with a pitch of 7.68 Å. **d**, The dimers of the reconstructed surface are covalently bound by a σ-bond. In addition, the overlap between the remaining dangling bond on each atom forms a (weaker) π-bond. Reproduced from [26].

surface. These dimers form ordered rows on the reconstructed Si(100) 2×1 surface.

2.2 Transport in silicon nanostructures

Describing the motion of charge carriers through a crystalline environment in a quantum mechanical picture is not a trivial task. A common simplification is to introduce a carrier *effective mass*. In this approximation electrons and holes are treated like free particles in a vacuum, but with a different *effective* mass which captures the effects of the periodic potential of the crystal.

2.2.1 The concept of effective mass

The concept of effective mass (see e.g. [28]) in solid-state physics is an approximation used to describe carriers in a crystalline environment. Depending on the symmetry of the crystal, the effective mass m^* is anisotropic and is thus represented by a tensor:

$$\left(\frac{1}{m^*}\right)_{ij} = \hbar^{-2}\frac{\partial^2 \epsilon(\mathbf{k})}{\partial k_i \partial k_j} \tag{2.1}$$

where $\mathbf{k}$ is the wave vector and $\epsilon(\mathbf{k})$ the energy of the charge carrier. This means that the effective mass is inversely proportional to the curvature of the dispersion relation $\epsilon(\mathbf{k})$ as determined by the material's band structure. For electrons in bulk silicon (the band

diagram for which is shown in Fig. 2.2) the above tensor can be diagonalized yielding a *longitudinal* and two degenerate *transversal* effective masses, $m_l = 0.92\, m_e$ and $m_t = 0.19\, m_e$, respectively, where $m_e \approx 9.11 \cdot 10^{-31}$ kg is the electron rest mass.
The effective mass concept is widely used to describe the motion of charge carriers under the influence of electric or magnetic fields. Calculations of bulk conduction properties commonly employ an *average effective mass* which for electrons in Si is given by

$$m^*_{\text{ave}} = 3\left(\frac{1}{m_l} + \frac{1}{m_t} + \frac{1}{m_t}\right)^{-1} \approx 0.26\, m_e. \tag{2.2}$$

2.2.2 The effective mass approximation

The following section briefly introduces effective mass theory (EMT) as developed by Kohn and Luttinger [29] to calculate transport properties of semiconductors. It follows an introduction by Davies [30]. For simplicity we will assume an isotropic effective mass. Let us initially consider a one-dimensional system. Suppose we need to solve for the wavefunction $\Psi(x)$ of a perfect crystal in the presence of an additional potential or perturbation $V(x)$. The Schrödinger equation then takes the form

$$[\hat{H}_0 + V(x)]\Psi(x) = E\Psi(x) \tag{2.3}$$

where $\hat{H}_0$ is the Hamilton operator of the periodic potential for which we assume we know the solutions, $\hat{H}_0\Phi_{nk}(x) = \epsilon(k)\Phi_{nk}(x)$. For a periodic potential these solutions are Bloch functions, $\Phi_{nk}(x) = u_{nk}(x)e^{ikx}$, where $u_{nk}(x)$ has the same periodicity as the potential and n is the band index. In the EMT approach, one makes two important assumptions: (i) Only the wavefunctions from one band play a significant part, so that the different bands can be treated independently. (ii) States from only a small region of k-space around the bottom of the band at $k = k_0$ contribute significantly to the solution. Under these two assumptions, the wavefunction of the problem can be written as[1]

$$\Psi(x) \approx \Phi_{nk_0}F(x) \tag{2.4}$$

This means that the wavefunctions can be decomposed into an atomic-scale part (i.e. a Bloch function at the local minimum of the energy band) and an *envelope function* $F(x)$ (see Fig. 2.5 b). Because of assumption (ii), the latter must be a slowly varying function

[1]For notational simplicity, we assume a single conduction band minimum at $k_0 = 0$ as is the case for GaAs, for example. If several minima are present (such as in Si) the corresponding wavefunction is a sum over the contributions from all band minima.

in real space. Using eq. (2.4), the Schrödinger equation (2.3) then reduces to a much simpler form

$$\left[\epsilon_n\left(-i\frac{d}{dx}\right) + V(x)\right] F(x) = EF(x). \tag{2.5}$$

The result is an equation for the envelope function alone, including an *effective Hamiltonian* which does not contain the periodic potential of the host crystal anymore. In three dimensions, the kinetic operator $\epsilon_n(-i\frac{d}{dx})$ is replaced by $\epsilon_n(-i\nabla)$. This effective Hamiltonian would still be very complicated if we consider the full band structure for $\epsilon_n(\mathbf{k})$. However, in most cases the dispersion relation around the conduction band minimum E_{cb} at $k = k_0$ can be fitted quite accurately by a parabola:

$$\epsilon_n(\mathbf{k}) = E_{cb} + \frac{\hbar^2(k-k_0)^2}{2m^*} \tag{2.6}$$

Substituting this into (2.5) we thus obtain

$$\left[-\frac{\hbar^2}{2m^*}\nabla^2 + V(\mathbf{r})\right] F(\mathbf{r}) = (E - E_{cb})F(\mathbf{r}) \tag{2.7}$$

The final result of the EMT approach is a Schrödinger equation which resembles that for free electrons, except for the effective mass, with the energy measured from the bottom of the conduction band. Regarding the applicability of the latter for devices in silicon, it is necessary to relax assumption (i) above. Silicon has several equivalent valleys in the conduction band, all of which must be considered to describe electronic states. The effective Hamiltonian then becomes a matrix of differential equations acting on a vector whose components are the wavefunctions in each band.

Despite its severe approximations, EMT has been quite successful in providing an accurate description of systems even well beyond its range of validity [31], such as calculating the electronic states of shallow donors in silicon [32].

2.2.3 Valley-splitting in silicon

The crystal symmetry of bulk silicon results in 6 energetically degenerate *valleys* as illustrated in Fig. 2.4 a. This degeneracy has a profound impact on the transport characteristics of silicon quantum devices.

By confining the carriers in one or more directions – and thus reducing the symmetry – the valley degeneracy can be partially lifted. This is illustrated in Fig. 2.4 a where electrons are strongly confined in z-direction (along [001]) resulting in a two-dimensional system. Experimentally, this can be realized in quantum wells of Si heterostructures [33, 34] or

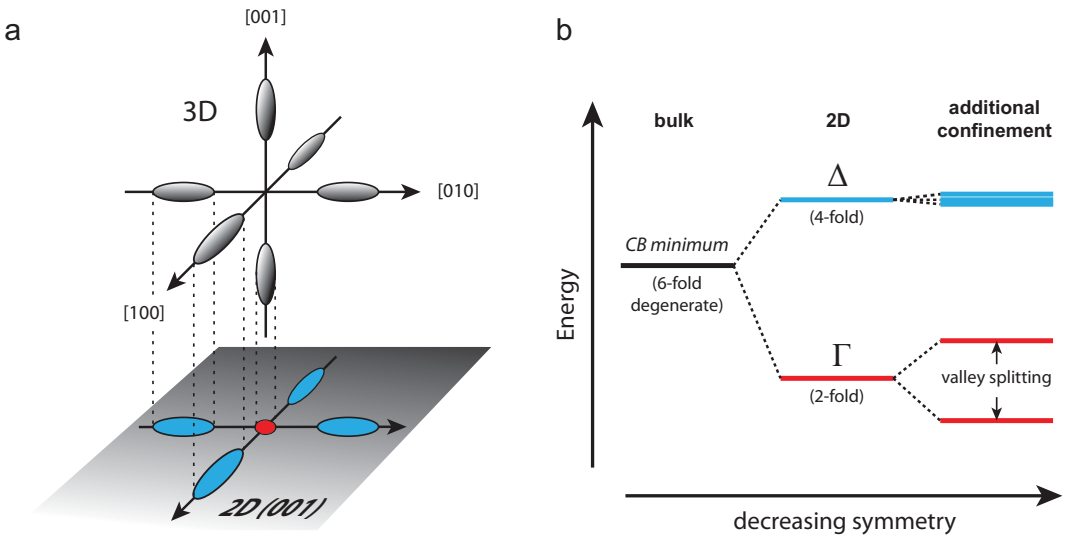

Figure 2.4: Valley splitting in silicon. **a**, The 6 conduction band minima, or valleys, within the 1st Brillouin zone of bulk silicon (see Fig. 2.2 a). If the system is confined along one direction, the resulting 2D bandstructure is a projection of the 3D case onto a plane perpendicular to the confinement direction. **b**, The 6-fold degeneracy of the conduction band minima of bulk silicon can be partially lifted by confining the electrons to two dimensions. The remaining degeneracies may be lifted by additional abrupt confinement.

in δ-doped silicon [35]. The corresponding 2D band structure is then a projection of the bulk band structure onto a plane perpendicular to the confinement direction in $\mathbf{k}$-space. The projection leads to 4 degenerate Δ-pockets as well as two Γ-pockets at $\mathbf{k} = 0$ which are lower in energy (Fig. 2.4 b).

The remaining degeneracies can be broken in the presence of sharp confinement or materials interfaces. The resulting *valley splitting* depends on the details of the confinement potential which must both be steep enough as well as occur on a nm-scale in order to yield a significant splitting. An abrupt change in confinement potential along a given crystal direction will generally lead to a coupling between the two valley states of the corresponding k-axis. Consider a confinement along the z-direction. A simplified schematic of the conduction band edge along $\hat{z}$ is depicted in Fig. 2.5 a. Within the framework of the effective mass approximation the wavefunctions for states close to the conduction band minima at $k_{\pm z} = \pm k_0 \hat{z}$ can then be expressed as [31]

$$\Psi(\mathbf{r}) = \sum_{j=\pm z} \alpha_j e^{i\mathbf{k}_j z} u_{\mathbf{k}_j}(\mathbf{r}) F(\mathbf{r}) \tag{2.8}$$

where $e^{i\mathbf{k}_j z} u_{\mathbf{k}_j}(\mathbf{r})$ are Bloch functions reflecting the periodic potential of the crystal and the coefficients α_j represent the respective contributions from both z-valleys. $F(\mathbf{r})$ is the

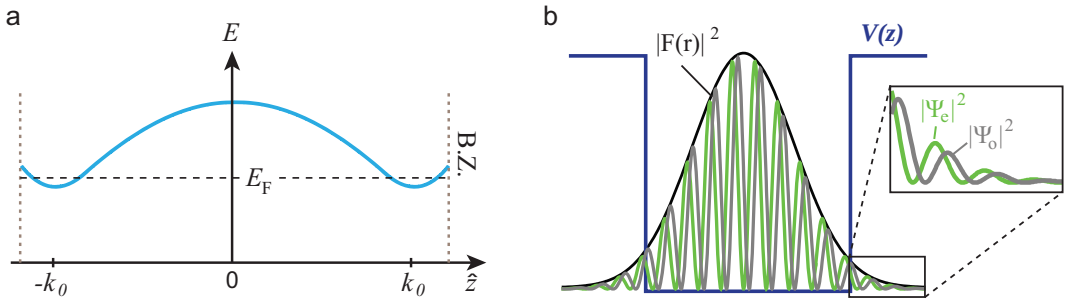

Figure 2.5: Valley splitting in the effective mass approximation. **a**, Simplified schematic showing the conduction band edge along [001] within the 1st Brillouin zone (BZ). The band minima occur at $\pm k_0 \approx 0.85\frac{2\pi}{a}$. **b**, In the presence of a sharp confinement potential $V(z)$ the eigenstates of the system can be expressed by pairs of even and odd functions, Ψ_e and Ψ_o, respectively. While both have the same envelope function $F(r)$, their fast-oscillating parts are out of phase by $\pi/2$ which can result in an energy difference between the even and odd valley combinations.

envelope function satisfying the equation

$$[\hat{H}_0 + V_v(z)]F(\mathbf{r}) = \epsilon F(\mathbf{r}) \tag{2.9}$$

Here, the quantum well is fully described by $\hat{H}_0$ while all the details of the valley interaction are captured in terms of an effective coupling potential $V_v(z)$ which will be treated as a perturbation. The form of this coupling potential is not *a priori* known and must be determined for each system. Using first order perturbation theory, eq. (2.9) can be transformed[2] into matrix form [31]

$$\begin{pmatrix} \epsilon^{(0)} & \Delta_1 \\ \Delta_1^* & \epsilon^{(0)} \end{pmatrix} \begin{pmatrix} \alpha_{-z} \\ \alpha_{+z} \end{pmatrix} = \epsilon \begin{pmatrix} \alpha_{-z} \\ \alpha_{+z} \end{pmatrix} \tag{2.10}$$

where $\epsilon^{(0)}$ is the eigenenergy of the unperturbed Hamiltonian $\hat{H}_0$. Diagonalizing the matrix equation we obtain the new eigenenergies

$$\epsilon_\pm = \epsilon^{(0)} \pm \Delta_1 \tag{2.11}$$

with the valley splitting $E_v = 2|\Delta_1|$.

Due to the symmetry of the problem it is a reasonable approach [31] to represent the eigenstates of eq. (2.10) by pairs of *even* and *odd* valley combinations corresponding to

[2]The atomic scale oscillations $u_{\mathbf{k}_j}(\mathbf{r})$ are dropped since they lead only to small corrections.

$(\alpha_{-z}, \alpha_{+z}) \propto (1,1)$ and $(1,-1)$, respectively:

$$\Psi_e(\mathbf{r}) = \cos(k_0 z) F(\mathbf{r}) \tag{2.12}$$

$$\Psi_o(\mathbf{r}) = \sin(k_0 z) F(\mathbf{r}) \tag{2.13}$$

Both wavefunctions have the same envelope but their fast-oscillating parts are phase shifted by $\pi/2$ as depicted in Fig. 2.5 b. The valley splitting can then be calculated as[3]

$$E_v = \langle \Psi_e | V | \Psi_e \rangle - \langle \Psi_o | V | \Psi_o \rangle \tag{2.14}$$

In chapter 6 we will use this approach to calculate the valley splitting arising from the lateral confinement in a few-donor silicon quantum dot. In this case, the valley splitting potential $V_v(\mathbf{r})$ will be identified as the confinement potential of the quantum dot itself.

2.2.4 Density of states in lower dimensions

In transport structures on the sub-μm scale, a strong confinement along one or more directions can lead to the formation of *subbands* that reflect the reduced dimensionality of the system [36]. This occurs when the characteristic confinement length scale is smaller than the Fermi wavelength λ_F of the system, i.e. the de-Broglie wavelength of electrons at the Fermi level. The formation of these subbands affects the number of states $n(E)$ that contribute to transport processes at a given energy. For a bulk material, the density-of-states (DOS) $\rho(E) = dn(E)/dE$ has the well-known square root dependence $\rho_{3\mathrm{D}}(E) \propto \sqrt{E - E_{cb}}$ where E_{cb} is the conduction band minimum. By contrast, the DOS in two dimensions is independent of energy,

$$\rho_{2\mathrm{D}}(E) = g_s g_v \frac{m}{2\pi\hbar^2} \tag{2.15}$$

Here, g_s and g_v account for the spin and valley degeneracy, respectively. Because of the constant density-of-states, the electron sheet density n_s is directly proportional to the Fermi energy, $n_s = g_s g_v m^* E_F / 2\pi\hbar^2$. As a result, the Fermi wavelength of a 2D system is related to the carrier density as

$$\frac{2\pi}{\lambda_F} = k_F = \sqrt{\frac{4\pi n_s}{g_s g_v}} \tag{2.16}$$

[3]The operator V can be related to $V_v(z)$ of eq. (2.9).

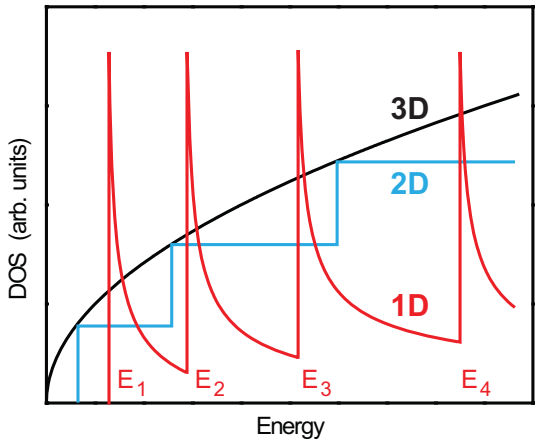

Figure 2.6: Density of states in 1, 2, 3 dimensions. Schematic comparison of the density of states as a function of energy for a three-dimensional system (black), a two dimensional system (blue) and a one-dimensional system (red). The latter diverges at certain energies E_n which indicate the bottoms of the 1D subbands.

The second 2D subband starts to be populated when E_F exceeds the bottom of the second band, which leads to the stepwise increasing DOS depicted by the blue curve in Fig. 2.6. If the dimensionality is reduced even further, each 2D subband splits into a series of 1D subbands with band bottoms at E_n, where n=1,2,... The one-dimensional DOS is then given by

$$\rho_{1\mathrm{D}}(E) = \sqrt{\frac{m^*}{2\pi\hbar^2}} \frac{1}{\sqrt{E - E_n}} \tag{2.17}$$

The "kinks" in the DOS (i.e. the energies for which $d\rho/dE$ diverges) are commonly referred to as *van Hove singularities*. The spacing between the discontinuities in the 2D and 1D DOS reflects the confinement of the system. It should be noted that even for 2D and 1D structures, the corresponding DOS is continuous in energy. This changes if the charge carriers are confined in all 3 dimensions as is the case for ("0-dimensional") quantum dots. Here, the continuum of states is replaced by a discrete spectrum which will be discussed in more detail in section 2.3.

2.2.5 Transport in planar dopant layers in silicon

The electronic properties and particularly the conductivity of semiconductors can be drastically altered by introducing comparatively small amounts of foreign materials. For silicon, typical (bulk) doping densities range from $10^{13}\,\mathrm{cm}^{-3}$ to $10^{20}\,\mathrm{cm}^{-3}$, roughly corresponding to a ratio of impurities to silicon atoms of $1/10^9$ to $1/100$. Depending on the host material, the dopants can act either as electron acceptors or electron donors. As a group-IV element, silicon is typically doped with group-III acceptors (such as B, Ga) or group-

V donors (P, As). Bulk doping of Si nanostructures is commonly achieved by thermal diffusion or ion implantation in conjunction with a suitable lithography mask. Here, the resulting doping profile typically varies (in all 3 dimensions) over length scales much larger than the lattice spacing. By contrast, the structures presented in this thesis are fabricated in δ-doped silicon, where the impurities are essentially confined to a two-dimensional plane in the Si host crystal yielding an abrupt doping profile in the plane-perpendicular direction on a length scale of a few Å. Our quantum electronic devices are realized by laterally patterning phosphorus δ-doped layers in silicon using STM-lithography. Here, the extremely high (sheet) doping densities ($n_s \sim 10^{14}\,\mathrm{cm}^{-2}$, corresponding to 1 P donor per 4 Si atoms) within the dopant plane has important implications for the transport properties of the two-dimensional Si:P structures which will be discussed in the next section.

Transport parameters of δ-doped Si:P

Transport in phosphorus δ-doped Si has previously been studied both theoretically [35, 37] and experimentally [38, 39, 40]. Qian *et al.* [35] have used density functional theory (DFT) to calculate the 2D bandstructure at 1/4 ML P coverage. Here, the donor electrons are represented as linear combinations of the products of two-dimensional plane waves (within the dopant plane) and 1D Gaussian functions (in z-direction). The resulting bandstructure is shown in Fig. 2.7 a, where the energy zero corresponds to the conduction band minimum (CBM) of bulk Si. As a result of the high doping density the conduction bands of the 2D system are pulled down below the Fermi level E_F which is calculated to lie approx. 99 meV below the bulk CBM [35]. As discussed above, the strong vertical confinement within the δ-doping plane breaks the 6-fold valley degeneracy of bulk Si thus resulting in the formation of 2D subbands. Here, two Γ subbands arise from the projection of the 2 z-valleys while the remaining x- and y-valleys form the fourfold degenerate Δ-bands (see Fig. 2.4). Considering exchange correlations (dotted lines in Fig. 2.7 a), Qian obtains a valley splitting of $\sim$20 meV between the Γ_1 and Γ_2 valleys resulting from the abrupt doping profile along the z-direction. Electronic transport through the Si:P δ-doping plane occurs via the 6 occupied subbands below the Fermi level. From fitting the curvature of each calculated subband, Qian obtains effective masses of $m_t^* = 0.211$ and $m_l^* = 0.95$ which are slightly modified from the corresponding bulk values.

In a more recent publication Carter *et al.* [37] have performed a full non-empirical bandstructure modeling of the system considering both valence and donor electrons. In contrast to Qian, who used an empirical pseudopotential to define the doping potential, Carter used

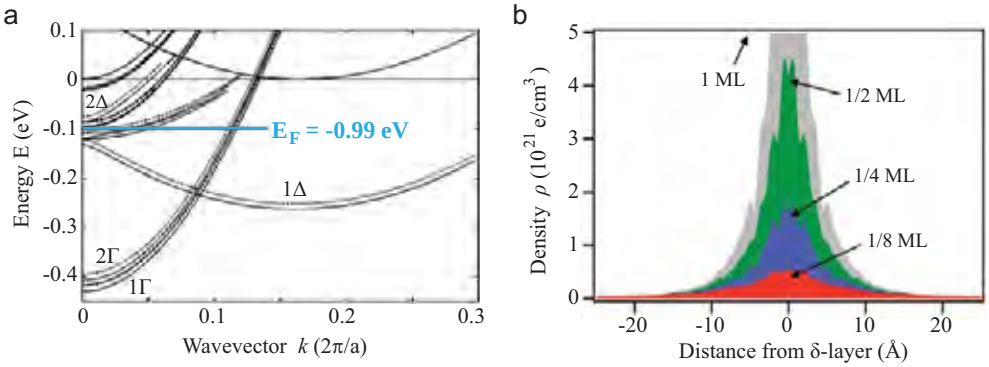

Figure 2.7: Theoretical calculations for δ-doped Si:P. a, Subband structure at a P doping density of 1/4 ML. The energy zero is placed at the conduction band minimum of bulk Si. The dotted lines show the band structure when exchange-correlations are considered. Reproduced from Qian *et al.* [35]. **b**, Plane averaged distribution of the donor electron density (perpendicular to the dopant plane) for different P doping densities. For 1/4 ML P coverage, the electron density drops to 1/10 of its peak value at a distance of ∼1 nm. Reproduced from Carter *et al.* [37].

a periodic (three-dimensional) superlattice to represent the dopants. The calculated donor electron density along z-direction is shown in Fig. 2.7 b for different doping densities. For 1/4 ML P coverage, the electron density drops to 1/10 of its peak value at a distance of ∼1 nm from the dopant plane, resulting in an effective electronic "thickness" of the dopant layer of ∼2 nm. They also calculated the 2D bandstructure for the system, obtaining results that are broadly consistent with the values reported by Qian. In particular, they find a Fermi level that lies 130 meV below the CBM of bulk Si and a Γ_1-Γ_2 splitting of 120 meV. The discrepancy with respect to Qian's values is most likely the result of the assumed ordering of the dopants in Carter's model, which is an inherent feature of the superlattice representation. This is in contrast to realistic δ-doped Si:P devices where the dopants are disordered due to the statistical nature of the donor incorporation process [41, 42]. To capture the effects of disorder, Carter repeated the calculations using a larger[4] supercell (with a disordered dopant distribution within the cell). For the disordered 1/4 ML case, they obtain a Fermi level at −70 meV and a Γ_1-Γ_2 splitting of 60 meV. These results will be used in chapter 6 as an input to calculate the excitation spectrum of a few-donor Si:P quantum dot.

Experimental transport parameters

To put our work into a larger context, we will briefly summarize some important transport parameters for our planar dopant-based silicon devices. While these may not be directly

[4]The max. size of the supercell is limited by finite computational resources. In the disordered case, the supercell extended 4 lattice sites in both lateral directions and 40 atomic layers in the vertical direction.

Transport in δ-doped Si:P at 4 K

quantity	symbol	typical values	Ref.
sheet electron density	n_s	$\sim 2 \times 10^{18}\,\mathrm{m}^{-2}$	Goh [39]
mobility	μ	$20 - 100\,\mathrm{cm}^2/\mathrm{Vs}$	Oberbeck [43], Goh [38, 39]
mean free path	l	$\sim 5 - 10\,\mathrm{nm}$	Goh [38], Reusch [40]
phase coherence length	l_φ	$< 100\,\mathrm{nm}$	Ruess [44], Goh [38]
Fermi wavelength	λ_F	$\sim$3 nm	from eq. (2.16)

Table 2.1: Summary of relevant transport parameters for δ-doped Si:P at 4 K.

relevant for the understanding of the work presented in this thesis, it will enable the reader to compare our system to other 2DEG structures in the literature.

The carrier density of δ-doped Si:P layers can be obtained experimentally from Hall-bar measurements [39]. We reliably obtain electron sheet densities n_s of $\sim 2 \times 10^{18}\,\mathrm{m}^{-2}$ which corresponds to planar doping densities of 0.25 ML. Table 2.1 summarizes several relevant transport parameters obtained in previous experiments on P δ-doped devices by our group.

At low temperatures, electronic transport in two-dimensional δ-doped Si:P layers is dominated by scattering of electrons with the ionized donor atoms within the doping plane [38]. Several characteristic length scales [36] define the transport properties of our system. The mean free path l is the inverse of the scattering time τ and corresponds to the distance an electron propagates between two collisions. In the Drude theory of conduction, the mobility μ is related to the scattering time by

$$\mu = \frac{e\tau}{m^*} \tag{2.18}$$

We typically find $l \sim 10\,\mathrm{nm}$ [38, 40] in our system due to the high doping densities which result in frequent collisions. This is reflected by a comparatively low mobility of typically $20 - 100\,\mathrm{cm}^2/\mathrm{Vs}$ [38, 39, 43]. By contrast, the spatial separation of dopants and 2DEG in GaAs/AlGaAs heterostructures allows for mobilities on the order of $10^7\,\mathrm{cm}^2/\mathrm{Vs}$ [45] with mean free paths of several μm.

Transport is diffusive in laterally patterned regions where the characteristic width W is larger than the mean free path, $l < W$. This is also true for the dopant-based planar nanowires which serve as electrical leads in the quantum devices presented in later chapters. Another important parameter is the phase coherence length l_φ which denotes the distance an electron propagates without undergoing a phase-randomizing inelastic scattering event. For our δ-doped Si:P layers we typically find l_φ on the order of several 10s of nm at 4 K.

The high doping density in our system results in a small Fermi wavelength which can be estimated from eq. (2.16). Assuming a two-fold spin and 4-fold valley degeneracy we obtain $\lambda_F \sim 3\,\mathrm{nm}$. We thus expect truly 2D transport characteristics within the δ-doped layer since the vertical confinement length scale ($\sim 1\,\mathrm{nm}$) is smaller than λ_F. For laterally patterned dopant nanowires with minimal widths of $4-5\,\mathrm{nm}$ we expect *quasi*-1D behavior, where $W \sim \lambda_F$.

2.3 Coulomb blockade

Consider a setup of conductors as illustrated in Fig. 2.8 a. An island with a self-capacitance C_Σ is weakly connected via tunnel junctions to two electrodes so that electrons can tunnel from the source lead via the island to the drain lead. If the size of the island (and therefore C_Σ) is small enough, the so-called *charging energy* $E_c = e^2/C_\Sigma$ required to add an extra electron onto the island may exceed the thermal energy of the electrons so that current through the island is suppressed. This phenomenon is called *Coulomb blockade*. Two elementary conditions must be satisfied to observe Coulomb blockade [46]:

(i) The thermal energy of the system must be smaller than the charging energy,

$$k_\mathrm{B}T \ll \frac{e^2}{C_\Sigma} \tag{2.19}$$

Experimentally, this can be achieved by measuring at cryogenic temperatures and devices with sufficiently small (typically sub-μm) islands. In this context the island is commonly referred to as "dot" to reflect its quasi 0-dimensional character.

(ii) The tunnel coupling between the dot and the leads must be weak enough so that a well-defined integer number of electrons can reside on the island long enough for the system to be measured. A lower limit for the tunnel resistances $R_{S,D}$ to the leads (see Fig. 2.8 b) can be estimated by considering the typical time-scale to charge or discharge the dot, $\Delta t = R_{S,D}C_\Sigma$. Taking into account the Heisenberg uncertainty principle $\Delta E \Delta t = (e^2/C_\Sigma)R_{S,D}C_\Sigma > h$, we obtain

$$R_{S,D} \gg h/e^2 \approx 25.8\mathrm{k}\Omega \tag{2.20}$$

In the device of Fig. 2.8 a, the tunneling of a single electron causes a discrete change in the island's electrostatic energy. In the Coulomb blockaded regime, the number of electrons on the island is fixed to an integer number N. Let us now consider a suitable *gate* electrode

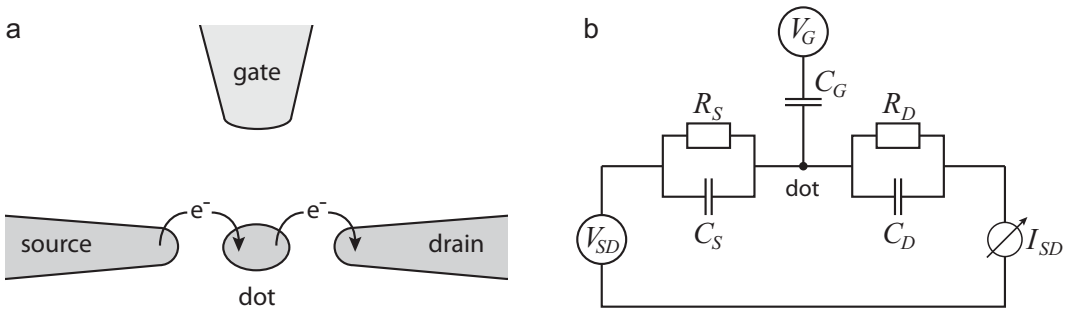

Figure 2.8: Schematic of a lateral quantum dot. **a**, A conducting island ("dot") is connected to source and drain contacts by tunnel junctions and to a gate by a capacitor. For very small dot sizes, the energy needed to add an extra electron onto the dot becomes significant and current from source to drain can be blocked. **b**, Circuit diagram for a gated dot. The source and drain tunnel barriers are represented as a parallel capacitor and resistor. The charging energy in this circuit is $e^2/(C_S + C_D + C_G)$.

which has capacitive coupling but no tunnel coupling to the island. By applying a voltage to the gate, we can raise (lower) the electrostatic energy of the island in a continuous manner until eventually an electron can tunnel off (onto) the dot thus minimizing the energy of circuit. Such gated devices, which allow for the controlled tunneling of individual charges, are therefore referred to as *single electron transistors* (SET). Controlled single electron tunneling was first experimentally observed in 1987 in gated aluminium tunnel junctions [47]. Since then, quantum dots have been realized in a vast and diverse range of materials such as metallic nanoparticles, organic molecules, carbon nanotubes as well as a variety of semiconducting nanostructures.

So far the phenomenon of Coulomb blockade has been introduced from a purely electrostatic point of view. However, with typical device sizes on the order of a few 100 nm, quantization effects become relevant. In particular, the confinement of charge carriers within the quantum dot will lead to a discrete spectrum of quantum mechanical states.

2.3.1 The constant-interaction model

The simplest theoretical model to describe a Coulomb blockaded structure with a discrete energy spectrum is the so-called *constant capacitance* or *constant interaction* (CI) model [48]. The introduction presented in this section follows refs. [49] and [50].

The CI model is essentially based on two assumptions: (i) The discrete energy spectrum is assumed to be independent of the number N of electrons on the dot. (ii) The interactions between the dot and all other electrodes as well as the Coulomb interactions between the electrons on the dot can be represented by capacitances which are assumed to be constant

(regardless of the electron number or applied voltages). The system can thus be fully described by a set of capacitances as illustrated in the circuit diagram of Fig. 2.8 b. Here, C_Σ is the sum over the mutual capacitances between the dot and all the other electrodes, $C_\Sigma = C_S + C_D + C_G$. The total energy of a dot with N electrons in the ground state can then be written as

$$U(N) = \frac{[e(N - N_0) + C_S V_{SD} + C_G V_G]^2}{2C_\Sigma} + \sum_{i=1}^{N} \epsilon_i \tag{2.21}$$

Here, we assume that the source-drain voltage V_{SD} is applied to the S electrode while keeping D grounded[5]. N_0 is the number of electrons in the dot at zero gate voltage V_G. The total energy is thus comprised of the electrostatic energy (where $C_S V_{SD}$ and $C_G V_G$ are continuous and represent the charge induced by the externally applied voltages) and the sum of the single particle energies ϵ_i. The latter reflect the confinement characteristics of the dot and may depend on additional parameters such as an external magnetic field. Transport experiments by definition entail a change in electron number on the dot. Such processes are conveniently described in terms of an electrochemical potential which is defined as the energy to required to add the N^{th} electron to the dot:

$$\mu_N = U(N) - U(N-1) = (N - N_0 - \frac{1}{2})E_c - e(\frac{C_S}{C_\Sigma} V_{SD} + \frac{C_G}{C_\Sigma} V_G) + \epsilon_N \tag{2.22}$$

Equation (2.22) describes the transition between the ground states of the N and the $N-1$ electron system, respectively.

Coulomb diamonds

Energy diagrams for the quantum dot are illustrated in Fig. 2.9 a. The continuous states in the source and drain leads are filled up to the potentials μ_S and μ_D, respectively. The discrete 0D-states in the dot are filled with N electrons up to μ_N. The energy spacing between the dot states is commonly referred to as the *addition energy* which is given by

$$E_{\text{add}} = \mu_N - \mu_{N-1} = E_c + \Delta E_N \tag{2.23}$$

The addition energy is thus the sum of the charging energy E_c and the single-particle level spacing $\Delta E_N = \epsilon_N - \epsilon_{N-1}$. The latter generally increases as the dot size is reduced. It should be noted, though, that even for small dots ΔE_N can be zero, e.g. when two

[5]This is often referred to as *asymmetric bias* and was the standard setup for the quantum dot measurements of this thesis.

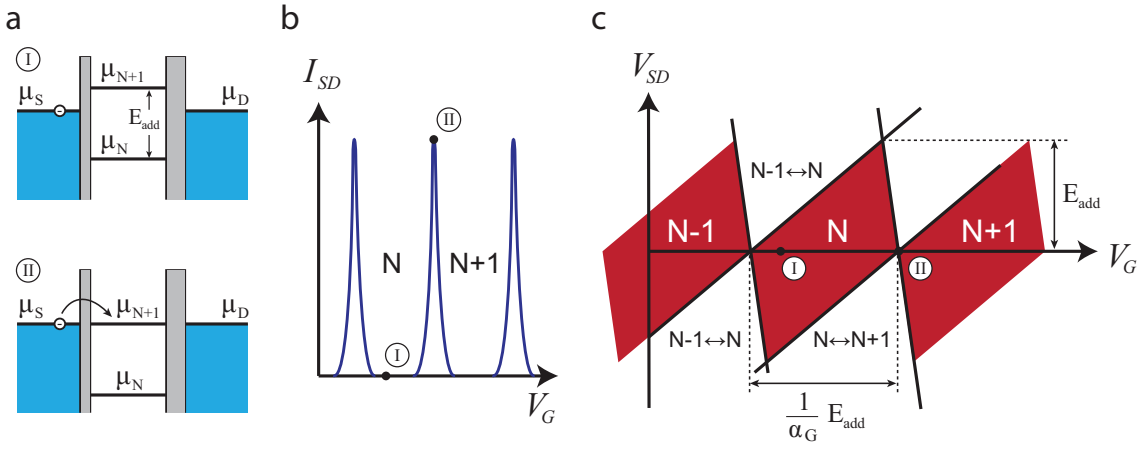

Figure 2.9: Coulomb diamonds. **a**, Low-bias energy diagrams for a quantum dot connected to source (S) and drain (D) leads via tunnel barriers. In case I, current is blocked and the dot contains a fixed number of N electrons. By contrast, in case II an electrochemical potential of the dot is aligned with the lead potentials μ_S and μ_D enabling conduction through the dot. **b**, By applying a gate voltage V_G the electrochemical potentials of the dot can be tuned with respect to the leads, resulting in a pattern of conductance peaks. **c**, The conductance as a function of bias voltage V_{SD} and gate voltage yields a so-called stability diagram of the quantum dot. Here, the current is blockaded in the diamond shaped regions. The height of these Coulomb diamonds corresponds to the addition energy.

consecutive electrons are added to the same spin-degenerate level.

In the upper panel of Fig. 2.9 a (case "I") transport through the device is blocked and the dot contains a fixed number of N electrons. By applying an appropriate gate voltage V_G the dot potential μ_{N+1} can be aligned with that of source and drain (case "II"). This allows the electron number on the dot to fluctuate between N and $N+1$ thus enabling conduction through the dot. At low bias voltages ($eV_{SD} \ll E_c$), this results in a pattern of conductance peaks as a function of the gate voltage as illustrated in Fig. 2.9 b. The spacing between these Coulomb peaks can be obtained by solving eq. (2.22) for V_G:

$$\Delta V_G = V_G^{(N)} - V_G^{(N-1)} = \frac{C_\Sigma}{eC_G}(\mu_N - \mu_{N-1}) = \frac{1}{e\alpha_G} E_{\text{add}} \tag{2.24}$$

Here, we have introduced the coupling factor or *lever arm* of gate G:

$$\alpha_G = \frac{C_G}{C_\Sigma} \tag{2.25}$$

Evidently $0 < \alpha_G < 1$. It is a measure for the "effectiveness" of a gate and converts the applied gate voltage into an energy.

We now consider a finite source-drain bias V_{SD} which is applied to the source electrode, i.e. $\mu_D = \text{const}$ and $\mu_S = \mu_D - eV_{SD}$. We can then formulate constraints for the number

N of electrons on the dot to remain stable. For $V_{SD} > 0$ these are:

$$\mu_N < \mu_D - eV_{SD} \tag{2.26}$$

$$\mu_{N+1} > \mu_D \tag{2.27}$$

Analogously, for $V_{SD} < 0$ we obtain:

$$\mu_N < \mu_D \tag{2.28}$$

$$\mu_{N+1} > \mu_D - eV_{SD} \tag{2.29}$$

The constraints can be converted into two border lines for $V_{SD} > 0$:

$$V_G = \frac{1}{e\alpha_G}\left[\epsilon_N + E_c\left(N - \frac{1}{2}\right) - \mu_D + e(1-\alpha_S)V_{SD}\right], \tag{2.30}$$

$$V_G = \frac{1}{e\alpha_G}\left[\epsilon_{N+1} + E_c\left(N + \frac{1}{2}\right) - \mu_D - e\alpha_S V_{SD}\right] \tag{2.31}$$

The lines for different N define diamond shaped regions in the V_{SD}-V_G plane (see Fig. 2.9 c), where conduction is blockaded. Since the border lines cross each other at $eV_{SD} = \Delta E_N + E_c$, the height of these *Coulomb diamonds* directly corresponds to the addition energy.

Excited state spectroscopy

Up to now we have assumed that transport through the dot occurs via a single level. However, additional levels may contribute if the bias exceeds the single-particle level spacing, $eV_{SD} > \Delta E_{N+1}$. This is illustrated in Fig. 2.10 where transitions between N and $N+1$ electrons are shown considering not only the ground states (GS) but also the excited states (ES) for both electron numbers (panel a). This leads to additional electrochemical potentials of the dot as depicted in Fig. 2.10 b. The additional levels cause an increase in device current as they enter the bias window and therefore result in additional lines of increased conductance outside the blockaded diamonds (Fig. 2.10 c). Panel d shows the corresponding energy diagrams for the three points (I to III) indicated in the V_{SD}-V_G plane. By measuring the *stability diagram* of a quantum dot, i.e. its conductance as a function of bias and gate voltages, it is thus possible to reconstruct the single-particle excitation spectrum of the system.

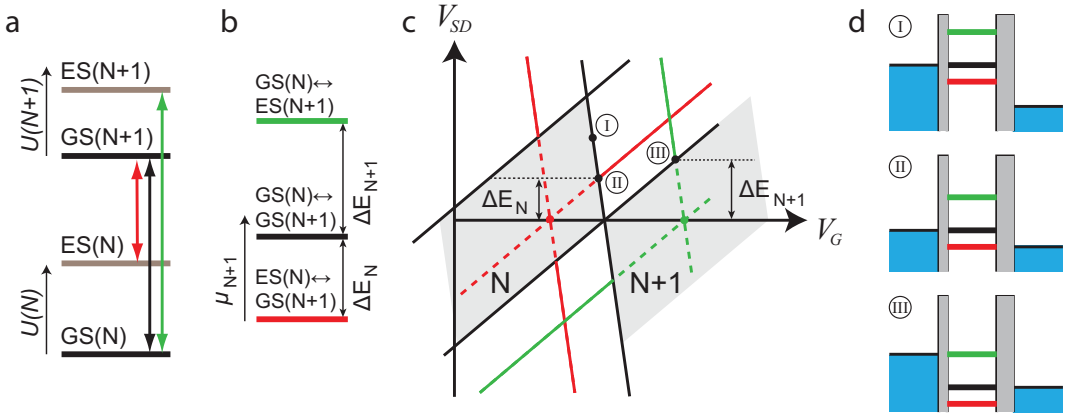

Figure 2.10: Excited state spectroscopy. **a**, Arrows indicate the possible transitions between different dot states for N and N+1 electrons. **b**, The corresponding electrochemical potentials for the transitions depicted in (**a**). **c**, Transport through these excited states results in lines of increased conductance in the stability diagram, running parallel to the diamond edges outside of the blockaded regions. The corresponding level alignment at the indicated positions is illustrated in **d**.

2.3.2 Limits of the constant-interaction model

Despite its simplicity, the constant-interaction model derived above has been very successful in describing transport phenomena in quantum dots in a variety of materials systems [46]. This is particularly true for quantum dots in the many-electron regime and for limited ranges of plunger-gate voltages. As the number of electrons is reduced or the gate-voltage ranges are extended, modifications of this description may become necessary. In particular, it is found that the experimental capacitances of few-electron dots change with the electron number and therefore depend on the applied gate voltages. For many practical purposes, however, the constant-interaction picture can still be used if one allows for gate voltage dependent lever arms $\alpha_G = \alpha_G(V_G)$. This will be discussed in more detail using the example of a few-donor quantum dot in chapter 6.

If the tunnel coupling between the dot and the source and drain leads is gradually increased, further corrections to the constant-interaction theory have to be taken into account. In the strong-coupling regime (see section 2.3.4), sequential resonant tunneling is no longer the dominant transport process and higher order tunneling processes have to be considered. One of the most important amongst these are so-called *co-tunneling* processes [51], i.e. correlated tunneling processes of two (or more) electrons, which will be described in the next section.

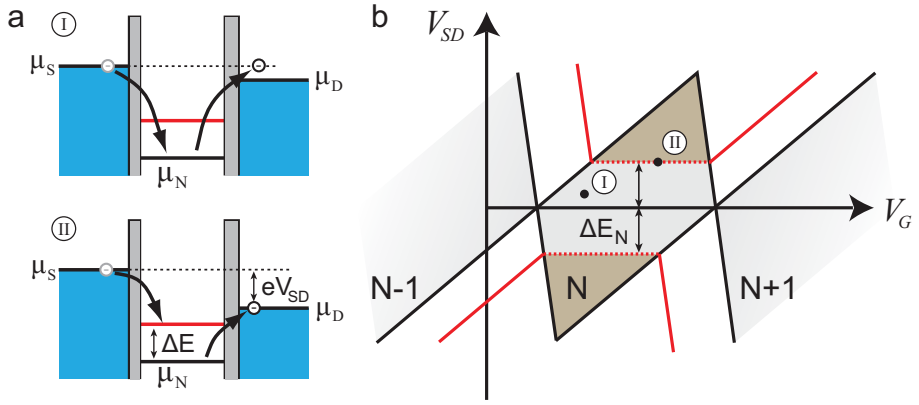

Figure 2.11: Co-tunneling processes. **a**, Schematic level alignment depicting *elastic* (I) and *inelastic* (II) co-tunneling processes. **b**, While sequential tunneling is forbidden within the Coulomb blockaded regions, elastic co-tunneling of carriers leads to a finite current within the Coulomb diamonds. When the bias voltage exceeds the energy separation ΔE_N to an excited state, inelastic co-tunneling becomes possible (dark gray region).

2.3.3 Co-tunneling

The constant interaction model presented above describes Coulomb blockade essentially as a classical phenomenon where single-electron transitions occur between well-defined charge states. At low bias (within the Coulomb diamonds), these transitions are forbidden as a result of energy conservation. However, electronic transport through a quantum dot can also arise from higher-order tunneling processes. The latter are energetically forbidden for sequential tunneling of individual electrons – but can occur if two (or more) electrons participate in the process [51]. This correlated tunneling or *co-tunneling* occurs via intermediate virtual states on the dot which may be occupied for a time $t_H \simeq \hbar/E_c$ which is limited by the Heisenberg uncertainty principle.

The two energy schematics of Fig. 2.11 a illustrate co-tunneling processes. In panel I, an electron tunnels via the virtual state μ_N below the Fermi level of both source and drain (μ_S and μ_D, respectively). This process is referred to as *elastic* co-tunneling since the transferred electron keeps its energy. Elastic co-tunneling can occur for any bias voltage and therefore leads to a small background conductance in the blockaded region (indicated by the grey shading in Fig. 2.11 b) where sequential tunneling is suppressed. At larger bias voltages, *inelastic* co-tunneling processes become possible (panel II of Fig. 2.11 a). Here, an electron tunnels into a virtual state (indicated by the red line) that corresponds to an excited state of μ_N. Simultaneously, an electron tunnels from the μ_N state on the dot to the other lead. Since this process leaves the dot in an excited state, the bias eV_{SD} must exceed the required excitation energy ΔE_N. Inelastic co-tunneling results in steps in

the differential conductance within the blockaded region. This is indicated by the dotted red line in Fig. 2.11 b, above which (in the dark gray region) both elastic *and* inelastic co-tunneling processes can occur.
For a quantum dot structure with the conductance G, a simple estimate for the co-tunneling rate Γ_{ct} can be given by [52]

$$\Gamma_{ct} \approx \Gamma_{se} \frac{G}{G_Q} \tag{2.32}$$

Here, Γ_{se} is the single electron tunneling rate and $G_Q = e^2/h$. Co-tunneling processes are less probable than single-electron tunneling if $G \ll G_Q$ and therefore become only visible if the dot is in the strongly coupled regime where $G \lesssim G_Q$.

2.3.4 Line shape of the Coulomb conductance peaks

Up to now we have treated the quantum dot as an isolated system. However, in a more realistic picture we need to consider the finite coupling of the quantum mechanical levels of the dot to the source and drain leads arising from an overlap of the corresponding wavefunctions. The tunnel coupling results in a finite energy width of the dot levels given by $\hbar\Gamma = \hbar\Gamma_S + \hbar\Gamma_D$. Here, $\Gamma_{S,D}$ are the tunnel rates to the source and drain electrode, respectively, and Γ therefore corresponds to an inverse average lifetime. Considering a finite temperature T, we can now differentiate two different transport regimes [48] for our system given by the *weak-coupling* limit, $\hbar\Gamma \ll k_\mathrm{B}T$, and the strong coupling regime, $k_\mathrm{B}T \lesssim \hbar\Gamma$.

Weak-coupling regime

In the weak-coupling limit the temperature is larger than the quantum mechanical broadening of the energy levels of the dot. For a theoretical treatment of the conductance through the quantum dot it is important to know how many dot levels contribute to the transport. Here, we will only consider the *quantum Coulomb blockade* regime, where the thermal energy is much smaller than the average single-particle spacing, $\hbar\Gamma \ll k_\mathrm{B}T \ll \Delta E$, so that transport occurs through a *single* dot level. A theoretical description of this regime was given by Beenakker [48]. Here, the energy levels of the dot are represented by delta functions while the electronic states in the source and drain leads are treated as a continuum with a thermal occupation that is governed by the Fermi-Dirac distribution

$$f(E) = \frac{1}{e^{E-\mu/k_\mathrm{B}T} + 1} \tag{2.33}$$

Beenakker derived an analytical expression for the Coulomb peak conductance $G^{(i)}$ arising from the dot level i:

$$\frac{G^{(i)}}{G^{(i)}_{max}} = \cosh^{-2}\left(\frac{\alpha_G(V_G^{(i)} - V_G)}{2k_{\mathrm{B}}T}\right) \tag{2.34}$$

where $V_G^{(i)}$ denotes the position of the Coulomb peak on the gate voltage axis. The peak amplitude $G^{(i)}_{max}$ is given by

$$G^{(i)}_{max} = \frac{e^2}{4k_{\mathrm{B}}T}\left(\frac{1}{\Gamma_S^{(i)}} + \frac{1}{\Gamma_D^{(i)}}\right)^{-1} \tag{2.35}$$

where $\Gamma^{(i)}_{S,D}$ represent the tunnel rates for level i to the source and drain leads, respectively. A characteristic of the weak-coupling regime is a decreasing peak amplitude as the temperature is raised. From fitting eq. (2.34) to an experimental Coulomb peak, it is therefore possible to determine the effective electron temperature of the system. This will be demonstrated for a donor-based quantum dot in the few-electron limit in chapter 6.

Strong-coupling regime

In the strong coupling limit, where $k_{\mathrm{B}}T \lesssim \hbar\Gamma$, higher-order tunneling processes need to be considered which goes beyond the formalism discussed above. Assuming non-interacting electrons the conductance in the zero temperature limit is given by the Breit-Wigner formula [53]:

$$G = \frac{2e^2}{h}\left(\frac{1}{\Gamma_S} + \frac{1}{\Gamma_D}\right)^{-1} \frac{h^2\Gamma}{\alpha_G^2(V_G^{max} - V_G)^2 + (h\Gamma/2)^2} \tag{2.36}$$

which corresponds to a Lorentzian lineshape. Here, the coupling constant $\Gamma = \Gamma_S + \Gamma_D$ is assumed to be independent of the level index i. The peak height is equal to the conductance quantum $2e^2/h$, where the factor 2 reflects the spin-degeneracy. In chapter 7 we will use eq. (2.36) to extract the difference in tunnel rates (Γ_S/Γ_D) for a single donor transport device.

2.4 Summary

In this chapter, we have briefly reviewed the theoretical background for the work presented in this thesis. In particular, we have introduced effective mass theory as a viable means to describe valley splitting in silicon. This will be the basis for more elaborate calculations of the electronic excitation spectrum of a few-donor quantum dot presented in chapter 6. We have also discussed relevant characteristics of transport in dopant-based silicon

nanostructures.

Furthermore, we have discussed the constant-interaction model of Coulomb blockade. Despite its limitations we will demonstrate how this model can be used to describe quantum dot devices both in the many-electron as well as in the few-electron regime.

Chapter 3

Experimental Methods

The following chapter gives a brief overview of the experimental techniques as well as the equipment used throughout this thesis. It is divided into two parts: the first part focuses on sample *fabrication*. Here, we describe the instrument that is central to the fabrication of the dopant-based silicon nanodevices presented in this thesis, a scanning tunneling microscope. We then briefly discuss the cleanroom equipment used for *ex-situ* post-processing of the samples.
The second part deals with sample *measurement* and introduces the equipment used to characterize the transport properties of the STM-patterned devices at low temperatures.

3.1 Scanning tunneling microscopy

The tool that is at the heart of our approach to fabricating functional P-doped nanostructures in silicon is a scanning tunneling microscope (STM). Invented by Binnig and Rohrer [22] in the early 1980's it has become a widely used instrument in surface science due to its unrivalled resolution. In this section, we will give an introduction to the basic principle of operation of a STM. We will then briefly discuss the underlying physics following the approach of Chen [54]. For a more detailed description and theoretical discussion, the reader is referred to several extensive review articles and textbooks [54, 55, 56].
The schematic of Figure 3.1 illustrates the basic components of a STM system. A sharp metal tip is scanned in a raster motion over a conducting surface in a vacuum environment. Piezoelectric actuators are used to move the tip in both lateral (x,y) as well as vertical (z) direction. If the distance between tip and sample is small enough (typically less than one nanometer), electrons can tunnel through the vacuum barrier between the two conductors.

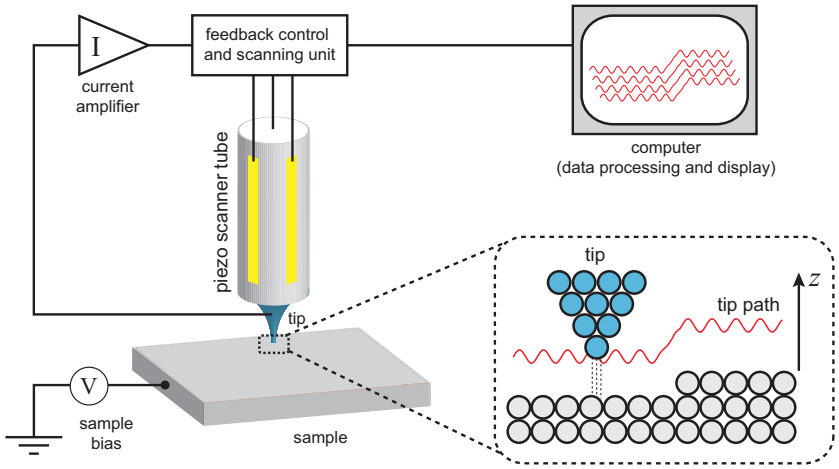

Figure 3.1: Schematic diagram of a scanning tunneling microscope. The simplified schematic illustrates the principle of operation of a STM in constant current mode: a sharp metal tip is scanned over a conducting surface using a piezoelectric scanner tube. A finite bias voltage between sample and tip results in a tunneling current which is kept constant by a feedback loop which regulates the z-height of the tip. By combining the lateral (x,y) and height (z) information, a topographic map of the surface is acquired.

This results in a finite tunneling current (typically $0.1-1$ nA) when a bias voltage is applied between the tip and the sample. An electronic feedback loop regulates the z-height of the tip so that the measured tunneling current remains constant. By recording the height of the tip as a function of the lateral position, a topographical map of the surface can be generated. This is referred to as *constant current mode* and is the only mode of operation which will be used throughout this thesis.

A simplified energy diagram for the sample/vacuum/tip junction is depicted in Fig. 3.2. Electronic states in both conductors are occupied up to the respective Fermi level E_F. $\Phi_{s,t}$ represents the workfunction for sample and tip, respectively. The vacuum gap of width z between the two conductors presents a tunnel barrier for electrons. In this simplified picture of one-dimensional tunneling through a rectangular barrier we can calculate the change in tunneling current $I(z)$ if the distance between tip and sample is changed by Δz [54]:

$$\frac{I(z)}{I(z-\Delta z)} = e^{2\kappa\Delta z} \tag{3.1}$$

Here, $\kappa = \sqrt{2m_e(\Phi_s - eV)}/\hbar$, m_e is the electron rest mass, and V is the applied bias voltage across the tunnel junction. Assuming a sufficiently small bias ($eV \ll \Phi_s$), we can estimate the change in tunneling current as a function of Δz. Using the appropriate value of $\Phi_s = 4.8\,\text{eV}$ for silicon, we find that the current signal changes roughly by a factor of

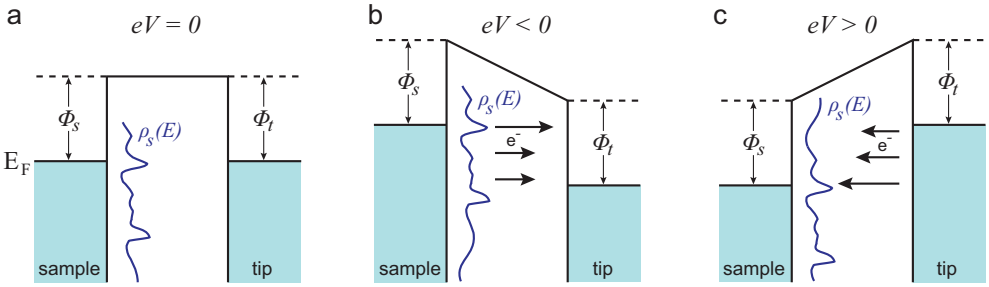

Figure 3.2: Energy diagram for the sample/vacuum/tip tunneling junction. The simplified band structure diagram illustrates different imaging modes of a STM. **a**, Sample and tip are in equilibrium and no net tunneling current flows. The Fermi level E_F separates the filled from the empty states. Φ_s and Φ_t are the workfunctions of the sample and tip, respectively. **b**, When a negative bias ($V < 0$) is applied to the sample, electrons tunnel from the sample's surface states (with density $\rho_s(E)$) to the metallic tip, causing a net tunneling current (*filled state imaging*). **c**, A positive sample bias ($V > 0$) results in a tunneling current flowing from the tip into the surface states of the sample (*empty state imaging*).

10 if z is varied by 1 Å. It is this exponential dependence of the tunneling current on the tip-sample separation (along with the high precision of the piezo elements) that allows for the sub-Å vertical resolution of STM.

In a more realistic picture, the assumption of small bias voltages does not hold anymore. In particular, imaging semiconductor surfaces typically requires a bias on the order of $1 - 2\,\mathrm{V}$ due to the finite bandgap of the semiconductor where no electronic states exist to tunnel from/into. In general, one must therefore consider the density of states of both sample and tip and integrate over the energy window corresponding to the applied bias. Evaluating these integrals is usually an involved process. A common simplification is to assume a constant DOS, ρ_t, for the metallic tip and only consider an energy dependent DOS, $\rho_s(E)$, for the sample. This is illustrated in Fig. 3.2, where the blue curve depicts the surface density of states of the sample. Tersoff and Hamann [57] have given an expression for the bias-dependent tunneling current in this case:

$$I(\mathbf{r}, V) \propto \rho_t(E_F) \int_{E_F}^{E_F+eV} \rho_s(\mathbf{r}, E) dE \tag{3.2}$$

When a negative bias (with respect to the tip) is applied to the sample, electrons will tunnel from the sample's occupied surface states to the tip (Fig. 3.2 b). This is referred to as *filled state imaging*. All STM images of silicon surfaces presented in this thesis fall into this category. Conversely, if a positive bias is applied to the sample, electrons tunnel from the tip into the unoccupied surface states of the sample (*empty state imaging*, Fig. 3.2 c). Despite its simplicity, the above model accounts for an important feature of images

acquired by STM in constant current mode: the generated "height" profile of the sample surface is actually a map of the local density of states within the energy range defined by the applied bias. STM images are therefore always a convolution of the spatial topography and the local electronic structure of the surface.

3.2 The VT-STM system

The main instrument for the fabrication of all devices presented in this thesis is a variable-temperature scanning tunneling microscope (VT-STM) by *Omicron Nanotechnology GmbH*. The system comprises two interconnecting ultra-high vacuum (UHV) chambers – *preparation* and *analysis* chamber – with a base pressure better than 1×10^{-11} mbar. Both chambers are pumped independently via *Varian Star Cell* ion pumps as well as titanium sublimation pumps (TSP) while pressures are monitored via ion gauges. *Balzers* quadrupole mass spectrometers (QMS) can be used to analyze the composition of the residual gas in both chambers. A fast exchange load-lock (FEL) allows for quick loading of both samples and tips which are moved between chambers in specially designed holders using a system of internal transfer arms and manipulators. The latter are equipped with resistive heating elements as well as contact brushes for direct current heating of the Si samples.

Preparation chamber: After pumping the FEL with a turbomolecular pump to roughly 10^{-6} mbar, the sample holder or STM tip is transferred into the preparation chamber. Here, the samples are outgassed for several hours using resistive heating (at $300 - 400°$C) as well as direct current heating (at $\sim$450°C). Furthermore, Si samples are typically "flashed" in this chamber, i.e. annealed to $\sim$1100°C for 1 min to prepare the surface for STM-lithography. The sample temperature is controlled via viewports using a *Mikron M90* infrared pyrometer. The preparation chamber is also equipped with a silicon sublimation source (SUSI) by *MBE Komponenten GmbH* that allows for Si overgrowth of completed samples. The SUSI produces a beam of thermally emitted Si atoms from a heated high-purity silicon filament that allows for growth rates of several Å/min.

Analysis chamber: After flashing, the sample is transferred to the analysis chamber which contains the actual STM stage (see Fig. 3.3 a). The chamber is fitted with a high-purity atomic hydrogen source by *EPI Ltd* which consists of a H_2 microdosing valve and a thermal cracker. The latter is a heated tungsten filament which causes thermal

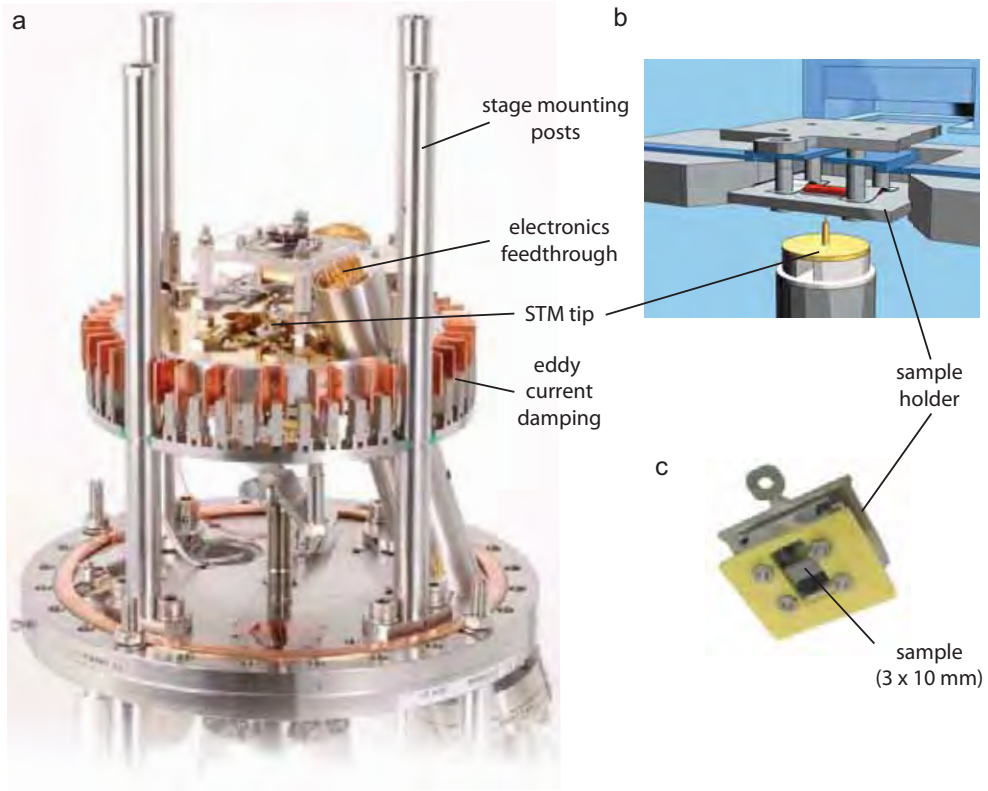

Figure 3.3: The VT-STM. a, The STM stage is mounted on a base plate suspended by springs which decouples the sensitive STM setup from ambient vibration with the help of eddy current dampers. The sample is mounted above the STM tip as illustrated in the schematic shown in **b**. Contact brushes on either side of the sample holder allow for direct current heating of the sample. **c**, The Si(100) wafer substrate is cleaved in $3 \times 10\,\mathrm{mm}^2$ pieces and clamped into the sample holder.

dissociation of the beam of incoming H_2 molecules into atomic hydrogen. This allows for *in-situ* passivation of the highly reactive Si(100) sample surface. The analysis chamber is also equipped with a microdosing source for high-purity (99.999%) phosphine (PH_3), which serves as a gaseous precursor molecule for phosphorus dosing of depassivated Si surfaces. A photograph of the STM stage is shown in Fig. 3.3 a. To decouple the sensitive STM setup from ambient vibrational noise, the entire STM is suspended on soft springs inside the mounting posts. Vibrations of the stage are further reduced by a passive eddy current damping mechanism consisting of an array of copper plates suspended between permanent magnets. The sample is mounted facing downwards above the STM tip as illustrated in the schematic of Fig. 3.3 b. The position of the tip is controlled by piezoelectric actuators that allow for coarse and fine motion of the tip in all three dimensions: coarse movements (in the range from μm to mm) are performed by a piezoelectric "stick-slip" stepper, while fine motion (nm to μm) is achieved via a piezo scanner tube. The STM tips are mounted magnetically on this scanner tube which allows for fast tip exchange.

Throughout this thesis, we have used electrochemically etched tungsten tips supplied by *Omicron Nanotechnology GmbH*. To reduce electronic noise, an *in-situ* pre-amplifier mounted on the STM stage is used for the tunneling current between the STM tip and the substrate.

3.3 STM hydrogen lithography

Ever since the invention of the STM in 1981 by Binnig and Rohrer [22], this novel tool has not only intrigued by its capability to *image* surfaces with unprecedented resolution – but also by its potential to *modify* and *pattern* such surfaces at the atomic scale. Among the most notable examples are the formation of the letters "IBM" with individual xenon atoms on a nickel (110) surface as well as the renowned "quantum corral" by Eigler's group [23] who patterned ferromagnetic cobalt adatoms into a ring on a copper surface and then imaged the resulting standing wave pattern of electronic surface states within the barrier. While the latter experiments are based on the principle of moving certain adatoms on the surface, it is also possible to realize structures by means of a lithographic process. The idea to use the tip of a STM to pattern structures by selectively depassivating silicon surfaces was developed in the early 1990's by Lyo and Avouris [58] for wet-chemically passivated Si(111)-7 $\times$ 7 and later by Lyding and Tucker [59] for Si(100)-2 $\times$ 1 surfaces using a hydrogen termination layer as a monatomic "resist". Since then, several groups have reported the patterning of Si(100):H surfaces using STM [60, 61, 62, 63, 64]. Si(100) is the most technologically relevant surface of silicon due to the fact that it forms the highest quality Si/SiO_2 interfaces. It also exhibits a comparatively simple surface reconstruction compared to other vicinals, such as Si(111).
The process of STM hydrogen lithography has been refined by our group over many years [44, 65, 66, 67]. In this section, we will briefly review the relevant processing steps which are illustrated in Fig. 3.4. For a more detailed discussion, the reader is referred to the existing publications [65, 66] and previous PhD theses [26, 68].

Surface preparation

To minimize surface contamination by ambient gaseous adsorbates, STM lithography is performed in an ultra high vacuum (UHV) environment. *In-situ* processing starts by outgassing the samples for several hours at $T \approx 450°C$ to remove residual adsorbates such as water vapor. During this step, the Si surface is protected from contamination by the native oxide layer which desorbs at higher temperatures around 760°C [69]. To

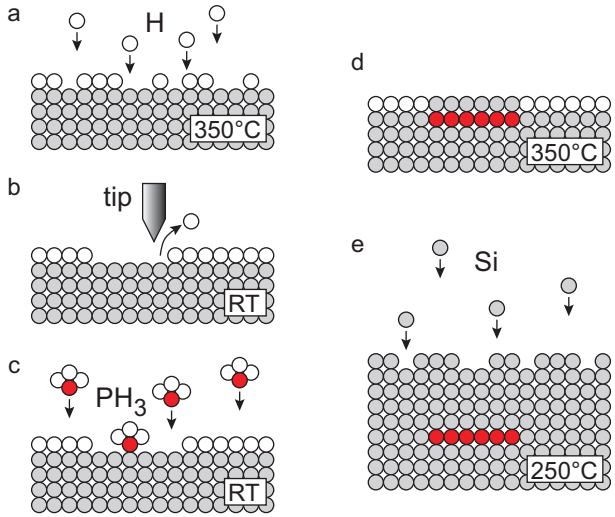

Figure 3.4: STM hydrogen lithography. The schematic illustrates the processing steps involved in STM lithography in UHV along with the typical sample temperature. **a**, The Si(100) surface is initially dosed with atomic hydrogen. **b**, This monatomic resist is then selectively desorbed with the STM tip. **c**, The surface is dosed with phosphine gas which adsorbs onto the exposed Si and dissociates. **d**, A quick anneal incorporates the P atoms into the topmost Si layer. **e**, In a last step, the sample is overgrown with epitaxial Si.

prepare the silicon surface for lithography, the sample is then quickly annealed ("flashed") to ∼1100°C for approx. 1 min. This is achieved by sending a dc current (typically $4-5$ A) through the clamped Si sample. During the anneal, the native SiO_2 layer is thermally removed along with remaining carbon residues [70]. Simultaneously, the Si(100)-2×1 surface reconstruction is formed as a result of the thermal activation of the surface Si atoms. After 1 min at 1100°C, the temperature is first quenched to ∼800°C and then slowly reduced to RT at a rate of ∼100°C/min. The slow cool-down yields a low-defect (2×1)-reconstructed surface.

Hydrogen termination

As a result of the (2×1)-reconstruction every surface Si atom is left with one electron that does not participate in a covalent bond with a neighboring atom. These unpaired electrons are referred to as *dangling bonds* (DB) and they are responsible for the high reactivity of the clean Si(100) surface. To passivate the surface, it is terminated with atomic hydrogen which (in contrast to molecular H_2) has a sticking coefficient close to one. The surface is exposed to H at a pressure of 5×10^{-7} mbar for 6 min (corresponding to an exposure of ∼140 Langmuir) to ensure saturation dosing. During the H dosing step (illustrated in Fig. 3.4 a), the sample is dc heated to 350°C to ensure the formation of a monohydride

layer, where exactly one H atom is covalently bound to each Si dangling bond. Here, the temperature is a trade-off between a low-defect Si surface (since atomic H causes etching of Si surfaces at RT [59]) and a high-quality H layer (since hydrogen thermally desorbs from the Si(100):H surface at temperatures above ∼470°C [71]). A common defect of the terminated surface are hemihydrides, where only one H is bound to a silicon dimer leaving one single dangling bond. These single dangling bonds are visible as bright protrusions in STM images. The H layer can be removed thermally (from the entire surface) by heating the sample above ∼470°C [71]. Alternatively, the H "resist" can be removed selectively by the spatially confined electric field between the STM tip and the sample.

Selective depassivation with the STM tip

In the early 1990's, several groups found [72, 73] that hydrogen could be desorbed at RT from a monohydride Si surface by applying a bias of several volts to a STM tip. Based on these early experiments, Lyding and Tucker [59] developed the idea of using the monatomic hydrogen layer as a resist for a novel form of STM-based nano-lithography (Fig 3.4 b). The desorption is the result of an electron-stimulated process in the strong electric field between the STM tip and the sample. Different mechanisms for the tip-induced desorption of hydrogen have been identified, depending on the applied bias voltage [74]. At low voltages (sample bias approx. +2.5 V to +5.5 V), inelastic tunneling processes cause the excitation of a vibrational mode of the Si:H covalent bond which eventually breaks the bond. At higher bias voltages (> 6 V), electrons emitted from the tip can directly excite the σ bond between Si and H, thus occupying the higher-energy anti-bonding level σ^* of the bond.

For the purposes of this thesis, different STM-lithography parameters were used during device fabrication. The patterning process usually begins with the inner structures (typically within one $400 \times 400\,\mathrm{nm}^2$ scan frame). Here, we aim to achieve sub-nm patterning precision with well-resolved edges of the desorbed regions. In particular, we want to minimize the lateral extent of the tip electric field in order to avoid excessive "stray desorption", i.e. the unwanted random desorption of single H atoms in the vicinity of the intended structure. For these inner device regions, we therefore use smaller bias voltages (typically around +4 V) and a lower feedback current ($1 - 2$ nA) at tip speeds of 100 nm/s or less. For larger outer structures (with feature sizes on the order of hundreds of nm) where precision is not paramount, we generally focus on minimizing the patterning time. This is achieved by a higher tip bias (typically $6 - 7.5$ V) and feedback current ($2 - 3.5$ nA) as

well as much higher tip speeds (up to 1000 nm/s). It should be noted, however, that the optimal desorption parameters may depend on the sharpness and the atomistic details of the individual tip.

Dosing and incorporation

After desorption, the entire surface is dosed with phosphine (PH_3) which serves as a gaseous precursor molecule for P incorporation. Here, the sample is kept at RT and exposed to PH_3 at a pressure of 5×10^{-9} mbar for 6 min (corresponding to an exposure of ∼1.4 Langmuir). PH_3 molecules selectively adsorb only onto the areas that were depassivated during H-lithography with a sticking coefficient of essentially 1 [75] (Fig. 3.4 c). By contrast, phosphine adsorption is inhibited in the H terminated regions.

The underlying reaction pathways and kinetics have been well-documented for the clean Si(100) surface [41, 71, 76]: an adsorbed PH_3 molecule undergoes a successive dissociation on the Si surface, losing all of its 3 H atoms in the process:

$$PH_3(\text{ads}) \rightarrow PH_2 + H \rightarrow PH + 2H \rightarrow P + 3H \rightarrow P(\text{incorp})$$

In STM images of dosed surfaces (see Fig. 3.5 c), the corresponding PH_x species can be identified by their apparent height and their relative position with respect to the Si dimers underneath [76]. A brief (typically 1 min) anneal at 350°C then causes the P atoms to substitute for a vicinal Si atom in the topmost layer of the substrate, ejecting a Si atom in the process [77] (Fig. 3.4 d). These Si adatoms tend to form chains on the Si surface, perpendicular to the dimer rows underneath. As a result of the incorporation, the P donor now occupies a substitutional Si lattice site where it is covalently bound to its 3 neighboring Si surface atoms. P dopant diffusion and segregation is therefore minimized during the subsequent processing steps. Importantly, the H mask stays intact during the 350°C anneal. The STM-defined doped regions thus maintain their integrity throughout the incorporation process [78]. Under the above conditions, we reliably obtain a P coverage of ∼0.25 ML which corresponds to a sheet doping density of $\sim 1.7 \times 10^{14}\,\text{cm}^{-2}$. This is consistent with theoretical studies of the P incorporation mechanism [41] as well as the experimental carrier densities measured on δ-doped Si:P Hall-bar devices [43].

The incorporation pathway will be discussed in more detail in chapter 7, where we demonstrate the controlled incorporation of a single P donor within a depassivated area of 3 adjacent dimers.

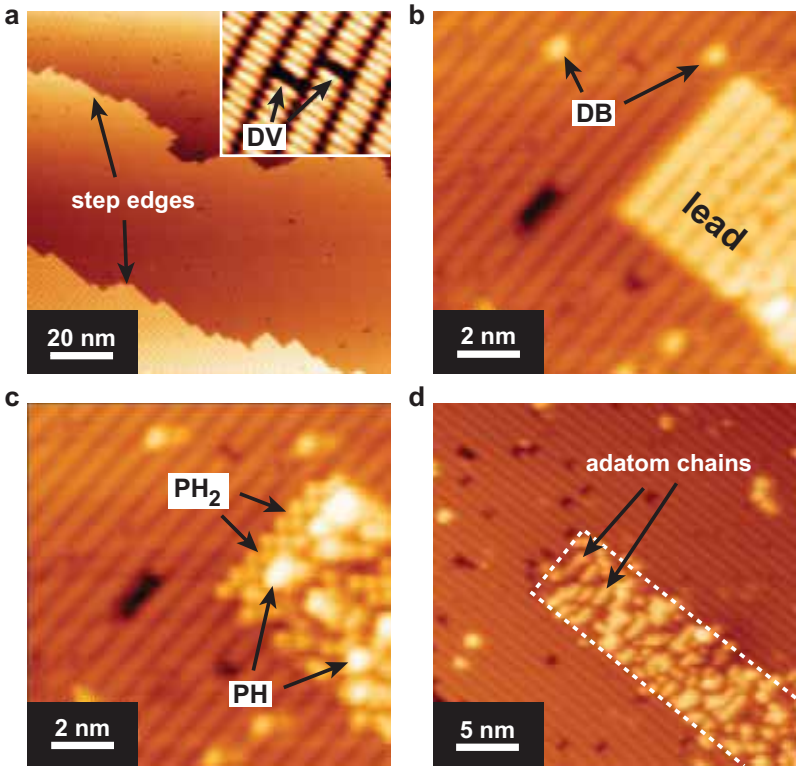

Figure 3.5: STM images of the Si surface. Representative filled state images of the Si surface taken at various stages of STM lithography. **a**, A clean Si(100) surface before H-termination showing monatomic steps ∼1.4 Å in height. The inset is a high-resolution image of the bean-shaped Si dimers along with two single dimer vacancy (DV) defects. **b**, A rectangular area (brighter region) has been desorbed on the H-terminated surface. Some single dangling bonds (DB) are visible. **c**, The same region after dosing with phosphine. The dissociation products PH_2 and PH are visible within the H-desorbed regions. **d**, Si adatom chains are observed in the patterned area (outlined by dashed line) after P incorporation.

Silicon overgrowth

After the incorporation anneal, the entire surface is overgrown with Si from a thermal sublimation source (Fig. 3.4 e) to achieve full electrical activation [79] of the incorporated donors and to encapsulate the patterned Si:P structure, removing it from surface states. The Si growth rate is typically on the order of ∼1.4 Å/min (1 ML/min). During overgrowth, the sample is dc heated to 250°C. This low growth temperature maintains the structural integrity of the Si:P device by minimizing the possibility of dopant diffusion out of the STM-patterned area [80].

While the surface roughness generally increases as a function of overgrowth thickness, we still find a good epitaxial quality of the surface after overgrowth of typically 25 nm [81]. It should be noted that earlier experiments have included an additional 470°C anneal (after donor incorporation) to remove the remaining H mask [44]. It is known that the presence

of surface hydrogen can hinder Si surface diffusion and thus reduce the epitaxial quality of the overgrowth surface [82]. However, the H mask was left intact during Si overgrowth for all devices presented in this thesis to minimize the thermal budget. While the surrounding H does indeed lead to a slightly increased roughness of the overgrowth surface (over the H terminated areas) [82], we did not find any detrimental effects on the electronic transport properties of our devices.

Some typical STM images of a Si(100) surface are depicted in Fig. 3.5 at several stages of the lithography process. Panel a illustrates a clean surface before H-termination. Two step edges (∼1.4 Å in height) are visible along with several dimer vacancies (DV), the most common surface defects which appear as dark features on the surface. Two single DVs are shown in the close-up in the inset of Fig. 3.5 a. In this high-resolution image, the individual bean-shaped Si dimers are clearly discernible. Fig. 3.5 b depicts the end of a ∼5 nm wide electrical lead structure after selective removal of the H resist by the STM tip. A few single dangling bond (DB) sites are visible, but it is known that no dissociative adsorption of PH_3 molecules can occur at these sites [41, 76]. The depassivated regions of the Si surface appear brighter than the surrounding hydrogen resist. This is a typical example of how STM images are a convolution of both the geometric as well as the electronic topography of a surface: even though the depassivated regions could be expected to be "lower" (due to the absence of the H layer), they appear "higher" (i.e. brighter) in the STM images due to the additional tunnel current contributed by the Si surface states [56]. Panel c of Fig. 3.5 shows the same area after dosing with phosphine where the dissociation products PH_2 and PH can be identified within the H-desorbed region. A similar lead structure after P incorporation is depicted in Fig. 3.5 d, where the ejected Si atoms are found to form adatom chains running perpendicular to the underlying silicon dimer rows. The latter are confined to the STM-patterned area (dashed line) thus confirming the structural integrity of the H-mask during the P incorporation anneal. Furthermore, the absence of ejected Si adatoms outside the patterned region corroborates the fact that single DB sites indeed cannot adsorb PH_3 molecules and thus do not participate in the incorporation process.

3.4 *Ex-situ* processing of samples

After successful STM-patterning and silicon encapsulation, post-processing of samples was carried out in the cleanroom environment of the Semiconductor Nanofabrication Facility at UNSW which is rated to *ISO class 5* (corresponding to *AS class 3.5*) with a maximum concentration of 10^5 particles $\geq 0.1\,\mu$m per cubic meter. This section briefly introduces the

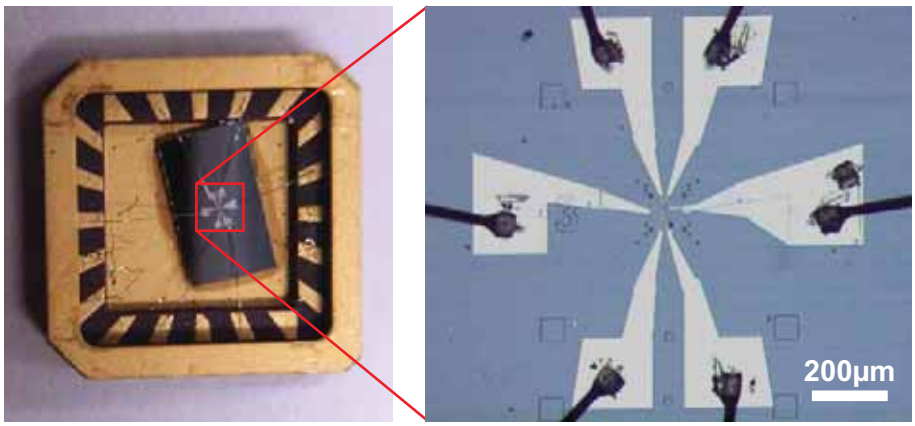

Figure 3.6: Packaged device ready to measure. A completed device glued and Al bonded into a chip carrier. The wet-etched registration marker array is clearly visible in the microscope image on the right along with the EBL-patterned *ex-situ* metallic contacts and bond pads.

equipment used for imaging and contacting of the devices and summarizes the fabrication steps to prepare the samples for electrical measurements. The relevant process parameters for each step are listed in the form of "recipes" in appendix A.4.

The alignment and definition of *ex-situ* metallic contacts was performed in a *FEI XL30* scanning electron microscope (SEM) which is equipped with a *Nanometer Pattern Generation System (NPGS)* by *JC Nabity Lithography Systems* for electron beam lithography (EBL). For high-resolution surface topography measurements and to determine the exact encapsulation thickness of completed devices, the samples were imaged with an atomic force microscope (AFM) by *Digital Instruments (DI)*. Wet etching and chemical processing was performed in designated fume cupboards while silicon dry etching was carried out in a home-built hollow-cathode reactive ion etcher (RIE). For metallization of aluminium ohmic contacts a *Sloan/Varian* e-beam evaporator was used at a typical pre-evaporation pressure of $\sim 10^{-6}$ mbar. The evaporator is equipped with a quartz thickness monitor to control the deposition rate and thickness of the deposited metal. To remove any residue of e-beam resist after developing, the samples were generally treated in a *Denton Vacuum PE-250* oxygen plasma asher.

After lift-off, the samples were cleaved to a length of ∼5 mm and then glued into a leadless ceramic chip carrier (see Fig. 3.6). E-beam resist is used as a glue to ensure that the samples can easily be removed from the carrier if further processing is necessary. In a final step, the contacts of the device are wire bonded to the chip carrier using a *Karl Suss* semi-automatic aluminium wedge bonder[1]. One downside of using Al is that it becomes

[1]Gold wire bonding was avoided due to possible contamination of the sample surface for subsequent processing steps, such as metallization of additional top-gates.

superconducting below a critical temperature $T_c = 1.2\,\mathrm{K}$, which will affect electronic measurements in zero magnetic field at mK-temperatures. However, this is easily overcome by applying a weak background magnetic field higher than the critical magnetic field of Al ($\sim$10 mT) [83].

3.5 Electrical characterization

3.5.1 Measurements at 4 Kelvin

After successful post-processing of a device, every sample is initially characterized at liquid helium (LHe) temperatures (4.2 K) in a designated dip station. It should be noted that the setup of this dip station is optimized for quick sample exchange rather than for low-noise measurements. The main objective of this first characterization is to check for good ohmic contact to the STM-patterned device. This is achieved by measuring the resistance between two terminals on one STM-patterned contact patch which is typically a few 10s of kΩ. This will be discussed in more detail in section 4.3.6 of the following chapter.
For gated devices, the next step is to determine the effective *gate range* for each gate, i.e. the voltage range where the gate leakage current remains below a certain threshold. Excessive leakage currents can alter the transport properties of nano-scale devices either temporarily (until the sample has been thermally cycled to well above the carrier freeze-out temperature) or permanently. The gate leakage characteristics for our devices exhibit a negligible temperature dependence below 4 K, so this initial characterization is crucial for subsequent measurements at mK temperatures. Finally, the transport properties may be measured as a function of gate voltage and/or magnetic field (up to 2 T). In the case of quantum dot devices, initial stability diagrams are recorded. If device performance at 4 K is satisfactory the sample is subsequently measured more extensively in a dilution refrigerator.

3.5.2 Measurements in a dilution refrigerator

Electronic measurements at milli-Kelvin (mK) temperatures were performed in a *Kelvinox K100* ^{3}He/^{4}He dilution refrigerator by *Oxford Instruments*. The latter is encased in a copper radiation shield to reduce electronic noise due to external radiation, particularly at radio and microwave frequencies. Since the greater part of the measurement data presented in this thesis have been taken at mK-temperatures, we will briefly describe the basic principle of operation of a dilution fridge [84] in the following section.

Principle of operation of a dilution refrigerator

A simplified schematic of a dilution refrigerator (reproduced from [84]) is shown in Fig. 3.7 a. Its principle of operation, originally proposed in 1951 by H. London, relies on the specific thermodynamic properties of the two stable helium isotopes at very low temperatures. When a mixture of ^{4}He and ^{3}He is cooled below a critical temperature it separates into two phases: the *concentrated phase* (rich in ^{3}He) and the lighter *dilute phase* (rich in ^{4}He). Since the enthalpy of the ^{3}He in the two phases is different, cooling power can be generated by "evaporating" ^{3}He from the concentrated into the dilute phase. The ^{4}He (which makes up the majority of the dilute phase) is inert and the ^{3}He 'gas' moves through the liquid ^{4}He without interaction. Here, the ^{3}He 'gas' is formed at the phase boundary in the mixing chamber at a temperature of a few mK. In a continuously operating closed-loop system the latter is pumped from the dilute phase and returned into the concentrated phase as illustrated in the schematic. The 1K pot is used to condense the ^{3}He/^{4}He mixture into the dilution unit. The still below further cools the incoming ^{3}He to below 1.2 K before it enters the heat exchangers and the mixing chamber. In the still itself, the ^{3}He is pumped away from the liquid surface at ~ 0.6 K. Here, ^{3}He evaporates preferentially due to its much higher vapor pressure than ^{4}He at this temperature. This in turn results in an osmotic pressure difference within the dilute phase which drives a flow of ^{3}He from the mixing chamber to the still. The ^{3}He leaving the mixing chamber also cools the returning flow of concentrated ^{3}He in a series of heat exchangers.

Fig. 3.7 b shows a photograph of the sample probe inside the *inner vacuum chamber* (IVC) along with the most important functional parts as pictured in panel a. The sample is mounted at the lower end of a copper rod which is thermally coupled to the mixing chamber. The device itself is cooled indirectly via the bonding wires and the thermal contact to the chip carrier. During operation, the IVC is in coarse vacuum ($\sim 10^{-5}$ mbar) to avoid convective heat transfer from the surrounding liquid helium bath to the sample probe. Several co-axial metallic shields (not shown) prevent radiative heating of the mixing chamber from the warmer parts of the cryostat. Two samples can be mounted simultaneously either in perpendicular (as shown) or parallel orientation with respect to a magnetic field which is created by a superconducting magnet coil mounted coaxially in the LHe bath of the cryostat (Fig. 3.7 c). The setup allows for homogeneous magnetic fields up to ± 8 Tesla (at an accuracy of 1 mT) which can be swept at a rate of up to 0.2 T/min. The sample is connected electrically to the break-out box at the top of the cryostat via twisted pair cables which are characterized by low noise pick-up. For better thermaliza-

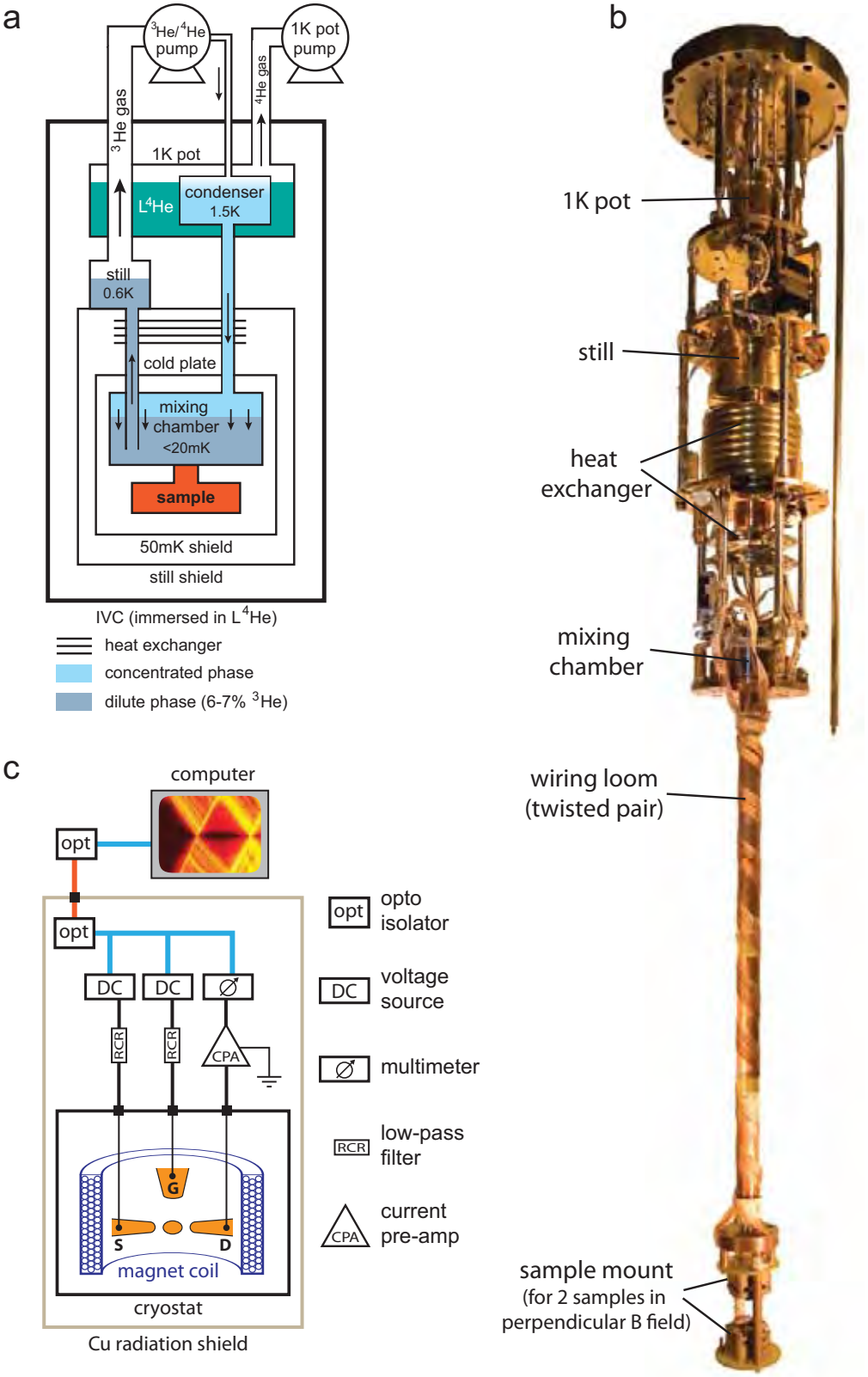

Figure 3.7: Schematic of a ^{3}He/^{4}He dilution refrigerator. **a**, Simplified schematic of a dilution refrigerator. **b**, Photograph of the sample probe mounted inside the IVC. **c**, Instrument setup for low-noise dc electrical transport measurements.

tion (to reduce the heat load on the mixing chamber) the wiring loom of 20 cables is wound around the probe many times at several points of the probe. The setup allows for base temperatures of ∼20 mK which can be monitored via a RuO_2 thermometer mounted close to the mixing chamber. It should be noted, however, that this does not necessarily correspond to the actual sample temperature. In particular, the electron temperature of quantum transport devices can be significantly higher than this bath temperature as will be discussed in more detail in chapter 6. The sample temperature can be raised up to ∼1 K by means of a resistive heater element. However, the transport data of the quantum devices presented in this thesis were acquired almost exclusively at base temperature.

Measurement setup

Fig. 3.7 c is a schematic of the typical instrument setup used to measure electronic transport through a quantum dot device. All electrical measurements were performed in direct current (dc) mode: two dc voltage sources (in most cases a *Yokogawa 7651*) are used to apply the gate and bias voltages. The latter is applied *asymmetrically*, meaning that the voltage is applied to one transport electrode (usually the source S) while the other electrode is grounded via the current pre-amplifier (CPA). We mainly used a *DL Instruments 1211* CPA and sometimes an older model *Stanford Research Systems SR-570*, both with variable gain. These low-noise pre-amps convert the source-drain current into a voltage with a typical gain factor of $10^6 - 10^9$ V/A which is then read out with a *HP/Agilent 34401A* digital multimeter. The instruments are connected to the break-out box of the cryostat with BNC cables (depicted as blue lines in Fig. 3.7 c), with passive inline RC-type low-pass filters (typically ∼ 100 Hz cut-off frequency) on the voltage cables to reduce high-frequency noise.

All instruments as well as temperature and magnetic field are controlled via GPI-Bus by an external computer. Galvanic coupling to the measurement setup inside the copper cage is avoided by using optical isolators, connected by a fibreglass cable (orange line in Fig. 3.7 c). Using the LabView programming environment, the measurement and data acquisition process can be controlled via automated software routines. Many of the measurement routines used throughout this thesis were originally programmed by Dr. A. Fuhrer, and modified or amended as needed. Depending on the sensitivity of the measurement, we recorded data at a typical acquisition rate of $2 - 5$ Hz.

Chapter 4

Advancements in device fabrication

One of the key challenges in fabricating functional devices using STM-lithography is connecting the planar, buried P-doped structures to the outside world [44]. In the course of this thesis, an improved strategy for aligning external electric contacts and surface gates to the STM-patterned devices has been developed which will be discussed in this chapter.

We briefly summarize the initial registration scheme based on optical lithography which has previously been adapted by our group [68, 85] and discuss its shortcomings. We then present an improved, complete electron beam lithography (EBL)-based fabrication scheme for aligning multiterminal Ohmic contacts and top gates to buried, phosphorus-doped nanostructures in silicon defined by STM H-lithography. By prepatterning a silicon substrate with EBL-defined, wet-etched registration markers, we are able to align macroscopic contacts to buried, conducting STM-patterned structures with an alignment accuracy of $\sim$100 nm. A key aspect of this alignment process is that, by combining a circular marker pattern with step engineering, we are able to reproducibly create atomically flat, step-free plateaus with a diameter of several hundred nm so that the active region of the device can be patterned on a single atomic Si(100) plane at a precisely known position.

To demonstrate the applicability of this registration strategy, we show low temperature measurements from a 50 nm wide P-doped silicon nanowire device patterned on an atomically flat terrace. We conclude the chapter by summarizing further advancements of our fabrication strategy as they are relevant for the realization of quantum transport devices presented in later chapters of this thesis.

4.1 Registration markers for UHV devices

The capability of the scanning tunneling microscope to perform nanolithography on H-passivated silicon surfaces has enabled the fabrication of atomically precise, highly doped phosphorus devices [63, 67, 85]. To achieve full electrical activation of the dopants as well as to avoid detrimental surface effects, these planar Si:P structures are encapsulated deep ($\sim$25 nm) within the silicon host crystal in the ultra high vacuum (UHV) environment of the STM system. Electrical characterization of such devices requires alignment of *ex-situ* macroscopic contacts to the buried dopant layers. Since the dopants are confined essentially to a monatomic plane occupying substitutional Si lattice sites, there is little contrast between the STM-patterned regions and the surrounding substrate. After removal from UHV, the encapsulated devices are thus generally not visible to optical and scanning electron microscopes (SEM) as well as atomic force microscopes (AFM), making it difficult to align directly to the encapsulated structures. As a consequence, it is necessary to introduce some form of registration markers that can be used to align external contacts.

Several methods exist to realize registration markers for STM applications [68], most of which rely on prepatterning of the initial substrate. However, the high temperature anneal ($\sim$1100 °C) required to form a low-defect (2×1)-reconstructed Si(100) surface in UHV for STM lithography (see chapter 3) places severe constraints on the potential types of markers used. A common approach is to pattern surface markers made of metals or alloys, such as tungsten [86], titanium [87, 88], or CrPt [89]. However, even refractory metals with a melting point far higher than that of silicon (1414°C), are still subject to surface diffusion at elevated temperatures [68, 90]. A second method relies on ion implantation to define markers prior to introducing the sample into UHV [91, 92], which can later be imaged in the STM. Again, thermally activated diffusion degrades the integrity of ion implanted regions [63]. Possible deterioration of surface quality in the device region due to surface contamination and/or diffusion of impurities therefore limits the practical use of alignment markers defined by metal deposition or ion implantation for our purposes [85].

An alternative approach is to etch marker structures directly into the substrate [93] rather than introducing any foreign materials. This method has previously been adapted and modified by our group [85] and enabled the alignment of *ex-situ* surface contacts to buried STM-patterned nanoscale devices, as will be discussed in the next section.

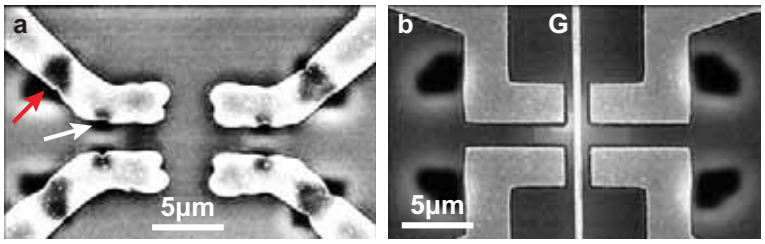

Figure 4.1: Optical vs e-beam lithography. **a,** SEM image of a contacted device which was patterned following the old fabrication scheme. An array of 4 inner markers (white arrow) was used to coarsely position the STM-patterned structure *in-situ*. Larger triangular markers (red arrow) were used to align *ex-situ* ohmic contacts defined by optical lithography. **b**, As a comparison, ohmic contacts were defined on a similar marker structure using e-beam lithography. This allows for patterning of much smaller well-defined structures such as a 250 nm wide top gate (G) aligned precisely between the ohmic contacts.

4.2 Shortcomings of previous registration scheme

In this section, we will briefly review the registration scheme previously used by our group to fabricate STM-patterned transport devices. Largely developed by F. Ruess [68, 85], this method relies on the use of optical lithography in conjunction with wet-etching to define registration markers on the silicon substrate prior to STM-patterning. To ensure a UHV compatible, contamination-free substrate, a thermal oxide layer is used as a lithography mask for the marker structure along with several rigorous wet-chemical cleaning procedures. The registration markers are defined by several etched structures of varying shape and size, etched to a uniform depth of ∼350 nm. These markers are designed to enable alignment of metal contacts after Si overgrowth using optical lithography. Fig. 4.1 a shows a SEM image of a contacted device after metallization of four-terminal ohmic contacts. Inner markers (indicated by the white arrow) are used to roughly define the position of the STM-patterned device, while larger triangular structures (along with larger outer markers) facilitate alignment during optical lithography.

This initial registration method was sufficient to fabricate several successfully contacted STM-patterned devices such as nanowires [85], dopant arrays [94], and tunnel junctions [95]. However, it is burdened with several shortcomings that severely limit its viability to fabricate more complex STM-devices, particularly top gated structures:

- **Poor alignment accuracy**: Using UV optical lithography in conjunction with the array of etched marker structures results in a comparatively poor overlay accuracy between external contacts and the buried STM-patterned structures on the order of ±500 nm. Here, the alignment accuracy is essentially limited by the precision with

which the optical lithography mask can be aligned to the sample in the mask aligner. This necessitates the patterning of large STM-patterned contact patches ($\sim 6\,\mu\mathrm{m}^2$) to reliably establish electrical contact to the doped regions after encapsulation. Depassivating such large regions on the Si(100):H surface is a time-consuming process, taking on the order of 1 hour/$\mu\mathrm{m}^2$ under the typical desorption conditions ($V_{tip} \sim -4$ to $-8\,\mathrm{V}$ and $I_t \approx 1-3\,\mathrm{nA}$). More importantly, the poor alignment accuracy severely limits the practicability of patterning top gates, which need to be patterned precisely over the nano-scale dopant devices.

- **Lack of *in-situ* metrology**: The device is generally STM-patterned *somewhere* in between 4 inner markers, which are $15\,\mu\mathrm{m}$ apart. Locating this inner device area prior to H-lithography is a time-consuming process that relies on large STM scan frames. Furthermore, in the absence of STM-compatible central markers it is virtually impossible to relocate the patterned structure once the STM tip has been moved away from its initial position. Multi-step processes, that require the STM tip to be retracted from the sample at some point[1], are therefore not viable with this method. Also, tip changes during the patterning process are not practicable since they require the tip to be completely removed from the sample. After a new tip has been installed, relocating the desorbed device regions would require the scanning of a very large area (defined by the innermost markers) on the order of 10s of $\mu\mathrm{m}^2$. With typical scan rates (at sufficient resolution) of $\sim$30 min per $1\,\mu\mathrm{m}^2$ this is generally not feasible.

- **Minimum feature size**: Using standard UV mask aligners to perform optical lithography for *ex-situ* metallic structures makes it challenging to reliably pattern feature sizes smaller than a few hundred nanometers. Defining multiple top gates over a STM-patterned device (which is typically patterned within a $400 \times 400\,\mathrm{nm}^2$ scan frame) is therefore not possible.

- **Flexibility of process**: STM-patterning is restrained by the necessity to be compatible with the pre-defined optical lithography mask for the ohmic contacts. Also, it is not possible to change the layout of a new device without going through the time-consuming and costly process of designing a new optical mask.

To address these issues, an improved, fully EBL-based alignment strategy was developed which will be discussed in the next section. The advantages of using EBL instead of optical

[1] An example are 3D devices [96], i.e. vertical structures containing several stacked STM-patterned regions with Si buffer layers grown in between.

lithography are demonstrated in Fig. 4.1 b which shows a SEM image of an exemplary device with a 250 nm wide top gate, patterned precisely between the four-terminal ohmic contacts.

4.3 Novel method for surface gate and contact alignment

The ability to align multiple gates and Ohmic contacts to buried STM-patterned dopant regions requires a high degree of overlay accuracy. With the initial alignment scheme adopted by our group, this has remained a key challenge for the realization more complex, gated nano- and atomic-scale devices. To overcome these challenges, an advanced alignment scheme has been developed as part of this thesis, which has two unique features. Firstly, the process is fully EBL-based, allowing smaller (<500 nm feature size) and shallower (∼60 nm) markers that can be imaged by the STM directly. This results in an increased overall alignment accuracy down to ∼100 nm. Secondly, by using circular markers, we are able to control the formation of large ($\geq$ 300 nm diameter) step-free plateaus in the center of the registration marker array such that the active region of the device can be STM-patterned onto an atomically flat Si(100) plane.

4.3.1 Etched registration markers

For our new registration scheme, we will retain the wet-chemical etching procedure [85] that has previously proven effective to prepattern the Si substrate without contaminating the surface. Several chemistries exist for wet-etching of silicon. The most commonly used etch chemistries for micromachining silicon wafers in industrial applications rely on aqueous solutions of alkali hydroxides, such as KOH [97]. For our markers, we use a solution of tetramethylammonium hydroxide (TMAH), a quaternary ammonium salt which has a slower etch rate than KOH and has been found to result in lower surface roughness of the etched Si(100) surfaces [98]. The etch rate can be controlled by adjusting the concentration as well as the temperature of the etchant [98].

Wet-etching requires a chemically robust etch mask to define the etched regions. We use a ∼50 nm SiO_2 layer which acts as a lithographic mask[2] and simultaneously protects the Si surface from possible contamination during the pre-patterning process [85]. While wet-etching is inherently a very clean method, it has the disadvantage of being an anisotropic process with varying etch rates for different crystal directions [98, 99]. For our purposes, this leads to an unfavorable etch profile. In particular, the sidewalls of an etched region on

[2]The etch rate selectivity of TMAH between Si and SiO_2 is on the order of 10^4 [98].

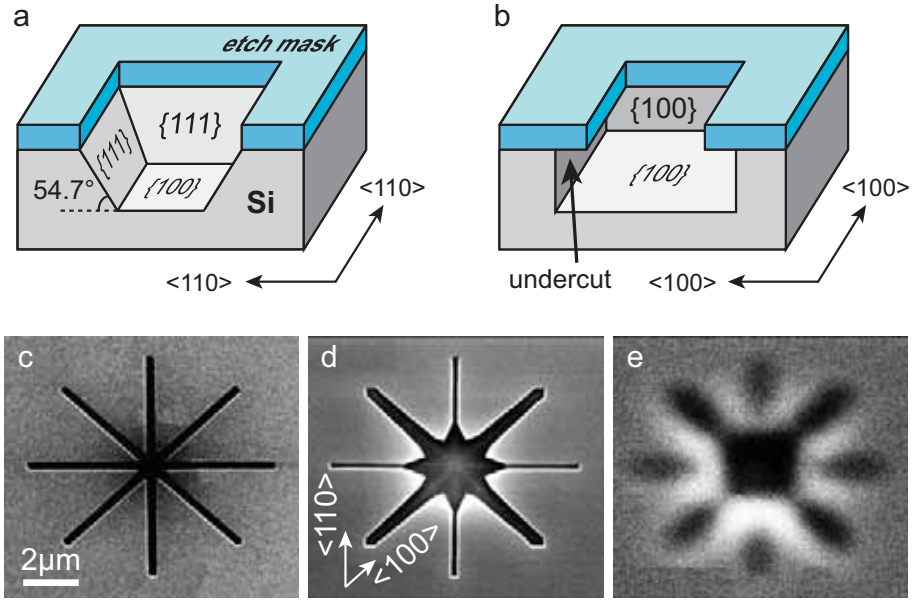

Figure 4.2: Anisotropy of wet etch process. **a**, Schematic etch profile illustrating the anisotropy of wet etching silicon. The etch trenches will generally have {111} sidewalls which form a ∼54.7° angle with the surface. **b**, Vertical sidewalls can be achieved if the etch mask is precisely aligned with the ⟨100⟩ axes. However, an inevitable lateral undercut effectively widens the structures. **c**, SiO_2 mask for an experimental star shaped marker structure. **d**, The same marker after wet etching (to ∼200 nm depth) and removal of the etch mask. While the lines parallel to ⟨100⟩ have vertical sidewalls, they are much wider due to underetching. **e**, The marker structure after a standard 1 min anneal at 1100°C yielding poor edge contrast.

a Si(100) surface will generally not be vertical but rather form a 54.7° angle with respect to the wafer surface, thus exposing the chemically more stable {111} surfaces as illustrated in Fig. 4.2 a. Indeed, the {111}/{100} etch ratio for 22% TMAH solution was determined to be approx. 0.08 [98]. Vertical sidewalls can only be achieved if the edges of the etched region are aligned precisely with the ⟨100⟩ crystallographic axes. However, the resulting etch profile in this case will always have a low aspect ratio [99], due to an unavoidable undercut as illustrated in Fig. 4.2 b.

The anisotropy of wet-chemical etching of Si(100) can be demonstrated experimentally by the star-shaped structure shown in the bottom row of Fig. 4.2. Here, panel c depicts a SEM image of the lithographic mask where four uniform ∼350 nm wide trenches have been etched into the SiO_2 layer. After a TMAH etch of the underlying Si substrate and removal of the oxide mask, the etch profile exhibits a drastic orientation dependence (Fig. 4.2 d): While the trenches along the ⟨110⟩ direction are narrow with slanted sidewalls, the ones along ⟨100⟩ have vertical sidewalls but are much wider with a less well-defined edge. Panel e shows the same structure after the 1100°C anneal in UHV which is necessary to prepare

the surface for STM-lithography. We observe a significant loss of integrity of the etched marker structure [85] due to a silicon step-flow process (see section 4.3.3). This results in a greatly reduced contrast in optical and SEM images. More importantly, the thermal degradation of the well-defined marker edges adversely affects the alignment accuracy, since the latter entirely depends on how precisely the position of the markers can be determined. The development of a novel type of marker structure was therefore necessary to improve the alignment accuracy of our registration scheme, as will be discussed in the next section.

4.3.2 Overview of new registration scheme

In this section, we will give an overview of the new registration scheme and briefly describe the involved processing steps before discussing the key issues in more detail in the subsequent sections.

As part of this thesis, the entire *ex-situ* part of sample processing was shifted from optical lithography to e-beam lithography. This includes the pre-UHV definition of a registration marker array on the sample chips as well as the alignment and patterning of metallic contacts and top gates on encapsulated STM-patterned devices. EBL is not commonly used in industrial silicon processing due to its low yield and comparatively high cost. However, for the fabrication of individual samples as in our case, it offers the advantage of a high alignment accuracy combined with the possibility to reliably pattern much smaller feature sizes down to ∼20 nm. Furthermore, EBL allows for much greater process flexibility since device layouts can easily be modified and tailored specifically for every sample without relying on a specific optical lithography mask.

A schematic overview of the fabrication process is given in Fig. 4.3 along with representative device images for several processing steps. We use commercially available n-type (phosphorus-doped) 2 inch Si(100) wafers with a miscut angle of $\pm 0.1^\circ$ and a bulk resistivity of $1 - 10\,\Omega$cm. The basic chemical processing steps are similar to the ones previously used by Ruess *et al.* [85]. To remove any remaining contamination, the substrate is wet-chemically cleaned in subsequent baths of sulphuric peroxide (3:1 H_2SO_4:H_2O_2), hydrofluoric acid (5% HF), and 6:1:1 H_2O:HCl:H_2O_2. Next, a 50 nm thermal dry oxide layer is grown onto the wafer substrate at 1100°C to act as a lithographic mask. Using e-beam lithography on standard polymethyl methacrylate (PMMA) e-beam resist, a hierarchical array of registration markers is defined in the oxide as illustrated in the schematic of Fig. 4.3 a and c. Importantly, this array comprises two types of markers (indicated by differ-

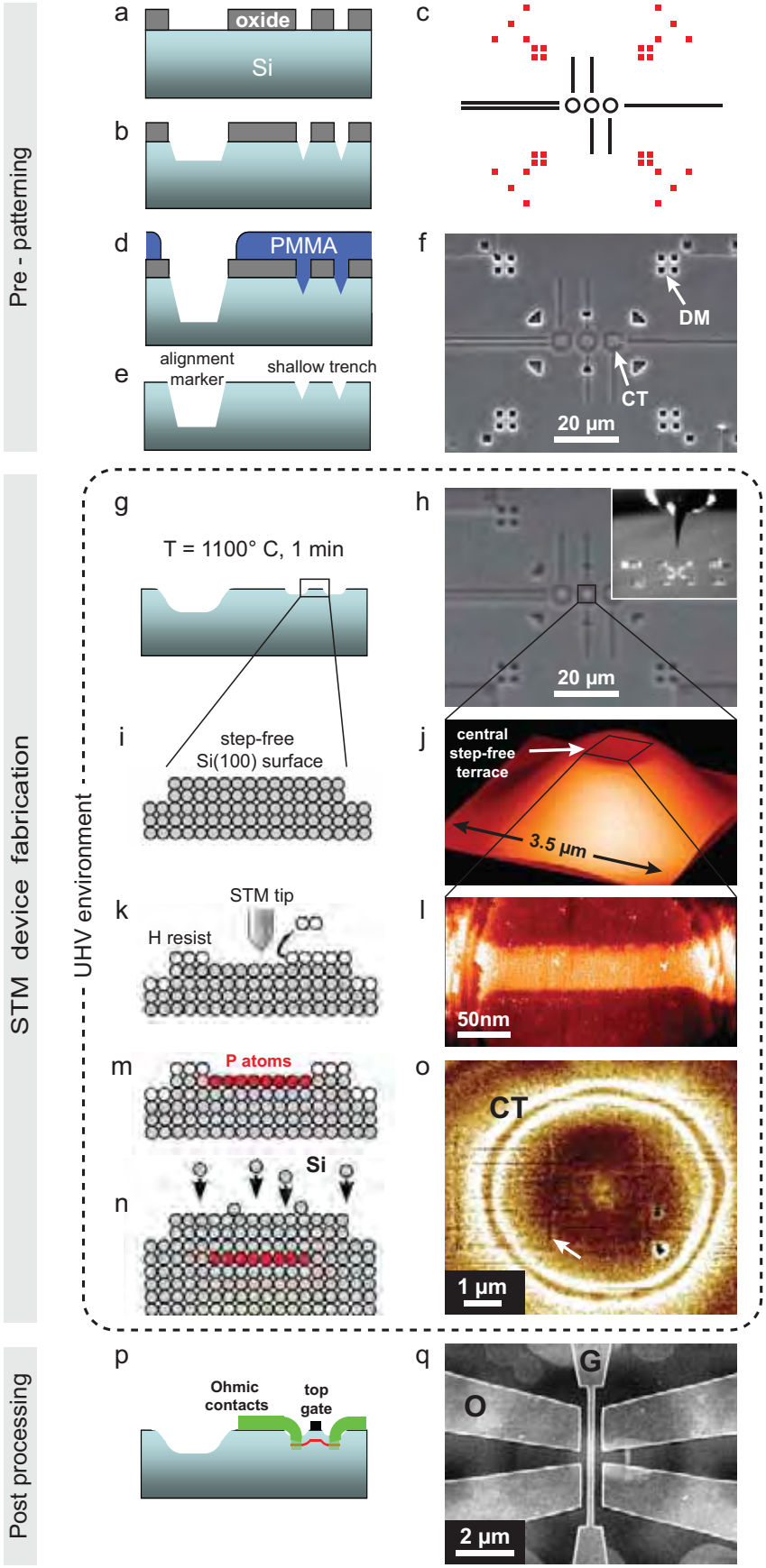

Figure 4.3: Overview of fabrication scheme. See text.

ent colors in panel c) that serve different purposes and are accordingly patterned in two subsequent EBL/wet-etching cycles with different etch depths:

(i) Outer, deeper structures (shown in red in panel c) serve solely as alignment markers and are used for both coarse alignment of the STM tip inside the UHV chamber with an optical microscope ($50\,\mu m^2$ squares, not shown) as well as for fine alignment (2×2 arrays of $2\,\mu m^2$ squares) during the EBL-processing steps after the sample is taken out of the UHV system.

(ii) Inner circular markers (shown in black in panel c) $\sim 5\,\mu m$ in diameter are used both to form a step-free Si(100) plateau that defines the central device region for high resolution STM lithography, but are also shallow enough to allow imaging with the STM, thereby providing extra alignment capability.

Pattern transfer [85] is achieved by etching the SiO_2 mask in buffered HF (15:1 NH_4F:HF) at 30°C (Fig. 4.3 a), followed by a wet-chemical etch of the exposed Si substrate in a 25% aqueous TMAH solution at room temperature. All markers are defined in one EBL step and initially etched to a depth of ∼100 nm (Fig. 4.3 b). To ensure good visibility in the SEM after the initial high temperature anneal ("flashing") in UHV, the outer markers are etched further in a second step to a depth of ∼400 nm. This is achieved by covering the shallow markers with a protective layer of PMMA (panel d) over the oxide mask, with EBL-defined windows opened over the deep markers. Fig. 4.3 f shows a SEM image of a registration marker sample before flashing with the deeper 2×2 square array markers (DM) and the shallow circular trenches (CT) at the center of the marker array (the outermost $50\,\mu m^2$ optical markers are not shown).

After wet etching of the marker array, the protective oxide layer is removed (panel e) in a buffered HF etch followed by a final full cleaning cycle (similar to the initial wafer clean) to remove any organic and metallic residues. The samples are then introduced into the STM system. After outgassing the sample for several hours at ∼450°C using a resistive heater, the sample is direct current heated to 1100°C for ∼1 min. This anneal removes the native oxide layer as well as residual traces of carbon and also forms the Si(100) 2×1 surface reconstruction. The flashing procedure also leads to a loss of integrity of the etched marker structures (Fig. 4.3 g) which adversely affects the alignment accuracy, as will be discussed in more detail in the next section. The corresponding rounding of the markers is clearly visible in SEM images of a marker sample after the anneal (Fig. 4.3 h). In a next step, the Si is terminated with atomic hydrogen which forms a monohydride resist for STM lithography [59] (Fig. 4.3 k). The photograph in the inset of panel h illustrates how

the STM tip appears with respect to the etched registration marker array when viewed through the optical microscope attached to the STM chamber. Using the microscope, the tip can be positioned within approx. $\pm 30\,\mu$m of the center of the array. Beginning with micron-sized scan frames, the central circular marker is then located using the STM in imaging mode (with a typical sample bias of $V_b = -2\,$V and a tunneling current of $I \approx 0.1\,$nA). This process typically takes on the order of 20 min. Here, the long straight trenches visible in Fig. 4.3 f and h are used to quickly guide the STM tip to the center of the array, where a step-free Si(100) plateau has formed as a result of the high-temperature anneal. The atomically flat terrace is generated on top of the "hillock" enclosed by the circular trench due to a thermally activated step-flow process (see section 4.3.4). This is illustrated by the schematic in Fig. 4.3 i. Panel j depicts a $3.5 \times 3.5\,\mu$m^2 STM image of the hillock which is $\sim$60 nm in height and $\sim 4\,\mu$m in diameter at the base. The active device area will be patterned on the step-free area on top of the hillock, which is precisely at the origin of the registration marker array. STM lithography is performed using the standard procedure [44] which has been described in detail in chapter 3: the required device pattern is formed by selective desorption of the H resist (Fig. 4.3 k) by using the STM tip with V_b ranging from $+4\,$V to $+7\,$V and I on the order of several nA.

Figure 4.3 l shows as an example a 50 nm wide nanowire device that has been patterned on a $\sim$300 nm wide terrace. This device will be discussed in more detail in section 4.3.6 below. After H desorption, the surface is dosed with phosphine (PH_3) which adsorbs onto the exposed Si sites. Phosphorus incorporation (panel m) is achieved by a 1 min anneal at 350°C. The entire sample is then overgrown with $\sim$25 nm of epitaxial silicon (panel n). Fig. 4.3 o shows a STM image[3] of an encapsulated device where the circular trench (CT) as well as the edges of larger STM-patterned contact patches are visible (indicated by the white arrow).

After removal from UHV, *ex-situ* ohmic leads are defined by EBL over these larger contact patches, using the deep etched structures as alignment markers (see section 4.3.5). After removing the native surface oxide by a $\sim$5 s dip in buffered HF, the leads are metallized with aluminium. A subsequent 15 min anneal at 350°C causes the Al to diffuse down to the STM-patterned contact patches thereby establishing Ohmic contact between the external leads and the buried device. In a final EBL-step, one or multiple top gates are patterned over the device, as illustrated in the schematic of Fig. 4.3 p. Panel q shows an exemplary SEM image of a completed device with 4 ohmic Al contacts (O) as well as a

[3]The image was reproduced from ref. [100]. A high-pass filter has been applied to increase the visibility of the edges of the device.

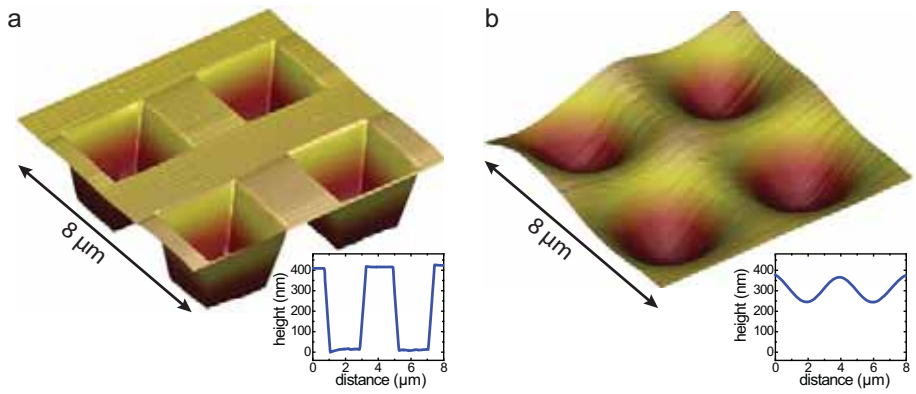

Figure 4.4: Wet etched EBL alignment markers. AFM scans of the wet etched deep alignment markers before (**a**) and after (**b**) the initial 1100°C anneal in UHV. These 2×2 arrays of etch pits (each approx. $2 \times 2\,\mu m^2$ in size) are used to align *ex-situ* metallic contacts and top gates defined by e-beam lithography. The height profiles shown in the insets illustrate the loss of integrity resulting from step-flow processes during the anneal.

metallic top gate (G) patterned on the native SiO_2 barrier.

4.3.3 Thermal degradation of the etched marker structures

Even though the temperature of the initial 1100°C anneal is far below the melting point of Si (1414°C), it causes drastic changes of the sample's surface morphology. Due to surface silicon diffusion during the anneal, the integrity of the etched alignment markers degrades, and their initially sharp edges become rounded as the etch pits fill up as a result of silicon migration. This can be seen in SEM images as well as AFM scans of the marker structure, as illustrated in Fig. 4.4. Here, the deep (∼400 nm) markers are found to decrease to ∼120 nm in depth during flashing, in agreement with previous observations [85, 101]. The shallow markers (initially 100 nm deep) reduce to ∼60 nm in depth. The rounding of the marker structure ultimately limits the alignment accuracy of the postprocessing EBL steps. To counteract this effect, we use arrays of etch pits rather than a single pit to define a single marker. The basic idea is that while the edges of each pit severely degrade during the anneal (making it difficult to determine its center), the *pitch* between repeated structures remains largely unaffected. The center of a regular array of pits can therefore be determined much more accurately, even if the edges of the individual pits are rounded. Using the 2×2 arrays of square markers shown in Fig. 4.4, we estimate our alignment accuracy for EBL-patterned structures to be approximately ±100 nm.

To reduce the detrimental effects of the flashing procedure on the integrity of the alignment markers, the use of reactive ion etching (RIE) to achieve marker structures with vertical

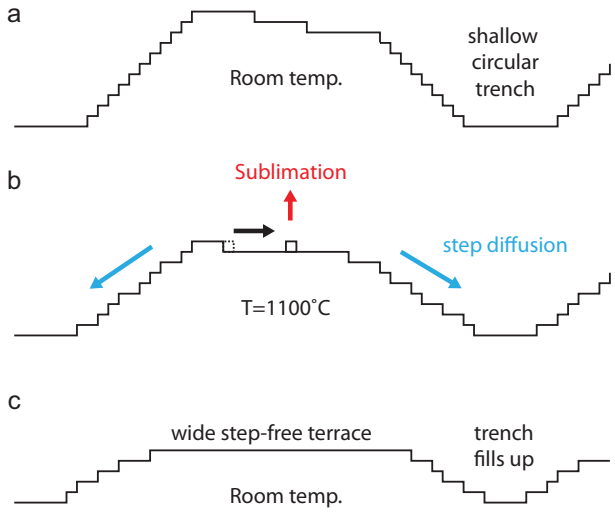

Figure 4.5: Schematic of step-flow process. **a**,Initially, the Si(100) surface enclosed by the shallow circular trench shows the usual step density. **b**, During a short ∼1100°C anneal in UHV, atoms detach from the step edges and diffuse over the terraces where they desorb into the vapor (red arrow). **c**, Eventually, a large step-free area forms in the center of the circular trench which defines the device region.

sidewalls and a high depth-to-width aspect ratio may seem desirable. Here, a chemically reactive plasma is created by electromagnetic excitation of a low-pressure gas. High-energy ions from the plasma are accelerated towards the sample, reacting with the surface substrate and thus causing an etch process. However, RIE is known to cause sub-surface damage as well as contamination of the exposed areas in the form of reaction by-products [102] and is thus avoided.

4.3.4 Formation of the central step-free terrace

No silicon wafer substrate can be cut with atomic precision along a specific crystal plane. Our high quality Si(100) wafers have a nominal miscut angle of ±0.1°, causing the terrace structure seen in STM images of the Si(100) surface (see, e.g., Fig. 4.6 a) with irregular monatomic steps occurring every few 10s of nanometers. In this section, we will discuss how this surface morphology can be controllably altered by "step engineering".

The formation of a large step-free plateau exactly at the origin of the registration marker array is extremely important to our alignment strategy. The exact nature of the kinetic processes that cause the surface morphology of Si substrates to change and lead to the formation of large step-free areas on Si(100) and Si(111) during high-temperature annealing is still a matter of debate [103]. It is believed that high temperature annealing causes the movement of atomic steps across terraces by a step-flow evaporation process. The steps eventually accumulate at barriers of extremely high step-density, such as micron-sized pe-

riodic gratings [103], ridge structures [104, 105] or, in our case, etched circular trenches, which leads to step-free regions between the barriers. Below its bulk melting point of 1414°C, the Si(100) surface undergoes a roughening transition at ∼1200°C, where atomic steps are spontaneously created on terraces [105, 106]. At temperatures below this transition, atoms at step edges may detach from the steps, diffuse on to the terraces as adatoms, and eventually desorb into the vapor [107], as illustrated in the schematic of Fig. 4.5. If the adatoms are predominantly derived from the steps[4], the rate of evaporation on a large terrace, per bounding step-edge site, will be larger than on a small terrace, which causes widely spaced steps to move faster than narrowly spaced ones. Since regions of high step density (such as the sidewalls of etched trenches) represent a barrier for step flow, a large terrace will form on an area enclosed by a trench once it has been cleared from all steps by step flow to the barriers. At the same time, due to surface diffusion, the trenches fill up with silicon and their edges become rounded, thus causing the observed degradation of integrity of the etched structures.

An example of such a step-free area is shown in the STM images of Fig. 4.6. While the Si(100) surface outside of the circular trench shows the typical stepped terrace structure (panel a), the terrace on top of the "hillock" (∼800 nm in diameter) is free of any atomic steps (panel c,d). We have tested several different shapes of the central shallow marker structures for their ability to create step-free areas, such as parallel lines, dot arrays, and circular trenches of different diameters. While all types of etched structures generally result in the formation of some step-free areas during flashing, only the enclosed circular trenches were found to be useful for our registration purposes, since they reliably provide step-free terraces at a predictable position, in this case, exactly in the center of the circular trench. In our case, we determined that the optimal diameter of these circular trenches is ∼5 μm with a trench width of 1 μm. For smaller diameters, no large terraces formed as the hillock enclosed by the circular trench did not extend to its full height after the anneal, while for larger diameters, pits were found to form in the middle of the terrace. The formation of such pits has been previously observed [105, 108] and was attributed to large step-free terraces eventually becoming unstable against the formation of vacancy clusters at some distance from the step edges when the terrace width exceeds the average adatom diffusion length before desorption.

We have also investigated how the terrace width changes with the etch depth of the shallow circular trench and have found that an initial depth (before flashing) of approximately 100 nm yields the largest step-free areas. It should be mentioned that we are limited in

[4]Some adatom-vacancy pairs will also form on terraces.

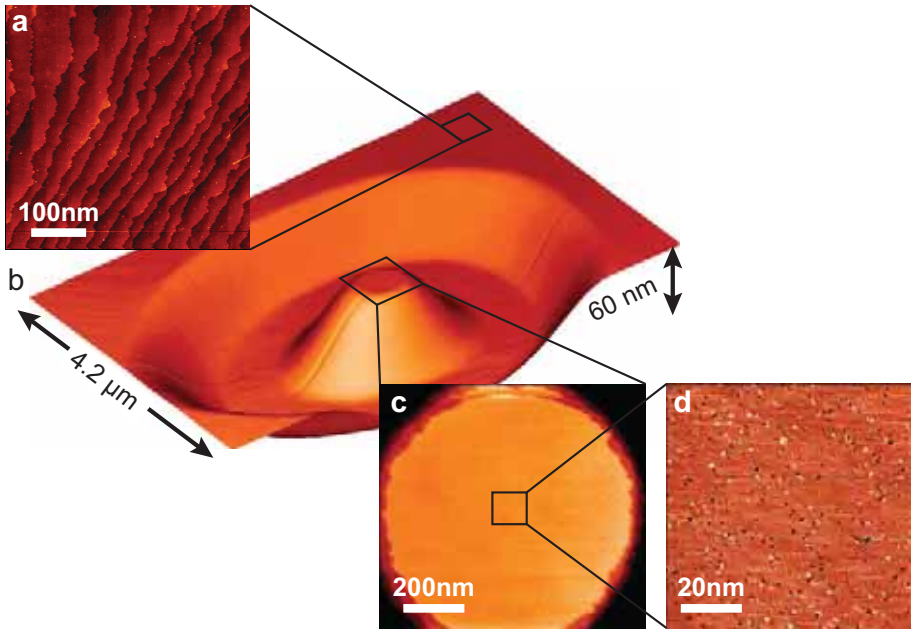

Figure 4.6: Engineering of atomically flat areas. a, STM image of the Si(100) substrate outside the etched marker structure showing the typical irregular terrace structure with steps of monatomic height occurring with a spacing on the order of 10's of nanometers. **b**, Step-engineering allows for the creation of atomically flat areas many hundreds of nm in size. The 3-dimensional STM image shows a circular wet-etched trench with a diameter of approx. 5 μm after the initial 1 min anneal at ~1100°C in UHV. **c**, A step-free circular area (~800 nm in diameter) has formed on top of the "hillock". **d**, A high-resolution image of the plateau reveals an atomically flat Si(100) surface showing some common surface defects such as dimer vacancies (dark spots).

varying the depth by the practicability of scanning these regions during STM lithography. If the trench is too deep (> 200 nm before flashing), the high surface corrugation on the slope of the hillock may cause an advanced decay of the STM tip and makes aligning the contact patches difficult as the visibility of the desorbed regions decreases for higher step density. If the trench is too shallow (< 50 nm before flashing), it becomes very difficult to locate the position of the central terrace due to the low surface corrugation (~10 nm) after flashing. While it is possible to pattern $20 \times 20\,\mu m^2$ step-free areas [105] at the bottom of micron-deep etch pits after annealing for ~1 h in UHV at similar temperatures, we have optimized a method of achieving atomically flat circular trenches that can be imaged and lithographically patterned by the STM. Furthermore, we generally avoid extended annealing times which tend to cause a significant increase in chamber pressure causing possible surface contamination. Typically, the largest terraces created by our method have measured up to 800 nm across (Fig. 4.6); however, we are able to reliably achieve step-free regions with several hundreds of nanometers in diameter. This is sufficient for

the active regions of our nano- to atomic-scale devices to be patterned on a single atomic plane.

Importance of step engineering

Since our planar P-doped quantum devices are patterned on silicon surfaces, it is important to understand how the microscopic surface morphology affects their transport properties. The influence of step density on electronic transport in δ-doped Si:P Hallbar devices has previously been investigated by our group [40]. Electrical conduction and magnetotransport measurements on these μm-scale devices showed no dependence on the miscut angle (and thus the step density) of the substrate.
However, the situation may change as the device size is decreased to the nm-scale where quantum effects become dominant and the atomistic details of the crystalline host material can no longer be ignored. This is true in particular for possible applications in silicon-based quantum computation schemes that rely on vast arrays of precisely positioned individual donors [14, 17, 109]. Indeed, Koiller *et al.* [21] have highlighted the challenges arising from strong oscillations of the exchange coupling between neighboring donors as a function of their relative spacing. These oscillations result from the valley structure of the silicon crystal and occur on the scale of the Si lattice constant. The positioning of the individual impurities with atomic-scale precision is thus a fundamental ingredient for the successful operation of donor-based qubits. Even though recent publications have focused on methods to overcome certain problems associated with non-ideal donor placement [110], it is evident that random atomic steps (causing changes in the donor spacing) on the initial patterning surface may be detrimental to the fabrication of future quantum computing devices.

4.3.5 Alignment of *ex-situ* contacts

The active region of our devices such as nanowires [67], tunneling gaps [95], and quantum dots (see chapters 5 and 6) can usually be patterned within a $400 \times 400\,\mathrm{nm}^2$ STM scan frame and thus fits on the central step-free terrace. To aid the formation of Ohmic contacts to such a STM-patterned device, large square contact regions up to approximately $3.5 \times 1.5\,\mu\mathrm{m}^2$ in size are consecutively patterned by the STM, aligned either side of the circular trench, and desorbed, as illustrated in the composite STM and SEM image of a final device in Fig. 4.7 a. The circular trench is clearly visible in the STM images acquired during lithography as well as *ex-situ* using AFM (panel b) and can thus be used to check the alignment of the EBL-patterned Ohmic contacts before metallization (panel c). The

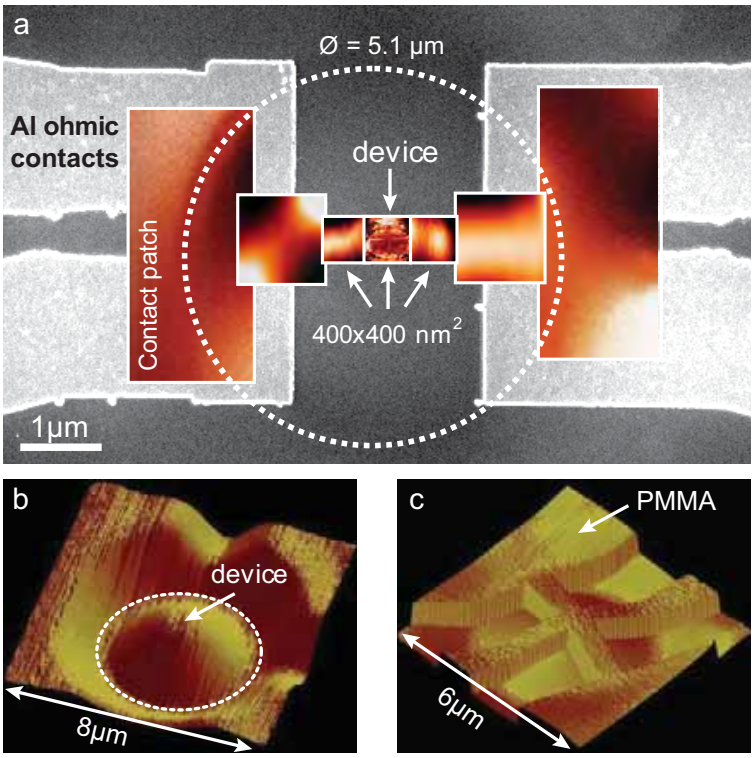

Figure 4.7: Alignment of *ex-situ* metallic contacts. **a**, Composite image of a contacted device showing all STM scan frames acquired during lithography, stitched together. The actual device is patterned on the central step-free terrace within a $400 \times 400\,\mathrm{nm}^2$ scan frame. Three consecutive patches of increasing size are then desorbed on either side. The bottom of the trench indicated by the dotted white line is clearly visible in the STM images of the large outer contact patches ($\sim 3.5 \times 1.5\,\mu\mathrm{m}^2$ in size) and serves to align the four-terminal Ohmic contacts shown in the SEM image in the background. **b**, AFM image of the circular marker after encapsulation. The onset of the trench (dashed line) is clearly visible and thus serves to check the alignment of the EBL-defined Ohmic contacts before metallization, as illustrated in **c**.

atomically flat, central terrace at the top of the hillock cannot be resolved with AFM. We therefore estimate the precision of this AFM alignment check, using the circular trench, to be approximately $\sim$100 nm. This is comparable to the accuracy of the EBL patterning step using the micron-sized 2×2 arrays of square markers described above (Fig. 4.4). From comparing SEM images of the final device after metallization to STM images acquired during H-lithography of the contact patches (Fig. 4.7 a), we estimate an overlap area between metallic leads and P-doped regions of approximately $2\,\mu\mathrm{m}^2$. Along with the ohmic contacts, standard cross-shaped markers are patterned during the initial EBL postprocessing step. These well-defined metallic markers then serve as alignment markers in a subsequent EBL step for the definition of one or multiple top gates over the STM-patterned device. The alignment accuracy of these top gated structures is thus limited by the accuracy of the penultimate EBL step.

It should be emphasized that, while STM lithography can be performed with essentially atomic precision, the *ex-situ* alignment of Ohmic contacts and top gates to the encapsulated device represents the critical step in the registration strategy developed in this chapter. We estimate the overall alignment accuracy between the buried STM-patterned P-doped device region and the surface metal contacts and top gates to be on the order of ∼100 nm. This value essentially reflects the positional uncertainty resulting from the thermal degradation of the etched marker structures and also corresponds to the measurement uncertainty when using AFM to verify the correct alignment of the EBL-patterned Ohmic contacts with respect to the circular trench.

4.3.6 An exemplary nanowire device

To demonstrate the applicability of the novel alignment strategy described above, we have patterned an exemplary nanowire device on the central terrace of a registration marker array. Fig. 4.8 a shows a STM image of the $50 \times 240\,\mathrm{nm}^2$ nanowire patterned on the atomically flat terrace formed within the circular trench. In a subsequent step, larger contact arms were desorbed on either side of the device (analogous to the ones illustrated in Fig. 4.7 a) before dosing the entire surface with phosphine for 6 min at a chamber pressure of $\sim 5 \times 10^{-9}$ mbar (corresponding to an exposure of ∼1.4 Langmuir), followed by a 1 min incorporation anneal at 350°C. Finally, the sample was overgrown with ∼25 nm of epitaxial silicon at 250°C. The low growth temperature maintains the structural integrity of the Si:P device by minimizing the possibility of dopant diffusion out of the STM-patterned area [80]. The Si encapsulation also ensures full electrical activation of the P donors yielding a carrier density of $\sim 2 \times 10^{14}\,\mathrm{cm}^{-2}$ [44]. The entire *in-situ* part of device fabrication including STM-patterning and overgrowth took roughly 10 hours for this device. After removal from UHV, *ex-situ* ohmic contacts are EBL-patterned over the contact patches, using the wet-etched registration array as alignment markers. Here, two leads are defined per STM-patterned contact patch for source (S) and drain (D), respectively. After metallization of the Al Ohmic leads, electrical contact to the buried P-doped region is established by a 30 min anneal at 350°C under N_2 atmosphere. In a last step, a 250 nm wide aluminium top gate (G) is EBL-patterned (perpendicular to the wire) over the central device area as shown in the SEM image of Fig. 4.8 b.

The device was subsequently characterized at 4.2 K to confirm good contact to the buried structure. Our low-doped ($\sim 10^{15}\,\mathrm{cm}^{-3}$) silicon substrates typically conduct down to temperatures around ∼40 K. At even lower temperatures, the substrate becomes insulating

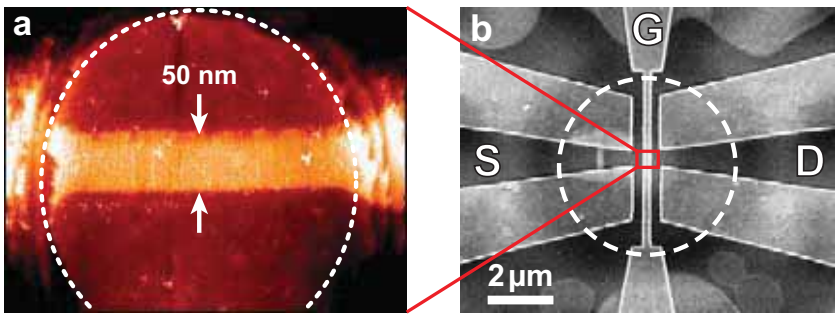

Figure 4.8: A 50 nm nanowire patterned on a step-free terrace. **a**, STM image of a $\sim 50 \times 240\,\mathrm{nm}^2$ nanowire device patterned on the atomically flat plateau (indicated by the dotted line) on the central circular marker. The image was taken after H-lithography (with the desorbed regions appearing brighter) but before the phosphine dosing step. **b**, SEM image of the completed device with EBL-patterned four-terminal Ohmic contacts for source (S) and drain (D) and a metallic top gate (perpendicular to the buried nanowire underneath). The dashed white line indicates the position of the circular trench.

due to the freeze-out of carriers and any measured current is therefore entirely confined to the STM-patterned P-doped structures of the device.

Fig. 4.9 a is a simplified schematic of the device with the large STM-patterned contact patches for S and D connected via the nanowire in between. The external Ohmic (terminals "1" to "4") are patterned in a four-terminal configuration. The first step is to check for good ohmic contact to the buried STM-patterned structure. This is achieved by simply measuring the resistance of the contact patches alone via their two metal terminals. The resulting IV-curves for source and drain are shown in Fig. 4.9 b and reveal two-terminal resistances of approx. 1.8 kΩ and 1.3 kΩ, respectively.

Fig. 4.9 c shows the current I_{SD} flowing through the nanowire as a function of the applied source-drain voltage V_{SD}. The linear IV-curves confirm Ohmic behavior of the device with a two-terminal resistance of ∼6.3 kΩ. However, this value is not equal to the resistance of the 50 nm nanowire since it also includes the contact resistances in series. To eliminate the contribution of the latter, we measure the wire in a four-terminal configuration by sending a dc current through one set of terminals (e.g. 1 and 3 in Fig. 4.9 a) while monitoring the resulting voltage drop via the other set of terminals (2 and 4) and obtain a nanowire resistance of ∼4.9 kΩ. By comparing this value to the 2T resistance of ∼6.3 kΩ we can roughly estimate the contact resistances to be on the order of several 100 Ω for our device. Previous STM studies by our group [80] estimate the effective (vertical) thickness of the initially planar Si:P devices to be ≤ 6 Å due to P segregation (along growth direction) during Si overgrowth at 250°C. Using this value and the lateral dimensions of the wire, we obtain a resistivity of $\sim 6 \times 10^{-7}\,\Omega$cm, comparable with other STM-patterned wire

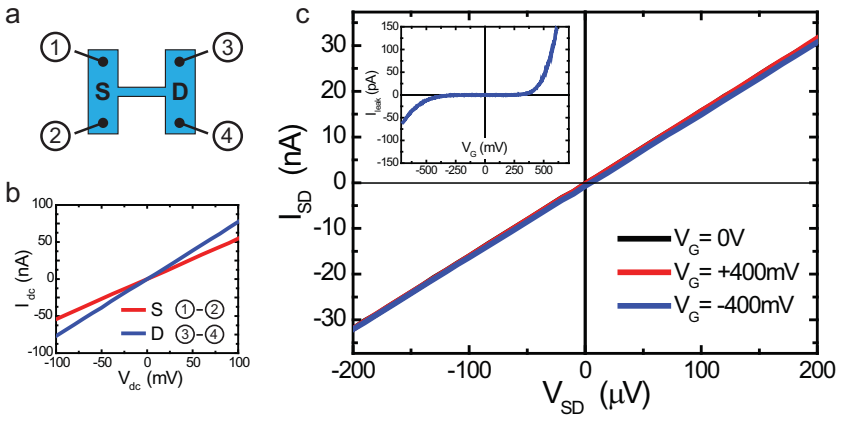

Figure 4.9: Transport characteristics of the nanowire at 4.2 K. a, Schematic of the four-terminal configuration with two *ex-situ* contacts (see Fig. 4.8 b) per STM-patterned contact patch for source (S) and drain (D), respectively. **b**, IV-curves through the contact patches yield two-terminal resistances of $R_{1\text{-}2} \approx 1.8\,\mathrm{k\Omega}$ and $R_{3\text{-}4} \approx 1.3\,\mathrm{k\Omega}$ for S and D, respectively. **c**, IV-characteristics of the nanowire reveal Ohmic behavior of the device. No significant change in wire resistance is observed as a function of the applied top gate voltage V_G. The inset shows the gate leakage current as a function of V_G. From this plot, we determine an effective gate range of roughly $-400\,\mathrm{mV}$ to $400\,\mathrm{mV}$.

devices of similar dimensions [67].

IV-curves were measured for different voltages applied to the top gate, $V_G = 0, \pm 400\,\mathrm{mV}$, as shown in Fig. 4.9 c. However, no significant change in device resistance was observed within the effective gate range. The latter is determined from the plot shown in the inset, which depicts the measured gate leakage current I_{leak} (flowing from the top gate to the S and D electrodes) as a function of the applied gate voltage. The gate range denotes the maximum voltage that can be applied to the gate before I_{leak} exceeds a certain threshold, in this case 10 pA. We obtain a gate range of approx. $-400\,\mathrm{mV}$ to $400\,\mathrm{mV}$ for our aluminium top gate patterned on the native $\sim$1 nm SiO_2 layer. This value is quite small[5], possibly due to an oxide defect resulting from the post-processing procedures. As a comparison, more recent transport devices by our group [111] incorporate a thick ($\sim$70 nm), low temperature UHV oxide on top of the STM-patterned and encapsulated structures, allowing for gate ranges on the order of $\pm 7\,\mathrm{V}$. The fact that gating action is not observed for our device can be attributed to the extremely high carrier density ($\sim 10^{14}\,\mathrm{cm}^{-2}$) within our planar Si:P structures, which is indeed orders of magnitude higher than the doping concentrations in other gated silicon nanowires [112].

The device presented in this section is a successful proof-of-concept for the improved registration scheme developed during this thesis, allowing for reliable STM-patterning of

[5] We typically obtain gate ranges of several volts for top gates patterned on native oxide.

devices on atomically flat Si(100) surfaces. Furthermore, the observed good ohmic contact to the buried structure highlights the high alignment accuracy achieved by our fabrication technique.

4.4 Further advances of device fabrication

Optimization of the fabrication scheme for our STM-patterned Si:P devices is a continuing and collaborative process within our group. The novel alignment method presented in the previous section has enabled the successful fabrication of several quantum transport devices, such as nanowires [113], Aharonov-Bohm nanorings [114], and quantum dots [115]. However, since then further advancements have again lead to important changes of the fabrication method. The most important improvement will be briefly summarized in the following section as it is relevant to the fabrication of devices presented in this thesis.

4.4.1 Aluminium vias to contact overgrown devices

An important advancement of the fabrication scheme is the introduction of an alternative method to form reliable ohmic contacts between the buried STM-patterned P-doped regions and *ex-situ* metallic leads. This new method relies on dry etched vertical contact holes and was developed as part of this thesis in collaboration with Dr. A. Fuhrer. It has lead to a significant increase in device yield.

Up to this point, contact to the encapsulated Si:P structures was established by lithographically defining aluminium metallic leads over the STM-patterned contact patches followed by a 350°C anneal for 15 min under N_2 atmosphere [44]. While this temperature is too low to cause uniform downwards diffusion of the Al through the Si substrate, it is sufficient for so-called "spiking" to occur [116]. Here, Si diffuses into the Al layer at a direct Si/Al contact leaving rectangular pits behind in the silicon substrate. At elevated temperatures the Al then refills these voids forming "spikes" [117]. Spiking is an uncontrolled and non-uniform process that is generally unwanted in semiconductor processing [117]. For our devices, it is evident that this contacting method (illustrated in Fig. 4.10 a) produces unreliable results since it depends on the random formation of spikes of sufficient depth within the small ($\sim 1\,\mu m^2$) overlap area between the metal lead and the STM-patterned contact patch beneath. The resulting Si pits caused by Al spiking can be clearly seen in SEM images of a contacted device after wet-chemical removal of the Al leads as shown in Fig. 4.10 b. Indeed, only a few spiking events (illustrated by the arrows) occur within the overlap area. This results in a low yield of successfully contacted devices

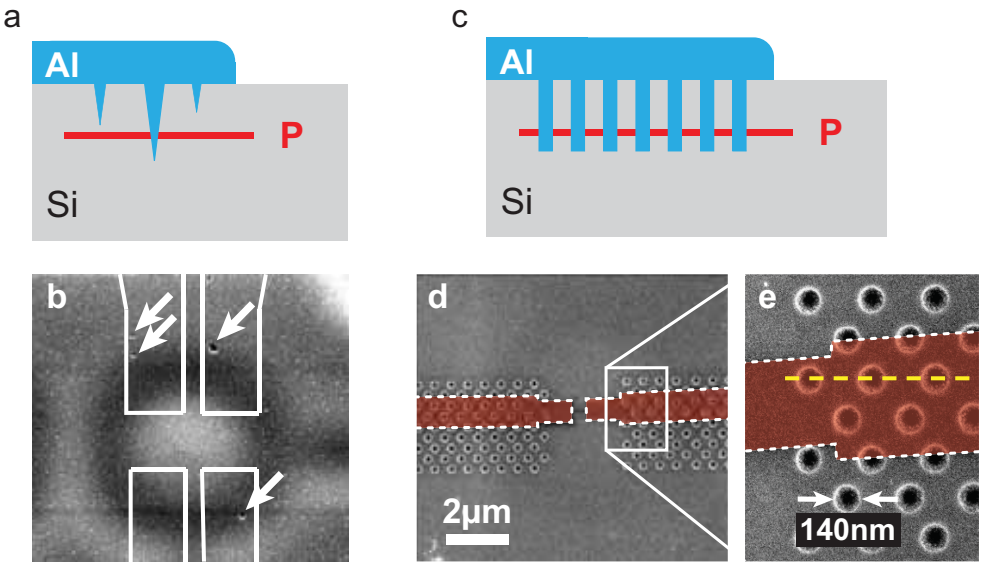

Figure 4.10: ***Ex-situ*** **contacting of buried devices. a**, Schematic of the previously used contacting method, relying on irreproducible spiking of the deposited Al leads down to the STM-patterned P-doped layer (red) during an anneal at ∼350°C. **b**, Pits resulting from Al spiking through the substrate are visible in SEM images (indicated by white arrows) after wet-chemical removal of the Al contacts (outlined in white). **c**, Schematic of the new fabrication scheme using RIE etched contact vias penetrating through the P-doped layer. **d**, An array of contact vias is EBL-patterned over each STM-patterned contact patch (indicated by the red shaded regions), as depicted in the SEM image of an exemplary 2-terminal device. The holes are ∼140 nm in diameter with a pitch of roughly 500 nm as shown in the close-up (**e**). The vias are typically etched to a depth of ∼70 nm, thus penetrating the P-doped layer below. A cross section of the contact vias along the yellow dashed line is depicted in Fig. 4.11.

as well as unpredictable contact resistances ranging from a few kΩ to hundreds of MΩ.

To overcome these problems, a new contacting method was developed which is illustrated in the schematic of Fig. 4.10 c. Here, an array of vertical holes, or *vias*, is defined over the P-doped contact regions. Subsequently, the metallic leads are deposited over the array, filling the contact holes. Since the latter penetrate through the dopant layer, a direct contact between the metal and the highly-doped Si:P regions is formed. Such metal vias are commonly used in the semiconductor industry to provide vertical interconnection in stacked integrated circuits [118]. Using vias in our devices has the additional advantage of rendering the previously used contact anneal at 350°C unnecessary, thus minimizing the thermal budget. To achieve a vertical etch profile and a high aspect ratio for the contact holes, we use a dry etch process rather than wet etching. The hole array is defined by EBL and subsequently etched in a hollow cathode reactive ion etching (RIE) system[6] to a depth of typically 70 nm to ensure that the vias penetrate through the P-doped layer

[6] A summary of the process parameters is given in appendix A.4.

∼25 nm beneath the Si surface.

A SEM image of an exemplary device is depicted in Fig. 4.10 d, where an array of contact vias has been defined over each of the two STM-patterned contact patches below (indicated by the red shaded regions). These P-doped patches are characterized by a vertical δ-doping profile with only a very small spread of the dopants along growth direction (≤ 6 Å) due to the overgrowth process at 250°C [80]. The actual contact area where the metal vias penetrate the P-doped layer, will therefore be quite small. To maximize this Al/Si:P contact area we increase the number of vias per contact patch, which is achieved by patterning the holes with a small diameter (∼140 nm) in a dense array with an average spacing of ∼500 nm. The latter is a tradeoff between maximizing the contact area and ensuring that enough of the dopant layer remains to conduct within the plane.

Aluminium is used as contact material due to its good processing properties: it is easy to evaporate, shows strong cohesion on Si, and it easy to bond to. One downside of using elemental Al is that it becomes superconducting below a critical temperature $T_c = 1.2$ K, which may affect electronic measurements at mK-temperatures. However, this is easily overcome by applying a weak background magnetic field higher than the critical magnetic field of Al (∼10 mT) [83].

To further investigate the etch profile of the contact holes, transmission electron microscope (TEM) images were taken[7] on a typical device. Here, a fine lamella is cut out of a STM-patterned sample which has undergone all the usual fabrication steps including silicon overgrowth (in this case approx. 30 nm). The position of the cut was chosen to give a cross section of the metal vias penetrating a contact patch as illustrated by the dotted yellow line in Fig. 4.10 e. The resulting TEM image in Fig. 4.11 a shows a cross section of 3 vias. The close-up of a contact hole in Fig. 4.11 b clearly shows that the Al penetrates into the etched hole, thus intersecting the P-doped layer (indicated by the dotted line) ∼30 nm below the Si surface. The encapsulation depth is determined from an atomic force microscope (AFM) scan of the overgrowth profile at the edge of the sample, illustrated in the inset. Grain boundaries are visible within the ∼70 nm thick Al layer. A high-resolution TEM image of the Si encapsulation layer (Fig. 4.11 c) reveals an undisturbed lattice structure which is further confirmation of the epitaxial quality of the low-temperature (250°C) overgrowth. This is in agreement with previous detailed STM studies of overgrowth surfaces [81].

By incorporating aluminium vias into our fabrication scheme, we consistently obtain good ohmic contact to our buried Si:P structures with low contact resistances on the order

[7] The TEM images were taken at EAG Labs in Raleigh, NC, USA using a Hitachi HD2300.

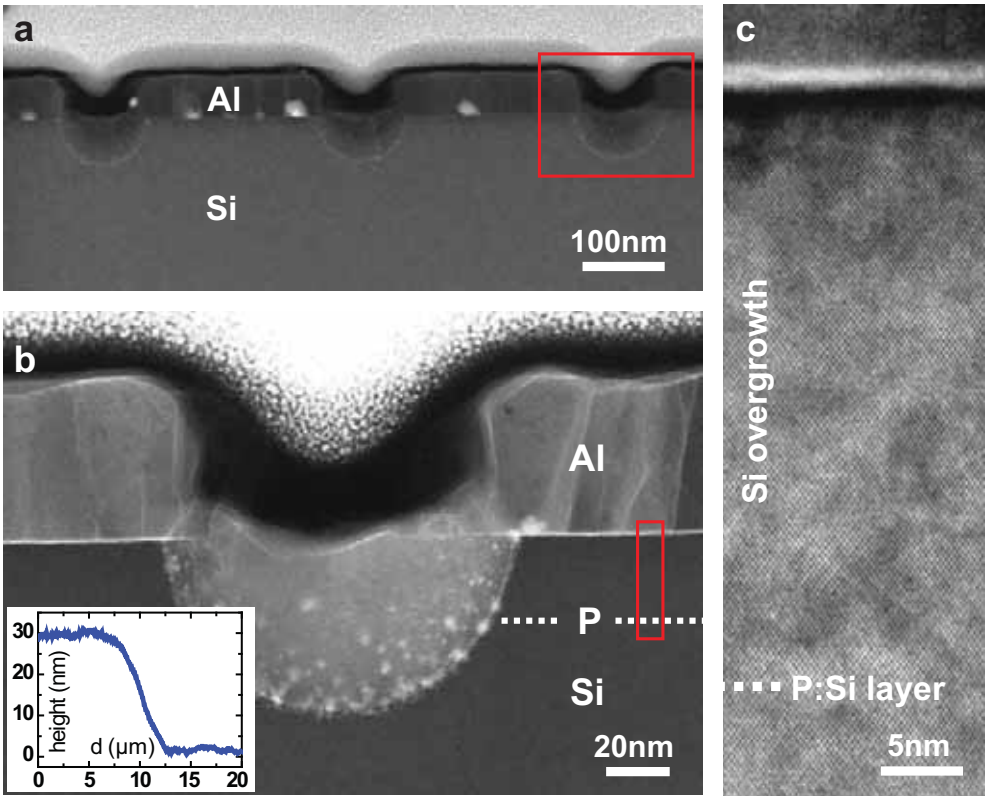

Figure 4.11: TEM images of contact holes. **a**, Transmission electron micrograph depicting the cross section of the contact region of a typical device. *Ex-situ* contacts are formed by a ∼70 nm thick aluminium layer EBL-patterned over the array of RIE vias. **b**, A close-up of such a via reveals that the Al penetrates through the STM-patterned P dopant plane. The encapsulation depth of the latter (∼30 nm) can be determined from AFM scans of the Si overgrowth profile at the edge of the sample, as illustrated in the inset. **c**, An atomic-resolution TEM image reveals an undisturbed lattice structure of the Si encapsulation layer.

of $1 - 30\,\mathrm{k\Omega}$. Generally, the Al/Si:P interface must be treated as a Schottky contact. Such a metal-semiconductor junction results in an Ohmic contact (i.e. a contact with voltage independent resistance) only, if the Schottky barrier height Φ_B is zero or negative. This is not the case for the Al/Si:P interface in our devices, for which a typical value of $\Phi_B \approx 0.7\,\mathrm{eV}$ is reported [119]. However, the extremely high P doping density in our devices results in a very small depletion region on the semiconductor side, so that electrons can directly tunnel through the barrier. In equilibrium (without any voltage applied across the Schottky contact) this depletion length x_d can be estimated as [25]

$$x_d = \sqrt{\frac{2\epsilon\Phi_i}{eN_d}} \tag{4.1}$$

where $\epsilon = \epsilon_0\epsilon_{\mathrm{Si}}$ is the electric permittivity, N_d is the bulk doping density, and Φ_i is the built-in potential. The latter can be calculated from $\Phi_i = \Phi_B - k_{\mathrm{B}}T\ln(N_c/N_d)$,

where $N_c = 2(2\pi m^*_{e,\mathrm{DOS}} k_\mathrm{B} T)^{3/2} h^{-3}$ is the effective density of states in the conduction band and $m^*_{e,\mathrm{DOS}} = 1.08 m_0$ is the Si effective mass[8] for density-of-states calculations [25]. We can estimate an effective *bulk* doping density for our samples from the sheet density ($\sim 10^{14}\,\mathrm{cm}^{-2}$) within the doping plane and the aforementioned maximum spread of the dopants (6 Å) in growth direction and obtain $N_d \sim 10^{21}\,\mathrm{cm}^{-3}$. At liquid helium temperature, eq. (4.1) then yields $x_d \approx 0.5\,\mathrm{nm}$ – which corresponds to only 1 Si lattice spacing. While this is a very rough estimate, it demonstrates that due to the high P-doping density the Al/Si:P interface in our devices can, for all practical purposes, be viewed as metal/metal-like junction with Ohmic characteristics.

4.5 Chapter summary

In this chapter, we have shown the use of UHV compatible, wet-etched EBL-patterned registration markers for *ex-situ* alignment of multiple Ohmic contacts and surface gates to STM-lithographically defined P-doped devices. By patterning a circular marker structure in the center of the registration marker array, we are able to generate step-free plateaus with a diameter of several hundred nm. This allows for the active region of a device to be patterned on a single atomic Si(100) plane at a precisely known position. Furthermore, we have highlighted the importance of step-engineering for possible future quantum computation devices that rely on atomically precise control over the position of individual donors.

The current overall alignment accuracy of EBL-defined structures with respect to the STM-patterned device is ∼100 nm, with the main limiting factor being the degradation of the integrity of the etched marker structures during the initial 1100°C surface preparation anneal of the sample in UHV. Using the new alignment scheme, we have demonstrated electrical transport measurements of a 50 nm wide Si:P nanowire patterned on a central terrace, which shows Ohmic conduction and a low resistivity of $\sim 6 \times 10^{-7}\,\Omega$ cm at 4.2 K. We have also discussed how the introduction of RIE etched contact vias enables the formation of reliable low-ohmic contacts between the external metallic leads and the encapsulated P-doped regions. This new contacting method has resulted in a drastic increase in the yield of successfully contacted STM-patterned devices.

[8] Assuming 6 degenerate bands, this is given by $6^{2/3}\sqrt[3]{(m^*_t)^2 m^*_l}$.

Chapter 5

A donor-based many-electron quantum dot

In this chapter, we demonstrate a fully functional multiterminal Si:P quantum dot device in the many-electron regime. The entire structure is STM-patterned on a single atomic plane of a Si(100) surface, including three donor-based in-plane gates. We show that such coplanar regions of highly doped silicon can be used to reliably gate nanostructures resulting in highly stable Coulomb blockade oscillations in our donor-based quantum dot. In particular, we compare the use of these all epitaxial in-plane gates with conventional metallic surface gates and find superior stability of the former for our device. These results highlight that in the absence of the randomizing influences of interface and surface defects the electronic stability of donor-based dots in silicon can be comparable to or better than that of quantum dots defined in other material systems.
Based on this successful demonstration of a many-donor quantum dot, we will then discuss the challenges in down-scaling of device dimensions within our planar donor-based architecture. We will introduce capacitance modeling as a viable tool to predict the electrostatic properties of new device designs which helps to improve the tunability of quantum dot structures of reduced size.

5.1 Quantum dots in semiconductor devices

To put our work in a larger context we will briefly review quantum dot structures in the literature and contrast our donor-based approach to these existing device architectures. Here, we will focus on quantum dots in the many-electron regime. A further discussion of

more recent devices in the few and single electron limit will be given in the following two chapters.

The first clear demonstration of Coulomb oscillations was performed by Folton and Dolan [47] in 1987 in a μm-sized aluminium tunneling structure. Since then, Coulomb blockade has been observed in a vast and diverse range of materials such as metallic nanoparticles [120], organic molecules [121], carbon nanotubes [122] as well as a variety of semiconducting nanostructures [123, 124, 125, 46]. The latter have received special interest since the advent of improved nanofabrication methods in the 1980's, such as electron beam lithography (EBL) and molecular beam epitaxy (MBE), which allow for high control over the electronic properties in semiconductor materials. This is true in particular for modulation doped GaAs/AlGaAs heterostructures which are arguably the best-studied quantum dot architecture due to their relative ease of fabrication and high carrier mobilities [46]. Here, quantum wells are formed by an engineered band-discontinuity along growth direction. The strong confinement (along z-direction) in the quantum well generates a two-dimensional electron gas (2DEG) where carriers are free to move in the x-,y-direction while quantization effects occur in the z-direction. Quantum dots can be created in these structures by introducing additional lateral confinement either by vertically etching the substrate [126, 127] or by using a suitable arrangement of surface gates which cause a local depletion in the 2DEG underneath [128, 123, 124]. A more extensive discussion of the early experiments in this field can be found in a review article by Kouwenhoven [46]. Similarly, quantum wells can also be formed in modulation-doped silicon/silicon-germanium heterostructures which generate a 2DEG at the interface (see e.g. refs. [129, 34] for a review of this field). Analogous to GaAs, quantum dots can be created in these structures by either directly etching the substrate [130, 131] or by using top gates [125]. While mobilities in Si systems are generally lower [132, 125] than in III-V materials, they offer clear advantages in the context of quantum information processing [14, 17] due to long spin lifetimes afforded by the abundant nuclear spin zero isotope ^{28}Si.

Silicon quantum dots have also been realized in field-effect transistor structures on Si/SiO_2 [133, 134, 135] or silicon-on-insulator (SOI) substrates [136]. By using polycrystalline silicon or metallic gates on an oxide barrier, an inversion layer is created between highly doped contact regions. Barriers between the dot and the leads can then be created by additional gates in multi-layer gate stacks [135].

Quantum dots can also be realized in semiconducting nanowires made from III-V materials (such as InAs [137]) or Si [138]. These nanowires are commonly grown by means of the vapor-liquid solid (VLS) mechanism using gold metal particles as catalysts and are

typically ∼10 - 100 nm in diameter [139]. The resulting whiskers are then transferred onto an insulating substrate (usually a silicon wafer with a SiO_2 layer) and contacts are lithographically patterned. After deposition of a suitable barrier material or dielectric, surface gates are defined in an additional lithography step which allow for confinement along the wire.

Quantum dots in all these material systems have since progressed towards the few- and single- electron limit. More recent developments will be discussed in more detail in chapters 6 and 7. A common feature of the architectures described above is the fact that confinement (at least along one dimension) is defined *extrinsically* by applying a voltage to some form of gate. This is in sharp contrast to donor-based devices where confinement is created *intrinsically* (even in the absence of any applied gate voltages) by the attractive potential of the ionized dopants. A donor-based architecture thus allows for significantly smaller overall device dimensions and – more importantly – a much greater control over the confinement landscape on a length scale comparable to the lattice spacing. This has important implications for the electronic properties as well as the scalability of these structures as will be discussed in this chapter. Donor-based quantum dots in the many-electron regime have previously been defined by ion implantation [140]. Here, several hundred P donors were implanted into a host silicon crystal to form a roughly spherical island ∼50 nm in diameter which (in conjunction with a metallic top gate) defined a tunable quantum dot. However, an inherent drawback of ion implantation is the comparatively low spatial control over the dopant position on the order of ∼10 nm even at low (14 keV) ion beam energies [140]. This is detrimental for possible donor-based quantum computation applications [14, 17] that rely on the precise positioning of dopants with sub-nm accuracy.

In the following section, we will present an alternative method to realize donor-based quantum dot structures in silicon using STM hydrogen lithography. We will demonstrate how this approach allows for unprecedented spatial control of the dopant distribution on the single nanometer scale. Furthermore, in contrast to other architectures our device is fabricated in a single-crystal silicon environment and does not contain any heterogeneous interfaces. This allows us to avoid common interface-related defects such as charge traps [141, 142] which cause current noise or lattice dislocations which may create leakage pathways [125].

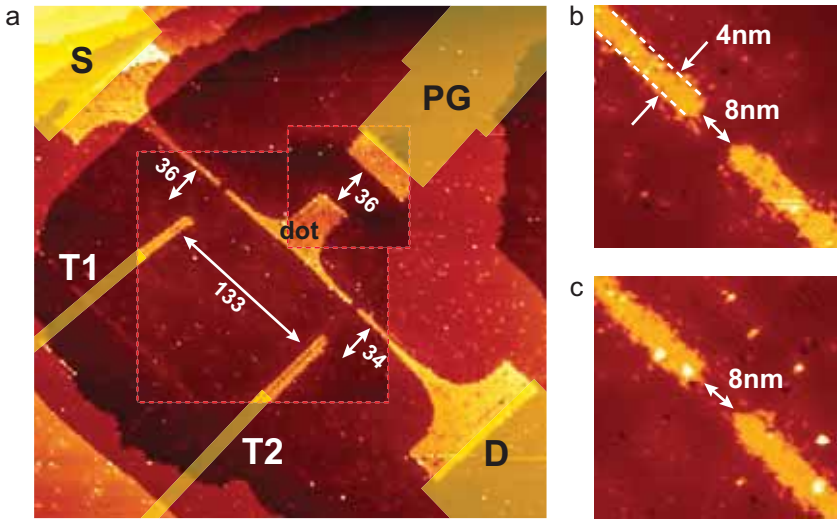

Figure 5.1: An in-plane gated donor-based quantum dot. a, Composite STM image of the device (bright regions) directly after performing STM lithography on a single atomic terrace on the H-terminated Si(001) surface. Three in-plane gates (PG, $T1$, $T2$) are used to tune the electron number on the quantum dot. With a saturation doped area of approx. 2100 nm^2, the dot is estimated to contain ∼4000 electrons. The dot is connected to source (S) and drain (D) via ∼4 nm wide leads (corresponding to ∼5 dimer rows), interrupted by 8 nm tunnel gaps as illustrated in the close-ups of the left (**b**) and right (**c**) gap.

5.2 A planar STM-patterned Si:P quantum dot

In this section we will demonstrate a fully functional multiterminal quantum dot that was fabricated in conjunction with Dr. A. Fuhrer. It is the first STM-patterned dopant-based device that showed Coulomb blockade. Up to this point, STM hydrogen lithography had realized individual components of a complete device architecture (such as donor nanowires [143] as electrical leads, nm-scale tunnel junctions [95], and isolated P-doped nano-islands [78]) with a major obstacle being the ability to electrically gate devices. While previous attempts to fabricate a Si:P quantum dot had relied on metallic surface gates [78], the current device follows a different strategy relying entirely on integrated donor-based in-plane gates to tune the electrochemical potential of the dot.

The device was patterned on a n-type $1 - 10\,\Omega$cm Si(100)-2 × 1 substrate which has been pre-patterned with an etched registration marker structure as discussed in detail in the previous chapter. Fig. 5.1 shows a composite STM image taken immediately after patterning the quantum dot structure on the terminated silicon surface by selective H-desorption with the STM tip in lithography mode ($V_{tip} \approx -4$ to -7.5 V and $I_t \approx 1-3$ nA). All of the active device area lies on a single monatomic terrace and appear bright in the STM-images due to a change in the electronic structure at a dangling bond site compared

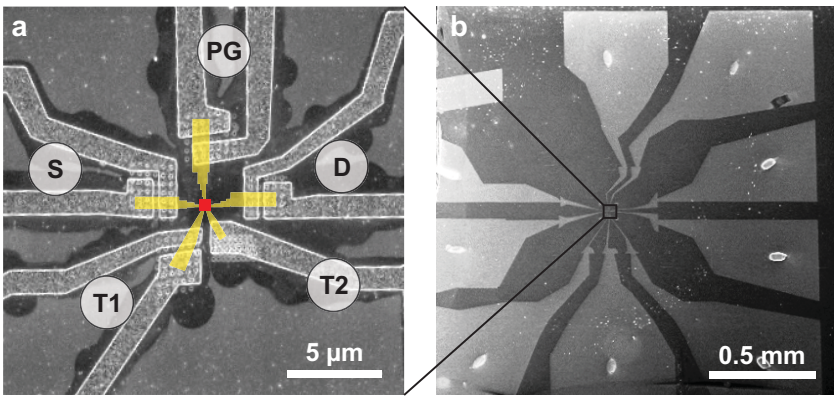

Figure 5.2: External metallic contacts for the Si:P quantum dot. **a**, SEM image of the completed device after Al metallization of the external ohmic leads. Two metallic leads are defined for each STM-patterned contact patch (yellow regions), except for $T2$. The arrays of etched contact vias are clearly visible over the contact patches. The central red square indicates the relative size and position of the STM image in Fig. 5.1 a. **b**, The metallic leads are extended out to larger bond pads.

to the surrounding H-terminated areas. The dot in the center is connected by two ∼8 nm wide tunnel gaps to the source and drain terminals which have a minimum width of ∼4 nm (∼5 silicon dimer rows as shown in the close-up images of Fig. 5.1 b and c). Three additional areas $T1$, $T2$, and PG were patterned to serve as in-plane gates to tune the electron number on the dot by applying corresponding gate voltages, V_{T1}, V_{T2}, V_{PG}. All five terminals of the dot are extended out to ∼3 μm long STM-patterned contact patches leading away from the device, as indicated by the yellow shaded regions in Fig. 5.1 a and Fig. 5.2 a, respectively. After STM-lithography, the entire surface is saturation dosed with phosphine for 6 min at room temperature at a chamber pressure of $\sim 5 \times 10^{-9}$ mbar (corresponding to an exposure of ∼1.4 Langmuir). A subsequent 1 min anneal at 350°C incorporates the P donors into the topmost layer of the Si surface in the areas where the hydrogen was desorbed by the STM tip. In a last step, the device is encapsulated by growing a ∼25 nm thick epitaxial silicon layer at 250°C over the entire structure. The entire *in-situ* fabrication for this particular device took approx. 30 hours.

The use of donor-based in-plane gate electrodes allows us to fully fabricate the electronically active device area *in-situ* in the UHV environment, thus completely avoiding defect prone interfaces [142] or metallic gate electrodes near the device. Importantly, the low thermal budget ($T < 250$°C) for the overgrowth process leads to minimal diffusion of the P dopants in the silicon and preservation of the STM patterned geometry on the sub-nm scale [44, 66]. After encapsulation the device is removed from the UHV environment and electron-beam lithography (EBL) is used to align two separate aluminum ohmic contacts

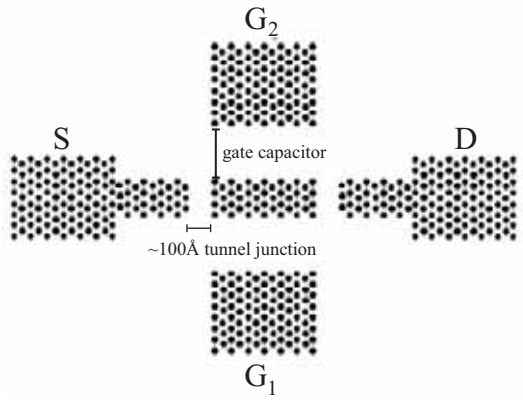

Figure 5.3: Proposed SET device. The quantum dot device of Fig. 5.1 is the first experimental realization of a planar single-electron transistor as proposed in this schematic by Tucker *et al.* [144].

to each of the donor patches as shown in the SEM image of Fig. 5.2 a. An array of 50 nm deep holes with a diameter of about 100 nm are defined over the donor patches using reactive ion etching to help form low resistance ohmic contacts (see section 4.4.1). In a last step, the sample is glued and wire bonded to a chip carrier using the large metallic bondpads shown in Fig. 5.2 b.

The concept of using STM-lithography to pattern donors in silicon was proposed approximately 10 years ago for the realization of atomically precise architectures enabling applications in single electronics and quantum computing circuits [144]. It should be noted that the few-donor quantum dot presented here is the first experimental realization of such a planar SET structure as proposed by Tucker *et al.* [144] (see Fig. 5.3). However, the donors defining the structure in this original concept paper were believed to be self-ordered over larger distances (∼100s of nm), which we know not to be the case for incorporated P donors [42].

5.2.1 Electrical characterization of the many-electron quantum dot

Following a brief initial characterization of the device at 4.2 K to confirm ohmic contact to the buried structure, the quantum dot was measured in a dilution refrigerator with a base temperature of ∼80 mK. To suppress the superconductivity of the aluminum contacts at mK-temperatures, we apply a background magnetic field $B = 100\,\mathrm{mT}$.

From the current versus voltage (IV) measurements of Fig. 5.4 a we can estimate the contact resistance to the buried donor layer to be ∼10 kΩ per contact. Here, IV curves are recorded using the two metallic terminals patterned for each individual STM-patterned contact patch (see Fig. 5.2 a). By contrast, contact combinations across gaps in the

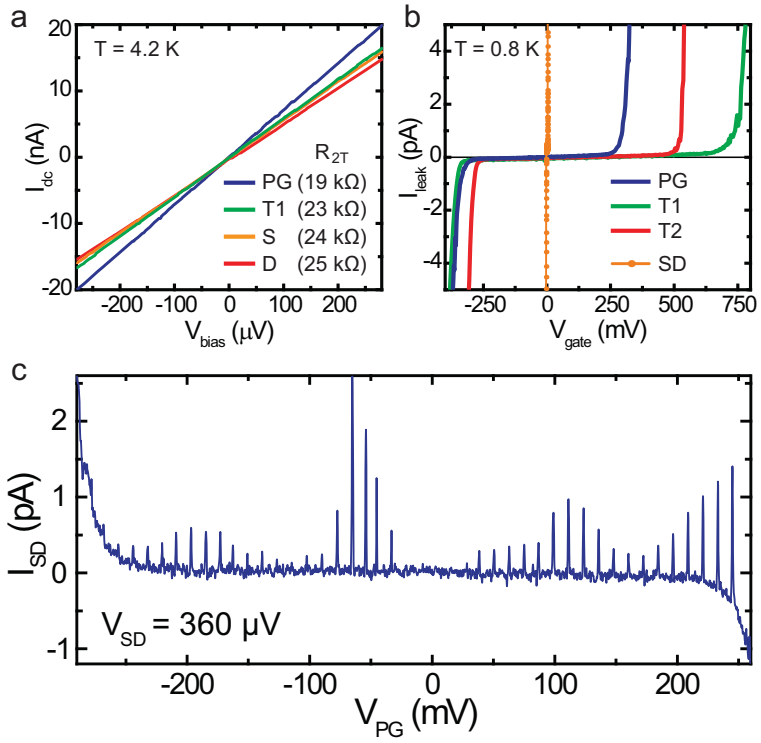

Figure 5.4: Electrical characterization of the Si:P quantum dot. **a**, The resistance between the two metallic terminals for each STM-patterned electrode confirms good ohmic contact to the buried dopant structure with two-terminal resistances of roughly 20 kΩ. **b**, Leakage current from each of the gate electrodes to all other contacts as a function of the applied gate voltage. In comparison, the orange IV curve is a measurement across the device from source to drain. **c**, The source-drain current (at $V_{SD} = 360\,\mu$V) shows regular oscillations as a function of the applied gate voltage V_{PG}. The modulation of the peak height is most likely due to a strongly modulated density of states in the narrow S and D leads.

patterned donor structure show insulating behavior for small applied bias voltages. Figure 5.4 b shows the corresponding IV traces for each of the three in-plane gates where we measure the leakage current I_{leak} flowing from the gate to any of the other terminals. From these plots we determine the effective gate range for each gate. The latter is defined as the maximum voltage that can be applied to a gate before I_{leak} exceeds a certain threshold, typically 100 pA. None of the gates show leakage for $|V_{gate}| < 250$ mV. It is interesting to note that the leakage curve for the plunger gate (PG) seems to be more symmetric than those of gates $T1$ and $T2$ where large positive voltages can be applied before leakage occurs. This may reflect the fact that the two narrow gate leads $T1$ and $T2$ get partially depleted for very positive voltages and thus exhibit larger positive breakdown voltages. For negative V_{T1} or V_{T2}, the breakdown is governed essentially by the gap size. The smaller gate range for $T2$ thus reflects its slightly smaller gate separation (34 nm) compared to the other two gates $T1$ and PG (both 36 nm), as illustrated in Fig. 5.1 a.

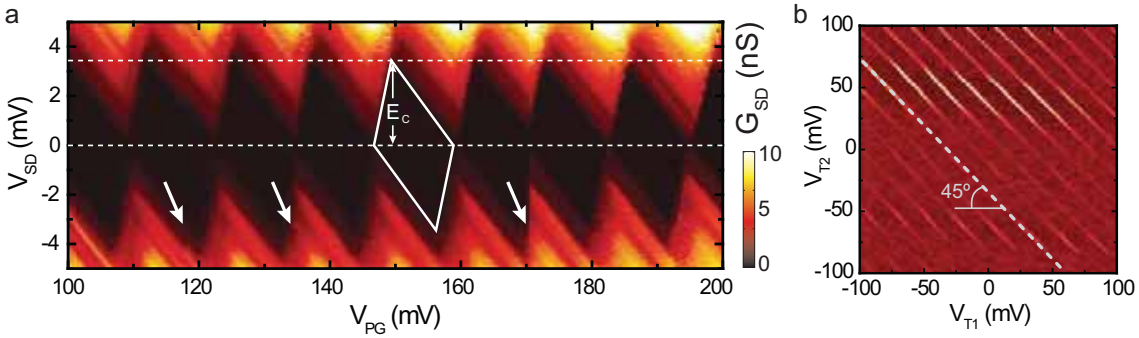

Figure 5.5: Stability diagram of a many-electron Si:P quantum dot. a, The device conductance G_{SD} plotted as a function of the bias voltage V_{SD} and the plunger gate voltage V_{PG} reveals stable Coulomb blockade with a constant charging energy $E_c \approx 3.3\,\text{meV}$. Only a few minor switching events are observed which are indicated by the arrows. **b**, CB oscillations as a function of the two gate voltages V_{T1} and V_{T2} at $V_{SD} = 100\,\mu\text{V}$. Over most of the gate range the peaks show a perfect 45° slope which is an experimental confirmation of the near identical geometric arrangement of these two gates relative to the dot.

Gate leakage currents only flow in the field emission regime when the applied gate voltage has sufficiently narrowed the barrier induced by the intrinsic region in the gap between donor patches. As a comparison, an IV trace through the dot (orange curve in Fig. 5.4 b) shows an almost immediate onset of current with the applied bias voltage. Here, the much smaller gaps between dot and source/drain contacts (∼8 nm) were designed to act as tunnel barriers. By applying a fixed bias voltage ($V_{SD} = 360\,\mu\text{V}$) clear Coulomb oscillations are observed in the source-drain current I_{SD} over the entire gate range of V_{PG}, as illustrated in Fig. 5.4 c.

One of the unique advantages of STM-lithography is that one knows with nanometer precision where the dopants are patterned within a device. From the dot area (∼2100 nm^2) and the known electron density of a saturation dosed Si:P layer ($n_s \sim 1.7 \times 10^{14}\,\text{cm}^{-2}$) we can thus estimate an upper limit for the electron number of $N < 4000$. We therefore expect our many-electron dot to be in the classical regime of Coulomb blockade, where the single particle spacing is much smaller than the charging energy, $\Delta E \ll E_c$ [48, 46]. This is consistent with the fact that the observed CB-peak spacing $V_{PG} \approx 12.5\,\text{mV}$ is approximately constant over the entire gate range (Fig. 5.4 c).

A stability diagram of the quantum dot device is shown in Fig. 5.5 a, where the differential conductance $G_{SD} = dI/dV_{SD}$ is plotted as a function of the applied bias and plunger gate voltages. Within the framework of the constant interaction model of Coulomb blockade (see section 2.3.1) the height of the Coulomb diamonds corresponds to the addition energy.

Capacitances of the quantum dot device (in aF)

C_Σ	C_S	C_D	C_{PG}	C_{T1}	C_{T2}	α_{PG}
48.5	9.7	9.7	13.2	7.2	7.2	0.27

Table 5.1: Summary of the experimental capacitance values extracted from the height $E_c = e^2/C_\Sigma$ of the Coulomb diamonds (Fig. 5.5 a) and the periodicity of the CB peaks, $\Delta V_{gate} = e/C_{gate}$ (Fig. 5.4 c).

From the plot of Fig. 5.5 a we estimate[1] $E_c = e^2/C_\Sigma = 3.3 \pm 0.2\,\text{meV}$. The mutual capacitances extracted from this and the CB peak spacing as a function each gate voltage, $\Delta V_{gate} = e/C_{gate}$, are summarized in table 5.1. Tuning the in-plane gates in our quantum dot leads to extremely stable CB-oscillations with only a few minor switching events as indicated by the white arrows in the stability diagram of Fig. 5.5 a. These are most likely caused by charge rearrangements in the vicinity of the device. The high stability of the device is further highlighted in a measurement of the dot conductance as a function of both V_{T1} and V_{T2} (see Fig. 5.5 b) spanning about half of the available gate range for each of the gates. Here, the CB-peaks move at a constant 45° slope indicating that the two gates $T1$ and $T2$ have the same capacitive coupling to the dot as expected from the symmetry of the device geometry.

It should be noted that the Coulomb peak heights in Fig. 5.4 c are observed to vary significantly. The smooth modulation occurs on a gate voltage scale on the order of ∼100 mV. Using the appropriate lever arm $\alpha_{PG} = 0.27$ for the plunger gate this translates to an energy scale on the order of a few 10s of meV, which leads us to attribute the observed variation in peak height to a strongly modulated density of states (DOS) at the Fermi level of our narrow source and drain leads. The tight lateral confinement within the ∼4 nm wide electrodes results in transversal quantization and thus a quasi-1D DOS [36], as illustrated in Fig. 2.6 of chapter 2. In a simple particle-in-a-box approximation [46], the spacing between these DOS peaks is estimated to occur on a characteristic energy scale $\hbar^2\pi^2/gm^*L^2$, where L is the width of the wire, m^* is the electron effective mass, and $g = g_s g_v$ accounts for the spin and valley degeneracy. Using the lead width $L = 4\,\text{nm}$, an averaged effective mass reported for δ-doped Si:P layers of $m^* = 0.28\,m_e$ [35], and assuming full spin and valley degeneracy ($g = 12$), this yields an expected spacing on the order of 10 meV – which is broadly consistent with the observed modulation of the peak height. Indeed, a modulated DOS in low-dimensional leads has been found to influence the transport properties of several other quantum dot structures [145, 146, 147]. This will

[1] In the many-electron regime $\Delta E \ll E_c$ and therefore $E_{add} = E_c + \Delta E \approx E_c$.

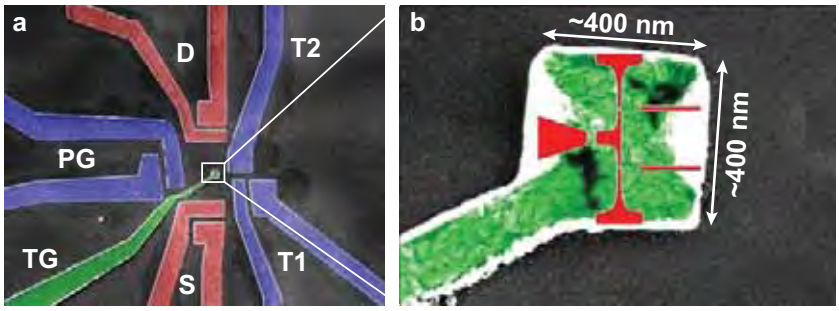

Figure 5.6: Metallic top gate over the buried quantum dot. **a**, False-color SEM image of the device after an aluminium top gate (TG) has been patterned on the native SiO_2 barrier. **b**, The composite close-up image illustrates the approximate relative position of the $\sim 400 \times 400\,\mathrm{nm}^2$ top gate with respect to the buried planar Si:P quantum dot (red), $\sim$25 nm below the surface.

be discussed in more detail in section 6.4.5 of the following chapter.

5.2.2 Patterning of a top gate over the planar quantum dot

In the previous section we have demonstrated how donor-based quantum dots can be realized in a planar architecture, relying exclusively on highly doped in-plane gates to tune the electrochemical potential of the dot. The plunger gate of this device was found to have a lever arm $\alpha_{PG} = C_{PG}/C_\Sigma \approx 0.27$ allowing for a total change of the electron number on the dot by $\sim$40 within the available gate range. Considering that the total number of electrons on the dot is roughly 4000, it is desirable to increase the tunability of the device. It may thus be advantageous to incorporate a top gate into our architecture for two reasons: Firstly, considering a simple plate capacitor model it is obvious that the capacity of two parallel (co-axial) plates will be larger[2] than that of two co-planar plates, resulting in a larger lever arm in the former case. Secondly, the presence of an oxide barrier between a top gate and the dot may afford a higher gate range compared to an in-plane gate, where the gate barrier is defined solely by the frozen-out Si substrate between the electrodes.

To investigate the effects on the functionality of the device, a surface gate was fabricated on top of the planar quantum dot. Importantly, this was done *after* the electrical characterization with just the donor structure and ohmic contacts presented in the last section. The resulting structure is shown in Fig. 5.6 with the small top gate TG (shown in green) aligned to lie between the ohmic contacts (red) and the contacts for the three in-plane gates (blue). We use a short oxygen plasma to remove organic residues and clean the surface before evaporating the aluminium top gate. The latter is therefore fabricated directly

[2]We assume an equal separation between the plates in both cases.

Changed capacitances of top gated device (in aF)

	C_Σ	C_{T1}	C_{PG}	α_{PG}	C_{TG}	α_{TG}
without	48.5	7.2	13.2	**0.27**	n/a	n/a
with top gate	∼84	3.7			73	**0.87**

Table 5.2: Comparison of some relevant capacitances of the planar quantum dot *before* and *after* fabrication of the metallic top gate (TG). The sum capacitance C_Σ nearly doubles and the top gate has a much higher lever arm α_{TG} compared to the plunger gate (PG) of the in-plane gated device.

on the native SiO_2 layer.

The device was subsequently re-measured at mK-temperatures. We find a top gate range of approx. $-400\,\mathrm{mV}$ to $400\,\mathrm{mV}$ (Fig. 5.7 a). We then again perform gate sweeps at low bias, this time as a function of the top gate voltage V_{TG} (Fig. 5.7 b) and find a CB peak period $V_{TG} \approx 2.5\,\mathrm{mV}$ that is much smaller than that of the in-plane gates. This is expected because of the stronger capacitive coupling of the top gate to the dot. In particular, the sum capacitance C_Σ nearly doubles as a result of the increased total capacitive coupling of the dot. Table 5.2 compares the new capacitances to those before the top gate was fabricated. Importantly, the top gate indeed exhibits a much higher lever arm $\alpha_{TG} \approx 0.87$ compared to the plunger gate ($\alpha_{PG} \approx 0.27$) of the planar device. The top gate thus allows for a total change in electron number by ∼320 – an increase of almost an order of magnitude compared to the planar device.

Despite the increased tunability, we find that the highly stable and regular Coulomb oscillations observed prior to the addition of the top gate (see Fig. 5.4 c) can not be reproduced when sweeping the top gate voltage. Figure 5.7 b shows an up- and down-sweep of V_{TG} which exhibits both considerably more noise as well as clear hysteretic behavior. Importantly, the presence of the top gate is detrimental to the device stability even when only the in-plane gates are used while keeping the top gate grounded. This is illustrated in Fig. 5.7 c which shows Coulomb oscillations as a function of the in-plane gate voltage[3] V_{T1}, both before and after the top gate was added to the device. The switching noise is significantly higher in the presence of the top gate (right panel in Fig. 5.7 c) even though the latter was grounded during this measurement. We attribute this to the fact that the metallic top gate provides a ground plane which effectively pulls the electric fields arising from the in-plane gate voltages closer to the defect-prone Si/SiO_2 interface.

Using the top gate, we also find that noise and hysteresis effects increase significantly

[3]Due to a contact problem, the gate PG could not be used during this measurement.

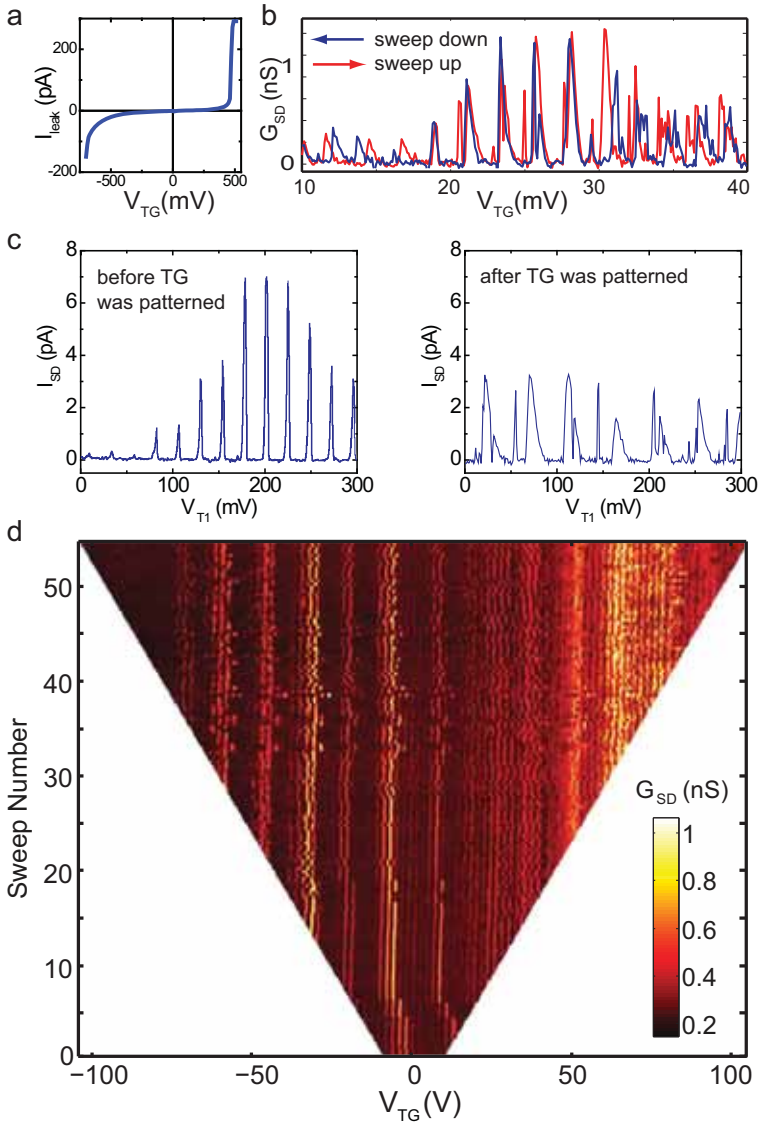

Figure 5.7: Reduced stability of the top gated device. **a**, Leakage characteristic for the Al top gate patterned on the native SiO_2 layer yielding an effective gate range of roughly $\pm 400\,\mathrm{mV}$. **b**, Up- and down-sweep of the top gate voltage V_{TG} showing clear hysteresis and switching effects. **c**, Coulomb oscillations (at $V_{SD} = 1\,\mathrm{mV}$) before (left panel) and after (right panel) the metallic top gate has been patterned over the device, showing reduced stability in the latter case. The lower average peak spacing in the right panel reflects the reduced lever arm of gate $T1$ in the presence of the top gate. **d**, Coulomb oscillations as a function of V_{TG}, where the gate voltage window is steadily increased with each sweep. Initially (for $|V_{TG}| < 10\,\mathrm{mV}$), the Coulomb peaks (bright vertical lines) are found to be more or less reproducible, with only a few minor switching events. However, as the V_{TG} window is increased the peaks first shift to different positions and eventually become very noisy and hysteretic.

(and often irreversibly for a specific cool-down) when increasing the V_{TG} range. This is illustrated in Fig. 5.7 d which depicts successive up- and down-sweeps of V_{TG} for a steadily increasing gate voltage window. In the first few sweeps the CB peaks (bright vertical lines)

are more stable, with only a few initial discontinuities, and occur at roughly the same values of V_{TG} for each sweep. With increasing gate voltage these peaks become unstable before nearly disappearing in the noise as V_{TG} exceeds $\pm 50\,\mathrm{mV}$. This unstable behavior often persists even after grounding the device for several hours and only disappears again after completely warming up the donor device. We attribute this behavior to the fact that more and more charge traps at the Si/SiO_2 interface [142] get activated as the electric field between the device and the top gate increases. It is important to note that no attempt was made to reduce the interface trap densities in our case. In particular, a thermal oxide (which is typically grown at temperatures around 1000°C) can not be implemented in our devices since it causes donor diffusion out of the STM patterned regions. However, it should be emphasized that similar switching noise may also be present in top gated single electron devices containing a higher quality thermal oxide [135, 140, 148]. It is possible that more controlled and slower growth conditions [149] for the native oxide may result in a marginal improvement of the device stability. More importantly, complete epitaxial fabrication of a purely in-plane gated donor device in a UHV environment has significant advantages over conventional metallic gate electrodes. This is true both in terms of alignment precision as well as avoiding the inevitable detrimental effects that impurities and charge traps near interfaces may have on electronic device stability [142]. By avoiding surface gates altogether, electric fields resulting from the voltages applied to in-plane gates only arise within the epitaxial silicon region, leading to very stable device behavior – even close to fields where gate leakage starts to occur (see Fig. 5.4 c).

The demonstration of epitaxial in-plane gates fabricated in a UHV environment is thus a crucial step towards reproducible gating of functional donor-based nanostructures. Based on the high stability of the in-plane gated dot, a decision was made to focus entirely on a planar architecture for subsequent quantum dot devices fabricated during this thesis. Relying exclusively on in-plane gates does however present a challenge for the scale-down of dopant-based devices as will be discussed in the next section. In the following chapters we will then demonstrate the highly stable operation of in-plane gated few-donor (chapter 6) and single donor (chapter 7) devices.

5.3 Challenges in down-scaling of planar Si:P quantum dots

Having demonstrated the successful operation of a STM-patterned Si:P quantum dot in the many-electron regime, the next goal – as with any other quantum dot architecture – was to reduce the size of the island towards the few-electron limit. Only by avoiding

the ensemble averaging inevitable in larger structures can the quantum properties of electrons and donors (such as their discrete spin states) be investigated in detail. However, reaching the few-electron regime cannot be achieved by simply decreasing the size of the entire structure. In particular, there are two key challenges that need to be addressed for successful down-scaling of a functional quantum dot device, which will be discussed in more detail in the following sections:

(i) *Tunnel coupling:* The tunnel characteristics of our planar tunnel junctions are sensitive to changes in the gap dimensions on the sub-nm scale. Maintaining the proper tunnel resistance therefore requires careful adjustment of the device geometry as the dot size is decreased.

(ii) *Device tunability:* The mutual capacitances will decrease significantly as the dot is reduced in size, particularly in a planar geometry. To ensure good tunability of the device it is therefore necessary to maintain good *capacitive coupling* between the dot and the in-plane gates. At the same time, gate leakage must be minimized to obtain a sufficient gate range.

5.3.1 Tunnel coupling to the external leads

Being able to perform transport spectroscopy requires the quantum dot to be connected to external source and drain leads which act as electron reservoirs. In order to observe Coulomb blockade (with a well-defined integer number of electrons on the island), the resistance between the island and these leads must be higher than the resistance quantum $h/e^2 \approx 26\,\mathrm{k}\Omega$. This is commonly achieved by introducing tunnel junctions between the dot and the leads.

In electrostatically defined lateral quantum dots in GaAs [45] and SiGe heterostructures [125], these tunnel gaps are usually defined by applying suitable voltages to the top gates resulting in a local depletion region that "pinches off" the 2DEG underneath. The tunnel barriers can therefore be tuned over a certain range by adjusting the external gate voltages. By contrast, the tunnel junctions in our planar devices are realized by gaps between the STM-patterned P-doped regions defining the island and the leads, respectively. At cryogenic temperatures, the low-doped intervening substrate acts as a tunnel barrier due to the freeze-out of carriers. The transport characteristics are therefore fixed by the geometry of the tunnel junction. While the effective barrier height can be modulated to a certain degree by the in-plane gate voltages, the extremely small dimensions of our donor dots make it difficult to realize dedicated barrier gates which tune *only* the tunnel coupling

to the leads. Particularly for few-donor devices (with dot diameters <5 nm), all in-plane gates will show non-proximal capacitive coupling which affects the dot potential and the tunnel barriers at the same time. This will be discussed in more detail in section 6.4.3 of the following chapter.

From previous studies of nm-scale dopant-based tunnel junctions [95, 100] we know that the tunnel resistance is exponentially dependent on the separation between the electrodes, with changes of a few nm in separation resulting in differences of several orders of magnitude in resistance [100]. Furthermore, it was found that both the gap separation and the lead width of the tunnel junction are crucial, with a low width-to-length aspect ratio of the gap resulting in a higher resistance [100].

The underlying physics determining the transport characteristics of our lateral tunnel junctions is not yet fully understood and is a matter of ongoing research. However, different tunneling regimes can be identified [100]: At low bias voltages ($eV_{SD} \ll E_b$ where E_b is the height of the tunnel barrier), tunneling can be described by the Simmons model [150], which assumes that the barrier is not influenced by the applied voltage resulting in a bias-independent ohmic tunneling resistance. At higher bias voltages, a transition occurs to the Fowler-Nordheim regime [25], where the effective barrier width decreases with the applied bias. This leads to an exponential increase of the tunneling current commonly observed in the field emission regime. For our purposes, the applied bias voltages during transport spectroscopy will generally be much smaller than the typical barrier heights ($E_b \sim 100\,\mathrm{meV}$) which can be estimated from temperature-dependent measurements of tunnel junction devices [100]. It is therefore the zero-bias resistance of the tunneling junctions that is relevant for our quantum dot structures.

The useful range of tunnel resistances for a quantum dot device is bounded by the resistance quantum as the lower limit ($\sim$26 kΩ) and the practicability of measuring small device currents as the upper limit (typically <1 TΩ). In the absence of a full theoretical description of the geometry dependence of the tunneling characteristics, we rely on general trends inferred from previous studies on tunnel junctions [100] as well as empirical data from previous quantum dots. In particular, the dimensions used for the tunnel gaps of the many-donor dot presented in this chapter (with $\sim$8 nm gaps and $\sim$4 nm wide electrodes) have yielded good results. It should be noted that a gap separation of 8 nm is consistent with values previously discussed in a proposal by Tucker and Shen [144]. They estimated the correct scale for lateral tunnel junctions used in donor-based silicon quantum dots to be a small multiple of the Bohr radius a_B, corresponding to $\sim$10 nm. The Bohr radius is a measure for the spatial extent of the donor wavefunction in Si and is

given by $a_B = 4\pi\epsilon_0\epsilon_{Si}\hbar^2/m^*e^2 \approx 2.5\,\text{nm}$, where $\epsilon_{Si} = 11.7$ is the Si dielectric constant and $m^* = 0.26\,m_0$ the average electron effective mass [151]. Tucker and Shen also identified $2a_B \approx 5\,\text{nm}$ as the lower limit for the gap separation to prevent direct electrical coupling by wavefunction overlap. For subsequent quantum dot devices we will retain the nominal gap dimensions that were used successfully for the many-donor quantum dot.

5.3.2 Capacitive coupling to the gates

Studying the transport properties of a quantum dot for different electron numbers can give useful insights into the underlying physics of the system [46]. A key requirement for a functional quantum dot device is therefore the ability to tune the electrochemical potential of the dot over a sufficient range by applying a voltage to a suitable gate electrode. The tunability of a gated device depends on two parameters: the gate lever arm and the effective gate range. In the framework of the constant interaction model (see section 2.3.1) the former is given by C_G/C_Σ, where C_G is the capacitance between gate and dot and C_Σ is the sum capacitance. C_G/C_Σ is largely determined by the geometry of the gate electrode, in particular its separation to the dot and the other electrodes. Due to the comparatively large gate separations (on the order of several 10s of nm), direct tunneling to/from the gate at low bias can be neglected[4]. The leakage characteristic of a gate is therefore governed by the field emission regime, where the bias voltages are sufficient to tilt the barrier profile thus decreasing the effective barrier width [25]. Previous studies of lateral tunnel junctions in our system have shown that the gate bias required to cause field emission (typically on the order of several 100 mV) increases significantly for higher separations [100]. The optimal gate separation is therefore a trade-off between maximizing the capacitive coupling (for small separations) and minimizing the gate leakage (for large separations).

One of the distinctive features of our dopant-based quantum dots is the fact that the dot size scales proportionally with the electron number. Moreover, due to the high sheet doping density (0.25 ML) in our system, the confinement length-scales of a donor-based few-electron quantum dot will be much smaller than in other quantum dot architectures. As an example, a planar Si:P dot with $N = 10$ electrons will have a diameter $<5\,\text{nm}$. By contrast, the effective diameter of both lateral [45] as well as vertical GaAs quantum dot structures with the same electron number is on the order of 100 nm [152]. Due to the small dot sizes, maintaining sufficient capacitive coupling presents a particular challenge

[4] This is in contrast to the tunnel barriers to the leads with separations $\lesssim 10\,\text{nm}$.

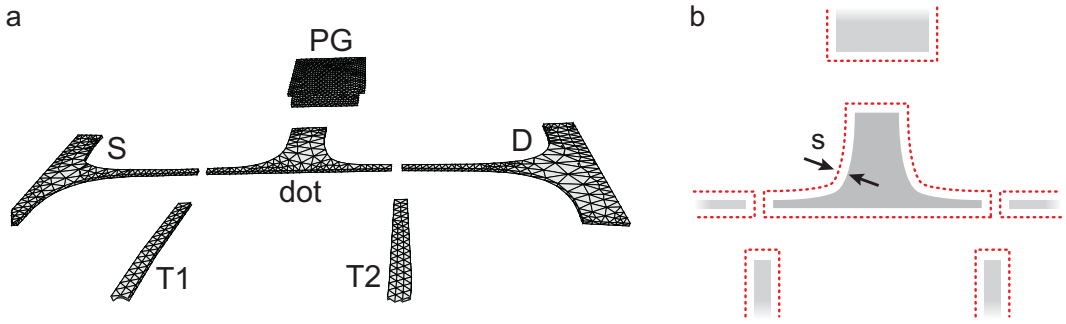

Figure 5.8: FastCap panel file. a, The cross-capacitances of the planar quantum dot are modeled using the FastCap software [154]. Here, the device is represented by a 3-dimensional wire grid or "panel file", with a uniform thickness (in z-direction) of 2 nm. **b**, We find better agreement with the experimental data when adding a lateral "seam" s around all patterned structures to account for the finite spread of charge density into the surrounding Si substrate.

for down-scaling in our dopant-based architecture.

Since STM-patterning of Si:P devices is a comparatively time-consuming process, it is desirable to optimize device geometry prior to fabrication. However, in contrast to top gated architectures, where the gate capacitance can often be easily estimated from a simple parallel plate capacitor model [153], predicting the capacitances for our planar devices is not straightforward. To facilitate down-scaling of our Si:P quantum dots, we will therefore use a numerical capacitance solver (FastCap) to model the capacitances and gate lever arms of new device geometries.

5.3.3 Capacitance modeling

FastCap is a finite-element multiconductor capacitance solver [154] which was originally developed to facilitate capacitance modeling of μm-scale integrated circuits for the microelectronics industry. As such, it relies entirely on classical electrostatics without any quantum corrections, treating the conducting structures as a perfect metal (with screening length zero) surrounded by a homogeneous dielectric. By contrast, in this thesis we will apply FastCap to estimate the capacitances of highly doped planar structures in silicon with dimensions on the nanometer scale. Nevertheless, we find surprisingly good agreement with the experimental values which we attribute to the extremely high sheet doping densities of our samples which result in metal-like screening lengths[5] on the order of nanometers. FastCap takes input in the form of a three-dimensional wire-frame model (so-called *panel files*) of the conducting structures where the surfaces are discretized into triangular or quadrilateral panels (see Fig. 5.8 a). Using a multipole acceleration algo-

[5] see section 6.5.2

Capacitances of the quantum dot device (in aF)

	C_Σ	C_{PG}	C_{T1}	C_{T2}	α_{PG}
experimental	48.5	13.2	7.2	7.2	0.27
FastCap, as desorbed	36	11	5.1	5.1	0.31
FastCap, with 2 nm seam	47	12	6	6	0.26

Table 5.3: Comparison between experimental capacitances for the many-electron quantum dot and the corresponding values calculated by FastCap, assuming a uniform thickness of 2 nm for the doped regions. The agreement between experimental and calculated values can be significantly improved when adding a 2 nm wide seam around the desorbed area of the dot (see Fig. 5.8 b) to account for the finite lateral extent of the donor electron density.

rithm, which greatly reduces computation time, the software then calculates the mutual capacitances for the set of conductors.

To demonstrate the applicability of this simple capacitance solver to our planar dopant structures, we will model the capacitances of the many-electron Si:P quantum dot presented in this chapter. The initial calculations were performed by Dr. A. Fuhrer [115] who matched the lateral contour of the wire-frame model (Fig. 5.8 a) directly to the STM images of the H-desorbed region of the device (see Fig. 5.1 a). In the vertical (z-) direction, a uniform thickness of 2 nm is assumed, in agreement with theoretical calculations for phosphorus δ-doped layers with similar sheet densities [37]. It should be noted that this "thickness" refers to the spatial extent of the electron charge density in the direction perpendicular to dopant plane (see Fig. 2.7 in chapter 2) and should not be confused with the finite spread of the dopants in z-direction due to segregation during the overgrowth process. Since the latter has been determined to be less than 6 Å [80] it is neglected for the capacitance calculations. Furthermore, only the central region of the device is considered, for which the dimensions are known with nm-precision (see Fig. 5.1). Based on these conditions, the calculated values were found to be in reasonable agreement with the experimental capacitances (see table 5.3) with errors on the order of $\pm 30\%$.

The implementation of FastCap for STM-patterned planar Si:P structures was later studied in more detail in our group by W. Tang [155] who also performed extended calculations for the many-electron quantum dot. In particular, he calculated that the error from neglecting the outer μm-sized contact structures is on the order of 10% [155]. More importantly, he found that a better agreement between the calculated and experimental capacitance values could be obtained by increasing the lateral extent of the wire-frame model *beyond* the edges of the actual donor region. This is illustrated in Fig. 5.8 b, where

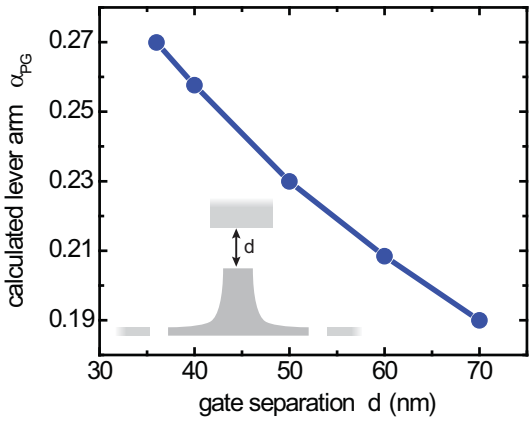

Figure 5.9: Lever arm vs gate separation. The calculated lever arm α_{PG} for the many-donor quantum dot as a function of the separation d between the in-plane gate electrode and the dot.

a "seam" of uniform thickness s is added laterally around the original contour. This seam accounts for the finite lateral extent of the electron wavefunction – which is expected to reach beyond the physical location of the dopants within the patterned region[6]. Interestingly, the best match with the experimental values was found [155] for a seam of 2 nm thickness (see table 5.3) – which is comparable to the Bohr radius (∼2.5 nm) for P donors in Si [151]. This is plausible since the latter is by definition a measure for the spread of the donor wavefunction in the surrounding Si host crystal. The resulting FastCap capacitances are summarized in

Based on this excellent agreement between the calculated values and the experimental data, FastCap was used to optimize the layout and improve the tunability of subsequent devices. Following a systematic approach to down-scaling, several devices of intermediate size were fabricated, such as a quantum dot with ∼770 electrons [111]. Here, a wide concave in-plane gate was patterned with the dot at the focal point, allowing for a comparatively large lever arm of 0.36 as predicted by capacitance modeling.

While FastCap can be used effectively to model the lever arm of a given gate geometry, no simple model exists to predict the corresponding gate range. It is therefore difficult to determine the optimal gate separation for a device. However, we can determine trends based on the experimental results of the many-donor device. Here, the separation of the plunger gate was ∼36 nm (Fig. 5.1) resulting in a lever arm of 0.27 and a gate range of approx. ±250 mV. Using FastCap, we can calculate how the lever arm changes as a function of the distance d between gate and dot. The results are depicted in Fig. 5.9 which shows a marginal decrease in α_{PG} from 0.27 to ∼ 0.19 as the gate separation is

[6]This is analogous to assuming a finite thickness of 2 nm in z-direction

doubled. By contrast, based on previous studies of lateral donor-based tunnel gap devices [100] we expect a much stronger dependence of the leakage characteristic on the gate separation. The small decrease in lever arm should therefore easily be compensated by the much greater gain in gate range, resulting in an overall increase of device tunability.
In the next chapter, we will demonstrate how these considerations have enabled the fabrication of a tunable few-donor quantum dot. In particular, for the two plunger gates of this device (patterned at increased separations of 44 nm and 57 nm, respectively) we find lever arms on the order of 0.1 and gate ranges exceeding ± 1 V.

5.4 Chapter summary

This chapter has demonstrated the fabrication of a functional STM-patterned donor-based quantum dot in the many electron regime. We have shown that donor-based in-plane gates are a viable alternative to metallic top gates to reliably tune the electrochemical of the dot. In particular, we find that such coplanar gates allow for highly stable operation of the device by circumventing the detrimental effects of interface or surface defects. We highlight this fact by comparing transport measurements of the purely in-plane gated device to measurements performed after a metallic top gate has been added to the structure, and find superior without the top gate.
We have also discussed the challenges associated with down-scaling of device dimensions in our planar donor-based architecture. In particular, we have identified the need to maintain sufficient capacitive coupling to the in-plane gates as a key issue for realizing tunable quantum dot devices in the few-electron regime. Here, capacitance modeling has been introduced as a viable tool to help optimize the layout of future devices.

Chapter 6

A few-donor Si:P quantum dot

Coulomb blockade of an STM-patterned quantum dot device was first demonstrated on a dot which was roughly 2100 nm^2 in size and thus contained several thousand P donors [115]. This device was discussed in detail in the previous chapter, along with the challenges related to downscaling within a planar architecture.

In this chapter we demonstrate the successful down-scaling of donor-based quantum dots to the few-electron limit. We present results from a dot approximately 20 nm^2 in size which is estimated (from the passivated area and dosing conditions) to contain $\sim$7 P donors. Low-temperature transport measurements reveal stable Coulomb blockade oscillations as well as a surprisingly dense excitation spectrum with an average energy spacing of $\sim$100 μeV. Modeling of the energy spectrum of the quantum dot using effective mass theory[1], we are able to show that this dense set of excitations can be attributed to valley splitting of electronic states in the highly confined dot.

6.1 Few-electron quantum dots in silicon

The first gated quantum dots to reach the few-electron limit were fabricated in modulation doped GaAs/AlGaAs heterostructures [152] due to their high mobility and relative ease of fabrication. However, silicon has attracted much attention as a host material for quantum electronic devices over the last 10 years. This is largely due to its favorable material properties for spin-based electronics [156] and quantum computation applications [14]: a weak spin-orbit coupling and the abundance of a nuclear spin-zero isotope. To date,

[1]This was done in collaboration with Prof. M. Eriksson and Prof. M. Friesen at the University of Madison-Wisconsin (USA).

silicon-based quantum dot structures have been fabricated in a variety of architectures.
In modulation-doped silicon/silicon-germanium heterostructures, quantum wells can be formed that generate a two-dimensional electron gas (2DEG) at the interface [34]. Quantum dots can be created in this system by introducing additional lateral confinement either by directly etching the substrate [131] or by using surface gates [125]. The latter have enabled the realization of devices in the few-electron regime [157, 158, 159] and also allow for the implementation of charge read-out techniques [160].
Quantum dots can also be realized in silicon nanowires [138, 139, 161, 162]. These nanowires are commonly grown by means of the vapor-liquid solid (VLS) mechanism using gold metal particles as catalysts and are typically ∼10 - 100 nm in diameter [139]. The resulting whiskers are then transferred onto an insulating substrate (usually a silicon wafer with a SiO_2 layer) and contacts are lithographically patterned. After deposition of a suitable barrier material or dielectric, top gates are defined in an additional lithography step which allow for confinement along the wire. Silicon nanowire quantum dots in the few-electron regime have been reported by several groups [138, 161, 162].
Quantum dots have also been realized in field-effect transistor structures on Si/SiO_2 substrates [135, 163, 164, 165]. By using metallic [135, 163] or polycrystalline silicon [165] gates on an oxide barrier, an inversion layer is created between highly doped contact regions. Barriers between the dot and the leads are created either by low-doped regions [165] or additional barrier gates in multi-layer gate stacks [163]. Charge sensing has also been implemented in this architecture [148, 153].
In all these approaches, confinement is (at least along one dimension) created by applying a voltage to some form of gate. By contrast, confinement within the donor-based structures presented in this thesis arises from the attractive potential of the ionized donors themselves. This not only allows for devices of smaller overall dimensions, but also leads to much steeper confinement slopes, the consequences of which will be discussed in this chapter.
Observations of previous silicon few-electron quantum dots show a variety of transport spectra with resonances of an average energy spacing ranging from 100 μeV to 10 meV. These resonance spectra arise from processes that can be either intrinsic to the quantum dot itself or due to extrinsic features [166] as will be discussed in more detail in section 6.4.5. Intrinsic resonances are commonly found to result from orbital excited states with a typical spacing on the order of several meV. By contrast, the ∼100 μeV spacing of resonances we observe in our device is a result of valley excited states arising from the strong lateral confinement within the dot.

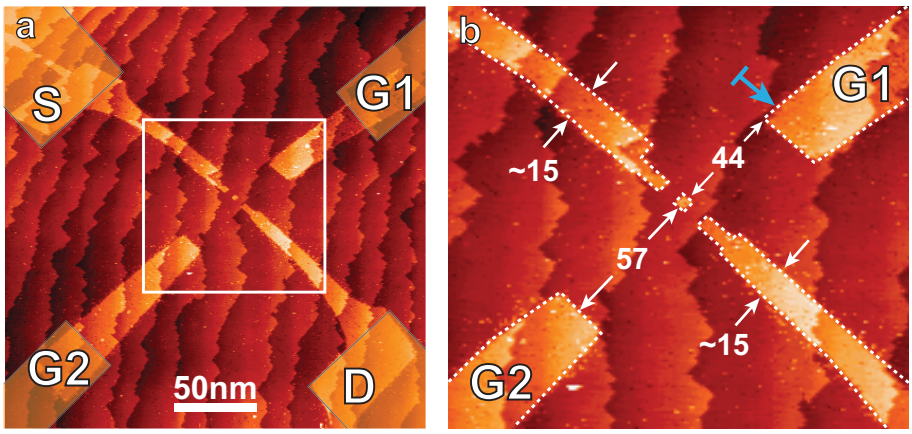

Figure 6.1: Few-donor quantum dot device. **a**, Composite STM image of the 4-terminal quantum dot device with source (S) and drain (D) leads and two in-plane gates ($G1$, $G2$) acquired during STM-lithography before PH_3 dosing. The superimposed orange shaded areas indicate the innermost parts of the contact arms for each electrode which were desorbed in a subsequent step. **b**, Close-up of the central area indicated by the white square in **a**. Gate $G1$ was patterned closer to the dot and with a deliberate shift (blue arrow) towards the D electrode to allow for control of the tunnel coupling symmetry (section 6.4.3). All dimensions are in nm.

6.2 Device geometry

In chapter 4 we outlined in detail the fabrication scheme as developed and enhanced within our group over recent years. The following section briefly summarizes the fabrication details relevant for the present device.

Figure 6.1 shows a STM image of the quantum dot structure after H-desorption of the central 4-terminal device with source (S) and drain (D) leads and two in-plane gates ($G1$ and $G2$). In a subsequent step, larger contact arms were desorbed for each electrode (indicated by the yellow shaded regions in Fig. 6.2) before dosing the entire surface with phosphine for 6 min at a chamber pressure of $\sim 5 \times 10^{-9}$ mbar (corresponding to an exposure of ~1.4 Langmuir). A device layout with two separate gates was chosen not only to achieve better tunability afforded by an increased capacitive coupling to the dot but also to allow for higher flexibility in gating operations via two independent gate voltages. This enables differential gating, i.e. a certain dot potential does not correspond to one fixed gate voltage but rather to an entire subspace of the parameter-space spanned by all gate voltages V_{G_i}. In the case of two gates, this means that the dot potential is constant along a line in the $V_{G1} - V_{G2}$ plane (as shown later in Fig. 6.6 c). Differential gating can be advantageous in terms of device stability where common defects like charge-traps can oscillate between two (or more) stable configurations at a particular potential thus causing switching noise [141]. If several gates are present, the operating point of the device can

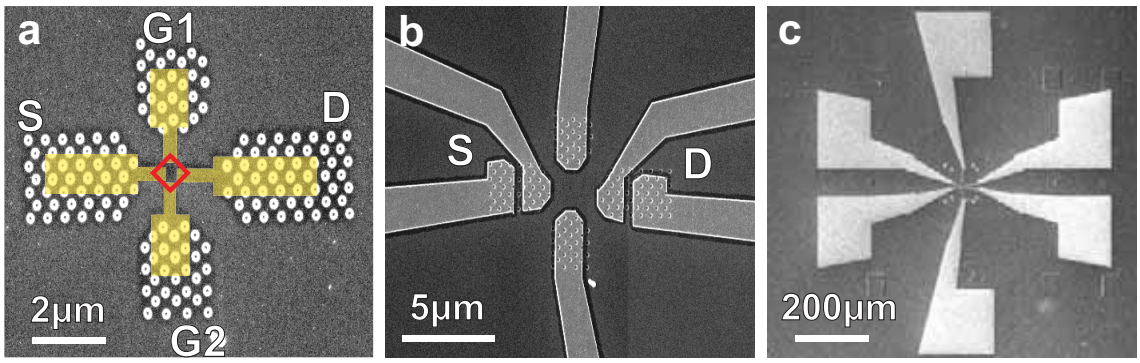

Figure 6.2: *Ex-situ* metallic contacts. a, SEM image of the encapsulated device after RIE etching of an array of contact holes which penetrate through the P doped layer. The position of the large STM-patterned contact patches for each of the 4 electrodes (approx. $2.5 \times 0.9\,\mu m^2$ for S and D) is indicated by the yellow shaded areas. The red square indicates the position of the central device as shown in Fig. 6.1. **b**, Al metal contacts are EBL-patterned over the contact holes, with one terminal per gate and two terminals each for S and D. The metal leads are extended out to larger bond pads shown in **c**.

be shifted to a different configuration of gate voltages where the oscillator is tuned out of resonance.

After PH_3 dosing and a P incorporation anneal for 30 s at ∼350°C the entire structure was overgrown with approx. 30 nm epitaxial Si. The latter was grown at a rate of ∼1.7 Å/min with a sample temperature of 250°C. After removal from UHV, an array of contact holes was defined in an EBL step and subsequently RIE etched down to the buried STM-patterned contact patches. The latter are indicated by the yellow shaded regions in the SEM image of Fig. 6.2 a. For the transport leads (S and D) the contact patches were patterned about twice as large as for the two gates to allow for 2 terminals per contact patch. In a last EBL step the aluminium contacts were patterned over the contact holes (Fig. 6.2 b and c). While quantum dot devices are typically measured in a 2-terminal configuration[2] where only one metal contact per STM-patterned patch is necessary, the additional contacts for the S and D leads allow us to determine that good ohmic contact has been made (see inset of Fig. 6.4).

6.3 Estimating the number of P donors on the dot

To understand the transport properties of our device it is important to estimate the number of P donors which constitute the quantum dot. One of the advantages of hydrogen lithography using a STM is the fact that the latter can be turned from a patterning tool into

[2]The contact resistance (∼kΩ) is negligible compared to the resistance of the tunnel gaps (∼GΩ)

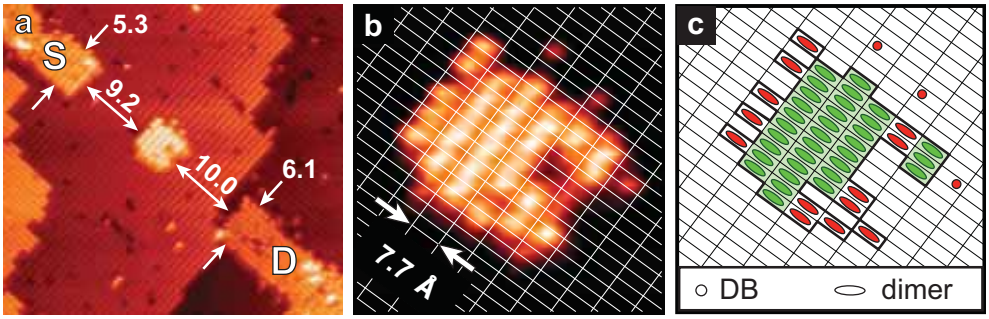

Figure 6.3: Estimating the number of donors on the dot. **a**, Close-up STM image of the $4.6 \times 4.6\,\mathrm{nm}^2$ desorbed area that defines the quantum dot. The dot is coupled to the source and drain leads via tunnel gaps. All dimensions shown are in nm. **b**, By overlaying a grid with dimer row spacing (7.68 Å), one can count the number of desorbed Si dangling bonds in the dot area. Along with an understanding of the P incorporation mechanism this allows for the identification of potential phosphorus incorporation sites highlighted in green in **c**. Stray dangling bonds (DB) and single bare silicon dimers which do not contribute to P incorporation are indicated in red.

a non-invasive imaging tool by simply adjusting the tip voltage (see chapter 3). While it is in principle possible to directly determine the number of incorporated donors by imaging the structure again *after* the incorporation anneal, this step was avoided in the case of the present device to reduce patterning time and minimize the risk of surface contamination. Instead, we estimate the number of donors from high-resolution images of the desorbed area in conjunction with a statistical study (see appendix A.1).

Figure 6.3 a shows a high-resolution STM image of the quantum dot in the center of the device before PH_3 dosing. The dimer rows of the Si(100) surface are clearly visible which allows for atomically precise surface metrology yielding tunnel gaps of 9.2 nm and 10.0 nm (12 and 13 dimer rows) between the dot and the S and D lead, respectively. A close-up of the H-desorbed area defining the quantum dot is shown in Fig. 6.3 b, where a dimer row grid has been superimposed. This allows us to count the number of desorbed Si dangling bonds (DB). At least 3 contiguous dimers within one dimer row are necessary to incorporate one P atom [76] as will be discussed in more detail in chapter 7. We can thus identify the potential incorporation sites represented by the green colored dimers in panel c. By contrast, the red regions do not contain enough adjacent dimers for P to incorporate.

Previous studies of δ-doped Si:P samples [39, 43] as well as μm-scale devices [44] have yielded electron densities of $\sim 2 \times 10^{14}\,\mathrm{cm}^{-2}$ corresponding to a planar dopant coverage of ∼0.25 ML. This is in agreement with theoretical studies of phosphorus incorporation in δ-doped devices [71]. For nm-scale desorbed areas, however, the density of incorporated P donors has been found [167] to decrease significantly for certain PH_3 dosing conditions

due to an edge effect: a PH_3 molecule at the edge of the desorbed area does not have enough neighboring Si dangling bond sites to lose all of its 3 H atoms and incorporation may be inhibited.

Dopant incorporation is inherently a statistical process. In order to quantify the decrease of doping density and thus estimate the number of donors in the present device, a statistical study was carried out in collaboration with Dr. J. Miwa and W. Tang using the same PH_3 dosing conditions. Here we patterned an array of desorption sites similar in size to the dot presented in this chapter. From STM-images after the dosing and incorporation step the number of incorporated P donors was determined for each site. A summary of this study is given in appendix A.1. For desorbed areas ∼5 nm in diameter we find an average donor coverage of 0.09 ML. Importantly, this value is significantly lower than the 0.25 ML donor coverage achievable on a bare Si surface [43] or larger depassivated areas [44]. Including error bars, the 0.09 ML coverage translates to an estimated number of 6 ± 3 phosphorus donors for our quantum dot device.

6.4 Electrical characterization at mK-temperatures

A initial characterization at 4.2 K confirmed that the sample was well contacted electrically and showed Coulomb blockade oscillations as a function of gate voltage. The quantum dot device was subsequently cooled down in a ^{3}He/^{4}He dilution refrigerator with a base temperature of ∼20 mK.

As discussed in chapter 3, we first check for good ohmic contact to the buried STM-patterned structure. This is done by simply measuring the resistance $R_{2\mathrm{T}}$ of the contact patches alone via their two metal terminals (Fig. 6.2). The resulting IV-curves for the source and drain contact are shown in the inset of Fig. 6.4 and reveal a two-terminal resistance of approx. 3 kΩ for both S and D electrodes.

The next crucial step is to determine the effective gate range for both in-plane gates, i.e. the maximum voltages that can be applied to each gate before the leakage current I_{leak} (flowing from a given gate to any of the other electrodes) exceeds a certain threshold, typically 100 pA. Fig. 6.4 shows the measured I_{leak} curves for both gates as a function of the applied gate voltage. From this plot we determine an effective gate range of -1.03 V to 1.37 V for $G1$ and -1.30 V to 1.82 V for $G2$, respectively. The smaller gate range for gate $G1$ is expected since it is patterned closer to the leads (see Fig. 6.1 b).

After these initial characterizations, we are now able to measure stability diagrams of the quantum dot device where the differential conductance dI/dV_{SD} is plotted as a function

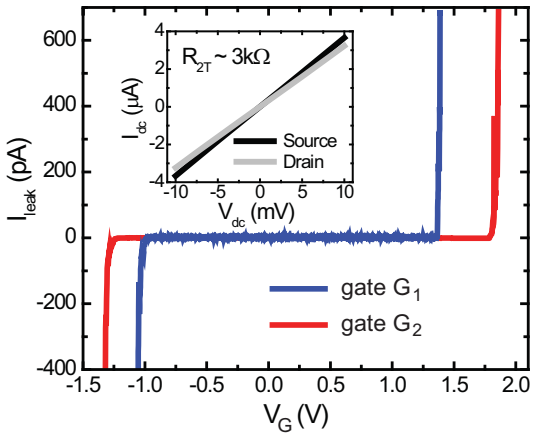

Figure 6.4: Determining the gate range. The graph shows the gate leakage current as a function of the applied gate voltage for each gate. We determine an effective gate range of -1.03 V to 1.37 V for $G1$ and -1.30 V to 1.82 V for $G2$, respectively. The smaller gate range for gate $G1$ is expected since it is patterned closer to the leads. The inset shows linear I-V curves through the contact patches for S and D with a two-terminal resistance of $\sim 3\,\mathrm{k}\Omega$, confirming good ohmic contact to the buried device.

of the applied bias and gate voltages as shown in Fig. 6.5. Here, the gate voltage is applied to both gates in parallel. For clarity, we label each of the diamonds with roman numerals which will be used in the following discussion. Importantly, these numbers do *not* correspond to the number of electrons on the dot. The latter is not known exactly since the gate range is not sufficient to deplete the dot with the pattern of Coulomb diamonds continuing all the way down to the negative end of the gate range. Under equilibrium conditions the electron number is expected to be equal to the number of donors on the dot. From the stability data we can immediately make several important observations, each of which will be addressed in more detail in the following sections:

- The addition energy E_{add}, given by the height of the Coulomb diamonds, increases as the gate voltage is lowered (see section 6.4.1).

- The device conductance decreases significantly with decreasing gate voltage (section 6.4.3).

- The device shows highly stable Coulomb blockade with only a few very minor charge rearrangements over a measurement time of approx. 15 hours (section 6.4.4).

- A great number of lines of increased conductance are visible outside of the blockaded regions. Their origin will be discussed in detail in sections 6.4.5 and 6.5.

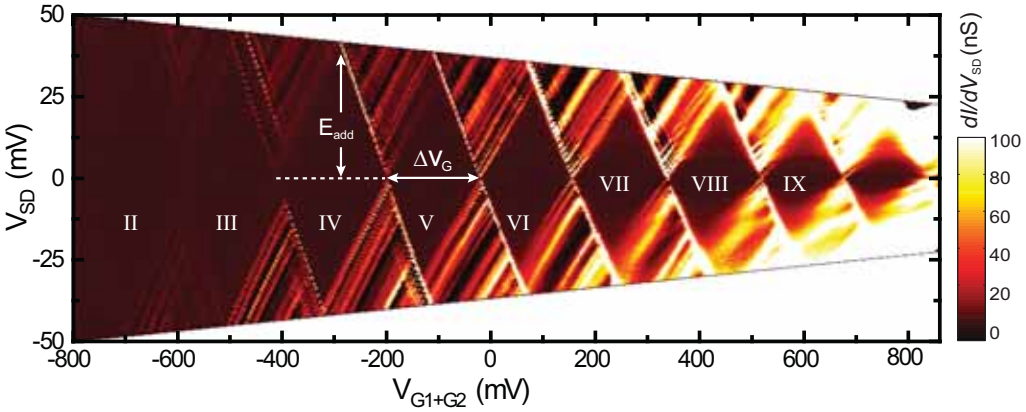

Figure 6.5: Low-temperature stability diagram. The device conductance dI/dV_{SD} was measured as a function of the bias voltage V_{SD} and the gate voltage applied to both in-plane gates in parallel. To limit the maximum current through the device, the bias voltage window was decreased for rising gate voltage, resulting in the overall trapezoidal shape of the data plot. A great number of conductance resonances are visible as bright lines of increased conductance running parallel to the edges of the Coulomb diamonds.

6.4.1 Addition energy spectroscopy

The height of each dark diamond in Fig. 6.5 is the addition energy, $E_{add} = E_c + \Delta E$, where E_c is the charging energy and ΔE is the single-particle level spacing. Here, E_{add} increases noticeably as electrons are removed from the dot: the extracted values are shown in Fig. 6.6 a, rising from < 20 meV to $\sim$50 meV within the available gate range[3]. Such a dramatic change in addition energy is only possible when the quantum dot is in the few-electron limit, so that the removal of electrons causes the actual size of the dot to change significantly. Interestingly, the measured addition energy of $\sim$50 meV at the lower end of the gate range actually exceeds the value reported for single P donors in bulk silicon [168]. This may reflect the fact that as the occupation number of the dot decreases, screening of the positive charge becomes less effective and the remaining electrons are more strongly bound by the increasing positive potential of the ionized donors.

The addition energy follows a smooth background curve (indicated in grey in Fig. 6.6 a) with prominent peaks for diamond "IV" and, arguably, diamond "VIII". Such local maxima of E_{add} generally reflect a stable electron configuration, typically due to a filled shell [46], so that the next incoming electron requires an extra energy ΔE in addition to the purely electrostatic charging energy E_c. In materials systems such as GaAs, circular few-electron quantum dots often exhibit a regular sequence of stable occupation numbers[4]

[3]The value for diamond "I" was obtained from another sweep not shown here.
[4]These are sometimes referred to as "magic numbers".

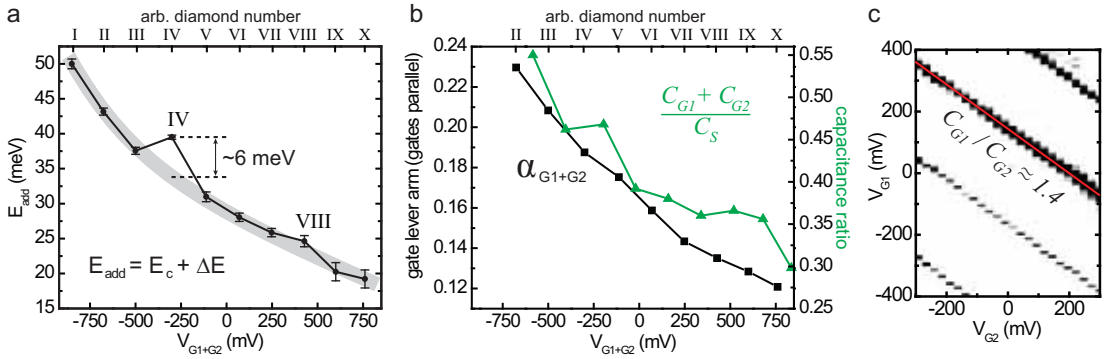

Figure 6.6: Addition energy and gate lever arm. **a**, The addition energy (extracted from Fig. 6.5) steadily increases as electrons are removed from the dot as illustrated by the smooth background curve (grey) which serves as a guide to the eye. Clear "kinks" are visible for diamond "IV" and possibly diamond "VIII" which may reflect higher orbital states. **b**, The extracted lever arm (for both gates in parallel) is also found to rise with decreasing gate voltage which is attributed to an increasing ratio of gate to lead capacitance. The latter is determined (for the source lead) from the negative slopes of the Coulomb diamonds in Fig. 6.5. **c**, From the slope of the Coulomb transitions in this gate-gate sweep we extract a ratio of the gate capacitances of $G1/G2 \approx 1.4$.

with increased addition energy [24, 152]. This sequence reflects a well-ordered 2D shell filling analogous to the filling of electron levels in atomic physics. In this context quantum dots are often being referred to as "artificial atoms" [24]. However, for silicon such a regular shell filling is typically not observed due to the additional valley degree of freedom. The latter results in a more complex spin filling that intricately depends on the atomistic details of the structure [163, 169, 170].

It is plausible to identify the baseline in Fig. 6.6 a as the charging energy with the "kinks" representing the single-particle energy spacing ΔE [122]. For diamond "IV" (which shows the most significant "kink") we can then roughly estimate ΔE to be on the order of 5-7 meV. This value is indeed consistent with the particle-in-a-box estimate for the orbital level spacing for a 2D dot of this size, as will be discussed in more detail in section 6.4.5. From the Coulomb diamonds of Fig. 6.5 we can also determine the gate lever arm as $\alpha_{Gi} = \Delta V_{Gi}/E_{add}$. The latter is a measure for the "effectiveness" of gate i, converting gate voltage into energy. In the CI model it is defined as the ratio of the gate capacitance to the total capacitance, $\alpha_{Gi} = C_{Gi}/C_{\Sigma}$. Fig. 6.6 b shows the extracted lever arm when both gates are used in parallel[5]. A clear increase is observed as the gate voltage is lowered which indicates a significant change of the capacitances between the dot and the electrodes. As a result, the simple constant interaction model of Coulomb blockade has limited validity [152] which is reflected by the observed change in E_{add}.

[5]The gate lever arm is additive, i.e. $\alpha_{G1+G2} = \alpha_{G1} + \alpha_{G2}$

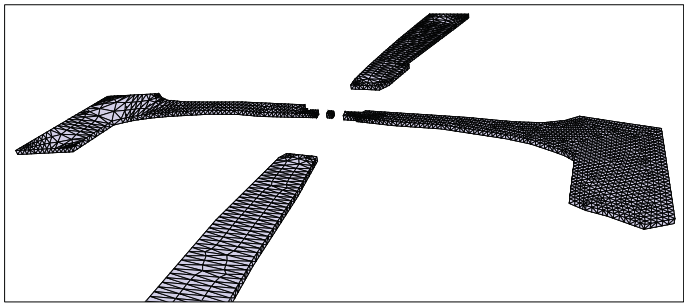

Figure 6.7: FastCap panel file. The cross-capacitances of the device were modeled using the FastCap software [154]. Here, the device is represented by a 3-dimensional wire grid.

The significant rise of α for lower gate voltages can be explained by the decreasing effective dot size as electrons are removed. This has a much stronger effect on the capacitive coupling to the leads than on the coupling to the gates which are much farther away [162]. Indeed, the ratio of gate to source capacitances (extracted from the negative slopes of the Coulomb diamonds [45]) is found to increase for lower gate voltages, as shown by the green curve in Fig. 6.6 b.

Since both in-plane gates can be used separately, the ratio of their respective capacitances can be extracted directly from the slope of the Coulomb transitions in a gate-gate sweep (Fig. 6.6 c). We obtain $C_{G1}/C_{G2} \approx 1.4$ which is consistent with the device geometry (Fig. 6.1 b) since gate $G1$ is patterned closer to the dot than $G2$.

6.4.2 Capacitance modeling

In chapter 5 we discussed how capacitance modeling was used to optimize device design for the down-scaling of our planar quantum dot structures. To verify the validity of this approach, it is instructive to compare the experimental capacitance values for the present few-donor device to the numerical predictions. We use the FastCap [154] software tool to model the capacitances of our device. The latter is represented by a three-dimensional wire-frame model as shown in Fig. 6.7. We assume a uniform thickness in z-direction of 2 nm, in agreement with theoretical calculations for phosphorus δ-doped layers with similar sheet densities [37]. It should be noted that this "thickness" refers to the spatial extent of the electron charge density in the direction perpendicular to dopant plane and should not be confused with the finite spread of the dopants in z-direction due to the overgrowth process. Since the latter has been determined to be less than 6 Å [80] we neglect it for our simple capacitance calculations. Furthermore, we only consider the central region of the device for which the dimensions are known with nm-precision (Fig. 6.1). Including the

Capacitances of the quantum dot device (in aF)

	C_Σ	C_S	C_D	C_{G1}	C_{G2}	α_{G1}	α_{G2}
experimental	5.16	2.32	1.93	0.53	0.38	0.102	0.073
FastCap	4.92	2.08	1.90	0.51	0.43	0.105	0.088

Table 6.1: The experimental values are extracted from diamond "V" in the stability plot of Fig. 6.5 as described in section 2.3.1. We assume that the measured value of E_{add} for this diamond corresponds directly to E_c since it lies on the smooth background curve in Fig. 6.6 a. For the FastCap calculations, a lateral "seam" of 2 nm was added around all four electrodes (as illustrated in 6.8 a) to account for the finite spread of charge density into the surrounding Si substrate. We assume the dot to be square with a variable edge length d. We find the best agreement with the experimental values for $d = 7.6$ nm.

outer μm-sized contact structures leads to corrections of only $\sim$10% [155].

Since the observed capacitance values vary strongly with gate voltage we will initially focus on diamond "V" of Fig. 6.5 for which we assume the diamond height to correspond to E_c as discussed above. Moreover, this diamond is close to zero gate voltage for which we expect the dot to be charge-neutral.

As described previously, the basic assumptions of FastCap are rather crude, assuming the conducting regions to be a perfect metal surrounded by a homogeneous dielectric, without any quantum corrections. Similar to assuming a finite thickness in the *vertical* direction, we add a *lateral* "seam" around the entire desorbed area of the device to account for the finite spread of the donor wavefunctions into the surrounding material.

Adding such a seam was found to yield better agreement with previous devices [155], as discussed in section 5.3.3. Here, a seam width of 2 nm was determined empirically to give the best match with the experimental values. Indeed, this value is plausible since it is similar to the effective Bohr radius $a_B \approx 2.5$ nm in silicon [151]. We will therefore again add a 2 nm seam around the desorbed areas for all four electrodes of the present device (see Fig. 6.8 a). By contrast, we will use the effective diameter d of the dot (which we will approximate as a square) as a fitting parameter for the FastCap calculations. The reason for this is that donor incorporation is inhibited at the very edges of the desorbed dot region (see section 6.3), and we therefore expect a smaller effective dot size. The calculated capacitances are summarized in table 6.1. We find the best match for an effective dot diameter of $d = 7.6$ nm (compared to a diameter of $\sim$4.6 nm of the physically desorbed dot area).

Considering the crudeness of the modeling approach the agreement with the experimental values is remarkably good, with errors of $\lesssim 10\%$. In particular, the assumption that the

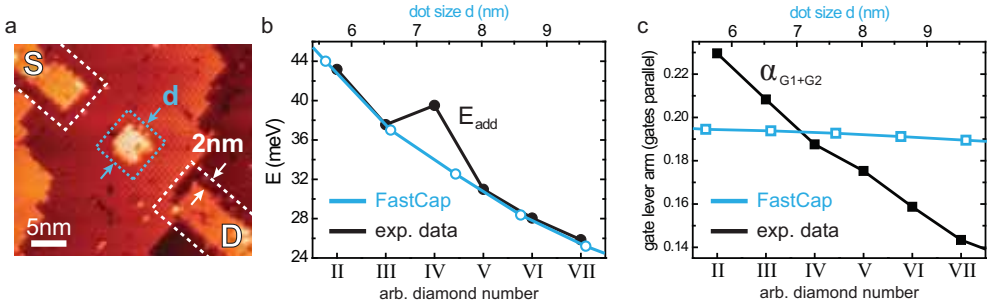

Figure 6.8: Capacitance modeling. **a**, For the FastCap calculations, a lateral "seam" of 2 nm was added around all four electrodes to account for the finite spread of charge density into the surrounding Si substrate. The dot is approximated as a square with a variable edge length d. **b**, The calculated values reproduce the rise in charging energy quite well assuming d increases from ∼5.5 nm to ∼9.5 nm as five electrons are added to the dot. However, the simple modeling does not account for the significant change in gate lever arm as shown in **c**.

nm-scale dopant regions can be represented by a homogeneous metal only holds if the screening length within the these regions is much smaller than the size of the doped areas [171]. We therefore attribute the excellent agreement to the extremely high doping density in our devices which results in a metal-like screening length on the order of ∼1 nm (see section 6.5.2).

Based on the excellent agreement with the experimental data, an attempt was made to reproduce the overall rising trend of the charging energy with decreasing electron number (see Fig. 6.6 a) by calculating the capacitances for different effective dot sizes. While the dimensions of the electrodes were fixed (with a seam of 2 nm as described above), the dot was assumed to be square with a variable side length d which was then used as a fitting parameter (see Fig. 6.8 a). The results are shown in panel b, which depicts the charging energy calculated from the FastCap sum capacitances via $E_c = e^2/C_\Sigma$. The calculated values reproduce the baseline of the experimental curve accurately assuming d increases from ∼5.5 nm to ∼9.5 nm as 5 electrons are added to the dot. However, despite the well-known effects of reduced screening it seems questionable whether such a drastic change in dot size is plausible for our donor-based quantum dot. We can further test the validity of the modeling results by calculating the gate lever arm over the same range as shown in Fig. 6.8 c. While the FastCap results (blue curve) reproduce the rising trend of the experimental data, the curves clearly do not match.

We thus conclude it to be unlikely that the observed increase in E_{add} is due to a change in the effective dot size alone. Another possible explanation is the varying tunnel barrier height between the dot and the leads which will be discussed in detail in the next section (6.4.3). The height of these barriers increases as the gate voltage is lowered resulting in

a stronger confinement along the S-D-axis. This in turn leads to a reduction of C_S and C_D and thus a lower sum capacitance. Such an increase in charging energy arising from a modulated tunnel barrier height has been observed in other quantum dot systems [122]. However, to include the effects of a variable barrier height is far beyond the capabilities of our simple capacitance modeling approach.

6.4.3 Tunnel coupling symmetry

An important advantage of STM patterning is that one can determine which tunnel barrier should dominate conduction by simply considering the geometry of the gaps directly from the STM images. Variations in the device dimensions even at the atomic scale have significant effects on the tunnel resistance. Previous experiments in our group have shown that both the gap length and the lead width of the tunnel junction are crucial, with a low width-to-length aspect ratio of the gap predicting a high resistance [100]. From Fig. 6.3 a we determine an aspect ratio of 0.58 for the S-side gap in contrast to 0.61 for the D side. Despite this small difference in values we already know that the tunnel junction to the S electrode is expected to have a higher resistance.

Figure 6.9 a shows another stability diagram of the device where the conductance is plotted on a logarithmic scale for better visibility of the transport resonances at low gate voltages. Here, the gate voltage is applied to gate $G1$ only (while keeping $G2$ floating). Over the entire gate range we observe a great number of lines of increased conductance running parallel to the diamond edges outside of the blockaded regions. For comparison, the diamonds are labeled with the same roman numerals (which do *not* correspond to the electron number on the dot) as in Fig. 6.5. Diamond "IV" is easily identified by its local maximum in peak height. We find that the diamond pattern has shifted towards higher gate voltages compared to Fig. 6.5. This is most likely due to several V_{G1} sweeps to the very edges of the gate range for $G1$ which may have caused some charge rearrangements in the vicinity of the device (see section 6.4.4).

Experimentally, an asymmetry in tunnel coupling manifests itself in an asymmetry of the observed transport features [145]. This is apparent from the data in Fig. 6.9 a: for $V_{G1} \geq 0$, predominantly lines with negative slopes are observed indicating a stronger coupling to the D electrode [145]. As we will discuss later in this chapter (section 6.5.2), we attribute the resonances visible in Figs. 6.5 and 6.9 a, with a spacing on the order of a few meV, to a modulated density of states in the source and drain leads. This can be understood by considering the simple energy schematic of Fig. 6.10 where the DOS in both S and D is

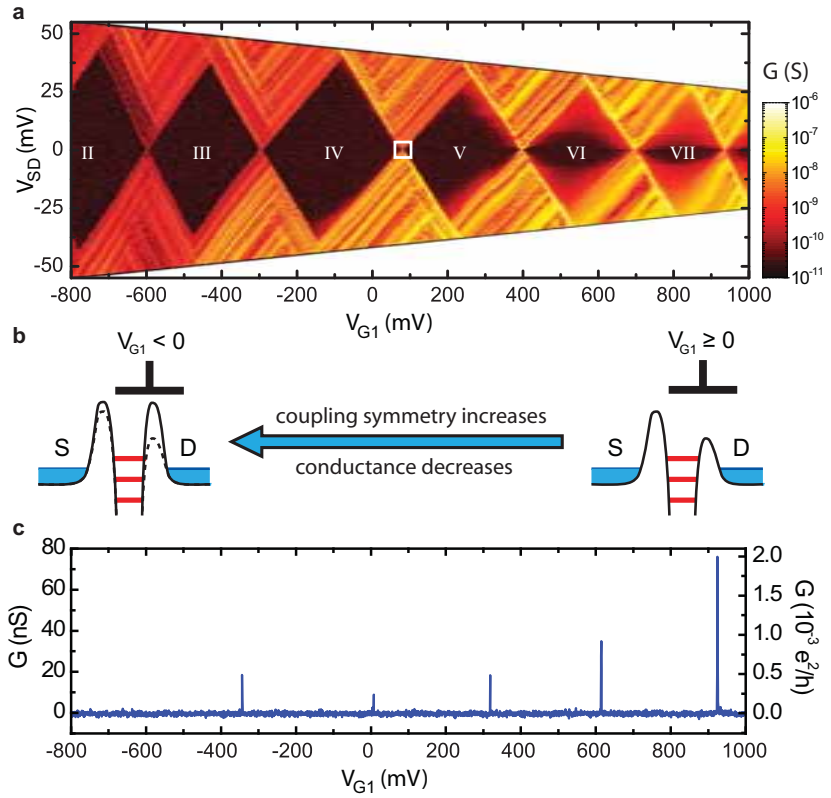

Figure 6.9: Tunnel coupling symmetry. **a**, Stability diagram where the gate voltage is only applied to gate $G1$ while keeping $G2$ floating. Here, the data is plotted on a logarithmic scale to increase the visibility of resonance features at lower gate voltages. The diamonds are labeled with the same roman numerals (which do *not* correspond to the electron number on the dot) as in Fig. 6.5, where both gates were used in parallel. The white square indicates the position of the close-up data of Fig. 6.13. While for $V_{G1} > 0$ conductance features are visible predominantly with positive slope, both positive and negative slopes are observed at the lower end of the gate range. This is a result of the gate voltage dependent coupling asymmetry as illustrated in the schematic energy diagram in **b**. **c**, The Coulomb peak conductance shows a decreasing trend for lower gate voltages ($V_{SD} = 60\,\mu$V).

strongly modulated. A transport resonance (i.e. a peak in the differential conductance) occurs whenever a dot level aligns with the potential $\mu_{S,D}$ in the leads. However, tunneling rates generally depend on the number of available states to tunnel from/into[6] so that a resonance can also occur when a dot level is aligned with a DOS peak within the bias window [147]. Now assume that the coupling constants to source and drain, Γ_S and Γ_D, are significantly different as illustrated by the narrower barrier and thicker arrow on the drain side in Fig. 6.10 a. Only when a DOS peak in the *weaker* coupled lead enters the bias window, eV_{SD}, will the device conductance show a noticeable relative increase. This is because tunneling through the corresponding (higher) barrier represents the rate-limiting

[6]This essentially follows from Fermi's Golden Rule.

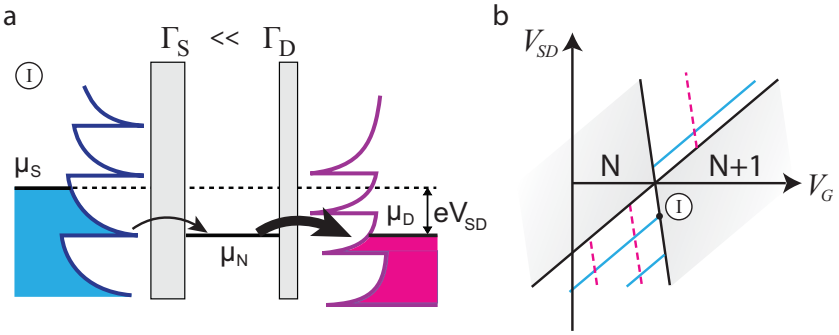

Figure 6.10: Resonances arising from DOS in the leads. **a**, Energy diagram of single-electron tunneling through a discrete quantum level, μ_N, in the presence of a strongly modulated DOS in the leads. For asymmetric tunnel barriers, $\Gamma_S \ll \Gamma_D$, transport through the S barrier is the rate-limiting process as indicated by the thin arrow. **b**, Schematic stability diagram showing lines of increased conductance resulting from the DOS peaks in the S (blue) and D lead (pink). The latter will be much less pronounced due to the stronger coupling to D as indicated by the dotted pink line.

process [145]. From the data of Fig. 6.9 a we thus conclude that for $V_{G1} \geq 0$ the tunnel barrier is higher on the S side – as expected from the device geometry. It should be noted that a disparity between conductance features with opposite slope does *not* automatically pinpoint DOS in the leads as their origin. A similar disparity is also commonly observed for resonances arising from dot excited states in asymmetrically coupled devices [165, 166].

The impact of variations in the device design at the nm-scale is also apparent if we consider the effect of the in-plane gates. Due to the small size of the dot, it is evident that an applied gate voltage will not only tune the electrochemical potential of the dot but will also affect the tunnel barriers to the leads [100]. This non-proximal coupling is a commonly observed feature of few-electron quantum dots in many materials systems [152, 158]. Gate $G1$ was patterned with a deliberate shift of ∼10 nm towards the D electrode as shown in Fig. 6.1. This allows for the ratio Γ_S/Γ_D of the tunnel rates to be tuned via the gate voltage V_{G1} as illustrated in Fig. 6.9 b. While making V_{G1} more negative increases the height of both tunnel barriers (resulting in a lower device conductance) the effect will be stronger on the D-side barrier which effectively results in an increased coupling symmetry, where $\Gamma_S/\Gamma_D \to 1$. This is clearly visible in the stability diagram, where the observed number of resonance lines with negative slopes increases for $V_{G1} < 0$.

Regarding the coupling strength between the dot and the leads, it is instructive to investigate the Coulomb peaks in more detail. From fitting the peakshape to theory [48] we determine an electron temperature of ∼260 mK. This value is higher than the nominal bath temperature of ∼20 mK. The discrepancy is too high to be accounted for by heating

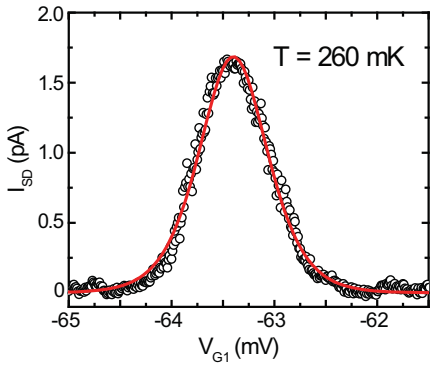

Figure 6.11: Electron temperature. The graph shows a more careful measurement of the Coulomb blockade peak closest to zero gate voltage at a source-drain bias of 40 μV. The red line is a fit to theory in the quantum CB regime [48] which yields an electron temperature of $\sim$260 mK.

due to external noise. The most likely explanation is that the device is in the transition region to the lifetime broadened regime where $k_{\mathrm{B}}T < h\Gamma$ [48]. In this regime, the Coulomb peaks are broadened by the finite tunnel coupling Γ to the source and drain leads rather than temperature [48].

6.4.4 Charge offset stability

One of the most important challenges for future large-scale integration of SET devices is noise due to random *offset charges* [134, 172]. Here, noise refers to intrinsic fluctuations of the current through the device. The offset charges originate from carriers bound to charge traps or impurities in the insulating environment of the device which are close enough to have a finite capacitive coupling C_t to the device. In the case of a quantum dot, the corresponding charge Q_t will cause a change $\delta V_G = Q_t/C_t$ in the effective gate voltage thus shifting the Coulomb blockade thresholds. As a consequence, the device will commonly exhibit noise in the form of random telegraph signals (RTS) [141] where the current fluctuates between two (or more) discrete levels that reflect the discrete charge states of the defect.

Charge offset noise affects the proper operation of many nanoelectronic devices, in particular single electron transistors (SETs) which are used to detect the charge state of a nearby dot [158, 173]. Furthermore, charge noise also presents a challenge for possible quantum computing applications [174].

The effects of individual charge traps on the transport spectroscopy of silicon quantum dots has been investigated by Pierre *et al.* [175] who used a simple capacitive model in order to discriminate the resulting features from other transport resonances. Long-term

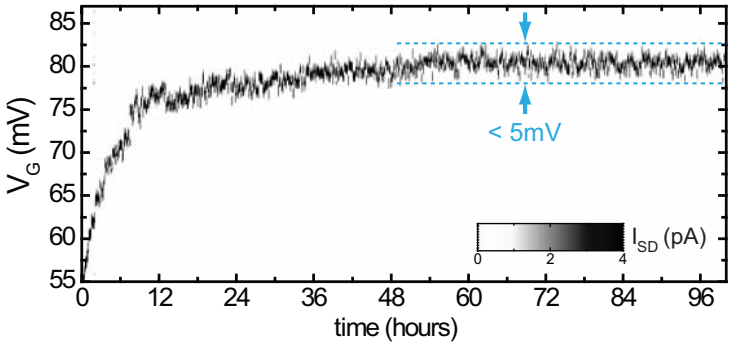

Figure 6.12: Charge offset stability. The graph shows the evolution of a Coulomb peak position in gate space over 4 days. The gate voltage was continuously swept from -60 mV to 140 mV (only the relevant part of the data is shown). After an initial drift the peak position stabilizes around 80 ± 2 mV, yielding a stability of ∼0.01e.

charge offset stability in Si based nanoelectronic devices has been studied by Zimmerman *et al.* [176, 177] who found the stability of SETs patterned on SOI material to be better than 0.01e over a measurement period of several weeks.

Fig. 6.12 illustrates the stability of the Coulomb peak position for our few-donor dot measured over four days. Here, the gate voltage was swept continuously within a fixed 200 mV window. After an initial long-term drift over approx. two days, the peak position stabilizes to within ±2 mV, which translates into a stability of ∼0.01e. These slow initial drifts were generally observed throughout all measurements of the device: whenever the gate voltage was moved over a large range (i.e. several 100 mV), subsequent sweeps at first showed substantial switching noise which then settled on a time scale of 10-20 hours. It should be noted that applying excessive gate voltages to the in-plane gates (resulting in leakage currents of several nA) was found to cause shifts of the charge transitions in the stability diagrams. This is attributed to charge rearrangements in the vicinity of the device which cause a change in the effective gate voltage as discussed above.

Most of the defects that create offset charges are associated with surfaces or material interfaces such as the Si/SiO_2 interface in MOSFET devices [142]. Due to the ∼30 nm epitaxial Si encapsulation layer and the absence of surface gates, detrimental effects arising from surface defects are circumvented in our quantum dot structure. However, we can not rule out the presence of impurities in the substrate surrounding the patterned structure. Based on the very low background doping density[7] of the substrate ($\sim 10^{15}$ cm^{-3}) there are a few possible explanations for the presence of switching noise in our devices. One possibility are additional P dopants in the plane of the device which are an unwanted

[7] The substrate doping corresponds to only ∼1 impurity per $(100\,\text{nm})^3$.

byproduct of the STM-lithography process due to stray desorption. However, the latter can be minimized by careful adjustment of the STM-desorption parameters, leaving room for further optimization in future devices. Another possible explanation is the presence of point defects in the silicon encapsulation layer [178] due to the low growth temperature used.

Gate voltage induced charge noise in P doped silicon has been studied previously by Ferguson *et al.* [179] who found that the current fluctuations in Si SETs arise from the slow ionization of phosphorus donors in the gate electric field. After applying a gate pulse the noise level typically equilibrated over several hours, which is consistent with the findings for our device.

6.4.5 Low-bias excitation spectrum

There are several possible explanations [166] for the great number and small energy separation of the conductance resonances in the stability diagram of Fig. 6.5, both intrinsic to the dot and extrinsic. Determining the origin of such resonances is at the heart of transport spectroscopy for any given quantum dot system.

To investigate the possible causes of the resonances in our structure we have measured stability diagrams at higher resolution around a particular Coulomb transition (near zero gate voltage) as shown in Fig. 6.13. The data reveal a very dense spectrum of resonances with an average spacing on the order of $\sim$100 μeV as illustrated in panel c. The predominance of lines with positive slope again reflects the asymmetric tunnel coupling to the leads as discussed in section 6.4.3. In order to distinguish intrinsic features arising from dot excited states from extrinsic features (such as those related to the DOS in the leads), one generally tries to match up corresponding pairs of resonance lines for positive and negative bias [46] as illustrated in Fig. 2.10 of chapter 2. However, the high density of resonances in conjunction with the coupling asymmetry makes it very difficult to reliably match the corresponding pairs in our case[8].

Considering the small dimensions of the device, the spectrum of observed resonances is surprisingly dense. To elaborate on this, we will briefly review the typical origins [166] of transport resonances in semiconductor quantum dot devices and discuss their applicability to the data of our quantum dot.

[8]While the tunnel coupling becomes more symmetric at the lower end of the gate range (see section 6.4.3), the strongly decreased device conductance leads to a much less well-defined low-bias spectrum thus making it equally difficult to identify excited state pairs.

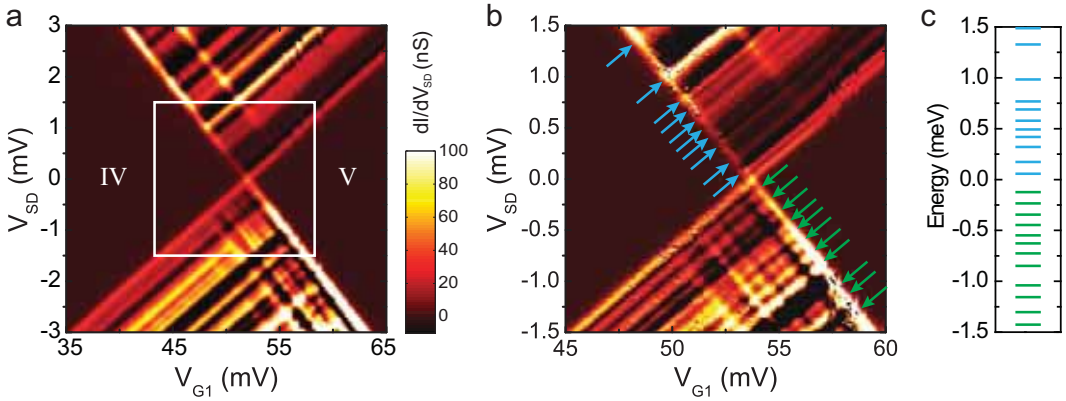

Figure 6.13: Low-energy transport resonances. **a**, A close-up of the charge transition between diamond "IV" and "V" (see Fig. 6.9 a) which is closest to zero gate voltage reveals a dense set of conductance features. The white square indicates the region of the higher-resolution sweep shown in **b**, where an even larger number of transport resonances emerges as indicated by the arrows. **c**, The extracted energy spectrum of the low-bias transport resonances (with pos. slope) yields an average spacing of $\sim$100 μeV.

Orbital excited states

A good approximation for the mean level spacing ΔE in two-dimensional dot structures (where lateral confinement is weaker than in z-direction) is given by [46]

$$\Delta E = \frac{\pi\hbar^2}{g m^* A} \tag{6.1}$$

where m^* is the electron effective mass, A is the effective area of the dot, and g accounts for the spin and valley degeneracies. Despite its simplicity, this approximation has been found to be quite reliable when applied to modulation-doped or inversion layer quantum dots [46, 135]. However, if we consider the appropriate values for our highly doped silicon dot, i.e. a spherically averaged effective mass of 0.28 m_e [35], a dot area of $\sim$20 nm^2 (Fig. 6.3), and full spin and valley degeneracy ($g = 12$), we find an expected level spacing of $\sim$4.5 meV. Evidently, this is more than an order of magnitude larger than the experimental value of Fig. 6.13 c which leads us to rule out orbital excited states as a plausible origin of the observed resonances.

Density of states in the low-dimensional leads

Due to the very narrow width of our source and drain leads ($\sim$5 nm) we expect to observe quasi-1D characteristics resulting from the tight lateral confinement [36]. The patterned width of the leads at the narrowest point is roughly 5 nm (see Fig. 6.1). Confinement along z-direction is even stronger, with a vertical spread of the donor electron density

of ∼2 nm [37] (see section 6.4.2). Both these confinement lengths are comparable to the Fermi wavelength of $2 - 3$ nm in our structures [180] leading to transversal quantization of propagating states. The discrete electronic states of the quantum dot then act as a "spectrometer" which effectively samples the DOS in the electrodes [147] as illustrated in Fig. 6.10.

The spacing between these DOS peaks can again be estimated from a particle-in-a-box approximation. However, for 1D confinement, a hard-wall potential (i.e. infinitely steep potential walls) yields a spectrum where the spacing between successive levels increases steadily, $\Delta E_n \sim n/L^2$ [46], where L is the width of the wire. Such an increasing level spacing is not consistent with the observations for our dot, where the densely spaced resonances are distributed evenly. A constant spacing of energy levels is however generally found for systems with a parabolic confinement potential. The latter is often used as an approximation for quantum dots where the confinement varies over distances of 10s of nanometers, such as top-gated Si MOS structures [181]. The constant level spacing for a harmonic potential is given by [46]

$$\Delta E_{harm} = \frac{\hbar}{g}\sqrt{\frac{8V}{m^*}}\frac{1}{L} \tag{6.2}$$

Here, V is the height of the parabolic potential well which we assume to be on the order of ∼100 meV in agreement with previous studies on tunnel junctions [100]. Using the same values for g and m^* as above for our leads, we obtain an average level spacing of ∼7 meV. Even if we consider the fact that both leads widen to approx. 15 nm further away from the dot (Fig. 6.1 b), the resulting spacing is still more than an order of magnitude too large to account for the observed resonances. Moreover, a harmonic potential does not seem to be a good approximation for the very sharp confinement potential present in our structure (discussed in more detail in section 6.5.2). We conclude that DOS modulations in the quasi-1D leads are unlikely to explain the observed spectrum.

It should also be noted that for Coulomb blockade devices the occurrence of negative differential conductance (NDC) is commonly argued to arise from a modulated DOS in the leads [145, 146]. The argument can be easily understood by considering Fig. 6.10 where the conductance is expected to first increase and then decrease every time a DOS peak passes the dot level. We do indeed observe NDC in our transport data (Fig. 6.13). However, other mechanisms can also lead to NDC in quantum dot devices such as energy-dependent tunneling [182]. This is caused by a varying tunnel rate between the leads and the dot for different discrete dot states. Qualitatively, if an excited state with a lower

tunnel rate comes into the bias window the sequential tunneling current through the dot will decrease due to the longer lifetime of electrons in this state.

Phonon absorption and emission

For the sake of completeness we include confined lattice vibrations in this discussion since they have been found to cause evenly spaced excitation spectra at comparable energy scales in nanowire [162] and carbon nanotube [183] quantum dots. Phonon emission and absorption can enhance current through a dot by offering additional inelastic tunneling processes [166]. However, a discrete phonon spectrum can only exist in heterostructures where material interfaces or sharp changes of material composition are present. This is the case for structures such as free-standing Si nanowires [162], carbon nanotubes [183], or molecular transistors in the Coulomb blockaded regime [169, 184]. By contrast, our structures inherently do not contain any material interfaces. The only modulated quantity is the P doping density. The P donors occupy substitutional Si lattice sites within the encapsulated structure. With Si and P being neighbors in the periodic table of elements, the relative difference in atomic weight (≈ 28, and ≈ 31, respectively) is very small.
In summary, it does not seem plausible that our highly homogeneous Si:P structures present a phonon cavity, so that a discrete spectrum of confined phonons can be ruled out as an explanation for the transport data.

Fluctuations of the local density-of-states

Another possible explanation for the observed spectrum is disorder in the leads, which may cause irregular fluctuations in the local density-of-states (LDOS) [185, 186]. As discussed previously (see Fig. 6.10), a modulated density-of-states can result in peaks in the differential conductance. The corresponding resonances can be very dense and have been observed [187] to occur on an energy scale comparable to the $100\,\mu$eV we observe.
The irregular fine structure of the LDOS arises from quantum interference of elastically scattered quasiparticles diffusing coherently within a length scale related to their lifetime at a particular energy E. In the case of an electron tunneling from the source to the dot these interfering quasiparticles are, in fact, holes at $E < \mu_S$ left behind in the emitting reservoir. Being in a nonequilibrium state, the holes then "float up" towards the Fermi level (due to inelastic collisions between electrons) and thus have a finite lifetime [187].
Disorder is inherent to our doped Si:P structures [38] and arises from the random distribution of the donor atoms within the doping plane after incorporation [71]. The influence

of disorder can be described using the dimensionless parameter $k_{\mathrm{F}}l$, where $k_{\mathrm{F}}l \gg 1$ corresponds to weak disorder [188]. Here, l is the electron mean free path and k_{F} is the Fermi wave vector. For δ-doped silicon the latter is given by $\sqrt{4\pi n_s/g}$, where n_s is the sheet doping density and $g = g_s g_v$ accounts for the spin and valley degeneracy. A very high doping density should thus correspond to weak disorder. To estimate k_{F} for our system we assume $g_s = 2$ and a four-fold degeneracy of the Δ valleys, $g_v = 4$ (see section 2.2). With a mean free path on the order of $\sim 5 - 10\,\mathrm{nm}$ [38] we then obtain a disorder parameter $k_{\mathrm{F}}l \gtrsim 10 \gg 10$ and thus conclude that our highly doped Si:P structures are in the limit of weak disorder. This may initially seem surprising, but is ultimately a result of a more efficient screening (of the disordered impurity potentials) for higher charge densities. It therefore seems questionable whether the weak disorder in our leads could result in such prominent resonances in our structure.

The effects of disorder-induced LDOS fluctuations have been studied experimentally in detail in μm-size vertical GaAs double-barrier structures [187] where they were found to cause irregular peaks in the differential conductance. More recently, Pierre *et al.* [146] investigated transport through single impurities in silicon MOSFETs with doping densities $\leq 10^{20}\,\mathrm{m}^{-3}$. They observed transport resonances with an average spacing on the order of $\sim 1\,\mathrm{meV}$ which they attributed to LDOS fluctuations in their $\sim 50\,\mathrm{nm}$ doped leads. With our significantly thinner leads ($\sim 5\,\mathrm{nm}$) and much higher doping density (corresponding to $\sim 10^{27}\,\mathrm{m}^{-3}$) we would expect the resulting level spacing to be even larger in our case, not smaller as observed.

In summary, we cannot completely rule out resonances arising from disorder effects, but with our very highly doped narrow leads we do not consider that these can account for the observed transport spectrum.

6.5 Valley-splitting in a few-electron Si:P quantum dot

An alternative explanation for the observed transport spectrum is to consider the unusual band-structure of highly doped δ-layers of phosphorus in silicon. The critical feature is the near degeneracy of four of the conduction band minima or *valleys* in the band structure (see chapter 2) and how this is affected by the strong lateral and vertical confinement. The phosphorus δ-layer that constitutes the conducting regions of the device is a two-dimensional sheet of charge, with a Fermi surface as shown in Fig. 6.14 b. Two valleys exist at the Γ-point in the center of the first Brillouin zone. These two out-of-plane valleys, Γ_1 and Γ_2, are lowest in energy and are known to be split by the strong quantum

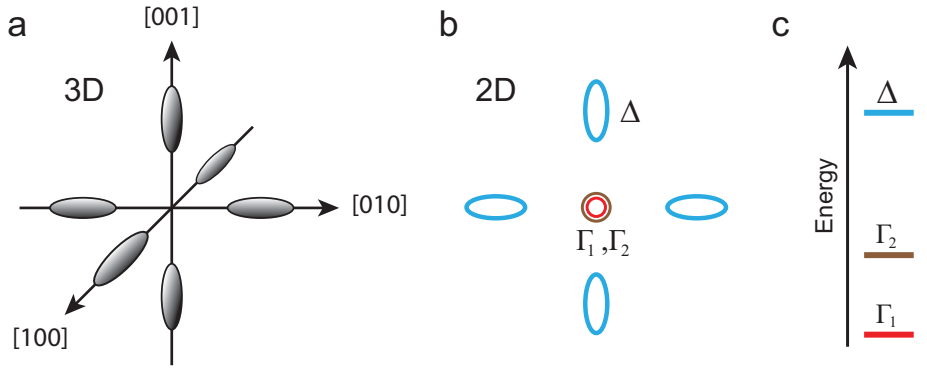

Figure 6.14: Valley degeneracy in silicon. **a**, The 6 degenerate valleys within the 1st Brillouin zone of bulk silicon. **b**, In δ-doped Si:P layers, where the electrons are confined along the vertical direction, the resulting 2D bandstructure is a projection of the 3D case onto a plane perpendicular to the confinement direction. This results in 4 (nearly) degenerate Δ valleys and two non-degenerate valleys Γ_1 and Γ_2 which are lower in energy (**c**).

confinement in z-direction, perpendicular to the doping plane [37, 35]. In addition, there are four Δ-valleys, two each in the x and y directions, which are usually degenerate in 2D devices. However, since our quantum dot device is also confined *laterally* on the nm-scale it is important to consider if any splitting of this degeneracy can give rise to the resonances observed in Fig. 6.13.

6.5.1 Valley-splitting in the literature

In contrast to material systems like GaAs heterostructures, the presence of 6 degenerate valleys in the band structure of bulk silicon presents a challenge in understanding and controlling the transport properties of silicon-based nanostructures. This is particularly true for spin-based quantum computational applications, since valley splitting is often found to be of a similar order of magnitude, 0.1 - 1 meV [189, 31], as the Zeeman splitting between different spin states. In order to avoid valley states competing with spin states for prominence in such devices it is generally favorable to have large valley splitting [189]. Furthermore, valley degeneracies present a possible source of decoherence for quantum computation applications [21].

Ohkawa and Uemura [190] and later Sham and Nakayama [191] were among the first to extend the effective-mass theory of Luttinger and Kohn [32] by considering the multivalley structure of Si. Experimentally, valley-splitting was first observed in the Shubnikov-de Haas oscillations of Si MOS structures in strong magnetic fields [192, 193]. Due to its profound impact on the transport characteristics of silicon nanostructures, valley-splitting has received a renewed interest over the last decade, both theoretically [31, 194, 195, 196]

and experimentally [189, 197]. The majority of this work has been focused on quantum wells in Si/SiGe heterostructures [31, 189] or Si/SiO_2 MOSFETs [197] where carriers are only confined in one direction. Boykin *et al.* [194] have performed atomistic calculations for Si/SiGe quantum wells and find a valley splitting on the order of $10\,\mu$eV to 1 meV which oscillates and decays with the quantum well width. Goswami *et al.* [189] were able to control the valley splitting of the lowest (Γ) subband by applying electric and magnetic fields to a quantum point contact in a stepped Si/SiGe heterostructure.

The impact of valley splitting on the spin filling of silicon quantum dots has been highlighted theoretically by Hada and Eto [198] as well as experimentally by Lim *et al.* [163] and Lansbergen *et al.* [199]. The need for proper control over valley splitting in silicon based quantum information processing schemes was emphasized by the theoretical work of Koiller *et al.* [21] who calculated how inter-valley electronic interference results in strong oscillations in the exchange coupling between electronic donor states. This in turn may present a challenge for donor-based quantum computer architectures [14, 17].

Qian *et al.* [35] have used both effective mass approximations as well as density functional theory (DFT) to calculate the band structure for phosphorus δ-doped silicon at a P coverage of 1/4 ML. They found a Fermi level about 100 meV below the bulk silicon conduction band minimum with 6 filled subbands: two Γ-subbands which are split by $\sim$20 meV and four degenerate Δ-subbands. These are located at energies of -370 meV (Γ_1), -350 meV (Γ_2), and -210 meV (Δ) below the bulk Si conduction band edge (see Fig. 2.7 a in chapter 2). Expanding on these results Carter *et al.* [37] performed further DFT calculations for δ-doped Si at several P doping densities, also considering some effects of doping disorder. In particular, they found that the Γ_1-Γ_2 splitting is significantly different for the ordered ($\sim$120 meV) and disordered case ($\sim$60 meV), respectively. Generally, DFT is a powerful tool to describe ordered periodic systems. However, due to the need to represent the modeled structure by periodic supercells of limited size[9] a full DFT description is less suitable for disordered or low-symmetry systems such as quantum dots. As an alternative, Friesen *et al.* [31] have developed an effective mass formalism to calculate valley splitting in quantum well structures. Their theory provides comparatively simple analytical results for several device geometries (such as quantum wells) which are found to be in excellent agreement with (more complex and computationally intensive) atomistic calculations. An enhancement of this theory will be presented in the next section which focuses on the calculation of valley excited states in our strongly confined silicon quantum dot.

[9] The size of the supercells is limited by finite computational resources.

6.5.2 Effective-mass modeling of the excitation spectrum

In collaboration with Prof. Mark Eriksson and Prof. Mark Friesen at the University of Madison-Wisconsin (USA) we have performed a numerical analysis of the many-body states in the few-electron quantum dot presented in this chapter. The numerical calculations were carried out by Mark Friesen[10]. In the following section we summarize the basic concepts[11] of this modeling approach to give a description of the observed transport resonances on the scale of $\sim 100\mu$eV (Fig. 6.13) as well as on the scale of $\sim 1-10\,$meV (Fig. 6.5). The results of this extensive analysis are published in ref. [201].

Low-bias regime: valley states

We have performed a numerical analysis of the many-body states in our few-donor quantum dot using effective mass theory. As discussed in section 6.3, the quantum dot is defined by a region in Si which is P-doped at a sheet density of ∼0.09 monolayers. Since our effective-mass calculations use the energy splitting between the Γ_1 and Γ_2 subbands of δ-doped Si as an input parameter, we use the published value which is closest to the donor density found for our dot structures, namely 0.125 ML [37]. While this does not exactly coincide with the peak value of 0.09 ML derived from our array experiments, it is still well within the variance of the experimental doping density (see Appendix A.1). Both values are substantially above the metal-insulator transition (MIT) [202, 203]. This means that the separation between P atoms in the quantum dot is smaller than the effective Bohr radius $a_B \approx 2.5\,$nm in silicon [151]. The electrons are therefore delocalized across the entire dot and it is justified to use a *jellium* approximation for the donor distribution where the positive charge of the ionized P donors in the dot is assumed to be homogeneously distributed over the entire area of the dot. Furthermore, due to the planar nature of the device, we will treat the confinement in vertical and lateral direction separately:

$$V(\mathbf{r}) = V(z) + V(x,y) \tag{6.3}$$

This approximation results in wavefunctions $\Psi(\mathbf{r}) = \Psi(z)\Psi(x,y)$. We thus represent the dot as a two-dimensional jellium with charge density $\sigma = 0.135\,\mathrm{C/m^2}$ corresponding to a 0.125 ML P coverage within the dot. To simplify the calculation for the lateral part, we assume the dot to be circularly symmetric, i.e. $V(x,y) = V(r)$ as illustrated in Fig.

[10] These calculations were carried out during several sabbatical visits of Prof. Friesen to UNSW between 2008 and 2010

[11] For a more detailed description of the computational methods, the reader is referred to refs. [31, 200].

6.15 b. A circular dot seems plausible as a first approximation considering the shape of the P incorporation area in Fig. 6.3. We adopt an anisotropic effective mass tensor, with $m_t = 0.21\, m_0$ and $m_l = 0.95\, m_0$, based on DFT calculations of δ-doped Si:P [35].

The goal is to self-consistently calculate the confinement potential and the charge distribution and subsequently solve for the eigenfunctions of an effective-mass Hamiltonian. Since the confinement potential is separable, this is achieved in two steps: First, we solve for the vertical component by considering a 2D sheet of charge. We then solve the lateral part of the effective mass equations which account for the lateral confinement potential. By constructing multi-electron wavefunctions in the Hartree approximation we are then able to compute the energies of the electronic states for different donor and electron numbers.

For brevity, we will only describe the vertical part of the self-consistent calculation[12]. We consider three (partially) filled bands: the Γ_1, Γ_2, and Δ bands. The former two correspond to "even" and "odd" combinations of the z-valleys as described in chapter 2. We use the splitting between Γ_1 and Γ_2 as an input to the calculations. Carter *et al.* [37] have reported values for the Γ_1-Γ_2 splitting in δ-doped Si:P for different sheet doping densities of ordered dopants. For the (more realistic) disordered case they only give the value for 1/4 ML. We thus estimate the corresponding splitting for 0.125 ML P density by scaling the 1/4 ML value in the same way as in the ordered case, as illustrated in Fig. 6.15 a.

For notational simplicity we will limit ourselves to a single Γ band. Extending the equations to the case of separate Γ_1 and Γ_2 bands, which were both considered for the actual calculations, is straightforward. In the Hartree approximation, the 1D charge density along the z-direction is given by $\rho = \rho_i + \rho_\Gamma + \rho_\Delta$, where the ionic and electron contributions are defined as

$$\rho_i(z) = \sigma\delta(z) \tag{6.4}$$

$$\rho_\Gamma(z) = -\sigma\beta_\Gamma F_\Gamma^2(z) \tag{6.5}$$

$$\rho_\Delta(z) = -\sigma\beta_\Delta F_\Delta^2(z) \tag{6.6}$$

where σ is the 2D charge density, $\delta(z)$ is the Dirac delta function and β_Γ and β_Δ are the filling fractions of the two respective bands, normalized to $\beta_\Gamma + \beta_\Delta = 1$. The corresponding envelope functions F_Γ and F_Δ are normalized to $\int F_\gamma^2 dz = 1$, where $\gamma = \Gamma, \Delta$ is the band index. The electrostatic potentials arising from eqs. (6.4)-(6.6) are calculated from

[12] The calculation of the horizontal component uses a similar approach [200].

Poisson's equation:

$$\frac{d^2V(z)}{dz^2} = -\frac{\rho(z)}{\epsilon} \tag{6.7}$$

where $\epsilon = \epsilon_{\mathrm{Si}}\epsilon_0$ is the permittivity. The envelope functions are then obtained by solving Schrödinger-like effective mass equations:

$$E_\Gamma F_\Gamma(z) = \left[-\frac{\hbar^2}{2m_l}\frac{d^2}{dr^2} + V(z)\right] F_\Gamma(z) \tag{6.8}$$

$$E_\Delta F_\Delta(z) = \left[-\frac{\hbar^2}{2m_t}\frac{d^2}{dr^2} + V(z)\right] F_\Delta(z) \tag{6.9}$$

which are coupled via the potential $V = V_i + V_\Gamma + V_\Delta$. Solutions for the electrostatic and envelope function equations must be obtained self-consistently. One generally starts with a "guess" for the initial wavefunctions, which in our case have a Gaussian form:

$$F_\gamma(z) = \left(\frac{2}{\pi a_\gamma^2}\right)^{1/4} e^{-(z/a_\gamma)^2} \tag{6.10}$$

The self-consistent loop is then performed numerically and iterated as follows[13]:

(i) Provide a Gaussian estimate for the Γ and Δ single electron wavefunctions in iteration α,

(ii) calculate the corresponding electrostatic potential using a Poisson solver,

(iii) incorporate the potential into a finite element Schrödinger solver and compute the corresponding eigenfunctions,

(iv) fit the eigenfunctions $F_\Gamma(z)$ and $F_\Delta(z)$ to Gaussian forms which will be used in iteration $\alpha + 1$,

(v) repeat until convergence is achieved, i.e. until the charge density does not change anymore from one iteration to the next.

The lateral part is again treated self-consistently in a similar way [201] solving for the envelope functions $F_\gamma(x, y)$. For the Δ band two equations $F_{\Delta_x}(x, y)$ and $F_{\Delta_y}(x, y)$ must be considered to account for the anisotropy of the effective mass. Due to the circular symmetry $F_{\Delta_x}(x, y) = F_{\Delta_y}(y, x)$.

The results of the full calculations for a dot with 7 P donors and 7 electrons are displayed in Fig. 6.15. The dot radius (i.e. the radius of the jellium of *positive* charge) is calculated

[13] We benchmarked our approach by reproducing the 1D donor electron density (in z-direction) for a δ-doped layer reported by Carter *et al.* [37]

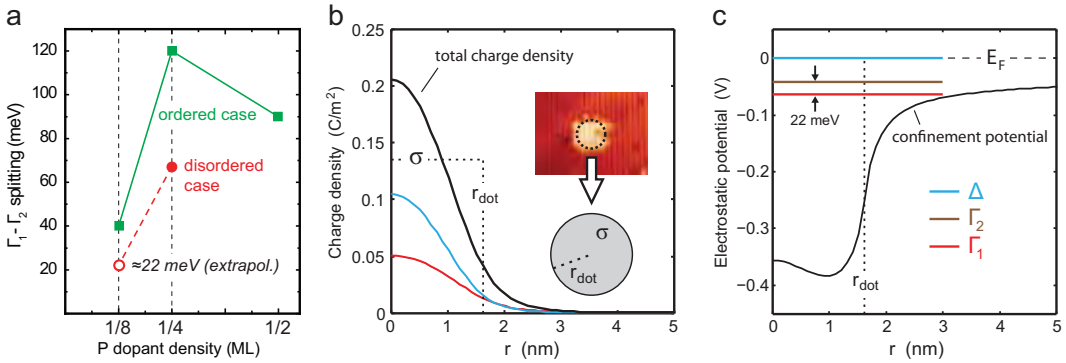

Figure 6.15: Self-consistent modeling of dot states. **a**, The graph illustrates how the Γ_1-Γ_2 splitting of ∼22 meV shown in **c** is estimated from the values reported by Carter *et al.* (solid symbols) [37] by simply scaling the value for the disordered case. **b**, The dot is modeled in a 2D jellium approximation where the positive charge is assumed to be homogeneously spread over a disk of radius r_{dot} as illustrated in the inset. The assumed sheet charge density $\sigma \approx 0.135\,\mathrm{C/m^2}$ corresponds to a 0.125 ML P doping density and r_{dot} is given by the number of P donors. The self-consistent calculation yields the charge density as well as the energy of three bound subbands, Γ_1, Γ_2, and Δ as shown in **c**. The confinement potential has a maximum slope of $\sim 1\,\mathrm{eV/nm}$. All results shown are for 7 donors on the dot ($r_{dot} \approx 1.6\,\mathrm{nm}$).

from the assumed sheet density (0.125 ML) and the number of donors, which in this case yields $r_{dot} \approx 1.62\,\mathrm{nm}$. The modeled dot is thus slightly smaller in diameter than the desorbed area of the actual device as illustrated in the inset of Fig. 6.15 b. This is consistent with the fact that donor incorporation is unlikely to occur at the very edges of the desorbed area as discussed previously in section 6.3. In contrast to the continuum of states in a 2D system [35], a discrete set of single particle levels exists in the quantum dot: Γ_1, Γ_2, and 4 degenerate Δ levels. In this context we will also refer to the multitude of Δ-subbands as the Δ-*shell*[14]. By definition, the Fermi level for the dot coincides with the highest of the three filled (or partially filled) levels. The corresponding charge distributions for the different bands are shown in Fig. 6.15 b. The electronic charge spreads out substantially beyond the edge of the "jellium disk" which again justifies the assumed "seam" of charge around the doped structure for the capacitance calculations discussed in section 6.4.2. Interestingly, the dimensions considered there (dot "diameter" of 5.5 to 9.5 nm) are consistent with the calculated lateral spread of the electron density (roughly 6 nm) in Fig. 6.15 b. The steep slope of the charge density curve reflects the small screening length in our structure which is on the order of 1 nm.

[14]This expression is commonly used in quantum dot terminology [24] in reference to atomic physics.

Valley splitting of the Δ subbands

The remaining 4-fold valley degeneracy within the Δ-shell is lifted by the steep lateral confinement which has a maximum slope of ∼1 eV/nm (Fig. 6.15 c). The valley splitting is calculated using a perturbative approach [31] as discussed in chapter 2. Here we assume that the perturbation is given by the self-consistent Hartree potential $V(x, y)$ as calculated above.

The full effective mass wavefunctions within the Δ band of our silicon quantum dot can be expressed as [31]

$$\Psi(\mathbf{r}) = \sum_{\xi=\pm x,\pm y} \alpha_\xi e^{ik_\xi|\xi|} u_{k_\xi}(\mathbf{r}) F_{\Delta_\xi}(x, y) F_\Delta(z) \tag{6.11}$$

The summation is over all 4 Δ valleys (see Fig. 6.16 a) where $e^{ik_\xi\xi}u_{k_\xi}(\mathbf{r})$ are Bloch functions and $k_{\pm\xi} = \pm k_0\hat{x}, \pm k_0\hat{y}$ represent the conduction band minima. The coefficients α_ξ describe the relative phase between the different valley contributions, with $\sum |\alpha_\xi|^2 = 1$. The lateral effective mass Schrödinger equation can then be written as:

$$\begin{pmatrix} E^{(0)} & \Delta_{11} & \Delta_{12} & \Delta_{13} \\ \Delta_{11}^* & E^{(0)} & \Delta_{22} & \Delta_{23} \\ \Delta_{12}^* & \Delta_{22}^* & E^{(0)} & \Delta_{33} \\ \Delta_{13}^* & \Delta_{23}^* & \Delta_{33}^* & E^{(0)} \end{pmatrix} \begin{pmatrix} \alpha_{-x} \\ \alpha_{+x} \\ \alpha_{-y} \\ \alpha_{+y} \end{pmatrix} = E \begin{pmatrix} \alpha_{-x} \\ \alpha_{+x} \\ \alpha_{-y} \\ \alpha_{+y} \end{pmatrix} \tag{6.12}$$

Diagonalizing eq. (6.12) gives the first order energy eigenvalues E_i. The off-diagonal elements[15] are the valley splitting terms, i.e. they represent the first order corrections to the unperturbed energy eigenvalues $E^{(0)}$ (see Appendix A.2).

The resulting energy levels are illustrated in Fig. 6.16 b. Here, valley splitting partially lifts the degeneracy of the Δ levels, yielding an energy difference of 0.22 meV and 0.32 meV, respectively. The remaining 2-fold degeneracy of the middle level is a result of the assumed circular symmetry of the dot. In addition, all levels are 2-fold spin-degenerate.

In order to understand what causes the great number of resonances in the stability diagram one must consider the electron occupation of these levels when N electrons are on the dot. For $5 \leq N \leq 12$, additional valence electrons reside in the Δ-shell since Γ_1 and Γ_2 can only each accommodate 2 electrons. This is illustrated for $N = 7$ in Fig. 6.16 c. However, in addition to the ground state, there exist several low-lying excited states and it is these valley excited states which cause the observed transport resonances. Considering

[15] Many of these are identical due to the symmetry of the problem.

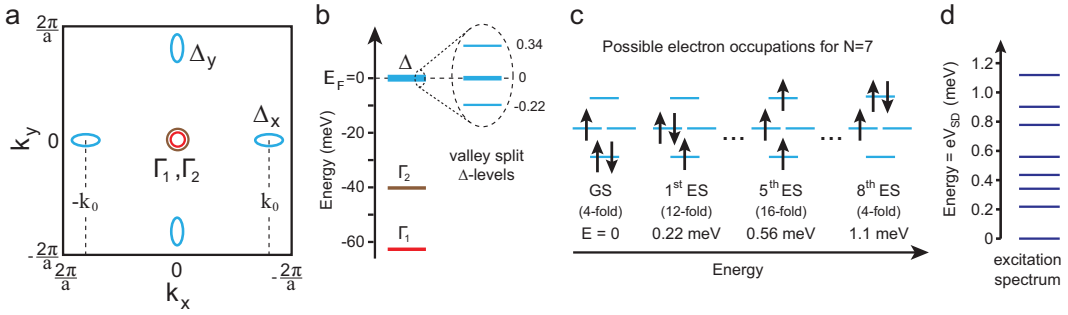

Figure 6.16: Valley splitting of Δ-bands for a circularly symmetric dot. **a**, Two-dimensional projection of the Brillouin zone for planar Si:P. The Γ band in the center of the BZ is lower in energy and split into Γ_1 and Γ_2 due to the tight confinement in z-direction while the 4 Δ bands centered around $\pm k_0\hat{x}, \hat{y}$ remain degenerate. **b**, Discrete set of single particle levels for the quantum dot. The steep lateral confinement causes valley splitting of the Δ subbands on the order of a few 100 μeV. The middle level remains degenerate due to the assumed circular symmetry. All levels are still 2-fold spin degenerate. **c**, For a dot occupation number of $N = 7$, 3 electrons will reside in the closely spaced Δ levels. (The remaining 4 electrons are in the two low-lying Γ-levels.) There are 52 combinatorial electron/spin configurations (some of which are shown along with their respective energy and degeneracy) representing a total of 7 low-lying excited states which will cause transport resonances at the bias voltages V_{SD} as shown in **d**.

all possible electron/spin configurations (many of which are degenerate) one obtains a resonance spectrum as shown in Fig. 6.16 d.

Many of the calculated valley excited states are still highly degenerate as a result of the assumed circular symmetry of the charge distribution. Although the quantum dot is close to symmetric, the statistical nature of the P incorporation within the H-desorbed area (Fig. 6.3) will invariably lead to an asymmetry in the confinement potential. To account for this anisotropy we use a perturbative approach. The latter requires one fitting parameter E_{anis} to account for the splitting between the Δ_x and Δ_y basis states (see Appendix A.2). Fig. 6.17 a illustrates how the remaining degeneracy within the Δ-shell is lifted as the corresponding perturbed eigenstates are expanded in the valley basis states. Fig. 6.17 b shows the resulting spectrum of excited states as a function of the anisotropy parameter. Looking at the observed data in Fig. 6.13 c, we find the best agreement for $E_{anis} \approx 0.2$ meV.

It should be noted that we have computed energy levels for all different combinations of donor and electron numbers on the dot, consistent with the range of possibilities for 6±3 phosphorus dopants. Some of the resulting spectra are shown in the appendix A.3. The best match to the experimental data corresponds to a 7-donor dot at the transition between 7 and 8 electrons. This case is depicted in Fig. 6.17 c which shows the energies of the resonances as they would appear in transport as a function of the source-drain

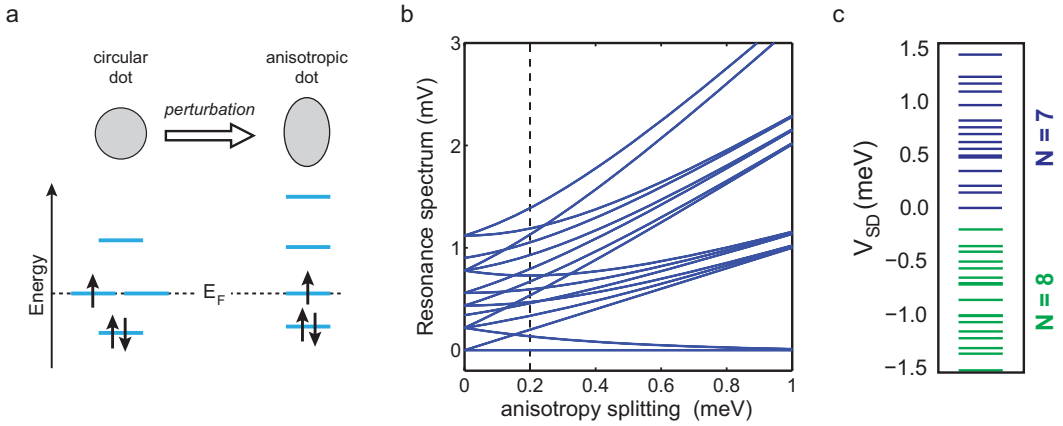

Figure 6.17: Anisotropy of donor distribution. **a**, The remaining degeneracy of the dot levels arises from the assumption of a perfectly circular charge distribution. This degeneracy is lifted when one accounts for a more realistic, slightly asymmetric charge distribution using a perturbative approach characterized by a single anisotropy parameter E_{anis}. The calculated resonance spectrum as a function of E_{anis} is shown in **b**. **c**, The calculated low-bias transport resonances for a 7-donor quantum dot with $N = 7$ and $N = 8$ electrons, respectively, and an anisotropy splitting of 200 μeV. While the calculated spectrum is not expected to match the experimental one (Fig. 6.13 c), it does reproduce the characteristic pattern as well as the average spacing well. The presence of several closely spaced lines in the calculated spectrum also explains the experimentally observed variation of amplitudes for different resonances.

voltage V_{SD}. The resonances at $V_{SD} > 0$ correspond to 7-electron excited states while those at $V_{SD} < 0$ correspond to 8-electron excited states. It should be emphasized that we do not expect the excited states in Fig. 6.17 c to *exactly* match the energies of those in Fig. 6.13 c, because the precise donor positions are both unknown and not included in a jellium calculation. We do, however, find that the calculation reproduces the density of levels, the typical spacing between those levels, and the characteristic fluctuations in that spacing. Particularly closely spaced levels should appear as brighter lines in the data, and such variation in brightness from level to level is indeed observed in the experimental data of Fig. 6.13 b.

The occupation of the Δ-shell provides a natural explanation for the experimentally observed closely spaced resonances. It should be highlighted, though, that there are conduction resonances also at higher energies well beyond the 1.5 meV shown here as is evident from Fig. 6.5. These cannot be explained by the finite number of many-particle states in the Δ-manifold alone. In order to understand these additional resonances it is necessary to extend the model derived above to include the source and drain electrodes.

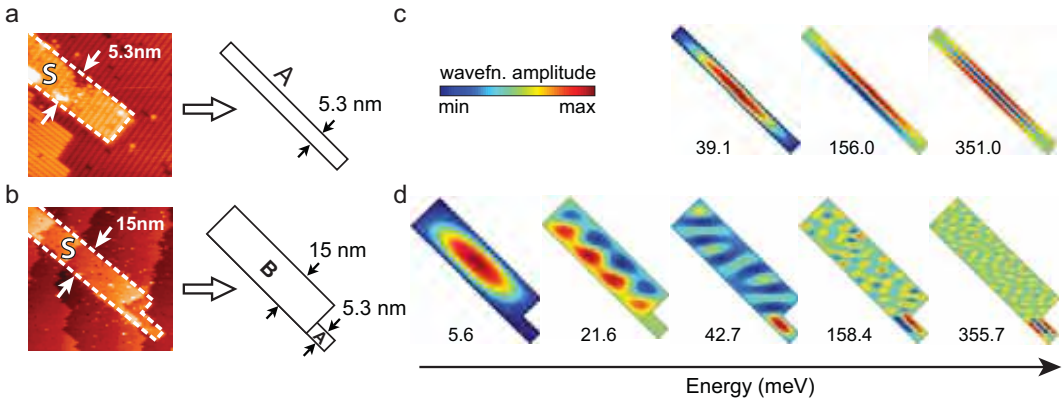

Figure 6.18: Eigenstates for a realistic lead geometry., Using a numerical Schrödinger solver, the electronic eigenstates were calculated for two geometries, representing the narrowest (5.3 nm wide) part at the very tip of the source electrode (**a**) as well as the more realistic geometry including the 15 nm wide part of the lead as illustrated in **b**. **c**, Resulting eigenstates for the Δ_x band with the lead oriented at 45° with respect to the ⟨100⟩ direction. **d**, Corresponding eigenstates are observed for both geometries in the narrow part of the lead at corresponding energy scales. However, not all wavefunctions (like the ones at 5.6 meV and 21.6 meV) of the realistic structure enter the narrow tip (region "A") of the leads. (Note that many intermediate eigenstates are not shown.)

High-bias regime: Modulated DOS in quasi-1D leads

As discussed in section 6.4.5, local peaks in the density of states (DOS) in the leads have been found to contribute to resonances in the conductance of various quantum dot structures [146, 204, 205, 163]. The narrow source and drain leads (Fig. 6.3) present quasi one-dimensional regions where the density of states is expected to have sharp maxima as depicted in Fig. 6.10 a. Such "kinks" in the DOS are commonly referred to as van Hove singularities. The energy spacing between these is determined by the width of the leads. For our ~ 5 nm wide leads, a simple particle-in-a-box estimate yields a spacing > 10 meV so that the van Hove singularities in the narrow part of the leads cannot explain the many resonances at bias voltages > 1.5 mV.

However, the STM-patterned leads are actually wider than 5 nm over most of their length (see Fig. 6.1 and the close-ups in Fig. 6.18 a,b), and thus may well exhibit van Hove singularities that are more closely spaced than those in the narrow tip of the leads. It is therefore useful to calculate the DOS in the leads to determine whether they contribute to the resonance spectrum. Because of their large size as well as the very high density of electrons, the self-consistent many-body method used to treat the quantum dot cannot be applied to the leads. Instead, the leads are analyzed using a single particle calculation, which is sufficient to reveal the number and average spacing of the DOS peaks. This

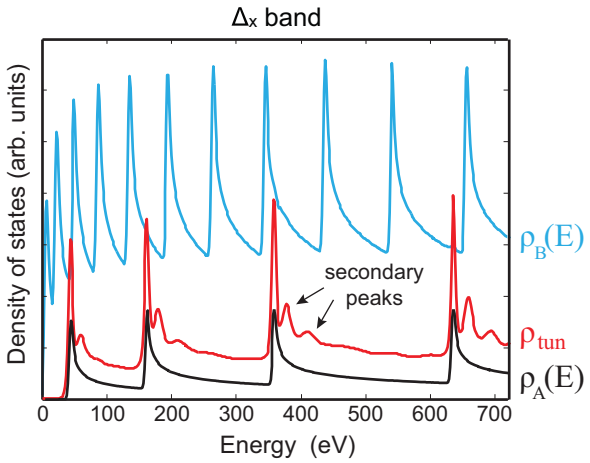

Figure 6.19: Tunneling density of states. The graph shows the calculated DOS for a long wire of width 5.3 nm (black) and 15 nm (blue), respectively. The effective *tunneling* DOS ρ_{tun} (red curve) for the realistic geometry of the source electrode (as depicted in Fig. 6.18 b) contains secondary peaks which cause additional transport resonances. (Only the results for the Δ_x band are shown.)

approach is illustrated in Fig. 6.18. Here, we consider both the very tip (Fig. 6.18 a) as well as the $\sim$ 15 nm wide part of the source lead (Fig. 6.18 b). It is plausible to ignore the wider extensions of the leads since their distance to the tip of the electrode exceeds the phase coherence length found in our structures, $\sim$ 100 nm at temperatures $<$ 1 K [38]. As a result, electrons traveling along the lead will have lost their "phase memory" of quantization and coherence effects over distances exceeding 100 nm.

The DOS is calculated by numerically solving for the eigenstates of a sufficiently long[16] (length$\gg$ width) piece of wire, as shown in the upper row of Fig. 6.18. The corresponding eigenenergies of the transversal modes determine the position of the van Hove singularities. The total DOS is then given by

$$\rho(E) = \sum_j n_j(E) \tag{6.13}$$

where $n_j(E)$ is the DOS for the j^{th} eigenstate including its "tail" which is given by a general analytical formula (see chapter 2).

The black line in Fig. 6.19 depicts the resulting density of states $\rho_A(E)$ computed for a uniform wire of width 5.3 nm (region "A" in Fig. 6.18 a) representing the narrowest part at the tip of the leads. As already expected from the particle-in-a-box estimate, the spacing of the van Hove singularities in this case is too large to explain the experimental data. However, the 15 nm wide region further up the source lead produces many more

[16] For the calculations, both geometries were assumed to be 300 nm long.

singularities $\rho_B(E)$ (shown by the blue line), which are much more closely spaced. For the realistic structure shown in Fig. 6.18 b it is thus important to ask whether any of the van Hove singularities of region "B" contribute to the local density of states in region "A" at the tip of the lead. Panel d in Fig. 6.18 shows several calculated wavefunctions for the lead geometry along with their respective energies. Some of these wavefunctions have almost no weight at the tip of the lead and will therefore not contribute to the density of states, but many of them do. We can thus approximately identify the effective *tunneling* DOS ρ_{tun} at the tip of the source lead by multiplying the density for each eigenstate by its fractional occupation f_j in the narrow region "A":

$$\rho_{\mathrm{tun}}(E) = \sum_j f_j n_j(E) \tag{6.14}$$

where

$$f_j = \frac{\int_A \Psi^2 dr}{\int_{A+B} \Psi^2 dr} \tag{6.15}$$

The resulting tunneling DOS contains many secondary peaks as shown for the Δ_x subband in Fig. 6.19.

The total DOS is then obtained by summing over the contributions from each subband. The slight misorientation of the leads from the crystallographic $[1\bar{1}0]$ axis spreads out the peaks arising from the different subbands due to the anisotropy of the effective mass. This in turn further increases the number of peaks in the total tunneling DOS, which shows an average peak spacing $< 10\,\mathrm{meV}$ as depicted in Fig. 6.20. Transport resonances will occur every time the manifold of dot levels aligns with one of the DOS peaks as illustrated in Fig. 6.10. The realistic lead geometry thus provides an explanation for the large number of resonances extending out to $\pm 50\,\mathrm{meV}$ in Fig. 6.5.

In summary, valley splitting of electronic states in the quantum dot in combination with confinement effects in the narrow leads provide a plausible and consistent explanation for the observed resonance spectrum. It should be noted however, that disorder effects are not taken into account in our effective mass approach and we cannot completely rule out the possible contribution of LDOS fluctuations to the measured transport resonances.

We do not expect our modeling to match all experimental observations on this device. In particular, the "kinks" in the addition energy (see Fig. 6.6 a) are likely to reflect higher orbital levels arising from the complex charge distribution of the realistic device which is not captured by the simple jellium approximation.

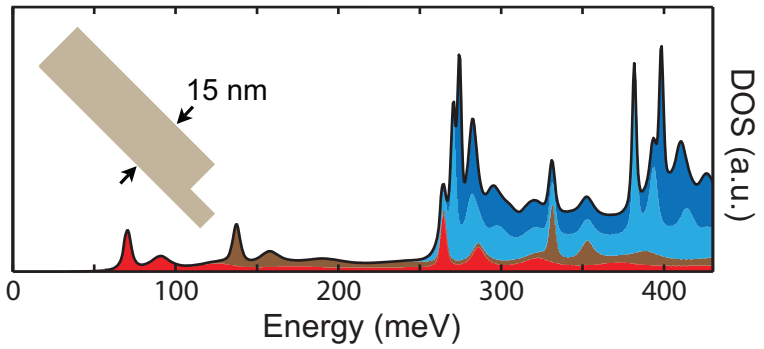

Figure 6.20: Total tunneling density of states., The calculated single-electron tunneling DOS (black curve) for the realistic geometry of the source electrode is summed over the contributions from the Γ_1 (red), Γ_2 (brown), as well as the Δ_x (light blue) and Δ_y (blue) subbands. It shows a large number of peaks with an average spacing $< 10\,\text{meV}$ explaining the observed transport resonances at higher bias voltages. The calculated DOS for each subband are shifted by their respective distance to the Fermi level. From Fig. 6.1 a misalignment of 2.5° from the $\langle 110 \rangle$ direction was estimated for the source lead, resulting in a shift between the peaks for Δ_x and Δ_y, respectively.

6.6 Magnetic field dependence of transport features

Magnetic fields are commonly used to investigate the transport properties of quantum dot devices [45, 46, 152, 166]. The following section gives a summary of the magnetospectroscopy performed on our few-donor quantum dot. Here, the device was measured in a magnetic field B (parallel to the dopant plane) up to 8 T. A parallel field orientation is commonly used for larger two-dimensional quantum dots (with typical diameters on the order of 100 nm) to avoid the effects of an additional magnetic confinement of the electronic wavefunction in the direction perpendicular to the B-field. This magnetic confinement occurs on a characteristic length scale of $l_B \sim \sqrt{\hbar/|eB|}$ [31] which is on the order of ∼10 nm for typical B-field strengths of a few Tesla. This value is indeed much larger than the confinement length scale (∼1 nm) of our donor-based structures so that the additional magnetic confinement can be neglected.

6.6.1 Zeeman shift of a charge transition

Figure 6.21 a shows the same low-bias stability diagram that is depicted in Fig. 6.13, but for several discrete values of the magnetic field B. We find that the charge transition moves towards lower gate voltages V_{G1} as the magnetic field is increased, as indicated by the blue arrows. To quantify this shift we plot the position of the Coulomb peak as a function of B in Fig. 6.21 b. Here, the peak position (V_{G1} ≈73 mV) has shifted compared to panel a (≈52 mV at 0.1 T) as a result of several gate sweeps over a large voltage ranges in between

the two measurements (see section 6.4.4). In Fig. 6.21 b we observe a linear shift of the peak position with B. As discussed in chapter 2, Coulomb peaks occur when the Fermi levels in the leads are aligned with an electrochemical potential μ_N of the dot. The latter can be tuned not only by an electric field (i.e. a gate voltage) but also by a magnetic field via the Zeeman energy $E_Z = \Delta s_z g \mu_B B$ [45]. Here, g is the gyromagnetic or *g-factor* which for electrons in silicon is very close to the free-electron value of $g = 2$ [206] and Δs_z is the total change in spin momentum associated with the transition μ_N. In most cases $\Delta s_z = \pm\frac{1}{2}$, thus reflecting the spin of the "incoming" electron of the charge transition μ_N. Using the appropriate lever arm $\alpha_{G1} \approx 0.10$ at this transition we can convert the observed slope $\Delta V_{G1}/\Delta B \approx -0.67\,\mathrm{mV/T}$ into an energy shift and which yields a g-factor of 2.3 ± 0.3, in reasonable agreement with the expected value of 2. The error bar for the experimental value is due to an uncertainty in both the fitted slope $\Delta V_{G1}(B)$ and the lever arm α_{G1}. Fig. 6.21 c depicts the height of the Coulomb peak as a function of B, showing a significant modulation on a scale of $\sim$2 T. To investigate the origin of this varying peak height we have performed direct magnetospectroscopy of the low-bias spectrum.

6.6.2 B-dependent Coulomb peak height

While the average spacing of the resonance features in Fig. 6.21 a remains roughly the same, changes in the line pattern are visible, both in position as well as intensity. To quantify the changes in the low-bias resonance spectrum we continuously sweep the bias voltage (at a fixed gate voltage) while increasing the magnetic field in small increments. The sweeps were performed separately for $V_{SD} < 0$ and $V_{SD} > 0$, as illustrated in Fig. 6.21 d and e. While V_{G1} is fixed, the position of the coulomb peak will shift down in gate voltage as B is increased. This leads to the observed linear shift of the ground state (GS) line in the magnetospectroscopy plots (indicated by the dashed line in Fig. 6.21 d and e). Importantly, the V_{G1} values for both sweeps ($V_{SD} < 0$ and $V_{SD} > 0$) were chosen so that only features with positive slope appear at that particular gate voltage, as indicated by the two dashed lines in Fig. 6.21 a. This was done to avoid artifacts arising from conductance lines with negative slope in the magnetospectroscopy data: a resonance line with negative slope would appear very similar to a resonance line with positive slope which splits as a function of B.

Apart from minor switching noise[17] (which causes small vertical discontinuities) it is obvious from the data in Fig. 6.21 d and e that most of the resonances move with respect

[17] This is consistent with the $\sim$0.01 e stability of the Coulomb peak position discussed in section 6.12.

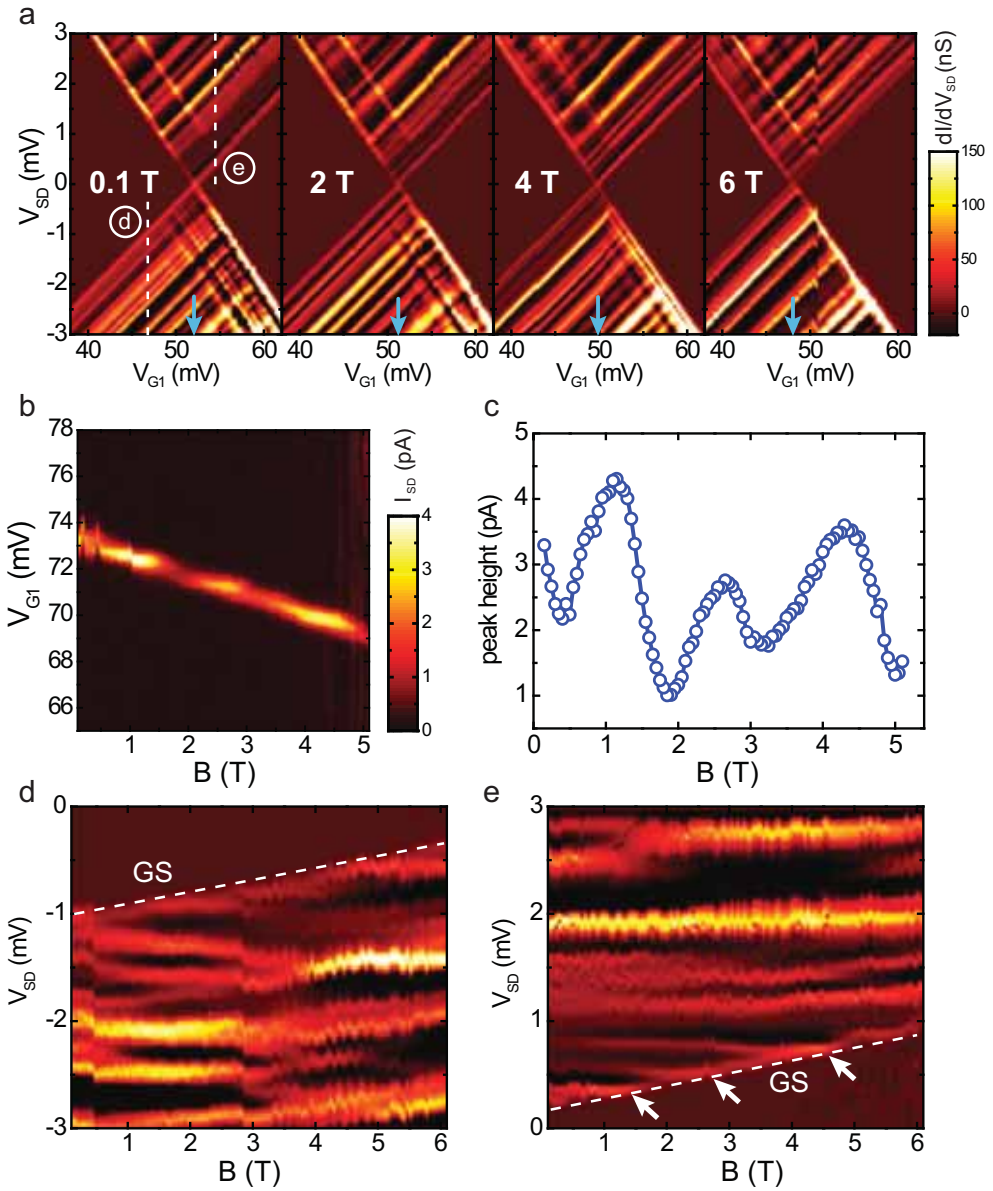

Figure 6.21: Magnetic field dependence. **a**, The charge transition of Fig. 6.13 for different values of the magnetic fields B. The transition shifts towards lower gate voltages, from $\sim$51.5 mV at $B = 0$ to $\sim$48 mV at $B = 6$ T, as indicated by the blue arrows. **b**, The Coulomb peak position shifts linearly in a magnetic field with a slope of -67 mV/T. A clear modulation of the peak height is observed as shown in **c**. Magnetospectroscopy measurements were performed at the gate positions indicated by the dotted lines in **a**. To avoid artifacts arising from resonance features with negative slope as the peak position shifts along the gate axis, the data was taken separately for $V_{SD} < 0$ (**d**) and $V_{SD} > 0$ (**e**), respectively. Most features shift with respect to the ground state (GS), eventually crossing it. These crossings (white arrows) coincide with the local maxima of the B-dependent Coulomb peak height of panel **c**.

to the GS line. Some lines even cross the GS line at the positions indicated in Fig. 6.21 e. These crossings are evidenced by an increase of conductance as both lines overlap. Indeed, the B-positions of the crossings coincide with the local maxima in the Coulomb peak height shown in 6.21 c. We therefore conclude that the observed smooth modulation of the Coulomb peak intensity originates from low-lying transport resonances crossing the GS line. This is in contrast to previous reports on B-dependent Coulomb peak heights in a donor-based quantum dot[18] [115] where the modulations occurred on a similar B-scale of 2 T. Here, the device was measured in a magnetic field perpendicular to the dopant plane and the varying peak height was attributed to a scrambling of the semiclassical electron trajectories in the quantum dot as the magnetic flux $\Phi = B/A$ through the dot area A was increased by multiples of the flux quantum Φ_0. Indeed, a flux quantum for this many-donor quantum dot (with a dot area $A \approx 2100\,\mathrm{nm}^2$) was found to be consistent with the observed B scale of 2 T. By contrast, the measurements on the present device were conducted in a parallel field on a device with a much smaller area resulting in a required B-field scale of several 100 T to change the flux through the dot by Φ_0.

6.6.3 B-field dependence of the low-bias spectrum

While the observed shifts of the resonances give a plausible explanation for the varying Coulomb peak height, the reason for these shifts in the low-bias excitation spectrum is still unknown. To evaluate the B-dependence of Fig. 6.21 d and e it is helpful to compensate for the linear shift of the GS line by skewing the data as shown in the composite plot of Fig. 6.22. Here, the bias voltage has been converted into an energy by multiplying with a geometric factor that accounts for the slopes of the respective diamond edges.

The magnetic field dependence of valley splitting in silicon quantum dots is still an area of ongoing research and the details of the magnetospectroscopy data of our quantum dot device are not yet fully understood. However, we can make several observations which we will briefly compare to results in the literature.

There is a general trend for the lines to shift towards lower energies with increasing field. However, there is a clear difference between the data sets for positive and negative bias: For $V_{SD} > 0$, most lines follow an almost linear trend and very few crossings and splittings are found. By contrast, more splittings are observed for $V_{SD} < 0$ and the lines tend to have a steeper slope. The differences between both spectra may indicate that the resonances are indeed due to dot excited states in which case they would correspond to different dot

[18] These measurements were performed on the many-electron quantum dot presented in chapter 5.

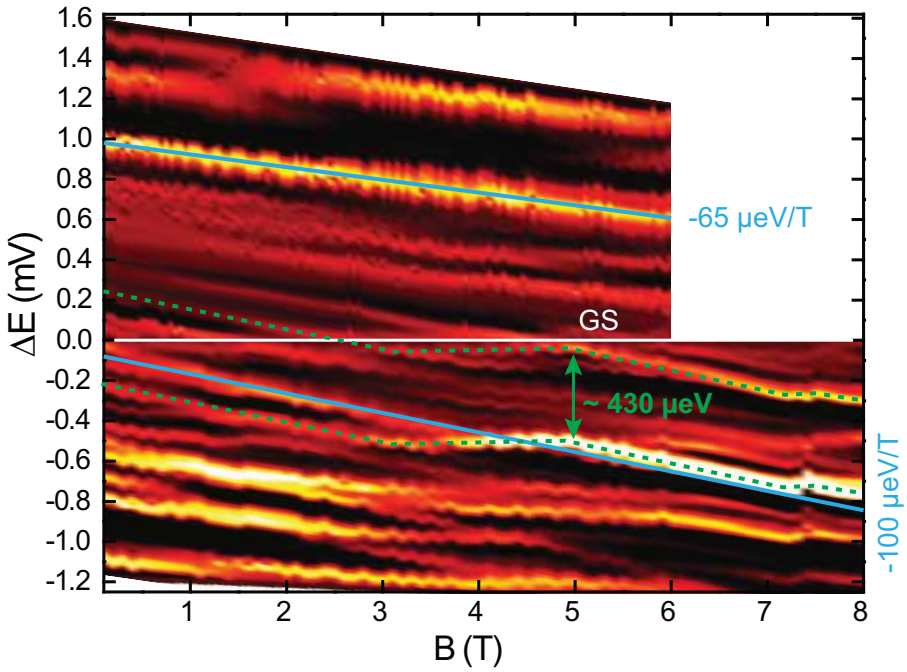

Figure 6.22: Resonance spectrum vs. B. To compensate for the linear shift of the charge transition along the gate axis, the bias spectroscopy data of Fig. 6.21 d and e is skewed. (An extended data set is shown for $V_{SD} < 0$.) Also, the bias voltage is converted into an energy via a geometric scaling factor that accounts for the slopes of the diamond edges. The lines of increased conductance shift down with respect to the (horizontal) GS line, with slopes ranging from $\sim$65 μeV/T to $\sim$100 μeV/T as indicated by the blue lines. Several pairs of lines can be identified which follow the same pattern as a function of B, one of which is highlighted by the dotted green lines. The energy spacing of these lines ($\sim$430 μeV) is likely to reflect the valley splitting of electronic states within the dot.

occupation numbers (since the corresponding lines for $V_{SD} > 0$ and $V_{SD} < 0$ terminate on different Coulomb diamonds as can be seen in Fig. 6.21 a).

In Fig. 6.22 we fit lines to two prominent features (blue lines), the slopes of which are representative for the positive and negative bias data. For $V_{SD} > 0$ we obtain a slope of roughly -65 μeV/T which is very similar to $E_Z = 58\,\mu$eV/T. Möttönen *et al.* [147] recently reported magnetospectroscopy measurements on a silicon MOS quantum dot where resonances with an average spacing of a few 100 μeV were attributed to a modulated DOS in the $\sim$50 nm wide leads. The corresponding resonances were found to shift linearly with respect to the GS line in a magnetic field at a slope of E_Z, resulting from a Zeeman splitting of the DOS for spin-up and spin-down electrons in the leads. From their B-field behavior, they were able to distinguish between DOS resonances and spin-split (orbital) excited states which move at a slope of $2E_Z$. However, the simple model of Möttönen *et al.* does not account for the variation in slopes or the observed crossings/anti-crossings

in our data. Furthermore, we have argued previously (section 6.4.5) that the low-bias resonances of Fig. 6.22 with a spacing on the order of 100 μeV are unlikely to originate from a modulated DOS in our very narrow leads.

For conductance features arising from spin-degenerate excited states we generally expect to observe a linear splitting in a B-field [166] with an increasing spacing given by the Zeeman energy $2|E_Z| \sim 116\,\mu$eV/T. Indeed, the fitted line in the negative bias data of Fig. 6.22 has a slope of approx. -100 μeV/T which is comparable to the expected Zeeman shift. However, while several lines split and merge at various B fields, there is no clear evidence for Zeeman splitting at $B = 0$. This may either be due to the fact that the observed resonances do not arise from dot excited states or (assuming that they are excited states) that these are not spin-degenerate.

There have been some recent reports on the magnetic field dependence of valley splitting, $\Delta E_v(B)$, in silicon devices [189, 207]. Goswami *et al.* [189] studied valley splitting in Si/SiGe heterostructures and found that the splitting ($\sim$1 μeV at $B = 0$) could be tuned by a magnetic field at a rate of $\sim$25 μeV/T. Xiao *et al.* [207] observed a B-dependent splitting between the two Γ-valleys in a few-electron silicon MOS-based quantum dot. Here, the valley splitting was found to increase at a rate of $\sim$37 μeV/T resulting in a linear shift of the valley excited state with respect to the ground state. Both observed slopes are significantly smaller than the values we observe in our data. Moreover, an increasing valley splitting should result in an increasing average spacing of the entire spectrum which we do not observe.

A more careful examination of the data in Fig. 6.22 reveals the presence of several pairs of lines which move parallel throughout the entire B-range of the plot. One of these pairs is indicated by the dotted green lines which are split by $\sim$430 μeV. Interestingly, this splitting is on the same order of magnitude as the calculated valley splitting and may thus be a further indication of the importance of valley splitting in our device.

Furthermore, in Fig. 6.22 we observe several levels crossing (particularly for $V_{SD} < 0$) roughly in the B-field range between $\sim$2.5 T and 5 T. At these B values, the Zeeman splitting is on the order of $\sim$300 to 600 μeV. The crossings may therefore reflect a change in the spin configuration of the different valley states [198].

Calculating the magnetic field dependence of the excitation spectrum for our device was beyond the simple effective mass model presented in section 6.5. It is plausible that the observed B-dependence reflects the atomistic details and the irregular confinement landscape of the actual device.

6.7 Chapter summary

This chapter has shown the experimental realization of a STM-patterned donor-based quantum dot structure in the few-electron regime. From high-resolution STM images and a statistical study, we estimate the dot to contain ∼7 P donors.

Transport spectroscopy at mK-temperatures revealed very stable Coulomb blockade oscillations as well as a surprisingly dense set of well-resolved resonances on the order of 100 μeV. This energy scale is far too small to be explained by simple confinement effects within the nm-scale quantum dot or the quasi-1D leads. Instead, the resonances are attributed to a splitting of the Δ-valleys in the conduction band, resulting from the abrupt lateral confinement potential, which gives rise to a dense set of many-body excited states. This interpretation is supported by extensive effective mass calculations which were performed in collaboration with Prof. M. Eriksson and Prof. M. Friesen at the University of Madison-Wisconsin. While the magnetospectroscopy data of the device is not yet fully understood, it gives further indications for valley splitting in the quantum dot.

The results of this chapter highlight the importance of the valley degree of freedom in ultra-small silicon quantum devices. Classical CMOS miniaturization is beginning to approach the length scales studied here. An understanding of the physics of sharp confinement potentials will therefore be crucial for continued developments in both quantum and classical devices in silicon.

Chapter 7

Transport properties of a single P donor

After demonstrating the fabrication of a donor-based few-electron quantum dot (chapter 6), a successful attempt was made to reach the ultimate scaling limit: a single donor transport device. Whilst our group has previously demonstrated the incorporation of an individual P donor on the Si(100)-2 $\times$ 1 surface by means of STM-lithography [66], being able to pattern exactly one donor at a precisely known position within a functional device is a much more complex task. Indeed, to achieve this in a deterministic way has required a deeper understanding of the adsorption and incorporation mechanism in nm-scale desorbed patches. In particular, the shape and exact size of the sub-nm hydrogen desorbed region for single dopant incorporation prove to be crucial.

In this chapter, we present a statistical study to optimize the patterning parameters for the reliable incorporation of a single P donor. Using a higher PH_3 dosing pressure of 5×10^{-8} mbar to achieve saturation dosing, we find that a patch of 3 adjacent dimers along one dimer row is necessary to incorporate one P atom.

Based on these results, an in-plane gated device was fabricated where exactly one phosphorus atom is placed between the source and drain leads. While there have been a few recent reports on transport through individual impurities in silicon structures, our approach allows for devices with unprecedented control over the number and spatial positioning of the dopant atoms. The latter can be controlled to a lateral accuracy of ± 6 Å. Low-temperature transport measurements reveal a stability diagram with three diamonds (corresponding to the three possible charge states of the donor) and a charging energy

that is in good agreement with the expected value for the bulk case. Furthermore, we observe clear indications for the donor excited states in the co-tunneling spectrum.

7.1 Single donor transport devices in silicon

Miniaturization of the single most important building block of modern silicon based electronic devices – the field-effect transistor (FET) – has advanced to a stage where device performance can depend on the number and the discrete distribution of individual dopants [2], with channel lengths approaching the 10nm-scale [3]. Consequently, being able to control dopant density and distribution on a sub-nm level is a key challenge for further scaling of conventional integrated nanoelectronic devices. The last decade thus has seen an increased interest in the electronic properties of individual impurities in silicon-based devices [208].

To date, there have been several reports on electronic transport through single dopants in silicon devices [146, 165, 209, 210, 211, 212, 213]. These experiments were performed in various FET architectures where the placement of few or single dopant atoms in the transport channel was achieved by either low-energy ion implantation [210, 211, 214] or indiffusion from higher doped contact regions [146, 165, 212, 213].

Ono *et al.* [211] observed conductance modulations at $T > 6\,\mathrm{K}$ in a silicon nanoFET which they attributed to an individual boron acceptor in the transport channel. However, they were unable to determine a charging energy. Sellier *et al.* [209] reported the observation of the D^0 and D^- charge states of a single arsenic donor in a gated silicon nanowire. Due to the high capacitive coupling between donor and gate in their FinFET architecture, they found a binding energy for the ionized D^- state which is drastically higher than the bulk value. They also observed excited state energies lower than the corresponding bulk values due to the Stark effect in the gate electric field. Expanding on these results, Lansbergen and co-workers [165] reported tight binding calculations which are in good agreement with the measured excited state energies. In particular, they observed a confinement transition between the Coulombic donor potential and a quantum well formed at the Si-SiO_2 interface under the gate. Using the same FinFET architecture, the same group have also recently shown transport through a double donor system [215]. Prati *et al.* [213] studied microwave-assisted transport through single As donors in a similar FinFET device. Like Sellier *et al.*, they find a reduced charging energy for D^0 due to the high capacitive coupling between the donor and the gate.

Pierre *et al.* [146] also reported transport through a single As impurity in the channel

of a nanoFET device. They were able to identify donor excited states via co-tunneling features in the D^0 diamond. Calvet and coworkers [212] have investigated the excitation spectrum of individual Pt impurities in a MOSFET channel identifying excited states via their magnetic field dependence. Transport through single phosphorus donors implanted in the channel of a Si nanoFET was reported by Tan *et al.* [210]. Again, a reduced charging energy for the D^0 state (on the order of 30 meV in contrast to 44 meV in bulk Si) was attributed to the strong capacitive coupling to the nearby metallic gates.

In many of the reported single donor transport spectra additional lines *not* arising from donor excited states are attributed to a strongly modulated density-of-states in the leads [146, 165]. The energy spacing of the corresponding resonances is found to be on the order of 1 meV [146] to a few meV [165].

Importantly, all previous devices share one essential drawback: the placement as well as the exact number of impurities in the transport channel is random. This results in many devices being necessary to show the desired result of one dopant in a suitable location. Evidently, such approaches are not suitable for scale-up of donor-based quantum computation architectures which require precise control over the number and location of vast arrays of dopants [14, 17].

7.2 Initial incorporation studies

A statistical study was carried out in co-operation with Dr. J. Miwa and T. Watson, to gain a better understanding of the adsorption and incorporation process in desorbed areas that are only a few lattice sites in size. The procedure is analogous to the incorporation study for the 7 donor device presented in the last chapter (see appendix A.1). Here, we desorb arrays of designated single donor incorporation sites, dose and anneal the surface, and subsequently re-image the array to identify the P related features. An exemplary array is shown in Fig. 7.1 after H-desorption (panel a) and after the dosing and incorporation anneal cycle (panel b). By comparing high-resolution STM images of each array site before and after the incorporation step, we thus obtain quantitative information on the likelihood of incorporating one or more P atoms in a patch of a given size.

Previous theoretical work has shown that a minimum of 3 adjacent dimers are necessary to incorporate one P atom from an adsorbed PH_3 molecule [71, 76]. Since the dissociation and incorporation pathway involves atom movements which exhibit a strong anisotropy on the (2×1)-reconstructed Si(100) surface [216], these 3 dimers should be oriented along one dimer row [71]. For our array study, we thus focus on patches where 3 adjacent dimers

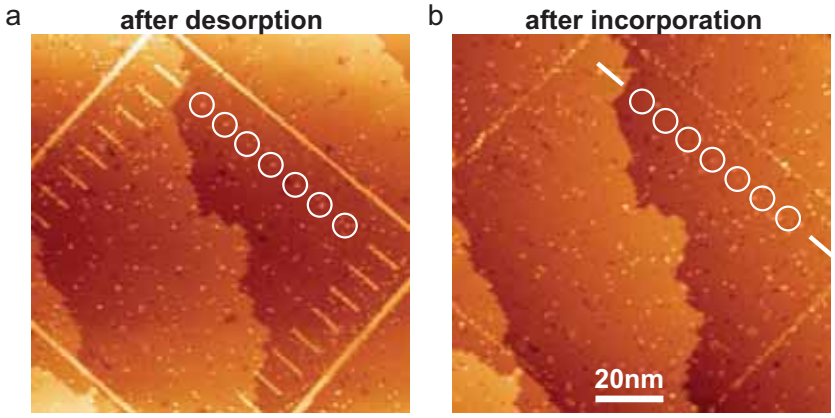

Figure 7.1: Single donor incorporation array. STM images of a 7×10 array of designated single donor incorporation sites after H desorption (**a**) and after the phosphine dosing and anneal cycle (**b**). The array sites in the first line are indicated by white circles. The desorption sites vary in size from approx. 2 to 5 dimers. The outer box and lines serve as registration markers. Several of these arrays were patterned.

have been desorbed along one single dimer row. Hydrogen lithography at this sub-nm scale is quite demanding on the quality of the STM tip and the exact adjustment of the desorption parameters. In particular, the desorption process for these large arrays involves many voltage changes on the STM tip which can affect the tip stability. As a result, the desorbed patches in a given array vary in size from approx. 2 to 5 dimers.

After desorption, every site is imaged to determine the exact number of depassivated Si dangling bonds (DB). The entire array is then dosed with PH_3 at a pressure of 5×10^{-8} mbar for 6 min (corresponding to an exposure of ~14 Langmuir). This value is a factor of 10 higher than the standard dosing conditions used for previous devices. It was chosen to ensure phosphine saturation coverage within the sub-nm desorbed region. After dosing, the sample is annealed to 350°C for 5 s. The short anneal time minimizes thermal drift of the sample and thus makes relocating the array easier for subsequent STM imaging. Fig. 7.2 illustrates some exemplary 3-dimer array sites before (top row) and after the incorporation process (middle). Nearby dimer vacancy (DV) defects can be used as registration markers to identify the precise location of each array site. Importantly, the surrounding hydrogen mask is still intact after the anneal. Incorporation reactions are evidenced by clear changes in the surface morphology as well as the apparent height profiles of the observed features as depicted in the bottom row of Fig. 7.2. A histogram of the observed feature heights after incorporation is shown in Fig. 7.3 a. Two dominant peaks are clearly discernible, roughly located at $\sim 30 \pm 10$ pm and $\sim 65 \pm 15$ pm, respectively. We attribute these peaks to two distinctive surface species: the incorporated Si-P heterodimer and the ejected Si

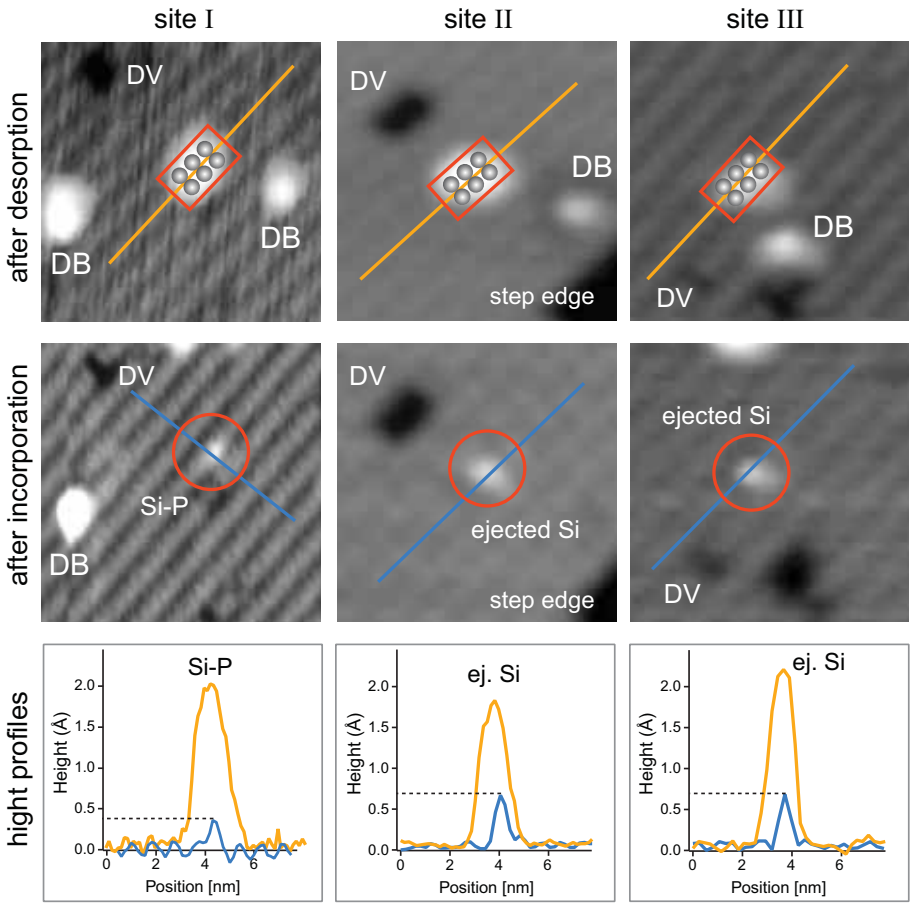

Figure 7.2: 3-dimer incorporation sites. Three exemplary array sites for which the H-desorbed patch is 3 dimers in size (top row). The presence of dimer vacancy (DV) defects facilitates identifying of the array sites after the PH_3 dosing and incorporation anneal cycle (middle row). Some individual dangling bonds (DB) are visible. These are mobile on the terminated Si(100):H surface during the elevated temperatures of the incorporation anneal [71] and therefore may not be present in the images after the anneal. Height profiles with respect to the surrounding hydrogen mask are shown in the bottom row, taken at the positions indicated by lines in the STM images above. (For better visibility of the overlay graphics the STM images are shown in b/w).

adatom, respectively. Examples for both features are shown in Fig. 7.2. The observation of a Si-P heterodimer (site "I") is a direct evidence for successful P incorporation at a given array site. It has been previously found to appear as an asymmetric protrusion $\sim 40\,\mathrm{pm}$ in height [66, 77] which is consistent with our findings. However, in many array sites the heterodimer is not observed since it is masked by the brighter Si adatom (sites "II" and "III" of Fig. 7.2) which is ejected as a result of the incorporation process [76]. While there are several stable configurations for the adatom on the surface [217, 218], we observe the latter predominantly as a bright feature centered on a dimer row. This is consistent with theoretical studies [217, 218] and indicates that the Si adatom resides in the dimer-bridge

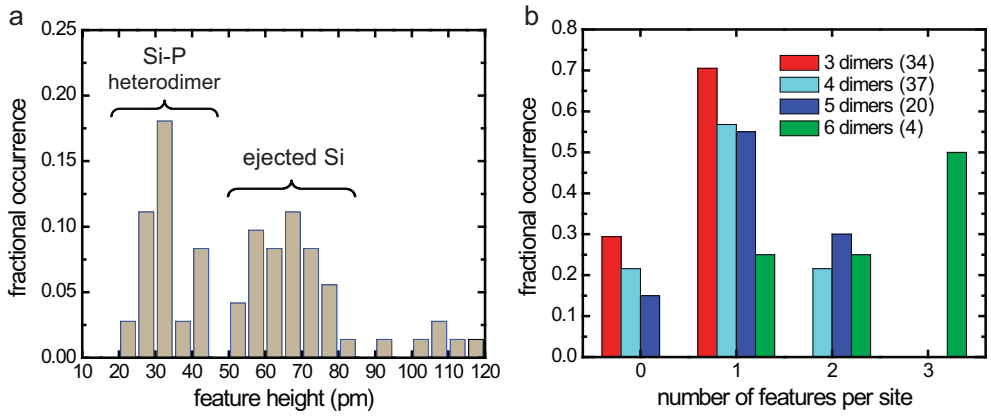

Figure 7.3: Results of statistical study. **a**, Histogram showing the heights (with respect to the surrounding H mask) of the features observed at the array sites after the incorporation cycle. Two peaks are clearly discernible which are attributed to the Si-P heterodimer and the ejected Si adatom, respectively. The few features approx. 100 to 120 pm in height are most likely due to single dangling bonds. **b**, The graph illustrates how the number of P-related features at a given array site after incorporation depends on the size of the initial H-desorbed patches (with the total number for each size shown in brackets). Evidently, a patch of 3 desorbed dimers is favorable for the reliable incorporation of one single P donor, with a success rate of ∼70%.

configuration where it is bound to the two Si atoms of one dimer below (see last panel of Fig. 7.4). In the presence of the surrounding hydrogen it is plausible that this is the energetically favorable position. Some additional features were observed with an apparent height ranging from $\sim 90 - 120$ pm in the histogram of Fig. 7.3 a. This range is broadly consistent with reported values for the (tip voltage dependent) apparent height of dangling bonds on the Si(100):H surface [59, 219]. The corresponding features are therefore most likely due to individual dangling bonds which do not indicate an incorporated donor.

While in principle an ejected Si atom should be present at every array site where a P incorporation has occurred we do not always observe it and rather see *only* the heterodimer (e.g. site "I" in Fig. 7.2). This is most likely due to a finite possibility for the Si adatom to diffuse away from the initial array site during the anneal. Indeed, Si adatoms have been found to be mobile on the H-terminated Si(100) surface at elevated temperatures [220].

The observed features show a considerable spread of heights in the histogram. There are two reasons for this: the apparent "height" of a feature represents the local tunneling current which can be influenced by the microscopic details of the STM tip and the surface (e.g. nearby surface defects), particularly for features on the sub-nm scale. Furthermore, the spread of the peak associated with the ejected Si adatom may reflect several different possible configurations of the adatom [216, 217, 218] which can either be in the aforementioned dimer-bridge configuration or in the end-bridge configuration where it is bound to

two Si surface atoms of different dimers.

To further confirm that the observed features with an apparent height from ∼50 to 80 pm are indeed due to the ejected Si atom, an attempt was made to image the array again after desorption of the entire remaining H mask. To avoid further surface reactions and diffusion processes, this was achieved by using the STM tip in lithography mode rather than heating the sample to the required ∼470°C [221]. However, it was found that the STM tip has a tendency to move individual Si adatoms away from the original incorporation sites as the surrounding H is desorbed. Indeed, single Si adatoms are known to be quite mobile on the Si(100) surface, particularly along the dimer rows [216, 222] – until they meet other Si adatoms to form chains or islands [223]. This makes evaluation of the STM images of the array without the H mask unreliable. As a result we will rely on the surface features observed after incorporation but with the H mask still intact. These are the relevant conditions when fabricating a transport device since the H mask in that case cannot be removed, as will be discussed in more detail in section 7.3.

Another important motivation for our statistical study was to determine the optimal size for the desorbed patches to ensure the reliable incorporation of precisely one donor. The results are illustrated in Fig. 7.3 b, where the probability of finding a certain number of P-related features after incorporation is plotted for different sizes of the initial desorbed patch. Here, only suitable patches with contiguous desorbed dimers along one dimer row were considered, 95 in total. It is evident that the ideal size for single donor incorporation patch is 3 adjacent dimers. If the patches are larger (4, 5, or 6 dimers in size) there is a finite chance of incorporating more than one donor. It should be noted that the arrays also included some 2 dimer patches, none of which showed evidence of a P donor after incorporation. This further highlights the validity of the theoretical predictions [71].

From our statistical incorporation study we conclude that the probability of incorporating a single P atom within a 3-dimer patch (3DP) is approximately 70% under the dosing and anneal conditions stated above. This number is easily sufficient to fabricate a single donor transport device as will be shown later in this chapter. However, it will need to be improved for future scale-up of devices containing a multitude of precisely positioned dopants [17]. It is very likely that further incorporation studies along with a deeper understanding of the incorporation process in the presence of a surrounding hydrogen mask will lead to significant improvements of the success rate. In particular, further array studies are currently underway to image the surface after PH_3 dosing (but before the anneal) to investigate how the dosing conditions affect the incorporation rate.

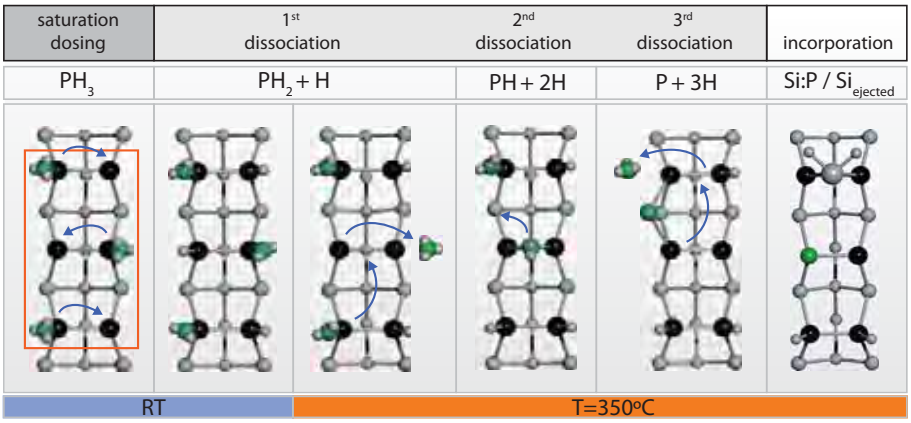

Figure 7.4: Incorporation pathway of an individual phosphorus atom. The panels illustrate the sequential dissociation process of the adsorbed phosphine (PH_3) molecules and the final incorporation reaction (see text). The 3-dimer patch is indicated by the red box in the first panel. Here, we assume saturation dosing of the initial surface. Reactions taking place at $T = 350°C$ are indicated by the red bar below. The Si adatom ejected in the final P incorporation reaction resides in the dimer-bridge configuration (last panel), consistent with our observations.

7.2.1 Incorporation pathway for an individual P impurity

We now give a summary of the complete incorporation pathway for a single P donor within a 3-dimer patch that is consistent with the findings from our statistical study. The underlying reaction pathways and kinetics have been well-documented for the clean Si(100) surface [41, 71, 76]:

$$PH_3(\text{ads}) \rightarrow PH_2 + H \rightarrow PH + 2H \rightarrow P + 3H \rightarrow P(\text{incorp})$$

The sequential reaction is illustrated in Fig. 7.4, where we explicitly consider the presence of the surrounding hydrogen mask as well as the position of the ejected Si adatom. The initial 3DP is indicated by the red box. During the phosphine dosing step at room temperature, PH_3 molecules adsorb on the bare Si surface, immediately dissociating to $PH_2 + H$ as depicted in the first panel. We assume the dosing rate to be high enough to achieve saturation coverage with PH_2. At this point, all 6 DBs are passivated by PH_2 and the associated H (2^{nd} panel) and further dissociation within the patch is inhibited at room temperature (RT). Thermal activation is required to desorb some of the phosphine fragments. During the short anneal at 350°C, some $PH_2 + H$ will recombine and desorb as PH_3, immediately allowing one of the remaining two PH_2 fragments to further dissociate to PH+2H (3^{rd} panel) – which is energetically favorable compared to desorption if free DBs are available [71]. Again, further reactions are inhibited until the remaining PH_2

fragment eventually recombines and desorbs, at which point the left over PH undergoes a final dissociation step to P+3H. Still at 350°C, the phosphorus adatom then incorporates into the top layer of the Si surface, ejecting a Si atom in the process [77]. The latter subsequently resides in the dimer-bridge configuration near the Si:P heterodimer [217, 218] as illustrated in the last panel of Fig. 7.4. It is this Si adatom that is seen in the STM images after the incorporation anneal (see Fig. 7.2). It should be noted at this point that even if only two or one PH_3 molecules adsorb to the initial 3DP, exactly one P atom will incorporate. However, for the sake of reproducibility we focus on saturation dosing conditions since sub-saturation dosing is much harder to control experimentally.

7.2.2 Placement accuracy of the single donor

Regarding placement accuracy, the single dopant can only be incorporated within the 3-dimer patch, substituting one of the 6 vicinal Si atoms. Since this patch can in principle be desorbed around a chosen dimer site, the overall spatial uncertainty of the dopant site is given by the area of the patch (i.e. 2×3 lattice sites or $\sim 7.7 \times 11.5$ Å^2). Our fabrication strategy thus allows for the deterministic placement of a single impurity in silicon with a lateral accuracy better than ± 6 Å. While the incorporated P may diffuse upward during the final low-temperature Si overgrowth step, the low thermal budget keeps vertical dopant segregation to a minimum, with an upper limit of ~ 6 Å [80].
Phosphine dissociation and phosphorus incorporation, diffusion and segregation have previously been studied in detail on clean Si(001), both theoretically [71] and experimentally [76]. However, few studies have investigated these processes in the presence of a hydrogen mask which confines many of the reaction pathways to within the desorbed areas. Future improvements in dosing and incorporation parameters along with an improved understanding of the incorporation mechanism within these ultra-small patterned dots will likely lead to atomic placement with an accuracy down to the single lattice site.

7.3 Fabrication of the single donor transport device

The results of the incorporation array study presented in the previous section lead to the successful fabrication of a single donor transport device. Here, we use a patterning approach that is similar to the previously discussed devices of this thesis with a few important modifications. Until now, devices were patterned on n-type lightly P-doped silicon wafers with a doping density of $\sim 10^{15}$ cm^{-2} (corresponding to a resistivity of $1 - 10\,\Omega$cm). As a result, there is a small but finite chance of a phosphorus donor from the

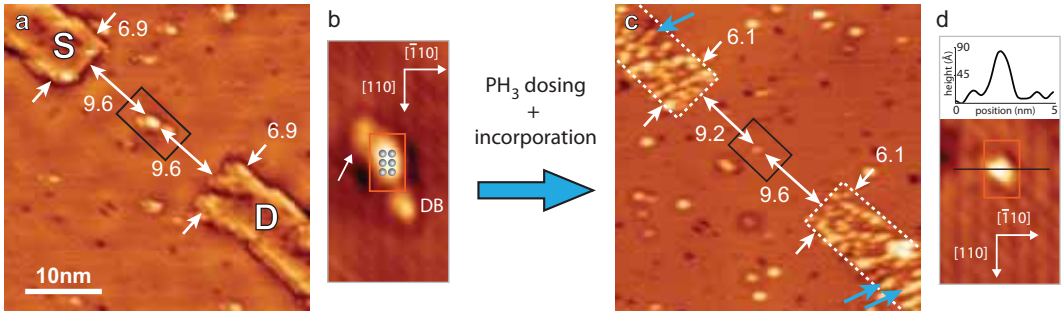

Figure 7.5: Incorporation of a single phosphorus atom. **a** High resolution STM image of the H-desorbed surface (before dosing) showing the innermost part of the source and drain leads. A close-up of the central 3 dimer patch is depicted in **b**. The additional features are due to a stray dangling bond (DB) and an imaging artefact to the left (white arrow) resulting from a slight double tip. **c**, The same site after PH_3 dosing and a 5 s incorporation anneal. Some ejected Si adatom chains within the S and D leads are highlighted by blue arrows. **d**, The close-up reveals a single protrusion at the site of the previous 3-dimer patch which is associated with a single ejected Si adatom. All dimensions are in nm.

background doping to be close enough to the channel between source and drain to appear in transport measurements. To avoid this ambiguity for our single donor device we choose a p-type (boron doped) substrate with a similar resistivity ($1 - 10\,\Omega$cm).

STM-patterning of the gated device was achieved in a two-step process: First, the intended incorporation area for the single donor as well as the innermost parts of the leads are desorbed. Here, the 3DP is patterned precisely in the middle between the leads as shown in Fig. 7.5 a. For the width of the leads as well as their separation to the central donor we chose approximately the same dimensions that had yielded good results for the few-donor quantum dot presented in the last chapter (see Fig. 6.3). A close-up of the single donor patch in Fig. 7.5 b reveals the required 3 adjacent desorbed dimers as well as two additional features which are due to a stray dangling bond and an imaging artefact, respectively, and will therefore not affect the incorporation process. Subsequent dosing and an incorporation anneal completes the first patterning step. Here, we use the same parameters as in the array study, i.e. a PH_3 exposure of ∼14 Langmuir and a 5 s anneal at 350°C. Next, the area is imaged again to verify the successful incorporation of a single P dopant. Here, a lead extension on the D side (blue arrow in Fig. 7.6 a) which has been desorbed along with the central structure in the first step serves as a marker that helps to relocate the initial incorporation site after the thermal drift caused by the anneal. Indeed, Fig. 7.5 c and d reveal a bright protrusion centered on a dimer row with a height of ∼70 pm with respect to the surrounding H mask (inset of panel d). This is consistent with the expected height (65 ± 15 pm) for a single ejected Si atom determined from the array

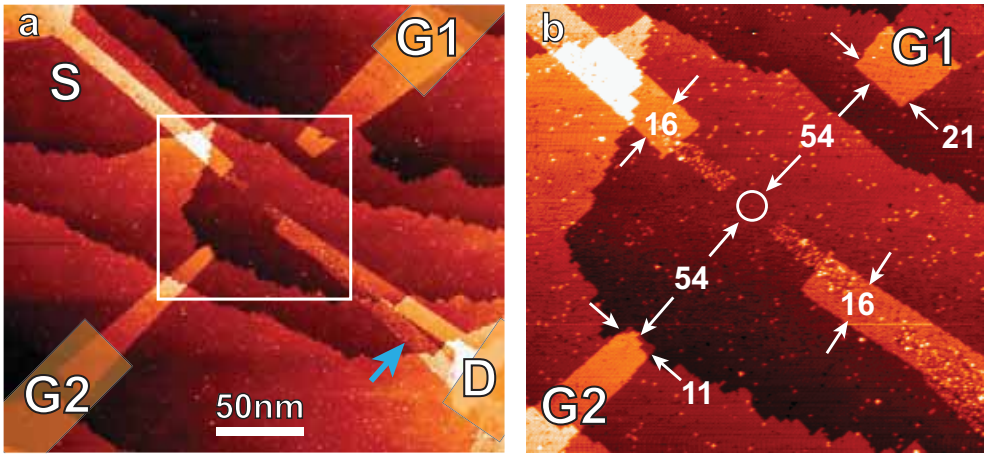

Figure 7.6: Single phosphorus donor transport device. **a**, STM image of the 4 terminal device with source (S) and drain (D) leads and two in-plane gates ($G1$, $G2$) acquired during STM-lithography after incorporation of the central single P donor but before PH_3 dosing of the outer electrodes. The orange shaded areas indicate the contact arms for each electrode which were desorbed in the subsequent step. The "lead" (blue arrow) on the D side incorporated in the first donor incorporation step served as a marker to relocate the initial incorporation site. **b**, Close-up of the central area as indicated by the white square in (**a**). Gate $G1$ was patterned to be twice as wide as $G2$, resulting in a reduced leakage (see text). The white circle indicates the position of the single P impurity (close-ups of which are shown in Fig. 7.5). All dimensions are in nm.

studies of section 7.2. We thus conclude that one single impurity has been successfully incorporated in the central desorbed 3-dimer patch. The tips of the S and D leads can be clearly identified by the ejected Si adatoms and adatom chains, some of which are indicated by blue arrows in Fig 7.5 c. The presence of such adatom chains perpendicular to the dimer rows underneath confirms the successful donor incorporation throughout the structure [66]. Furthermore, the fact that ejected Si is only observed within the desorbed regions confirms the structural integrity of the nm-scale leads during the incorporation anneal.

In the second patterning step, the in-plane gates $G1$ and $G2$ are aligned and desorbed along with the extensions of the leads as shown in Fig. 7.6. Owing to the discrete spectrum of the P donor, a current flowing from S to D will be modulated in a characteristic way when a voltage is applied to either of the gates. As for the 7 donor quantum dot of the last chapter, we choose a two-gate layout to allow for higher tunability with two independent gate voltages. However, in contrast to the few-donor dot we pattern both gates with the *same* separation (54 nm) to the central impurity, but with different widths to investigate how the gate leakage characteristics are affected by the width of the electrodes.

For the second dosing and anneal cycle we use the standard parameters (∼1.4 Langmuir

of PH_3 and 30 s at 350°C) which have proven to yield reliable results for many previous devices [115, 201]. It is important to note that as a result of the initial P incorporation process, the central 3DP is effectively re-passivated and can therefore not incorporate any additional donors during the second dosing and anneal cycle. Furthermore, lateral diffusion during the second anneal at 350°C is inhibited for the incorporated single P impurity which occupies a substitutional Si site. After the second donor incorporation step, the entire structure is overgrown with silicon from a thermal sublimation source. The low sample temperature of 250°C during this process minimizes vertical segregation to a maximum of a few lattice sites [80], while ensuring good epitaxial quality of the overgrown Si [81]. Due to a calibration error, the encapsulation thickness for the single donor device was ∼180 nm. While this is much higher than the standard 25 nm for previous devices it is not expected to be detrimental to the transport characteristics – particularly in the absence of surface gates.

After removal from UHV, RIE etched contact holes and aluminium contacts were defined over the STM-patterned patches in subsequent EBL steps. *Ex-situ* processing was identical to the 7 donor device, as described in more detail in section 6.2. Again, two metal terminals are patterned for both S and D allowing us to determine that good ohmic contact has been made (see Fig. 7.7). Only one terminal was patterned for each in-plane gate.

7.4 Low-temperature transport characteristics

An initial brief characterization at 4K confirmed that the sample was well contacted electrically. Two Coulomb peaks were observed as a function of gate voltage. The single donor device was subsequently cooled down in a ^{3}He/^{4}He dilution refrigerator with a base temperature of ∼20 mK. Like the few-donor quantum dot presented in the last chapter, all electrical measurements were carried out by applying a dc voltage to the source electrode while keeping the drain grounded.

As discussed in chapter 3, we first check for good ohmic contact to the buried STM-patterned structure. This is done by simply measuring the resistance R_{2T} of the contact patches alone via their two metal terminals. The resulting IV-curve for the S electrode[1] is shown in the inset of Fig. 7.7 revealing an Ohmic (i.e. linear) characteristic with a two-terminal resistance of approx. 36 kΩ. This resistance is higher than the corresponding value (∼3 kΩ) for the few-donor dot of the last chapter, most likely resulting from the smaller STM-patterned contact patches which were used in an attempt to reduce the

[1]The D electrode could not be measured due to a misalignment of one of the two metallic contacts.

overall patterning time (approx. 12 hours for the present device).

The next crucial step is to determine the effective gate range for both in-plane gates, i.e. the maximum voltages that can be applied to each gate before the leakage current (flowing from a given gate to any of the other electrodes) exceeds a certain threshold, typically 100 pA. Fig. 7.7 shows the measured leakage curves for both gates as a function of the applied gate voltage. From this plot we determine an effective gate range of -0.73 V to 1.3 V for $G1$ and -0.52 V to 1.0 V for $G2$, respectively. It is evident that the narrower gate, $G2$, has a smaller gate range. This is possibly due to a higher potential gradient around the tip of a narrow electrode which results in a smaller effective tunnel barrier. It may thus be favorable to pattern future devices with wider gates with rounded edges rather than narrow gates. The leakage characteristic for $G1$ shows a very steep onset, where the leakage current increases by more than an order of magnitude within a 1 mV increase of gate voltage. We attribute this to an avalanche-type breakdown [25] rather than direct tunneling processes. This occurs when the field strength at the gate becomes large enough to cause avalanche multiplication of substrate carriers and has been observed before for our planar Si:P structures [100]. The leakage curves for both gates are strongly asymmetric for positive and negative gate voltages with a significantly higher break-through voltage for $V_G > 0$. This is consistent with the findings from the few-donor quantum dot (see Fig. 6.4 in chapter 6) and may reflect the fact that the gate electrodes themselves get partially depleted for very positive voltages [115]. It should be noted that both gates of the single donor device (with a gate separation of 54 nm) have a significantly smaller gate range than the ones of the few-donor dot. Here, the device was patterned on a n-type substrate with two in-plane gates at distances of 57 nm and 44 nm from the dot (see Fig. 6.1 in chapter 6) resulting in a gate range of -1.3 to 1.8 V and -1.0 to 1.4 V, respectively. By contrast, the single donor device was patterned on a p-type substrate (with the same nominal resistivity of $1 - 10\,\Omega$cm). For the resulting (bipolar) n^{++}-p-n^{++} junction between the gate and the other electrodes one would therefore expect a higher barrier and therefore a higher gate range than for the corresponding n^{++}-n-n^{++} profile of the few-donor device. The reasons for the smaller gate range of the single donor device are not yet understood. One possibility is that an increased number of dangling bonds (arising from stray desorption or thermal H desorption during the first incorporation anneal) has resulted in the uncontrolled incorporation of P donors between the gates and the leads thus creating a leakage pathway. However, further investigations of the gate leakage characteristics as a function of device geometry as well as substrate type will be necessary for future devices.

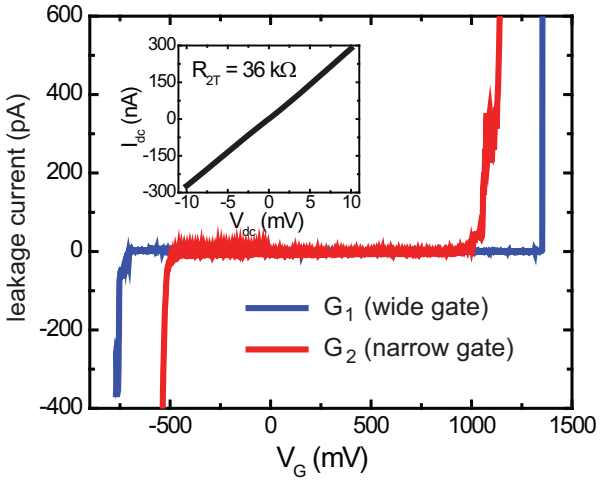

Figure 7.7: Determining the gate range. Leakage current as a function of the applied gate voltage for each gate. The wider gate $G1$ has a higher gate range with a very sharp onset of the leakage current at approx. +1.35 V. We determine an effective gate range of -730 mV to 1300 mV for $G1$ and -515 mV to 1020 mV for $G2$, respectively. The inset shows a linear IV curve through the contact patch of the source electrode with a two-terminal resistance of $\sim$ 36 kΩ, confirming good ohmic contact to the buried device.

7.4.1 Stability diagram of a single donor

Transport characteristics of the single donor device at mK-temperatures are shown in Fig. 7.8 a, where the current I_{SD} through the device is plotted as a function of the bias voltage V_{SD} and gate voltage V_G (applied to gates $G1$ and $G2$ in parallel). As discussed in previous chapters, the electrodes of our transport devices are formed of Si:P δ-layers which are doped well above the metal-insulator transition and will therefore conduct even at mK-temperatures [224]. By contrast, the surrounding substrate is very lightly doped silicon which represents tunnel barriers at low temperatures due to the freeze-out of carriers. This is illustrated in the energy schematic of Fig. 7.8 c. Electronic transport from S to D thus occurs via the discrete states of the single P donor in the channel. For isolated phosphorus donors in bulk silicon there are two bound states, the charge-neutral D^0 state and the two-electron state D^- [225], as depicted in Fig. 7.8 b. In addition to these ground states there exists a spectrum of excited states which will be discussed in more detail in section 7.4.4 below. For the bulk Si:P system, the two ground states have a binding energy of 45.6 meV and $\sim$1.7 meV, respectively [168, 226], resulting in a charging energy of $45.6 - 1.7 \approx 44$ meV for D^0. For the donor in our transport device, we also expect two bound states D^0 and D^- [209]. However, the donor spectrum may be different from the bulk case due to the proximity of the highly-doped electrodes. Indeed, several groups have reported a lowering of the electrochemical potential for the D^- transition resulting from

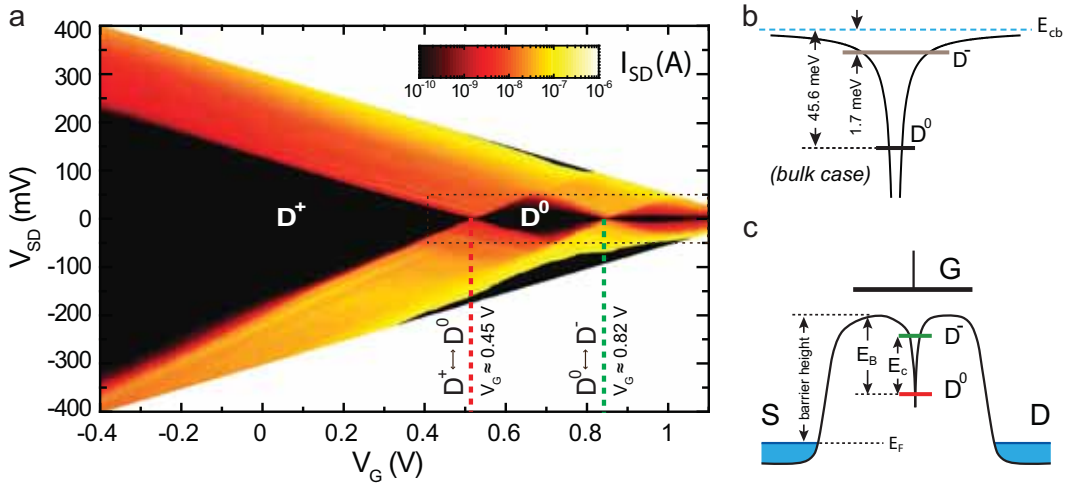

Figure 7.8: Transport characteristics of a single donor device. **a**, The source-drain current (log scale) as a function of bias voltage (V_{SD}) and gate voltage (V_G) yields the expected stability plot for a single donor where the D^+ region does not close for lower gate voltages. The $D^+ \leftrightarrow D^0$ and $D^0 \leftrightarrow D^-$ transitions occur at reproducible positive values of V_G. To limit the current through the device the V_{SD} window was decreased with rising gate voltage, resulting in a trapezoidal plot. The dotted box indicates the region shown in Fig. 7.9. **b**, Energy schematic of the Coulombic potential profile for an isolated P donor in bulk Si where the D^0 and D^- states are separated from the Si conduction band edge E_{cb} by their binding energy, 45.6 meV and ~1.7 meV, respectively. **c**, By contrast, the donor potential in our device is strongly modified by the nearby S and D electrodes. At low temperatures, the low-doped substrate represents tunnel barriers of a certain height with respect to the Fermi level E_F in the leads. The electrochemical potentials of the D^0 and D^- states reside below the top of the barrier. They can be shifted down by applying a positive gate voltage which will also decrease the barrier height. The energy difference between both states is the charging energy E_C.

a strong capacitive coupling to a surface gate [165, 209, 213]. This was found to result in a significantly increased binding energy for D^- which translates[2] to a decreased charging energy for D^0. Calderon *et al.* [196] recently studied how the presence of heterointerfaces affects the charging energy of shallow donors in silicon. In particular, they found that nearby insulating barriers and metallic gates result in a strong reduction of the charging energy.

In the stability diagram of Fig. 7.8 a, the current is suppressed in the diamond-shaped dark regions due to Coulomb blockade. An immediate observation is that the "diamond" for $V_G < 450$ mV does not close. This is the expected behavior [165] for the positively ionized D^+ state since the single P donor cannot lose more than its one unbound valence electron. Indeed, the blockaded bias region increases nearly linearly with decreasing gate voltage all the way down towards the lower end of the gate range. Importantly, the device

[2] An increased binding energy effectively shifts the D^- level closer to the D^0 level since the latter is charge neutral and thus not affected by the capacitive coupling to the surface gate.

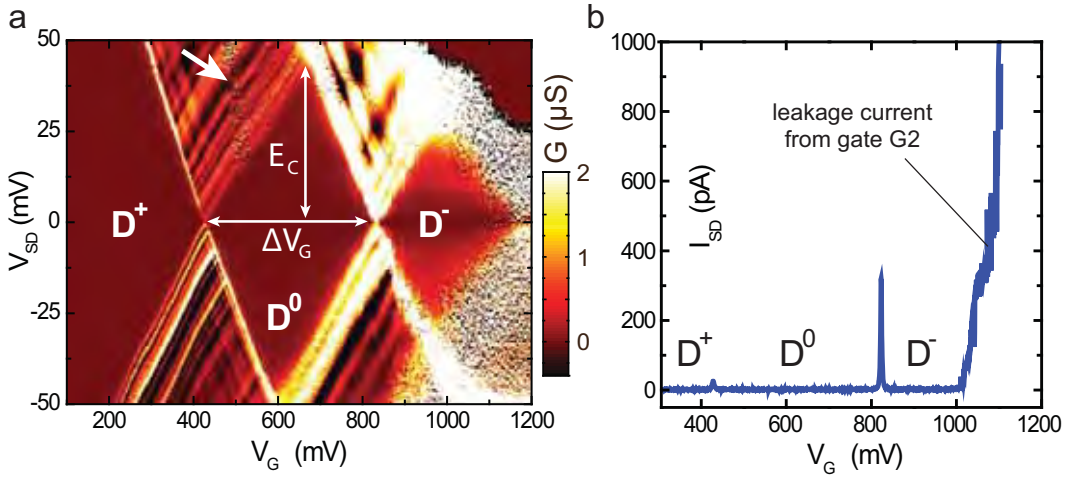

Figure 7.9: Stability plot of a single P donor. **a**,The differential conductance dI_{SD}/dV_{SD}, plotted as a function of bias and gate voltage (applied to both gates in parallel). From the D^0 diamond, we estimate a charging energy of 47 ± 3 meV. An additional feature (indicated by the arrow) is most likely due to the charge transition of a nearby charge trap. We also observe a roughly diamond-shaped region for $V_G > 820$ mV which may reflect the D^- charge of the donor. However, the well-resolved Coulomb blockade behavior disappears above ~900 mV and the current noise increases drastically due to leakage from gate $G2$. **b**, The leakage current from $G2$ (see Fig. 7.7) is clearly visible in the measured drain current for $V_G > 1000$ mV.

conductance remains quite high throughout the gate range, on the order μS. This allows us to rule out the presence of additional "hidden" charge transitions below $V_G = 450$ mV which might not be visible if the device conductance were to decrease significantly [158]. We thus identify the diamond between $V_G \sim 450$ mV and 820 mV in Fig. 7.8 a as the charge-neutral D^0 state of the P donor.

In other architectures for single donor transport devices [165, 209] it is possible to measure the binding energy, i.e. the energy difference between the bound states and the top of the barrier between donor and leads as illustrated in Fig. 7.8. This requires the effective barrier height to be determined from the temperature-dependent source-drain IV characteristics over larger temperature ranges (typically on the order of 100 K [209]). In our devices, the barrier is defined by the low-doped intervening Si substrate which becomes conducting above the freeze-out temperature of $\sim 40 - 50$ K [100]. The barrier height is therefore difficult to determine for our sample due to the limited temperature range available [100], so that the binding energy is not directly experimentally accessible. However, we can readily determine the charging energy (i.e. the energy difference between D^0 and D^-) from the height of the D^0 diamond. This is illustrated in the stability diagram of Fig. 7.9 a which shows the device conductance dI_{SD}/dV_{SD} as a function of bias and gate voltages. It should be noted that the D^0 diamond is slightly asymmetric with respect to the $V_{SD} = 0$ axis

which leads to different values of E_C for positive and negative bias, ∼46 meV and ∼48 meV, respectively. This asymmetry is most likely due to a slight change in capacitive coupling to the leads for different charge states resulting in different slopes of the corresponding diamond edge [162]. Taking the average value and accounting for the relatively smooth increase of conductance at the tips of the diamond (resulting from the high conductivity of the device), we estimate an experimental charging energy of 47 ± 3 meV. Interestingly, this value is comparable to the bulk value of ∼44 meV. This is in sharp contrast to the reported single donor devices mentioned above [165, 209, 213] where the D^0 charging energy was found to be significantly reduced (by roughly a factor of $\sim 0.6 - 0.7$) due to the strong electrostatic coupling to the gate. We attribute the observed bulk-like value for E_C in our device to the absence of surface gates and the weaker capacitive coupling between the in-plane gates and the donor in our planar architecture[3]. It should be noted that an additional charging feature is visible in the stability diagram as a diagonal line of increased noise, indicated by the white arrow in Fig. 7.9 a. This may be due to a nearby charge trap with a weak capacitive coupling to the gates. At some particular gate-voltage configuration, the trap comes into resonance, fluctuating between two charge states. By applying different voltages to the two in-plane gates, this resonance can be shifted away from the $D^+ \leftrightarrow D^0$ transition (see Fig. 7.11).

We also observe a roughly diamond-shaped region for $V_G > 820$ mV in Fig. 7.9 a which we associate with the two-electron D^- state. The large extent of this diamond is contrary to what one would expect for a bulk-like system, where D^- is only weakly bound by ∼1.7 meV [226]. Furthermore, we observe a drastic change of the transport characteristics for gate voltages above ∼900 mV, where the stable Coulomb blockade behavior and the well-defined diamond edges vanish and the current noise increases strongly. This can be attributed to the onset of leakage from the narrow gate $G2$ (since V_G is applied to both gates in parallel in Fig. 7.9 a). While the leakage current is not visible in the differential conductance of 7.9 a, it can easily be seen in the direct current signal of panel b for $V_G > 1000$ mV. The strong gate leakage affects the reliability of the data at the highest gate voltages so that we cannot extract a dependable value for the charging energy of D^-. As will be discussed in the next section, the gate voltage not only shifts the electrochemical potential of the donor states, but also modulates the height of the tunnel barrier along the transport direction. What appears like a "closing D^- diamond" in Fig. 7.9 a may thus in fact be a signature of the vanishing tunnel barriers between the donor and the leads resulting in a sharp increase of direct tunneling from S to D. However, the reasons for the

[3] see section 5.3

large extent of the D^- diamond are not yet fully understood. One plausible explanation is a strongly decreasing gate lever arm as the gate voltage is increased. This is consistent with the decreasing slopes in Fig. 7.9 a as will be discussed in more detail in section 7.4.2 below. A reduced lever arm would indeed cause the D^- diamond to be "stretched" along the gate axis.

Looking at the stability diagram of Figs. 7.8 a and 7.9 a, it is important to note that the D^0 diamond is *not* centered around $V_G = 0$. Instead, the $D^+ \leftrightarrow D^0$ transition reproducibly[4] occurs at positive gate voltages around $\sim 450 \pm 30\,\mathrm{mV}$. It may at first seem counter-intuitive that the isolated donor is not in the charge-neutral D^0 state under equilibrium conditions (i.e. $V_{SD} = V_G = 0$). Considering the stability of our data it is unlikely that this behavior could be explained by offset charges. Instead, we attribute this characteristic to the gate-voltage dependent potential profile of our sample, which can be justified by a simple quantitative analysis. In contrast to the bulk case (Fig. 7.8 b), the Coulombic donor potential in our transport device is modified due to the proximity of the highly-doped S and D electrodes, resulting in the double barrier profile illustrated in Fig. 7.8 c along the transport direction. The tunnel barrier is formed by the intervening substrate which is insulating at low temperatures. Importantly, the exact height of this barrier is unknown for our device. However, based on previous studies of planar Si:P tunnel junctions of similar geometry[5] [100], we can assume a barrier height of $\sim$100 meV and, as a first approximation, a bulk-like binding energy of 45.6 meV for D^0. The charge-neutral state then resides approximately $100\,\mathrm{meV} - 45.6\,\mathrm{meV} \approx 54\,\mathrm{meV}$ *above* the Fermi level in the leads when no gate voltage is applied. This is illustrated in the schematic of Fig. 7.8 c. As mentioned previously, a voltage applied to the in-plane gates shifts the electrochemical potential of the donor states. This means that the donor remains positively ionized until a sufficient positive gate voltage brings the D^0 electrochemical potential into resonance with the Fermi energy in the leads. Using the experimental gate lever arm $\alpha \approx 0.1$ (see table 7.1), we can roughly estimate the required gate voltage as $\frac{1}{e\alpha} 54\,\mathrm{meV} = 540\,\mathrm{mV}$. This is in reasonable agreement with the experimentally obtained value for the first charge transition of $\sim 450 \pm 30\,\mathrm{mV}$, particularly considering the crudeness of the model. This may be a further indication that the single donor in our device is indeed in a bulk-like state that is only weakly influenced by the nearby in-plane electrodes.

[4] This behavior is consistent even between different cool-downs of the sample.

[5] While these tunnel junctions were patterned on n-type substrates, the difference in barrier height (between n-type and p-type substrate) is expected to be small due to the very low background doping density ($\sim 10^{15}\,\mathrm{cm}^{-3}$) in both cases.

Capacitances of the single donor device (in aF)

C_Σ	C_S	C_D	C_{G1}	C_{G2}	α_{G1+G2}
3.5	1.35	1.75	0.21	0.19	0.1

Table 7.1: Experimental capacitance values extracted from the D^0 diamond in the stability plot of Fig. 7.9 a as described in section 2.3.1. Here, we have used the average value of ∼47 meV for the charging energy E_C to determine C_Σ. The values for source and drain capacitance are extracted from the slopes of the diamond edges at the $D^+ \leftrightarrow D^0$ transition.

7.4.2 Device capacitances

From the peak spacing ΔV_G at zero bias we obtain a combined gate capacitance of $C_G = e/\Delta V_G \approx 0.4$ aF. We also determine an average gate lever arm $\alpha = E_C/\Delta V_G \approx 0.1$, which is a measure for the effectiveness of the electrostatic coupling between gate and donor. The changing slopes of the diamond edges in Fig. 7.9 a indicate that α actually decreases for higher gate voltages. This is consistent with the results from the few-donor quantum dot, where α was found to decrease by roughly a factor of 2 throughout the gate range (see Fig. 6.6 in chapter 6). We attribute the decreasing lever arm to the lowering of the tunnel barriers for positive gate voltages which results in a weaker confinement of the electronic states along the *S*-*D* direction. This in turn will lead to a stronger capacitive coupling $C_{S,D}$ to the leads while the capacitances C_G to the farther gates remain roughly constant so that $\alpha_G = C_G/(C_S + C_D + C_G)$ will decrease [122]. In a system where the capacitances are dependent on the applied gate voltage, the simple constant interaction model of Coulomb blockade [48] no longer applies. The experimental capacitances summarized in table 7.1 are thus approximate values that are only valid at the $D^+ \leftrightarrow D^0$ transition while the extracted lever arm is the *average* value for the D^0 diamond.

Gate $G1$ shows a slightly stronger capacitive coupling to the donor than $G2$. This is consistent with the geometry of Fig. 7.6 b since $G1$ is wider. Regarding the leads, from the slopes of the Coulomb diamonds we find a higher capacitance for the D electrode. With a roughly identical width of both leads, this implies that the incorporated donor should be located closer to the D electrode. This will be discussed in more detail in the next section (7.4.3).

7.4.3 Asymmetry of tunnel coupling

As was discussed in detail in section 6.4.3 of the previous chapter, an asymmetry in the tunnel coupling to source and drain manifests itself in a disparity of the observed

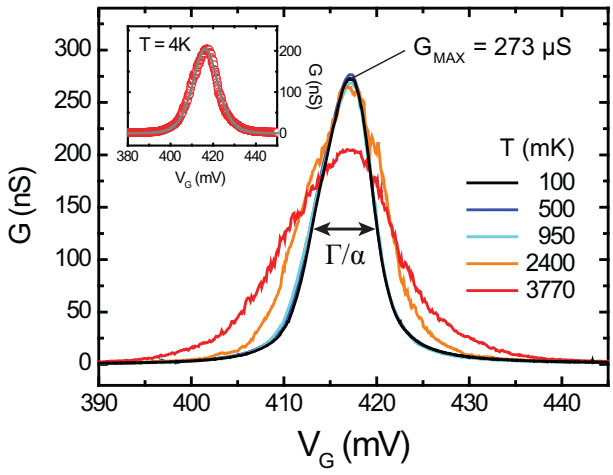

Figure 7.10: Temperature dependence of the D^0 peak. Low-bias ($V_{SD} \approx 100\,\mu$eV) conductance of the $D^+ \leftrightarrow D^0$ transition. The peakshape does not change noticeably for $T \lesssim 1\,$K indicating that here the peaks are broadened by the finite coupling to the leads rather than temperature. In this lifetime-broadened regime the coupling constant can be extracted directly from the FWHM of the Coulomb peak multiplied by the gate lever arm, yielding $\Gamma \approx 680\,\mu$eV. *Inset:* When T is raised to $\sim$3770 K, the bath temperature of the cryostat corresponds well to the temperature extracted from a fit (grey line) to the quantum CB theory [48], indicating the cross-over to the temperature-broadened regime around 4 K.

transport resonances. In the stability diagram of Fig. 7.9, lines of increased conductance are observed predominantly with positive slope indicating a stronger tunnel coupling to the D electrode. This is consistent with the stronger *capacitive* coupling to the drain (table 7.1). It thus seems plausible that the donor in the channel is located closer to the drain lead. The dimensions of the central device area after incorporation are shown in Fig. 7.5 c, where we observe the ejected Si adatom to be one lattice site ($\approx$3.8 Å) closer to the *source* lead. However, the adatom does *not* reside directly above the incorporated P donor, but is shifted along the dimer row as illustrated in the last panel of Fig. 7.4. We conclude that the incorporated P donor resides to the right of the observed Si adatom in Fig. 7.5 c, and is therefore indeed at least one lattice site closer to the D electrode – in excellent agreement with the electrical results.

To gain a quantitative understanding of the tunnel coupling asymmetry in our device, we have measured the temperature dependence[6] of the first charge transition. Fig. 7.10 shows the low-bias conductance G of the $D^+ \leftrightarrow D^0$ transition up to $\sim$4 K. It is evident that the Coulomb peakshape does not change at temperatures below $\sim$1 K, indicating that here the device is in the lifetime broadened regime [48], $k_B T < h\Gamma$, where Γ is the

[6]This T-dependent data was measured in collaboration with Dr. H. Huebl at the Walther Meissner Institute, Germany.

coupling constant. The latter is the sum of the two tunnel rates for the source and drain tunnel barrier, respectively, $\Gamma = \Gamma_S + \Gamma_D$ [48, 227]. The Coulomb peaks for $T < 1K$ are broadened due to the finite tunnel coupling between the dot and the leads (rather than temperature) so that Γ corresponds to the FWHM of the peak, assuming that only one quantum level contributes to the transport through the donor [228]. This assumption is justified since the donor excited states are much higher in energy (see section 7.4.4) than the bias voltages used in Fig. 7.10. Using $\alpha \approx 0.1$ to convert gate voltage into an energy, we obtain $\Gamma = \alpha \cdot \mathrm{FWHM} \approx 680\,\mu\mathrm{eV}$ from the peak at 100 mK. We can use this value to get a rough estimate for the tunneling asymmetry: in the lifetime broadened regime the (T-independent) peak maximum G_{MAX} is given by [228]

$$G_{\mathrm{MAX}} = \frac{2e^2}{\hbar} \frac{\Gamma_S \Gamma_D}{(\Gamma_S + \Gamma_D)^2} \tag{7.1}$$

Here, the factor 2 accounts for spin degeneracy. Using the experimental values for Γ ($= \Gamma_S + \Gamma_D$) and $G_{\mathrm{MAX}} \approx 270\,\mu\mathrm{S}$, we obtain $\Gamma_S = 1\,\mu\mathrm{eV}$ and $\Gamma_D = 679\,\mu\mathrm{eV}$. This means that there is indeed a considerable asymmetry in the tunnel coupling with tunneling through the source barrier being the rate-limiting process. Differences of more than two orders of magnitude in the tunnel rates have also been found for other single donor transport devices [229].

It should be noted that the above method gives only a rough estimate for the tunnel rates, since it relies on the experimental value for the Coulomb peak height G_{MAX}. A more elaborate approach introduced by Foxman *et al.* [227] is independent of the absolute value of G_{MAX} and relies on the T-dependence of the Coulomb peak for higher temperatures (where $h\Gamma < k_{\mathrm{B}}T$). However, the cross-over to the temperature-broadened regime in our device occurs around 4 K. Since measurements were only performed up to 4.2 K, we do not have sufficient data to extract the required T-dependence of the peak height in this regime.

7.4.4 Single donor excitation spectrum

A close-up of the $\mathrm{D}^+ \leftrightarrow \mathrm{D}^0$ transition is depicted in Fig. 7.11 for two different gate configurations. We observe a great number of transport resonances in the stability diagram as lines of increased conductance running parallel to the diamond edges outside the blockaded regions. The average energy spacing of these resonances is on the order of $\sim$1 meV. It is worth noting that this energy scale is an order of magnitude larger than the $\sim$100 μeV spacing observed for the few-donor dot of the last chapter. Many of these lines terminate

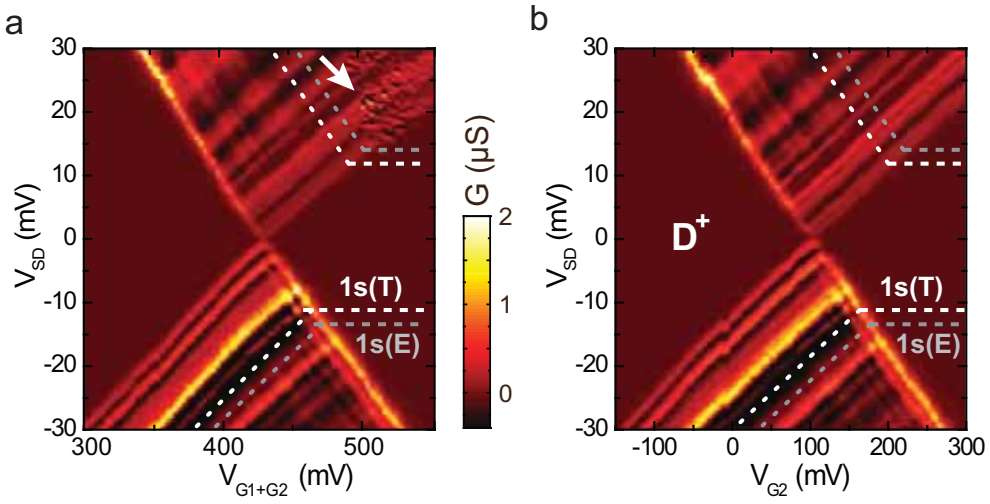

Figure 7.11: Resonance spectrum. **a**, Close-up of the $D^+ \leftrightarrow D^0$ transition in Fig. 7.9 a, where both in-plane gates were used in parallel. The superimposed lines indicate the expected position of resonances arising from the first two single-electron excited states of an isolated donor in bulk Si, with the 1s(T_2) and 1s(E) states ∼11.7 meV and ∼13.0 meV above the GS. The corresponding resonances may appear in the sequential tunneling regime (dotted lines) or the co-tunneling regime (horizontal dashed lines). **b**, To shift the background charging feature (indicated by the arrow in **a**) out of the window, only V_{G2} was swept while keeping V_{G1} at a fixed value of 750 mV.

on the edge of the "empty" D^+ diamond and therefore cannot be due to excited states of the donor electron [152, 165] (since the corresponding D^+ state contains no electrons). Instead, we attribute the resonances to a quasi-1D density of states in our nm-scale S and D leads. Such DOS features have previously been observed in many quantum dot systems [170, 205, 204] as well as single donor devices [165]. Furthermore, in chapter 6 we presented modeling results for the density-of-states in our narrow source and drain leads (see section 6.5.2). In particular, the single-particle calculations revealed how transversal quantization in the wider (∼16 nm, see Fig. 7.6) part of the S and D electrodes contributes to the effective tunneling DOS at the tip of the leads, resulting in transport resonances on the order of a few meV. Indeed, we can use a very simple particle-in-a-box estimate for the average level spacing. To account for the roughly even spacing of the observed resonances we assume a harmonic confinement potential [46], which was discussed in more detail in section 6.4.5:

$$\Delta E_{harm} = \frac{\hbar}{g}\sqrt{\frac{8V}{m^*}}\frac{1}{L} \tag{7.2}$$

Here, m^* is the electron effective mass, L is the width of the lead, and g accounts for the spin and valley degeneracies. V is the height of the parabolic potential well which we assume to be on the order of ∼100 meV in agreement with previous studies on tunnel junctions [100]. Using a spherically averaged effective mass of $0.28\,m_e$ [35], a width of

16 nm, and assuming two-fold spin and 4-fold valley degeneracy[7] ($g = 8$), we find an expected level spacing ΔE of ∼3 meV, in reasonable agreement with the observed data. Another possible explanation is that some of the features may be due to disorder-induced fluctuations in the local density of states in our highly doped leads [187, 146].

Excited states of confined quantum structures are commonly identified via their effect on the sequential tunneling characteristics. In the case of transport devices these manifest themselves in the form of lines of increased conductance in the un-blockaded regions [46]. In addition to the DOS related features, one would therefore expect to find resonances arising from excited states of the single P impurity. The energies of the lowest D^0 excited states for isolated phosphorus donors in bulk silicon are summarized in table 7.2. The 6-fold degeneracy of the conduction band minimum of bulk silicon is reflected by the manifold of six 1s states, comprising the ground state and the first two excited states. The nomenclature commonly used in the literature derives from group theory[8] and reflects the symmetry of the corresponding state.

The proximity of gates and interfaces has been found to strongly influence the excited states of other single donor transport structures via the Stark shift in gate electric fields on the order of several MV/m [165, 230]. However, in our device the gate voltage is typically applied symmetrically to both in-plane gates on either side of the transport channel. As a result, the gate electric field at the position of the donor is most likely negligible and no Stark shift is expected. Furthermore, the donor is encapsulated deep in the silicon crystal and thus not affected by any interface-related confinement [165]. In the absence of nearby interfaces and strong gate electric fields, we would thus expect to see resonances at the positions indicated in Fig. 7.11 a, where the gate voltage is applied to both gates in parallel. However, we do not see any clear indication of the excited states in the data. For $V_{SD} > 0$, no features are visible at the corresponding energies, but this is likely to be due to the asymmetry in the tunnel coupling which reduces the visibility of the features with a negative slope. For $V_{SD} < 0$, no conductance line is immediately obvious for the 1s(T_2) state. While we do find one resonance at ∼13 meV which may indeed originate from the 1s(E) state, the latter could also be due to a DOS feature that coincidentally resides at that particular energy. Fig. 7.11 b shows the same transition for a different gate voltage configuration. Here, only V_{G2} is swept while keeping V_{G1} at a fixed value of 750 mV. This allows the background charging feature causing switching noise in Fig. 7.11 a (indicated by the white arrow) to be moved out of the window. Apart from this, the both sweeps

[7] see section 2.2

[8] Donor eigenstates in silicon belong to the tetrahedral (T_d) point group [32].

Excitation spectrum of P donors in bulk Si

State	Nomenclature	ΔE (meV)	Degeneracy
GS	$1s(A_1)$	0	1
1^{st} ES	$1s(T_2)$	11.70	3
2^{nd} ES	1s(E)	13.01	2
3^{rd} ES	$2p_0$	34.11	6
4^{th} ES	$2p_\pm$	39.19	12

Table 7.2: The excited state (ES) energies of the D^0 state for isolated P donors in bulk silicon [168, 225]. Their energy ΔE is given with respect to the ground state (GS) energy, 45.6 meV below the silicon conduction band edge.

show essentially the same spectrum, which further highlights the stability of our device. We conclude that for our sample the direct determination of excited states from the unblockaded region of the stability diagram is inconclusive due to the dense spacing and relative predominance of resonances arising from the strongly modulated DOS in the leads. However, higher-order tunneling processes can provide a means to separate lead-related features from those that are a clear signature of the donor spectrum [146].

7.4.5 Observation of co-tunneling features

With Coulomb peak conductances on the order of several 100 nS the coupling between donor and leads in our device is sufficiently strong for co-tunneling features to become visible within the Coulomb blockaded region [231] of the D^0 diamond. The latter is illustrated on a logarithmic scale in Fig. 7.12 a. Panel b of the same figure depicts a bias sweep at a fixed gate voltage which shows a strongly rising conductance with clear peaks within the blockaded region. To increase the visibility of these resonances in the stability plot we have subtracted a smoothed curve (indicated by the red line) for every value of V_G.

Co-tunneling processes can be either *elastic* (in which case the corresponding conductance lines may reflect local maxima of the DOS in the leads [146]) or *inelastic* via a donor excited state [231]. In the latter case, the applied bias must exceed the lowest excitation energy of the dot, $eV_{SD} \geq E_1$, and the corresponding features are typically found to be more pronounced with a clear step in the current [146].

Conductance resonances in the co-tunneling regime are visible as roughly horizontal lines within the D^0 diamond in Fig. 7.12 c. While there are several such lines for $V_{SD} < 20$ mV, two sets stand out due to their relative magnitude and – more importantly – the fact that they are symmetric in V_{SD}. They occur at bias voltages of $\sim \pm 15$ mV and ~ 11 mV and

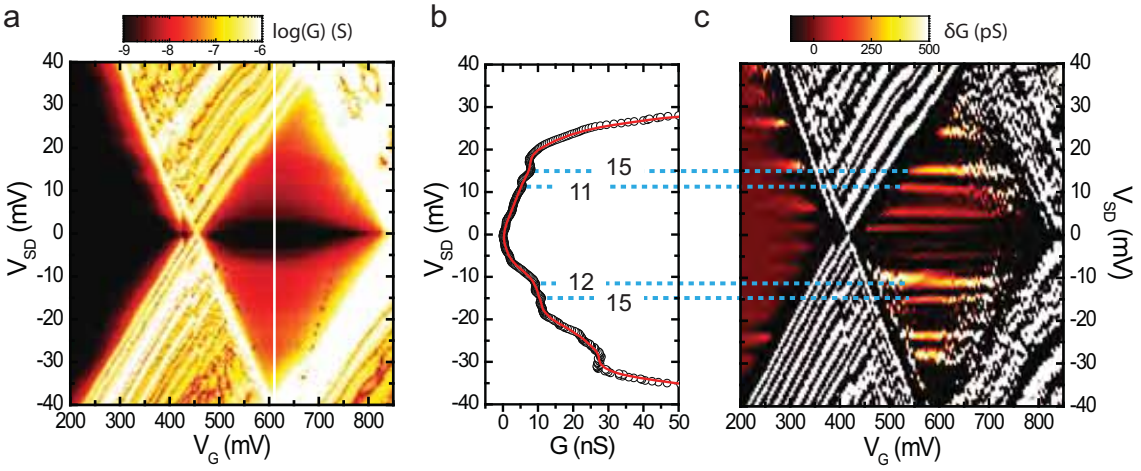

Figure 7.12: Co-tunneling features of D^0 **a**, When plotting the device conductance on a logarithmic scale, structure within the blockaded region of D^0 becomes visible, indicating higher-order co-tunneling processes. **b**, The conductance as a function of bias voltage (at a fixed gate voltage indicated by the white line in **a**) shows clear peaks. **c**, To make these peaks more visible on the strongly rising background, we subtract a smoothed curve (red line in **b**) for every V_G. Two prominent sets of resonances, symmetric in V_{SD} are remarkably similar in energy to the first two excited states E_1 and E_2 for isolated P donors in bulk Si.

$\sim -12\,\mathrm{mV}$, respectively. Remarkably, these values are very close to the first two excited state energies of P donors in bulk silicon [225] of $E_1 = 11.70\,\mathrm{meV}$ and $E_2 = 13.01\,\mathrm{meV}$ for the $1s(T_2)$ and the 1s(E) state, respectively (see table 7.2). In contrast to previous reports, where the bound states of single donors were found to be strongly influenced by nearby interfaces and strong gate electric fields [165], our planar architecture thus allows for level spectroscopy of a single impurity with a bulk-like spectrum.

There are additional features in the co-tunneling spectrum, many of which are less pronounced or do not seem to occur in pairs symmetric in V_{SD}. These may be due to elastic co-tunneling processes, reflecting peaks in the density-of-states in the leads [146]. Another prominent and symmetric set of lines is observed at approx. $\pm 24\,\mathrm{meV}$. The origin of this feature is not yet understood since the next bulk excited state is $\sim 34\,\mathrm{meV}$ above the ground state. Due to the weak electric field in our device it seems unlikely that this $2p_0$ excited state would be Stark-shifted so significantly.

7.4.6 Magnetic field dependence

The following section gives a summary of the magnetospectroscopy measurements on our single donor device. The experiments were performed in a parallel magnetic field up to 8 T.

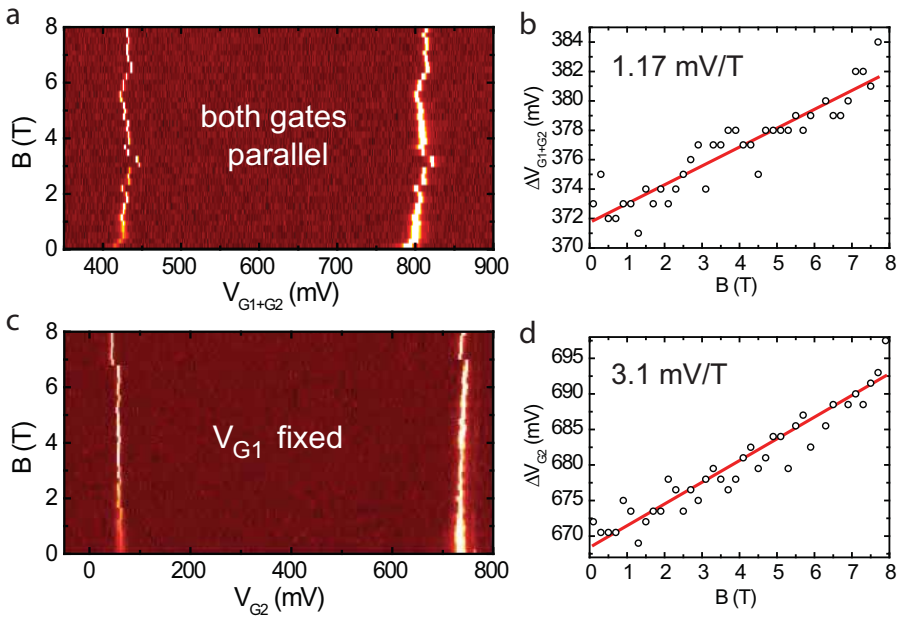

Figure 7.13: Coulomb peak spacing vs. B. a, The gate voltage was swept for different parallel B-fields. Both gates were used in parallel. The extracted peak spacing ΔV along with a line fit is shown in **b**. Using a lever arm of $\alpha \approx 0.1$ we obtain a g-factor of approx. 2.0. **c**, The same measurement sweeping only V_{G2} while keeping $V_{G1} = 950\,\mathrm{mV}$ fixed shows considerably less switching noise. **d**, The extracted peak spacing can be used to calibrate the average lever arm for gate $G2$ within the D^0 region.

Coulomb peak spacing vs. B

To further confirm that we are indeed measuring transport through a single donor, we have measured the Coulomb peak spacing as a function of a magnetic field B, as illustrated in Fig. 7.13. A magnetic field breaks the spin degeneracy of the donor states, splitting them into a spin-down[9] and a spin-up state which are separated by the Zeeman energy $E_Z = \pm 2\Delta s_z g \mu_B B$ [45]. Here, g is the gyromagnetic or g-factor which for electrons in silicon is very close to the free-electron value of $g = 2$ [206], μ_B is the Bohr magneton, and $\Delta s_z = \pm\frac{1}{2}$ is the total change in spin momentum associated with a particular charge transition. For D^0, the spin-down level thus becomes the ground state resulting in a shift of the corresponding $D^+ \leftrightarrow D^0$ Coulomb peak towards lower gate voltages. Conversely, the $D^0 \leftrightarrow D^-$ peak is expected to shift up in gate voltage since the second "incoming" electron must be spin-up, forming a singlet ground state due to the Pauli exclusion principle.

In Fig. 7.13 a the gate voltage was applied to both gates in parallel. The many switching events are most likely due to the charge fluctuations of a nearby charge trap as the gate

[9] By convention, "spin-down" refers to the spin oriented parallel to B which is lower in energy.

voltage is repeatedly swept over a large range in a comparatively short time[10]. To minimize the error arising from this noise as well as from long term drift in the absolute peak positions, we extract the peak spacing for the D^0 as illustrated in Fig. 7.13 b. We find that the width of the D^0 diamond increases as a function of the applied B field, which is the expected behavior for a single donor as described above. A linear fit (indicated by the red line) yields a slope of 1.17 mV/T which (using a gate lever arm $\alpha \approx 0.1$) translates into an energy shift of 117 μeV/T. From the latter we determine an experimental value for the g-factor of ∼2.0, in excellent agreement with the expected value.

To reduce the switching noise in the magnetospectroscopy data, we have repeated the sweep for different gate configurations. In Fig. 7.13 c, only the voltage on $G2$ was swept while keeping V_{G1} at a fixed value of 950 mV. Indeed, the peak positions are much more stable which indicates that the charge trap remains in a stable configuration. It is thus plausible that the charge trap is located closer to gate $G1$ resulting in a stronger coupling to the latter. The extracted peak spacing is depicted in Fig. 7.13 d. Using the g-factor of 2.0 determined from panel b, we can now use the slope of the linear fit to estimate the average lever arm for gate $G2$. We obtain $\alpha_{G2} \approx 0.04$ which is in reasonable agreement with the determined capacitance values summarized in table 7.1.

Resonance spectrum as a function of B-field

Fig. 7.14 a shows a close-up of the first charge transition for different magnetic fields. The transition is found to shift towards lower gate voltages which is consistent with the magnetospectroscopy data of Fig. 7.13. While the resonance pattern remains roughly the same, slight changes are visible, particularly at low bias voltages. As discussed in the previous section, a magnetic field splits the one-electron state D^0 into a spin-down ground state and a spin-up excited state. The latter is commonly seen as an additional conductance feature separated from the GS line by the Zeeman energy [152, 166]. To check for Zeeman splitting of the GS line, we perform bias sweeps at a fixed gate voltage while increasing the magnetic field in small increments. Here, we only consider the negative bias side since we do not expect to see the spin excited state for $V_{SD} > 0$ due to the coupling asymmetry. The resulting magnetospectroscopy data is illustrated in Fig. 7.14 b where we convert V_{SD} into an energy via a simple geometric factor that accounts for the slopes of the Coulomb diamond. Since we keep the gate voltage fixed, the shift of the charge transition along the gate axis translates into the observed linear shift of the GS

[10]Stability of our devices was discussed in more detail in section 6.4.4.

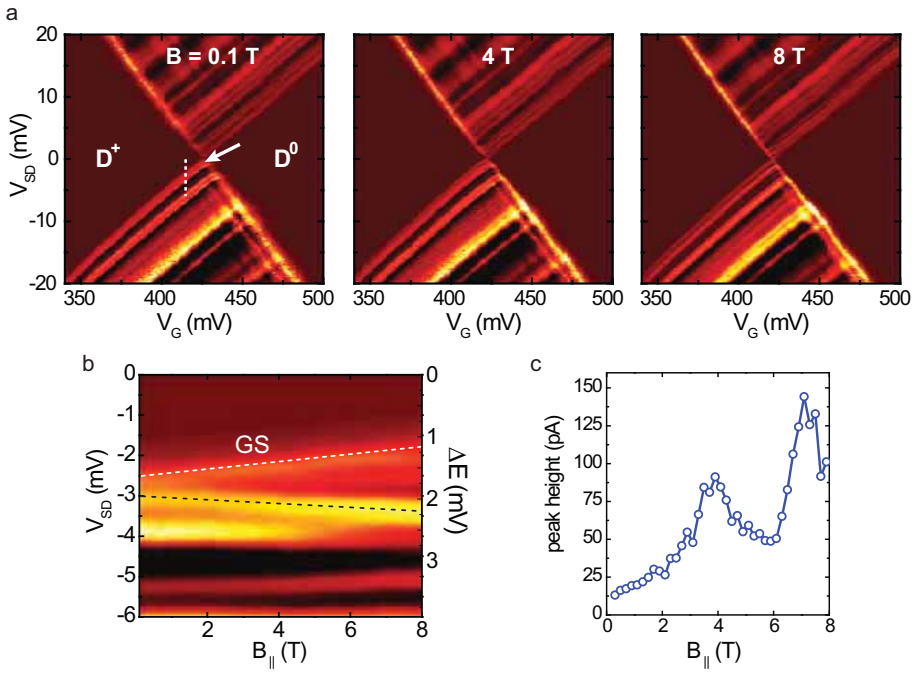

Figure 7.14: Magnetospectroscopy. **a**, A close-up of the $D^+ \leftrightarrow D^0$ for different magnetic fields. The ground state (GS) line (indicated by the arrow) of D^0 is expected to split into a spin-down GS and a spin-up excited state. **b**, To investigate possible Zeeman splitting of the GS line, we have performed direct magnetospectroscopy at a fixed gate voltage (indicated by the dotted line in **a**). Here, a simple geometric factor converts V_{SD} into an energy ΔE, shown on the right y-axis. The slope of the GS line ($\approx$59 μeV/T) reflects the linear shift of the first charge transition to lower gate voltages by the Zeeman term $-\mu_B B$. We observe a low-bias resonance (black dotted line) that moves away from the GS line. However, the slope of this feature ($\approx$ 30 μeV/T) is only half of the expected value for the spin excited state. Instead, we attribute this resonance to a DOS peak in the source electrode which moves with respect to the GS line as the latter shifts with B. This is further evidenced by an observed modulation of the Coulomb peak height (V_{SD} = 100 μeV) of the $D^+ \leftrightarrow D^0$ transition.

line along the bias axis. The experimental slope of $\sim$59 μeV/T is in excellent agreement with the expected value of $\mu_B \approx 57.8\,\mu$eV/T. We also find a resonance that is very close to the GS line at zero field and moves the opposite direction, indicated by a black dotted line. However, its slope of $\sim$30 μeV/T is only half the expected value for the spin excited state. Furthermore, close inspection of the feature reveals that there is a finite splitting between both lines even around zero field. We thus attribute this feature to a DOS peak in the source. Indeed, resonances arising from a strongly modulated DOS in the leads have previously been found to shift linearly in a magnetic field with a slope corresponding to half the Zeeman energy [147].

Fig. 7.14 c shows the peak height of the first charge transition as a function of B. We find a strong modulation on a scale of a few T. A similar behavior was already observed for

the few-electron dot (section 6.6.3). It is plausible that this modulation is caused by DOS features crossing the GS line as the corresponding $D^+ \leftrightarrow D^0$ transition shifts with B. We conclude that like the orbital excited states, the spin excited state is masked by the relative predominance of the DOS features. However, it is possible that further improvements in the layout of future devices will enable direct spectroscopy of the excitation spectrum of single donors. In particular, wider tunnel gaps resulting in a lower coupling may reduce the disparity between extrinsic resonances caused by a strongly modulated DOS in the leads and intrinsic features arising from donor excited states.

7.5 Chapter summary

The importance of single donor architectures for future nanoelectronic devices has been highlighted in a very recent review article by Koenraad *et al.* [208], identifying "STM-controlled placement of P and subsequent overgrowth by silicon" as "the most promising method at the moment" for the controlled scaling of silicon devices towards the single-donor limit. This limit has been reached with the experimental realization of the STM-patterned single donor transport device described in this chapter. From an extensive statistical study we determine the ideal size of the H-desorbed region for the reliable incorporation of exactly one phosphorus donor. For a desorbed patch of 3 adjacent dimers along one dimer row we find a $\sim$70% probability of incorporating one P donor when using a phosphine dosing exposure of $\sim$14 Langmuir. Furthermore, we estimate the spatial positioning accuracy for the individual impurity to be better than ± 6 Å.

We have reported low-temperature spectroscopy of a gated single phosphorus donor in a single-crystal silicon transport device. In addition to the unprecedented patterning accuracy of our fabrication approach, there is no ambiguity as to the type of dopant within the channel in contrast to recent publications [165, 209]. We find a stability diagram that is consistent with the 3 possible charge states of a single donor. The measured charging energy of the charge-neutral D^0 state is in good agreement with the value for P in bulk silicon. While we are not able to identify the donor excited states directly from the stability plot, we observe clear indications for bulk-like excited states in the co-tunneling characteristics.

Controlling the doping profile as well as the location of individual dopants will be crucial for future scaling of classical devices in silicon. Furthermore, this chapter highlights how STM-based fabrication techniques provide a viable pathway for the scale-up of novel donor-based quantum computation architectures.

Chapter 8

Conclusions and future work

This thesis has demonstrated that STM hydrogen lithography can be used as a viable tool to realize planar highly-doped quantum dot devices in silicon. We have shown how the size of these dopant-based quantum dot structures can be reduced from the many-electron regime to the single donor limit. This down-scaling was achieved in several steps, which have been discussed in detail in chapters 5 to 7. An initial requirement for successful down-scaling was to improve the alignment accuracy of our fabrication scheme. In chapter 4, we have developed an improved strategy to align *ex-situ* metallic contacts and top gates to the dopant regions with an overall alignment accuracy of $\sim$100 nm. This method relies on a hierarchical array of alignment markers which is etched directly into the Si substrate and therefore avoids possible surface contamination by any foreign materials. A defining feature of this new alignment strategy is the controlled formation of step-free areas in the middle of a central etched marker, which allows the active area of a device to be patterned on a single atomic plane. We have highlighted the importance of this for possible applications in quantum computation architectures, that rely on the atomically precise positioning of arrays of individual donors. Furthermore, we have introduced a new method to form reliable ohmic contact to the overgrown dopant structures by using vertically etched contact vias that form contact channels between the EBL-patterned metallic leads and the buried STM-patterned μm-sized contact patches below.

While individual components of a complete device architecture (such as donor nanowires, nm-scale tunnel junctions, and isolated P-doped nano-islands) had previously been realized by STM-lithography, a major remaining obstacle was the ability to electrically gate devices. In chapter 5 we showed how donor-based in-plane gates can be used as a viable alternative to top gates to reliably tune the electrochemical of a quantum dot. Here, we demonstrated a fully functional multiterminal quantum dot which was the first STM-

patterned dopant-based device to show Coulomb blockade. We found that the in-plane gates allow for highly stable operation of the device by circumventing the detrimental effects of interface or surface related defects. To highlight this fact, we compared the initial stable measurements of the planar device to transport data that was obtained after a metallic top gate was added to the structure. We found superior stability without the top gate which we attribute to charged defects at the oxide interface underneath the top gate. As a result, all further devices fabricated during this thesis were patterned in an entirely planar architecture, without any surface gates. We outlined the particular challenges of down-scaling in a planar architecture with a key obstacle being the need to maintain sufficient device tunability by keeping good capacitive coupling between the in-plane gates and the dot. Here, we have shown how capacitance modeling can be used to help improve the geometry of future devices by predicting the lever arm.

The next step in down-scaling was discussed in chapter 6 where we presented a quantum dot in the few-electron regime with an estimated number of 7 P dopants forming the dot. Transport spectroscopy of this device at mK-temperatures revealed very stable Coulomb blockade oscillations again highlighting the advantages of a fully planar devices fabricated in a fully epitaxial silicon environment. We found a surprisingly dense set of well-resolved transport resonances with an average energy spacing on the order of 100 μeV. These resonances were attributed to valley splitting of the Δ-subbands in the conduction band resulting from the abrupt lateral confinement potential of the nm-scale donor device. To support our interpretation, we presented extensive effective mass calculations for our few-donor structure. These results are a testament to the importance of the valley degree of freedom in ultra-small silicon quantum devices. In particular, a deeper understanding of the physics of the sharp confinement potentials in our devices will be crucial for possible applications in donor-based quantum computation applications, where the interplay between valley and spin excited states has been identified as a possible source of decoherence.

The ultimate scaling limit of donor-based quantum dots was reached in chapter 7, where we demonstrated the controlled fabrication of a gated single donor transport device. The realization of this device followed an extensive statistical study that focussed on optimizing the size of the H-desorbed region for the reliable incorporation of exactly one phosphorus donor. Here, we found that for a desorbed patch of 3 adjacent dimers along one dimer row the probability of incorporating one P donor is $\sim$70%. The spatial positioning accuracy for this individual impurity was determined to be better than $\pm$6 Å, which is comparable to the Si lattice spacing.

We presented low-temperature transport spectroscopy of the gated single phosphorus donor in the single-crystal silicon environment of our device. We find a stability diagram that is consistent with the 3 possible charge states of a single donor. Importantly, the measured charging energy of the charge-neutral D^0 state is in good agreement with the value for P in bulk silicon. We also observe clear indications for bulk-like excited states in the co-tunneling characteristics. We attributed this to the absence of interfaces and strong gate electric fields which have been known to strongly affect the donor bound states in previous single donor devices.

The successful down-scaling of donor-based silicon quantum transport devices from the many-electron regime to the single donor limit is the key achievement of this thesis. This goal has been achieved in the comparatively short time span of a PhD thesis. As a comparison, for quantum dots in GaAs/AlGaAs heterostructures – arguably the best-studied quantum dot architecture – reaching the single-electron limit has taken well over a decade and was the result of a collaborative effort of many research groups. The STM-lithographic placement of P donors followed by epitaxial overgrowth has just recently been highlighted in a review report by Koenraad and Flatte [208] as the "most promising method" for the "controlled scaling of silicon devices towards the single-donor limit". The single-donor device presented in this thesis proves the validity of this statement. Indeed, our approach allows for precise control over the exact number of impurities as well as their position within the device with a spatial accuracy comparable to the lattice spacing. This result therefore presents an important step towards the realization of donor-based quantum computer architectures that rely on arrays of precisely positioned individual donors in silicon.

8.1 Future work

The results of this thesis form the basis for a multitude of exciting experiments that will need to be performed in the near future. It should be mentioned that several of these experiments are already on-going within our group. The projects can be roughly divided into three categories.

8.1.1 Device tunability

A remaining challenge of our planar architecture is the non-proximal coupling of the in-plane gates which affect both the dot potential as well as the tunnel coupling of the dot to the leads. To increase device control, it would be desirable to be able to tune the

tunnel coupling and the electrochemical potential of the dot independently. This is true in particular for devices containing a linear array of nm-scale dots or single impurities. Several possible solutions exist:

- *Improvement of device design*: By further optimizing the layout of the planar structures it may be possible to separate "plunger gates" (to control the dot potential) from barrier gates. An alternative may be to increase the number of gates to allow for local compensation of the potentials from gates that are farther away.

- *Integration of top gates*: We have previously shown that top gates have a different coupling characteristic compared to in-plane gates. By adding top gates to the planar architecture it may be possible to achieve better control over the potential landscape of the device. For example, the top gates could determine the overall tunnel coupling while the in-plane plunger gates could be used to locally compensate the top gate voltage and thus tune the dot potential. Key issues which need to be addressed in this context are the device stability in the presence of surface gates and a further improvement of the alignment accuracy of the top gates with respect to the donor device.

- *Reduction of gate leakage*: The main reason for the non-proximal coupling of the in-plane gates is their comparatively large separation to each other and to the dot. These large separations are necessary to reduce gate leakage through the (shallow) insulating barrier defined by the intervening intrinsic silicon substrate between the (n-type) phosphorus dopant regions. An alternative method to increase the effective barrier height may be to incorporate additional p-type dopant regions (from a separate doping source) between the gates and the dot. While this would require an additional STM-lithography step, the resulting pn-junctions could act as "channel stoppers" for leakage currents. Indeed, the VT-STM is already equipped with a suitable dosing source for (p-type) boron dopants.

8.1.2 Scale-up of single donor devices

Having reached the ultimate scaling limit of a single donor, the next goal is the controlled scale-up of devices that contain several individual impurities within at precise array. In chapter 7 we have shown that we can incorporate precisely one donor within a suitable desorbed area with a ∼70% chance. While this is sufficient to realize a single donor device, it is obviously too low to reliably fabricate a device that contains several individual

impurities. For example, for a device containing 3 P donors the overall success rate for incorporating one donor in each of the three designated incorporation sites would only be $0.7^3 \approx 0.34$. It will thus be necessary to further optimize the dosing and incorporation conditions to achieve an incorporation probability close to 1. Detailed studies are currently underway to achieve this.

The first step of scaling up will be the realization of a controlled double donor device. Here, the key issues will be to achieve independent gating of both impurities as well as controlling the coupling between the donors, as discussed above. A long-term goal will be to pattern several donors in a linear array. This may enable the demonstration of advanced gate operations such as the coherent charge transfer by adiabatic passage (CTAP) [109] along the donor chain.

8.1.3 Spin measurements

A donor-based quantum computer architecture relies on measuring and controlling the nuclear and/or electron spins of individual donors. An important first step in this direction will be measuring the electron spin state of an isolated P impurity. This has only recently been demonstrated for the spin of a single electron bound to a phosphorus donor in silicon [232]. This is achieved by coupling a single electron transistor (SET) to the impurity. By applying a magnetic field, the electron spin states of both the donor and the SET island are split by the Zeeman energy. The relative tuning between the spin-split levels in donor and SET can be controlled by suitable gate pulses so that only electrons with a certain spin state can tunnel between the two. This allows for a single-shot readout of the spin state of the donor electron. Furthermore, the evolution of the spin state can be measured as a function of time which yields the lifetime T_1 of that particular spin state. The latter is an important parameter for possible quantum computation applications since it defines an upper limit for duration of logical qubit operations.

Experiments are currently underway in our group to reproduce the spin readout scheme described above in our planar architecture. Here, the SET is realized by a many-donor quantum dot similar to the one presented in chapter 5 of this thesis. This planar SET is weakly coupled to a single P donor which is patterned at a distance of a few 10's of nm from the island of the SET. Determining the spin lifetime characteristics of our system will be an important step towards fabricating a donor-based silicon qubit.

Appendix

A.1 Statistical incorporation array studies

In order to estimate the number of phosphorus atoms in the few-donor quantum dot device presented in chapter 6, a statistic study of incorporation sites was carried out in collaboration with Dr. J. Miwa and W. Tang.

For δ-doped Si:P samples [43] as well as μm-scale desorbed areas [44] we reliably obtain a planar dopant coverage of $\sim$0.25 ML. For nm-scale desorbed areas, however, the density of incorporated P donors is found to decrease which we attribute to an edge effect: a PH_3 molecule at the edge of the desorbed area does not have enough Si dangling bond sites to lose all of its 3 H atoms and can thus not be incorporated. To quantify the resulting decrease of doping density, we have STM-patterned an array of desorption sites (see Fig.

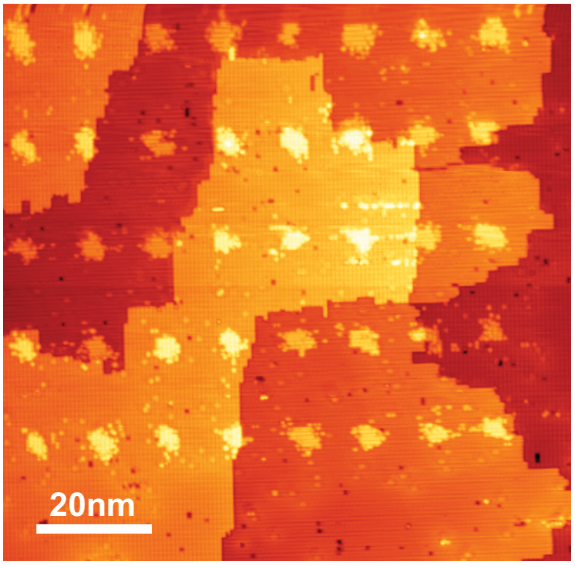

Figure A.1: Array of incorporation sites. STM image of a 8×5 array of desorption sites (bright areas) that are similar in size ($\sim 4 \times 4\,\mathrm{nm}^2$) to the few-donor quantum dot presented in chapter 6. Each desorption site was subsequently imaged in higher resolution both before and after the dosing and incorporation step (see Fig. A.2). Several of these arrays were patterned.

A.1) approximately the same size ($\sim$4×4 nm^2) as the few-donor quantum dot of chapter 6. The incorporation anneal parameters were identical to the ones used for the quantum dot device (30 s at 350°C). Four exemplary desorption sites are shown in Fig. A.2. By imaging each desorption site before (top row) and after the incorporation step (bottom row) we can directly determine the number of incorporated P atoms as a function of the number of desorbed Si dangling bonds (DB). The number of P donors for each site can be determined from the number of ejected Si adatoms, indicated by the black circles in the bottom row of Fig. A.2.

While it is in principle possible to determine the number of P donors in an actual quantum dot device in a similar way, it requires a more elaborate registration marker structure to relocate the patterned area after the incorporation anneal. To reduce STM pattern-

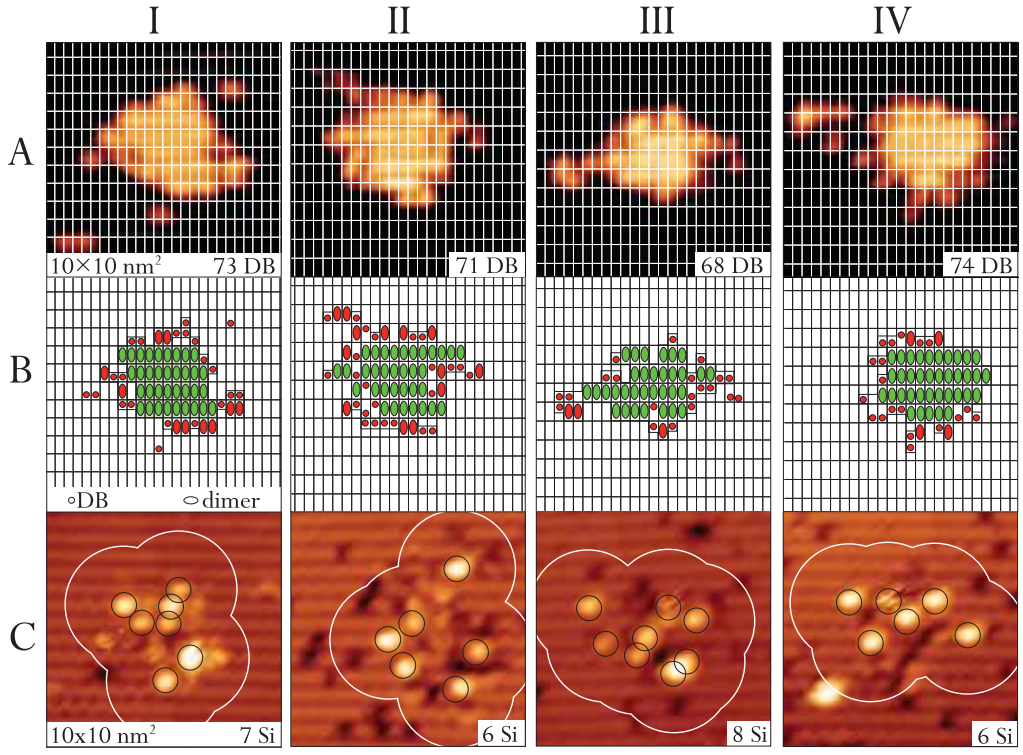

Figure A.2: P incorporation for comparable dot areas. Four exemplary desorption sites (column I-IV) that are very similar in size and shape to the few-donor dot presented in chapter 6. *Row A*: Close-up STM images of the H-desorbed sites before dosing and incorporation. The background has been darkened and a grid with dimer row spacing has been superimposed to count the number of Si dangling bonds (DB), analogous to Fig. 6.3 in chapter 6. *Row B*: The green areas represent possible P incorporation sites. *Row C*: The same sites after P incorporation. The number of incorporated P atoms for each site can be determined from the number of the ejected Si adatoms (black circles). The surrounding white line schematically illustrates the spatial extent of the electronic wavefunctions by adding one Bohr radius ($\sim$ 2.5 nm in Si) around each individual P incorporation site. The strong overlap justifies the treatment of the dot as a jellium of positive charge.

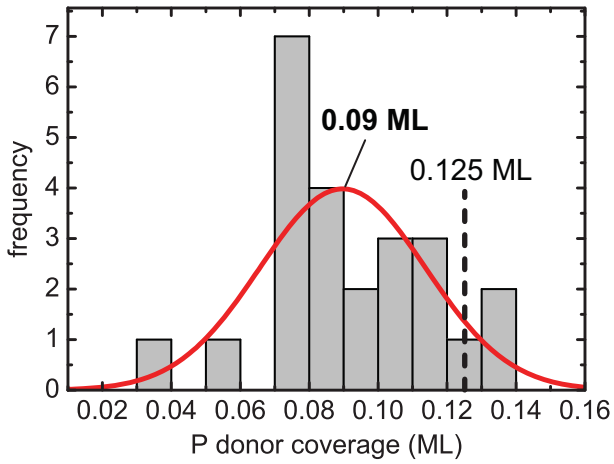

Figure A.3: Donor counting statistics. Phosphorus donor coverage of nm-scale H-desorbed areas such as shown in Fig. A.2. The data was obtained from 24 desorption sites, very similar in size and shape to the few-donor quantum dot presented in chapter 6. A Gaussian fit to the data (red curve) peaks at a P donor coverage of 0.09 ML for contiguous desorbed areas. For our dot this yields a most likely number of $N = 6 \pm 3$ donors in the dot. For the effective-mass calculations we assume a P coverage of 0.125 ML which lies well within the variance of the data.

ing time and minimize the risk of surface contamination, the STM imaging step after P incorporation was avoided for the quantum dot device described in chapter 6.

The results of the desorption array study are summarized in the histogram of Fig. A.3 where we plot the relative occurrence of different P donor coverages (expressed as a fraction of a monolayer) for the array sites. A Gaussian fit to the data peaks at a P coverage of 0.09 ML. For the few-donor dot of chapter 6 with a desorbed area of 66 dangling bonds (see Fig. 6.3) this translates to an estimated number of 6±3 P donors. The error reflects the variance of the data in Fig. A.3. Even though a P coverage of 0.09 ML is lower than in δ-doped layers, the average spacing between the donors (∼13 Å) is still much smaller than the Bohr radius of ∼2.5 nm in silicon. This is illustrated in the bottom row of Fig. A.2 where we have added one Bohr radius around every P incorporation site as indicated by the white lines. The strong overlap justifies the treatment of the dot as a jellium of positive charge.

Since our effective-mass calculations use the energy splitting between the Γ_1 and Γ_2 subbands of δ-doped Si as an input parameter, we use the published value [37] which is closest to the donor density found for our dot structures, namely 0.125 ML. While this does not exactly coincide with the peak value of 0.09 ML derived from our array experiments, it is still well within the variance of the experimental data (Fig. A.3).

A.2 Effective mass calculations for the laterally confined dot

In chapter 6 we have calculated the low-bias excitation spectrum of a few-donor silicon quantum dot. Here, the strong confinement within the dot was found to lift the degeneracy of the Δ levels causing transport resonances on the order of $\sim 100\,\mu$eV. The following section gives some more details on how the valley splitting was calculated.

For the Δ band, two envelope functions are required[1] to describe the lateral component of the wavefunctions due to the anisotropic effective mass:

$$\begin{aligned} E_x F_{\Delta_x}(x,y) &= \left[-\frac{\hbar^2}{2m_l}\frac{\partial^2}{\partial x^2} - \frac{\hbar^2}{2m_t}\frac{\partial^2}{\partial y^2} + V(x,y)\right] F_{\Delta_x}(x,y) \\ E_x F_{\Delta_y}(x,y) &= \left[-\frac{\hbar^2}{2m_l}\frac{\partial^2}{\partial y^2} - \frac{\hbar^2}{2m_t}\frac{\partial^2}{\partial x^2} + V(x,y)\right] F_{\Delta_y}(x,y) \end{aligned}$$

It is easily seen that $F_{\Delta_x}(x,y) = F_{\Delta_y}(y,x)$ which reflects the radial symmetry of the problem.

As discussed in chapter 6, valley splitting of the 4-fold degenerate Δ levels is calculated using a perturbation approach represented by the matrix equation

$$\begin{pmatrix} E^{(0)} & \Delta_{11} & \Delta_{12} & \Delta_{13} \\ \Delta_{11}^* & E^{(0)} & \Delta_{22} & \Delta_{23} \\ \Delta_{12}^* & \Delta_{22}^* & E^{(0)} & \Delta_{33} \\ \Delta_{13}^* & \Delta_{23}^* & \Delta_{33}^* & E^{(0)} \end{pmatrix} \begin{pmatrix} \alpha_{-x} \\ \alpha_{+x} \\ \alpha_{-y} \\ \alpha_{+y} \end{pmatrix} = E \begin{pmatrix} \alpha_{-x} \\ \alpha_{+x} \\ \alpha_{-y} \\ \alpha_{+y} \end{pmatrix} \tag{A.1}$$

The (complex) off-diagonal elements $\Delta_{\mu\nu}$ are the valley splitting terms, many of which are identical due to the radial symmetry. To evaluate these terms, the wavefunctions are expressed as pairs of even and odd combinations of the valley states along the Δ_x and Δ_y direction, respectively,

$$\begin{aligned} \Psi_e(\mathbf{r}) &\sim \cos(k_0\xi) F_{\Delta_\xi}(x,y) \\ \Psi_o(\mathbf{r}) &\sim \sin(k_0\xi) F_{\Delta_\xi}(x,y) \end{aligned}$$

where $\xi = x, y$. We thus obtain

$$\Delta_{11} = \Delta_{33} = \int \cos(2k_0 x) F_{\Delta_x}^2(x,y) V(x,y) dx dy$$

$$\Delta_{12} = \Delta_{22} = \Delta_{13} = \Delta_{23} = \int \cos(k_0 x)\cos(k_0 y) F_{\Delta_x}(x,y) F_{\Delta_y}(x,y) V(x,y) dx dy$$

[1] This is in contrast to the single *vertical* component $F_\Delta(z)$ of eq. (6.9).

The integrals are all real (i.e. $\Delta_{\mu\nu} = \Delta^*_{\mu\nu}$) and involve only cosine terms due to wavefunction symmetries. Diagonalizing eq. (6.12) then yields the valley-split energy eigenvalues which are depicted in Fig. 6.16 of chapter 6:

$$\begin{aligned} E_1 &= E^{(0)} + \Delta_{11} + 2\Delta_{12} \\ E_2 &= E^{(0)} - \Delta_{11} \qquad \text{(2-fold degenerate)} \\ E_3 &= E^{(0)} + \Delta_{11} - 2\Delta_{12} \end{aligned}$$

Anisotropy splitting

The remaining 2-fold degeneracy is a result of the circular symmetry. It is lifted by considering the anisotropy of the confinement potential in the realistic device. A perturbative approach is used to account for this anisotropy which is characterized by a single parameter E_{anis}. Eq. (A.1) is then replaced by

$$\begin{pmatrix} E^{(0)} - \frac{E_{anis}}{2} & \Delta_{11} & \Delta_{12} & \Delta_{12} \\ \Delta_{11} & E^{(0)} - \frac{E_{anis}}{2} & \Delta_{12} & \Delta_{12} \\ \Delta_{12} & \Delta_{12} & E^{(0)} + \frac{E_{anis}}{2} & \Delta_{11} \\ \Delta_{12} & \Delta_{12} & \Delta_{11} & E^{(0)} + \frac{E_{anis}}{2} \end{pmatrix} \begin{pmatrix} \alpha_{-x} \\ \alpha_{+x} \\ \alpha_{-y} \\ \alpha_{+y} \end{pmatrix} = \tilde{E} \begin{pmatrix} \alpha_{-x} \\ \alpha_{+x} \\ \alpha_{-y} \\ \alpha_{+y} \end{pmatrix}$$

Diagonalizing above matrix yields the 4 non-degenerate energy eigenvalues shown in Fig. 6.17:

$$\begin{aligned} \tilde{E}_{1,2} &= E^{(0)} - \Delta_{11} \pm E_{anis}/2 \\ \tilde{E}_{3,4} &= E^{(0)} + \Delta_{11} \pm \sqrt{4\Delta_{12}^2 + (E_{anis}/2)^2} \end{aligned}$$

A.3 Few-electron quantum dot: Modeling results for different donor numbers

We have modeled the transport spectrum as discussed above for a variety of different combinations of donor and electron numbers on the dot, consistent with the range of possibilities for 6 ± 3 P dopants. The results are summarized in Fig. A.4. As discussed in section 6.5, the best match to the experimental data of Fig. 6.13 corresponds to a seven-donor dot at the Coulomb blockade transition between seven and eight electrons (highlighted in red in Fig. A.4).

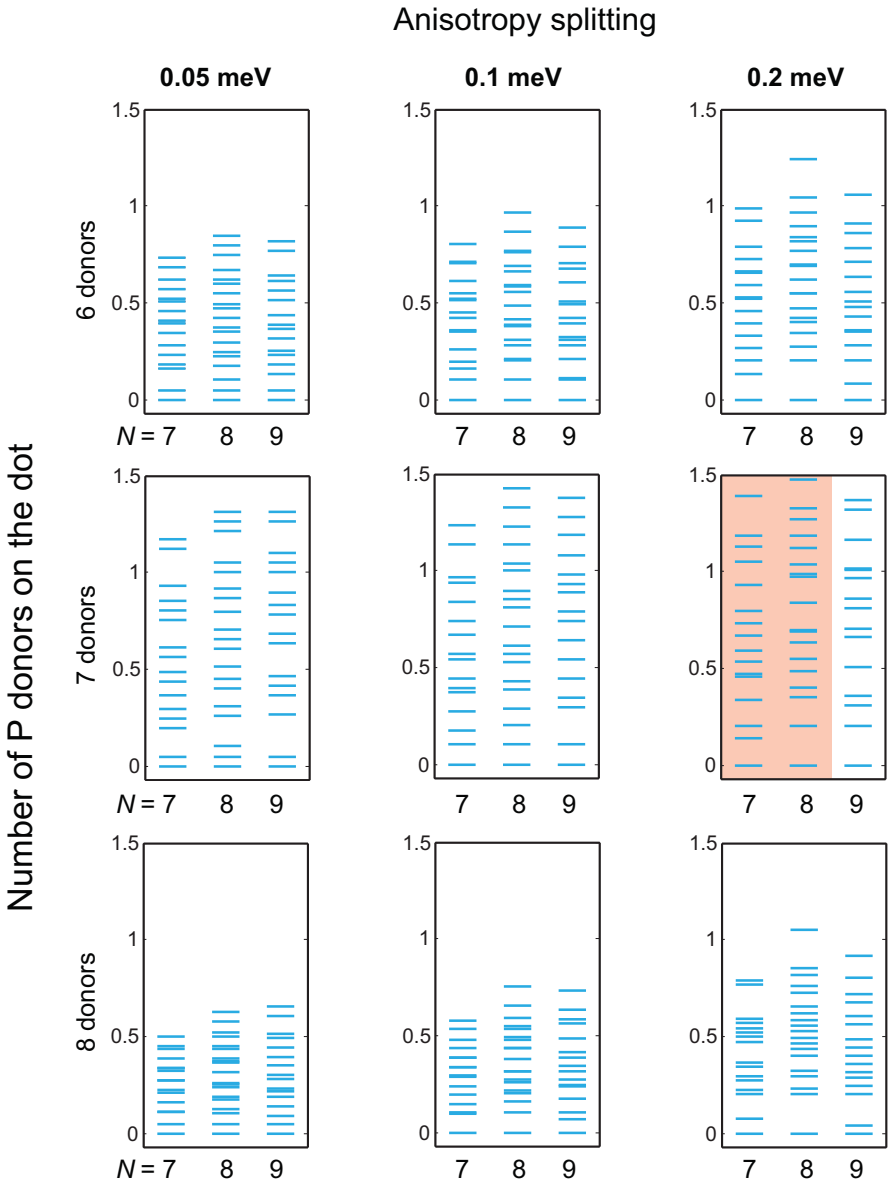

Figure A.4: Calculated resonance spectra for different donor numbers. Overview of the calculated excited state energies for the few-donor quantum dot discussed in chapter 6 assuming the dot to contain 6, 7, and 8 phosphorus donors, respectively. For each donor number the resulting resonance spectrum is shown for a varying number of electrons on the dot, $N = 7, 8, 9$. The asymmetry in the confinement potential due to the statistical incorporation of the P donors is accounted for by a perturbation approach characterized by a single anisotropy parameter. For visual clarity, the spectra for each configuration are shown for three discrete values of this anisotropy splitting. The best fit to the experimental data was obtained for the configuration highlighted in red.

A.4 Recipes

Post-processing of completed STM-patterned devices in a cleanroom environment is a crucial part of successful device fabrication. The following tables briefly summarize the process flow along with the relevant parameters for both the patterning of EBL-defined RIE-etched vertical contact vias as well as the EBL-patterning of *ex-situ* metallic contacts.

Processing of vertical contact vias

Step	Operation	Parameters/Description
1	Measure encapsulation thickness	Use Dektak or AFM to determine the thickness of the SUSI encapsulation
2	NPGS files	prepare NPGS e-beam patterning files for contact holes and Ohmics
3	Dehydration bake	180°C for 5 min on hotplate cool down for 2 min
4	Spin on double layer EBL resist	spin on 2 layers of PMMA A4 at 2500 rpm for 60 s, $\Rightarrow \sim$ 350-400 nm resist, avoid edge beads
5	Bake resist	10 min at 180°C on hotplate
6	EBL: write holes	write array of holes (100 nm diameter, 500 nm pitch), $E_{beam} = 15$ kV, spot size 2, area dose for holes: 3500 μC/cm^2
7	Develop resist	40 s MIBK:IPA = 1:3 then 20 s IPA stop bath, blow dry with N_2
8	RIE: etch holes	flow rates CHF_3:CF_4 = 10:10, chamber pressure $p = 14$ kPa, etch for 8 min at 150 W, $\Rightarrow$ approx. 60-70 nm etch depth
9	Remove PMMA	10 min in NMP at 40°C, squirt with acetone, then IPA, blow dry with N_2, O_2 plasma ash if necessary
10	SEM imaging	check for correct position of RIE holes

Processing of *ex-situ* aluminium contacts

Step	Operation	Parameters/Description
1	Dehydration bake	180°C for 5 min on hotplate cool down for 2 min
2	Spin on single layer EBL resist	spin on PMMA A4 at 5000 rpm for 30 s, $\Rightarrow \sim$ 100-150 nm resist
3	Bake resist	10 min at 180°C on hotplate
4	EBL: write Ohmics	write ohmic contact structure at $E_{beam} = 15$ kV, spot size 2-3 (inner contacts), 6 (bond pads), area dose 180 μC/cm^2
5	Develop resist	40 s MIBK:IPA = 1:3 then 20 s IPA stop bath, blow dry with N_2
6	Plasma ashing	remove residual resist on patterned Ohmics, 90 s O_2 plasma ash at 50 W
7	Remove native oxide	10 s in buffered HF (1:5 in H_2O), 30 s rinse in deionized water, blow dry with N_2
8	Metallization	deposit approx. 80 nm of Al
9	Remove resist	60 min in NMP bath at 40°C, ultrasonic bath if necessary, squirt off with acetone then IPA
10	Packaging	cleave sample if necessary, glue into chip carrier with PMMA, bond with Al wire bonder

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