

Achieving near 100% Fill factor for small pixel LGADs: Study of First Trench Isolated LGADs fabricated at Micron Semiconductor Ltd

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ABSTRACT: This paper presents the development and characterization of Trench-Isolated LGADs (TI-LGADs). This architecture replaces traditional junction termination structures with narrow trenches to minimize inter-pixel distance (IPD) and enhance fill factor (FF). Fabricated by Micron Semiconductor Ltd., TI-LGADs demonstrate excellent electrical isolation, low leakage currents, and no premature breakdown up to 1000 V. Transient Current Technique (TCT) measurements and TCAD simulations reveal an IPD of less than 5 μm , a significant improvement over standard LGADs which have an IPD of $\approx 50 \mu\text{m}$. The devices exhibit a gain of 2–3, consistent with simulations, and maintain good pixel isolation with minimal crosstalk. These results highlight the potential of TI-LGADs for fine-segmented, high-resolution 4D tracking applications, paving the way for future optimizations and radiation-hard designs.

KEYWORDS: Particle tracking detectors (Solid-state detectors); Radiation-hard detectors; Solid state detectors; Detector modelling and simulations II (electric fields, charge transport, multiplication and induction, pulse formation, electron emission, etc)

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1 Introduction

Low-Gain Avalanche Diodes (LGADs) are silicon-based detectors recognized for their internal charge multiplication via impact ionization, typically achieving a low gain of $\mathcal{O}(10)$ [1]. LGADs are based on an n-on-p structure with an additional highly doped p^+ layer sandwiched between the p-bulk and the n-implant ($n^{++}-p^+-p-p^{++}$), resulting in a high field at the junction between the n^{++} and p^+ layers. The doping profile is carefully designed to create an electric field that is high enough to cause impact ionization, and hence charge multiplication, producing larger signals than those from a PIN diode. Subsequently, this enhances the signal-to-noise ratio (SNR), enabling LGADs to produce signals large enough to be separated from the noise, thereby improving the detection efficiency for low-energy or minimally ionizing particles. In the past decade, extensive research and development have been carried out to enhance the spatial and timing resolution of LGADs for precise track reconstruction and to develop these detectors to withstand extreme radiation fluences. 50 μm thick LGADs have demonstrated the capability to achieve timing resolutions below 30 ps [2, 3], and tolerate radiation fluences exceeding 10^{15} 1 MeV neutron equivalents per cm^2 ($\text{n}_{\text{eq}}/\text{cm}^2$) [4]. LGADs, with their exceptional properties, are not only a candidate for future high energy physics (HEP) experiments but also valuable in the fields of synchrotron, medical, and space applications [5–8].

LGADs show strong potential as a key technology for advancing 4-D tracking applications [9, 10], but are limited by the coarse segmentation of current technologies. To prevent early device breakdown from high electric fields near the periphery of the segmented junction electrodes, standard LGADs incorporate a deep n^+ implantation known as a Junction Termination Extension (JTE), and electrical isolation between the pads is achieved by a p^+ implant (p-stop or p-spray) [11]. A schematic view of the standard LGAD is shown in figure 1(a). There is a discontinuity in the gain layer near the JTE and p-stop implants, which makes this region a *no-gain* area. The gap between the gain layer implants is called the *Inter-Pixel Distance* (IPD). Electrons generated by a laser or a minimum ionizing particle

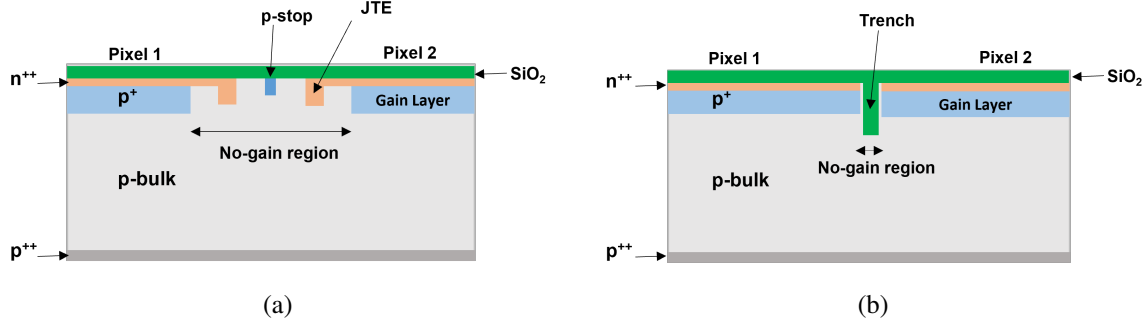


Figure 1. Schematic comparison of the (a) standard, and (b) trench-isolated LGAD.

(MIP) that drift into the no-gain region do not experience multiplication, which results in reduced charge detection efficiency [12], consequently, reducing the fill factor (FF). The FF is defined as:

$$FF = \frac{\text{pixel area with multiplication}}{\text{total pixel area}} \quad (1.1)$$

To increase the effective FF of LGADs, different strategies have been implemented in recent years, namely: i) inverse LGADs (iLGADs) [13], ii) Resistive silicon detectors (RSD) also known as AC-LGADs [14], and iii) Deep-Junction LGADs (DJ-LGADs) [15]. This paper focuses on an alternative segmentation architecture, known as Trench-Isolated LGAD (TI-LGAD). This architecture has been extensively implemented in CMOS technology [16] as well as in silicon photomultipliers [17] over the years. In this technique, electrical isolation to avoid crosstalk between pixels is achieved by etching physical trenches in the silicon substrate which are subsequently filled with silicon oxide [18, 19]. TI-LGADs replace the pixel periphery, consisting of the JTE and p-stop/p-spray, with a single narrow trench ($\approx 1\text{--}2\text{ }\mu\text{m}$ wide), potentially reducing the IPD to $< 10\text{ }\mu\text{m}$ [20]. The schematics of TI-LGAD can be seen in figure 1(b) compared to the standard LGAD. TI-LGADs enable IPD to be reduced to a few microns allowing fine segmentation of pixelated devices with a $FF > 90\%$ for 4D tracking applications [21]. In addition to the efforts put in by Fondazione Bruno Kessler (FBK) in producing several batches of TI-LGADs [22], this work focuses on the development of TI-LGADs by Micron Semiconductors Ltd., U.K.. In this work, extensive simulation studies are performed using Sentaurus TCAD to optimize the trench parameters, FF, and electrical isolation. Measurements carried out using the Transient Current Technique (TCT) to probe the inter-pixel electrical isolation are discussed along with the calculations of IPD and FF.

2 Fabrication of TI-LGADs

This study presents the first batch of TI-LGADs that is fabricated by Micron Semiconductor Ltd. These devices are designed to minimize the no-gain region, enable fine pixel segmentation, and enhance the FF, as explained in figure 1(b). Trench parameters, including width and depth, were optimized using TCAD simulations (values discussed later in this paragraph); therefore, no variations in these parameters were introduced in the fabrication of this batch. The trenches are fabricated at the Scottish Microelectronics Centre (SMC), Edinburgh, whereas the rest of the fabrication is performed at Micron Semiconductor Ltd., Lancing, U.K.. The optimal trench design is based on the capabilities of the tools at the SMC, which uses Deep Reactive Ion Etching (DRIE) [23], to etch trenches into the silicon.

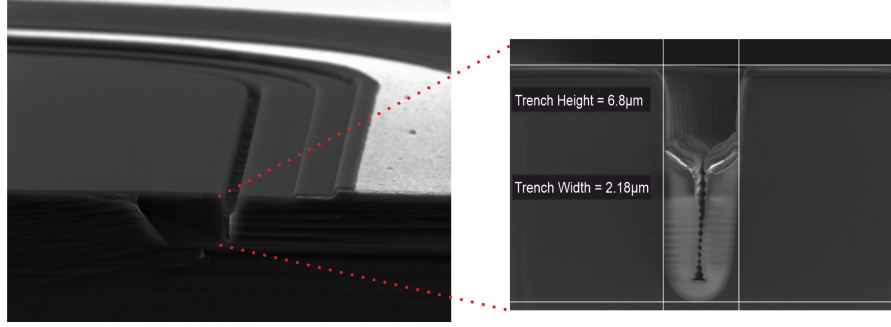


Figure 2. The image on the left is an SEM image that shows a cleaved detector and the fabricated trench that surrounds the active region. The image on the right shows a close-up of the trench with the final dimensions of the oxide-filled trench. Width = 2 μm , depth = 7 μm .

The key to the design is the control of the aspect ratio of the trenches. Careful control of the etching parameters allows deep and narrow trenches to be created. TCAD simulation shows that narrower trenches provide better isolation and that the depth of the trench does not have a significant effect on the isolation as long as the trench is deeper than the gain region, as shown in figure 3(a).

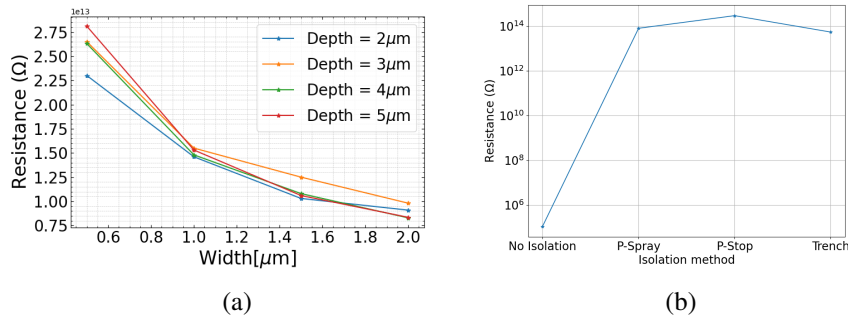


Figure 3. (a) Simulation of the dependence on the resistance between adjacent pixels as a function of trench width and trench depth. (b) Simulation of the dependence on the resistance between adjacent pixels for a variety of isolation methods.

In the simulation, isolation is evaluated by measuring the resistance between two adjacent pixels at a voltage above the full depletion, as described in ref. [24]. In these simulations, a fixed oxide charge was present at the interface of the trench with a value of $1 \times 10^{12} \text{ cm}^{-2}$. Based on feasible processing capabilities and simulation results, the optimized trench is 2 μm wide and 5 μm deep. Figure 2 shows an SEM image of the edge of a cleaved device. The trench is clearly seen surrounding the active region, left of the image. To the right of the trench is a bias ring. The image on the right of figure 2 shows the dimensions of the trench with a width of 2 μm and a depth of 7 μm . This is slightly deeper than the expected trench depth due to a slight over-etch of the trench to ensure the depth was greater than the critical value of 2 μm . One can see that the trench is not filled with oxide; this was due to the etching of the oxide prior to the junction implantation. The etching of the trench is caused by insufficient thermal oxide growth while filling the trenches, which resulted in an “open” trench. As the trench was slightly open, while performing the wet etch of the junction window, the etchant could enter the trench and therefore some oxide in the trench was chemically etched away.

However, based on simulations and experimental results, this does not affect the isolation capability of the trench. This is shown in figure 3(a) where the inter-pixel resistance is simulated as a function of the trench width and depth. One can see that by reducing the width of the trench, the resistance increases, however changing the depth of the trench has no significant impact on the resistance. It should be noted that for a trench with a depth of less than $2\text{ }\mu\text{m}$ the simulation showed early breakdown, hence these depths were not considered for the fabrication.

Simulations were performed using other typical isolation structures, such as the p-stop and p-spray, to verify the inter-pixel resistance achieved by the trenches is sufficient. Figure 3(b) shows the inter-pixel resistance for the different isolation methods, including a no-isolation method. The no-isolation method is used as a reference which is the same structure as the p-spray method but without the p-spray implantation. The resistance is measured for the case of a fixed oxide charge of $1 \times 10^{12}\text{ cm}^{-2}$, where the inter-pixel resistance shows comparable results for the p-spray, p-stop, and trench isolation methods. This verifies that the trench isolation method developed shows good isolation. As the fabrication process was limited in terms of the width of the trench, the final fabricated trench is designed to be $2\text{ }\mu\text{m}$. The fabrication of the TI-LGAD was performed on $250\text{ }\mu\text{m}$ thick, high resistivity, 6-inch p-type silicon wafers. Although fabrication on a $250\text{ }\mu\text{m}$ thick substrate is not ideal for timing studies, it serves as a proof-of-concept and may be useful in other applications that do not require a fast timing response.

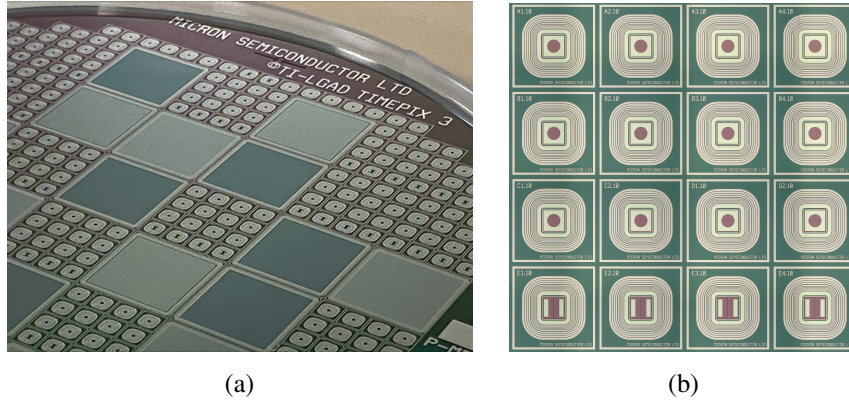


Figure 4. (a) Processed TI-LGAD wafer, (b) Pad test structures, 1st line contains A devices: LGADs with JTE, 2nd line contains B devices: LGADs with Trench and JTE, 3rd line contains C devices: PIN and D devices: LGADs with Trench, and bottom line are E devices: 2×1 Pixels with trench in the middle and around the pad.

This batch consists of 4 wafers, differing only in doping concentrations of the gain layer. The results from this paper are focused on the wafer with the expected gain of 3–4. The wafer layout contains both full-sized TimePix3 sensor arrays and pad test structures, hence the wafer layout consists of two types of blocks: TimePix3 sensor arrays and pad test structures. There are five types of pad test structures with an active area of $1 \times 1\text{ mm}^2$, described as follows:

- **A-devices:** 1×1 Standard LGAD pad with JTE used as the terminating structure.
- **B-devices:** 1×1 LGAD Pad with a combination of the JTE and the trench used as the terminating structure. The trench is located $5\text{ }\mu\text{m}$ from the inner part of the JTE towards the active area.
- **C-devices:** 1×1 PIN Diodes Pad with JTE used as the terminating structure.

- **D-devices:** 1×1 LGAD Pad with a trench used as the terminating structure.
- **E-devices:** 2×1 LGAD Pixels with a trench used as the terminating structure, and also to isolate the pixels. These devices' pixels have a size of $500 \mu\text{m} \times 1 \text{ mm}$.

In addition to pad devices, there are pixelated devices with a $55 \mu\text{m}$ and $110 \mu\text{m}$ pixel pitch compatible with the Timepix3 ASIC [25]. Figure 4 shows a fabricated wafer with Timepix3 sensors and pad devices. The results of the Timepix3 sensors will not be discussed in this paper.

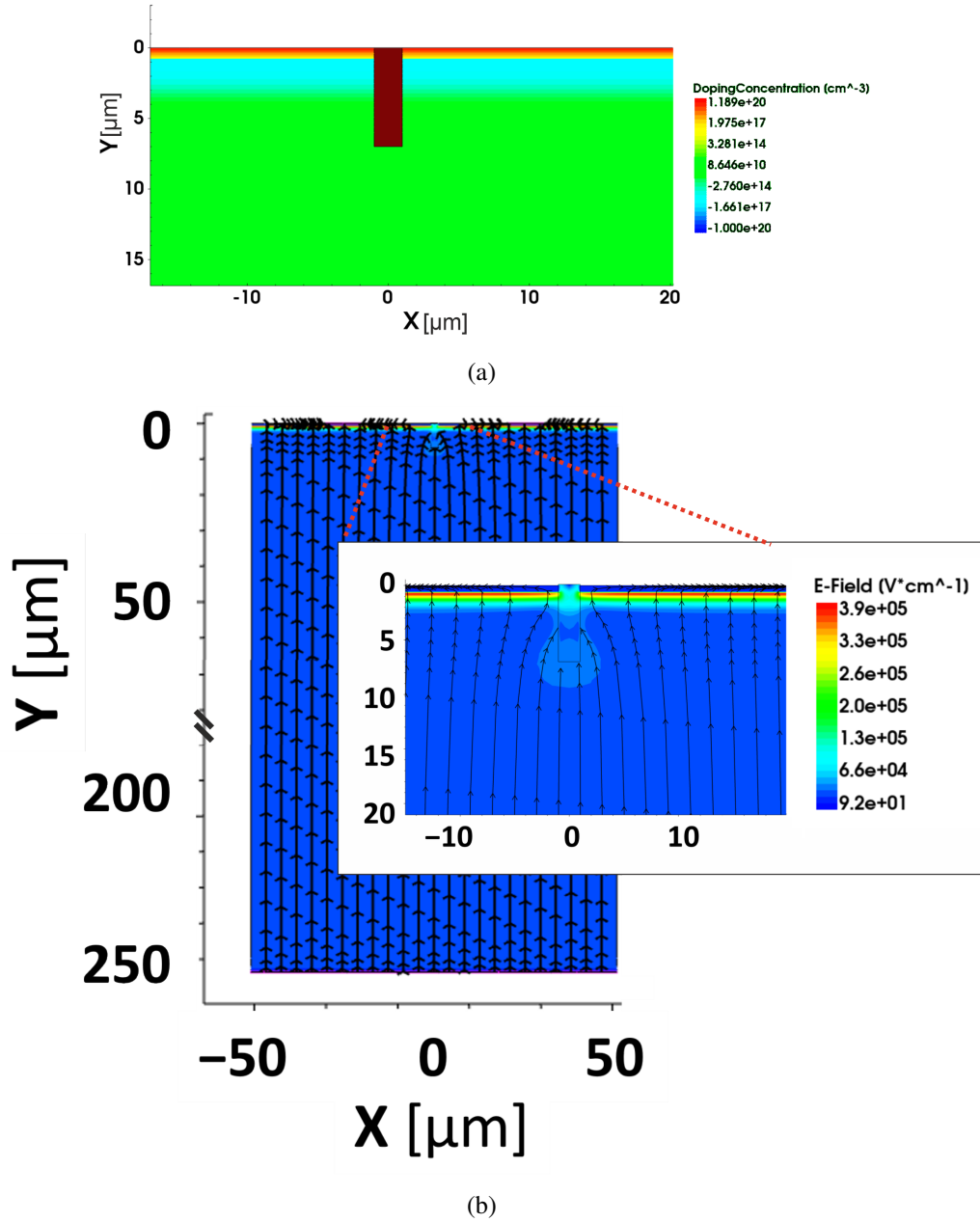


Figure 5. Simulated TI-LGAD structure in Sentaurus TCAD shows (a) doping concentrations across the device, (b) electric field at 500 V.

3 Methods

3.1 Simulation

TI-LGAD simulation studies were performed using Sentaurus TCAD. The device geometry was generated using the Structure Editor (SDE) tool. The device structure is $100\text{ }\mu\text{m}$ wide and $250\text{ }\mu\text{m}$ thick p-type silicon. A $2\text{ }\mu\text{m}$ wide and $7\text{ }\mu\text{m}$ deep trench, filled with silicon oxide, is placed at a position marked $X = 0\text{ }\mu\text{m}$, between two pixels. The structure is designed so that the edges of the detector are far from the trench and just the region around the trench is simulated, i.e. the region between pixels. A uniform highly doped n^{++} implant is present on either side of the trench, that is, from position $X = -50\text{ }\mu\text{m}$ to $X = -1\text{ }\mu\text{m}$ (pixel1) and $X = 1\text{ }\mu\text{m}$ to $X = 50\text{ }\mu\text{m}$ (pixel2). A p^+ gain layer is implanted below the n^{++} layer to create the typical gain layer doping profile, as described in ref. [6]. The simulated doping profiles presented in this study are derived from secondary ion mass spectrometry (SIMS) measurements performed on real devices fabricated at Micron Semiconductor Ltd as shown in ref. [6]. These profiles were subsequently adjusted to account for an additional thermal processing step required for the production of TI-LGADs. The device simulation includes a fixed oxide charge of $1 \times 10^{12}\text{ cm}^{-2}$ in order to better represent a real working device with a saturated fixed oxide charge. Figure 5(a) shows the simulated TI-LGAD structure with the doping concentrations and figure 5(b) shows the electric field at 500 V in the region around the trench.

The simulation of the IPD is carried out using the transient simulations within the TCAD SDEVICE tool. Transient simulations are carried out with the charge injection using infrared (1064 nm) wavelength from a monochromatic source. A 1-dimensional laser scan is performed in the simulation by injecting light at a range of positions along the surface, starting at $X = -40\text{ }\mu\text{m}$ to $X = +40\text{ }\mu\text{m}$. The simulations are performed at a range of voltages, 0–300 V to understand the behavior of the IPD as a function of voltage.

3.2 Transient Current Technique

In this work, a TCT setup installed in AGH University of Krakow was used to study the isolation and determine the IPD experimentally. This TCT setup is manufactured by Particulars [26], which includes both a red (660 nm) and an infrared (1064 nm) pulsed laser. When the pulsed laser illuminates the detector it generates free charge carriers within the bulk of the detector. The infrared light penetrates the full thickness of the detector and uniformly generates free charge carriers along its path, whereas, the red light penetrates only a few micrometers in silicon, therefore generating free charge carriers only at the surface [27]. The laser intensity can be controlled within the TCT software and the intensity is set to match the charge produced by a MIP for an infrared laser. The laser is focused onto the device under test (DUT) by a dedicated optical system that provides a Gaussian profile spot ($\sigma_{\text{Red}} \sim 8\text{ }\mu\text{m}$, $\sigma_{\text{IR}} \sim 10\text{ }\mu\text{m}$). The DUT is placed on a 3D movable stage (x, y, z) with a precision of $\sim 1\text{ }\mu\text{m}$.

The DUT was mounted on a 4-channel readout board, the Chubut-2 [28]. As we are working with a 2×1 pixel device, pixels are connected to two channels of the Chubut-2, and the remaining two channels are grounded by a $50\text{ }\Omega$ resistor. The bias voltage is applied through an HV line. Chubut-2 comes with built-in broadband amplifiers with a 40 dB gain and 50 MHz to 4 GHz bandwidth, allowing both outputs to be directly connected to the oscilloscope. This enables us to record signals from both pixels at once. A 1D scan in the x -direction is performed where the laser traverses from metal (left) to metal (right) in $1\text{ }\mu\text{m}$ steps, so that it moves across pixel1, trench, and then pixel2, as shown in figure 6(a).

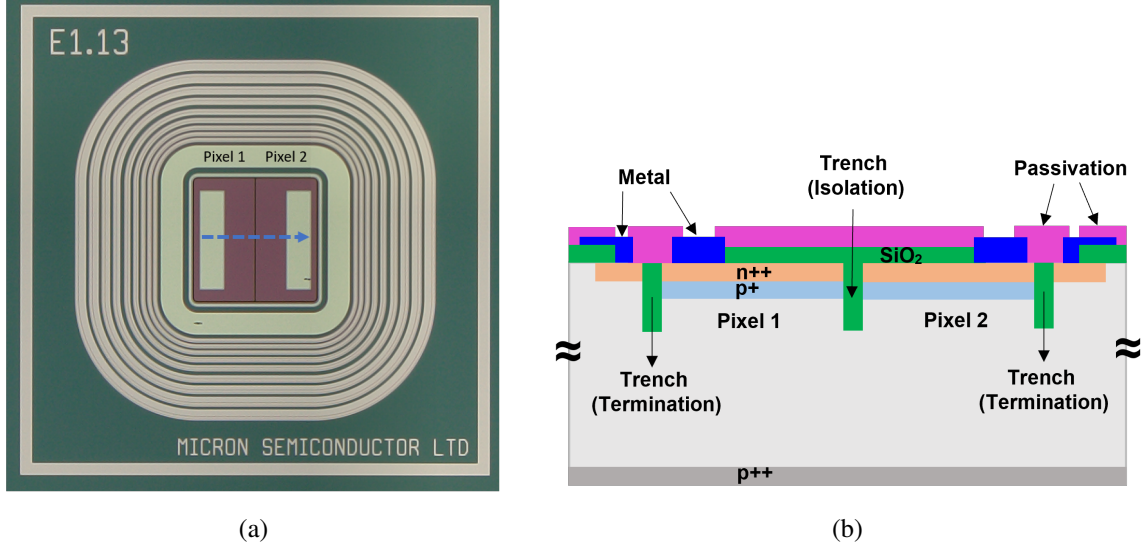


Figure 6. (a) Device E, 2×1 pixels. The arrow indicates the direction of the 1-D linescan with the measurements starting on top of the electrode of pixel1 and finishing on top of the electrode of pixel2. (b) Cross-section of the device E.

4 Results and discussions

4.1 Electrical characterizations: simulation and experiment

Electrical characterization of this batch is carried out using the probe station at the University of Glasgow where the current-voltage (IV) and capacitance-voltage (CV) characteristics were observed. Figure 7(a) shows the leakage current (I_{leak}) of a standard LGAD with JTE (A-devices) is of the order of 100s of picoamperes (pA). LGAD with a combination of JTE and trench as the termination structure (B-devices) has a slightly higher leakage current than A devices. For the devices that include only a trench as the termination structure around the pad periphery (D-devices), and devices that have a trench in the middle of the two pixels as well as around the pad periphery (E-devices), the leakage current increases by almost an order of magnitude. I_{leak} does not increase significantly with an increase in voltage as the expected gain is ~ 3 , which refers to a lower electric field in the multiplication region and no breakdown is observed up to 300 V.

These results show that the trench has a direct impact on the leakage current, but does not cause early breakdown. A few pad devices are tested for voltages up to 1000 V, and no breakdown voltage is observed, as shown in figure 7(b). The 2×1 pixel devices show good uniformity in terms of the leakage current for several devices, with one device (E3) showing higher current ($\sim 1 \mu\text{A}$) as shown in figure 8(a). The guard ring (GR) current, shown in figure 8(b) for all the devices, is in the pA range up to a bias of 200 V, showing a well-controlled fabrication with a small surface current contribution. The CV curves show that the depletion voltage of the gain layer (V_{GL}) is ~ 24 V and the full depletion voltage (V_{FD}) is ~ 120 V for all devices, as shown in figure 9. The simulation of the CV curves shows excellent agreement with the experimental measurements in terms of V_{GL} and V_{FD} .

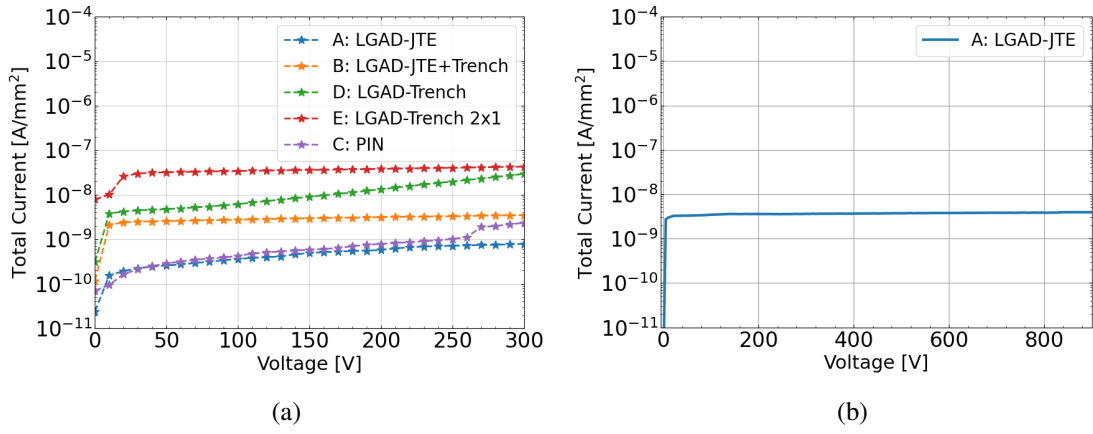


Figure 7. (a) Leakage current of diode and LGADs with various termination structures from Run 3455, Wafer-6. (b) IV measurement of the standard LGAD (A-Device) from the same wafer shows no breakdown up to 1000 V.

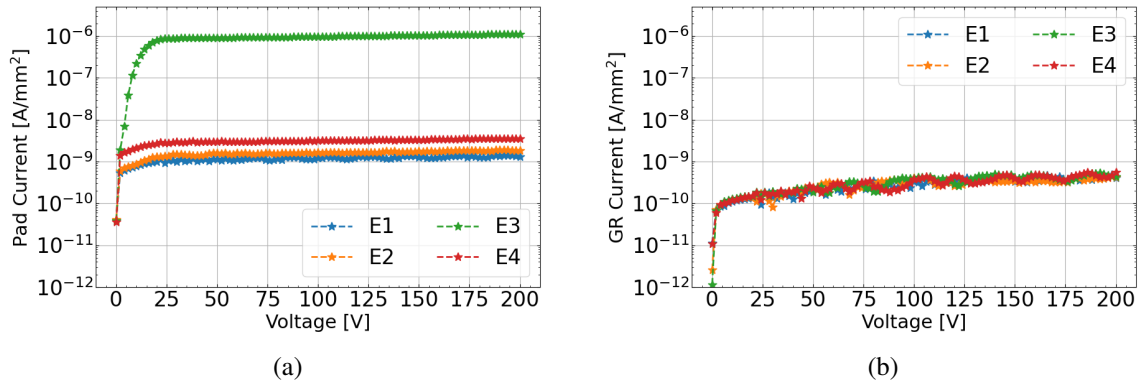


Figure 8. Leakage current from (a) Pad and (b) GR of the Trench isolated E-devices from Wafer-6. No premature breakdown is observed for these devices since pad- and GR-current are within the range of nanoamperes.

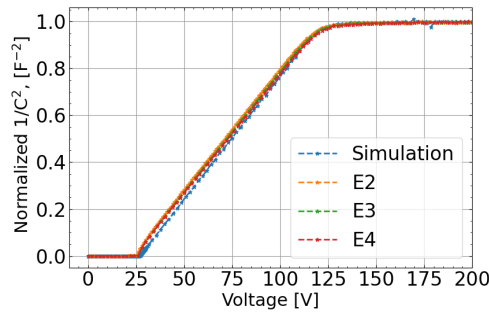


Figure 9. Experimental and simulated inverse square of capacitance as a function of the reverse bias voltage curves, explains the good agreement between experimental measurements and simulations.

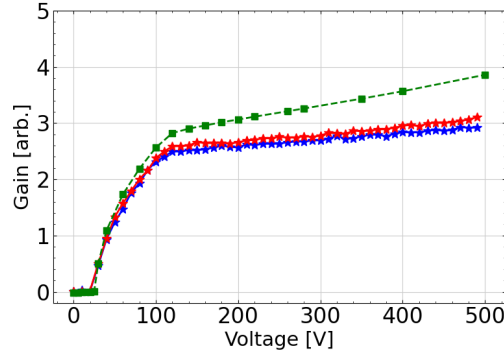


Figure 10. Gain of the standard- (blue) and TI-LGAD (red) from the same wafer, as a function of voltage. The expected gain from simulations (green) agrees well with the experimental measurements.

4.2 Gain

After successful electrical characterization of the sensors, charge collection (CC) measurements were performed using the TCT setup as described in section 3.2. The IR laser of wavelength 1064 nm was used for CC measurements as it traverses the sensor thickness, hence mimicking a MIP. Therefore, the laser intensity was calibrated to the most probable value (MPV) of a MIP to induce charge in the sensor [29]. The laser intensity was kept the same for all scans and sensor types, creating ~ 2.6 fC charge. The gain of the devices was obtained using equation (4.1). Since the wafer under test has the second lowest GL doping, the results in figure 10 show that the gain is between 2.5–3 for bias voltages above V_{FD} , which is expected. TCAD simulations show a good agreement with a gain in the range 3–4.

$$\text{Gain}[V] = \frac{CC_{LGAD}[V]}{CC_{PIN}[V \geq V_{FD}]} \quad (4.1)$$

4.3 Isolation (simulation and experimental)

4.3.1 Pixel isolation

One of the key requirements of a pixelated detector is that the pixels are isolated, i.e. each pixel only registers a signal if there is a charge interaction within the pixel area. The laser response from the TI-LGADs is observed to validate the pixel isolation via trenches. For this study, the TCT system is used with an IR laser (1064 nm) and focused to a spot size of $10 \mu\text{m}$ to observe the signal on each pixel of a 2×1 pixel sensor when the laser traverses the detector thickness. To perform the electrical isolation measurement, 2D charge collection maps of pixel1 and pixel2 are generated by performing a 2D TCT raster scan of the entire pixel array. Figure 11(a) plots the charge collected on pixel1 as a function of laser position. One can see the structure of the 2×1 array, with pixel1 on the left (Red) and pixel2 on the right (Blue) of the image.

The rectangular regions in the center of each pixel are metal electrodes that reflect the laser and thus no charge is seen when the laser hits these regions. The gap between the GR and the 2×1 pixel array can also be seen. Figure 11(a) shows that when the laser illuminates the region of pixel1, the charge collected from pixel1 is high and when the laser illuminates the region of pixel2, the charge collection from pixel1 is close to zero. The response of pixel2 is similar as shown in figure 11(b). This result confirms that the pixel isolation is effective. Although a small collected charge can be

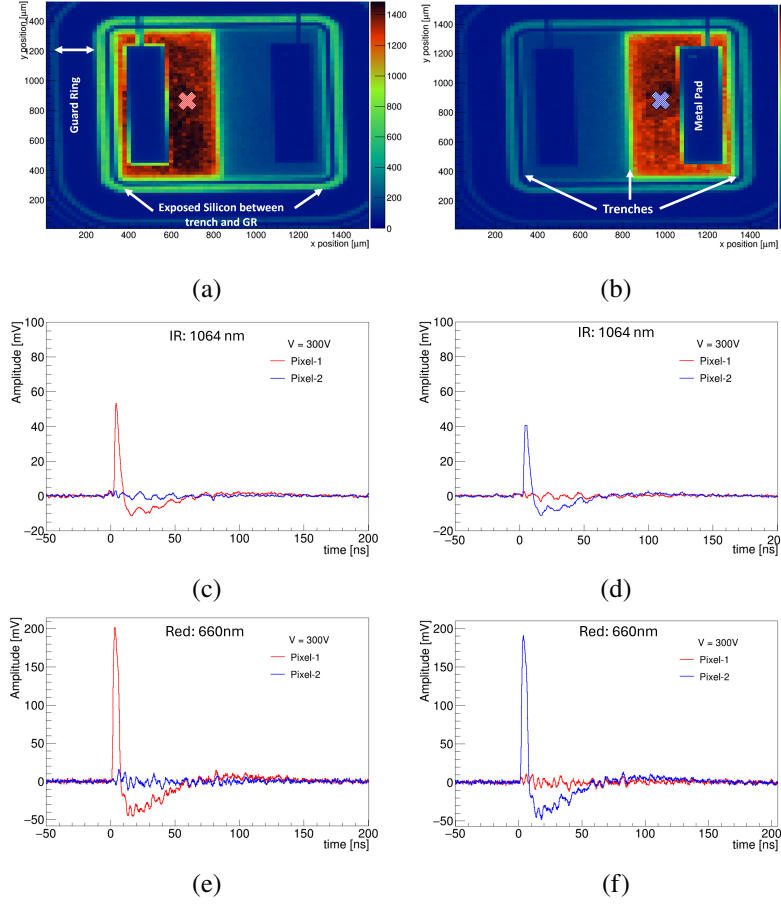


Figure 11. 2D maps of TI-LGAD showing excellent isolation between pixel1 and pixel2, when (a) pixel1, (b) pixel2, are observed independently. (c) and (d) shows waveforms when the IR laser is incident on pixel1 and pixel2, respectively, while (e) and (f) show waveforms when the red laser is incident on pixel1 and pixel2, respectively. Cross in (a) and (b) shows the laser position from where waveforms are obtained. Device is also shown in figure 6(a).

observed on the adjacent pixel. However, looking at the waveforms observed for both pixels when the infrared laser illuminates pixel1 (figure 11(c)) and pixel2 (figure 11(d)), no clear signal is present on the adjacent pixel. Similar is the case with the red laser, as shown in figure 11(e) and 11(f). To investigate the issue of small charge collection observed on adjacent pixels, we analyzed the simulated Transient Current Technique (TCT) waveforms on pixel1 and pixel2 using infrared (figure 12(a)) and red (figure 12(b)) laser. As expected, pixel1—the pixel under test—exhibits the collected signal. In contrast, pixel2 displays a bipolar signal. This bipolar response arises from the movement of charge carriers that do not ultimately contribute to the collected charge on pixel1. Despite not being collected, these carriers still induce a transient current in pixel2. The current reverses direction during the process, resulting in a bipolar waveform that integrates to zero, consistent with the principles described in [30]. We further observed that the amplitude of the bipolar signal on pixel2 diminishes as the laser injection point moves away from the trench, indicating a spatial dependence. The apparent charge collection on adjacent pixels, as shown in figure 11, may thus be attributed to a coarse resolution of the bipolar signal. When the bipolar signal is not fully resolved, its integral can yield a small non-zero value, falsely suggesting a net charge collection.

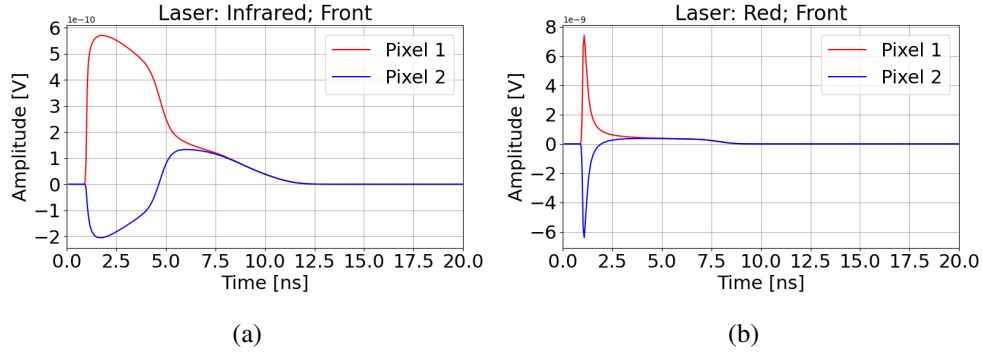


Figure 12. TCT waveforms obtained using TCAD simulations with (a) infrared (front illumination) and (b) red laser (front illumination), at 20 μm away from the trench.

4.3.2 Calculation of Inter-pixel Distance

The interpixel distance (IPD) plays a crucial role in determining the fill factor of the device. The IPD was measured using the TCT setup described in section 3.2. In this setup, a 1D scan is performed where waveforms are recorded as a function of laser position on the top surface of the detector. The laser moves from the metal electrode on top of pixel1 to the metal electrode on top of pixel2, crossing the trench (figure 6(a)). The laser travels a distance of 700 μm for each scan in steps of 1 μm . The collected charge is calculated for each waveform by integrating the signal. The charge collected is plotted as a function of laser position, and the profile can be represented by an s-curve function, which is defined as

$$f(x) = \left[\text{erf} \left(\pm \frac{x - c_1}{c_2} \right) + 1 \right] * c_3 + c_4, \quad (4.2)$$

where x is the laser position, and c_1 , c_2 , c_3 , and c_4 are free fitting parameters. The erf is the Gauss-error function given by

$$\text{erf}(x) = \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} dt. \quad (4.3)$$

The IPD is then calculated by the difference of the laser position where the normalized charge reaches 50% of the average maximum value of both pixels, as shown in figure 13(a). An example of the charge profiles obtained from 1D laser scans and the s-curve fitting is shown in figure 13(b).

The laser scans as a function of position are performed with increasing voltage 150 V to 300 V in steps of 30 V. Figure 14 shows the experimental and simulated CC profiles versus laser position on the device at a reverse bias 300 V. The 1-dimensional charge collection profile obtained from the simulations is slightly different as compared to the experimental results due to the difference in the laser beam profile in the simulation and experiment. This can be compared by looking at the FWHM (σ) of both curves. Figure 14(a) is obtained from the infrared laser (1064 nm) while figure 14(b) is the result of the red laser (660 nm). While the laser is illuminating pixel1, a small amount of collected charge is seen on pixel2, and vice versa. Quantitatively, this charge is smaller for the infrared laser than the red laser and can be referred to as the crosstalk. However, this crosstalk produces no clear signal on the adjacent pixels, as shown in figure 11. Section 4.3.1 explains the phenomenon that might be the reason for crosstalk. The red laser was used as it penetrates only a few microns in silicon, while the IR penetrates the entire thickness of the device under test. The IPD obtained from

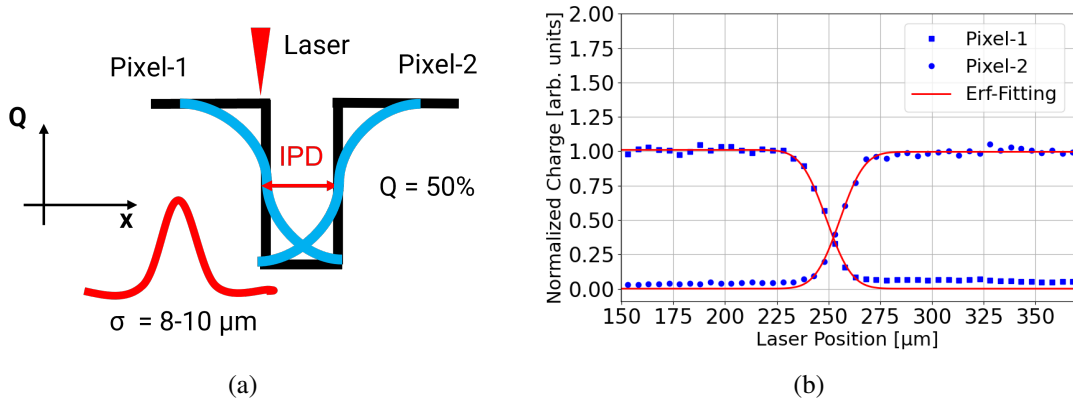


Figure 13. (a) Schematics of the calculation method of inter-pixel distance. (b) Example of an IPD calculation using s-curve fitting using eq. (4.2).

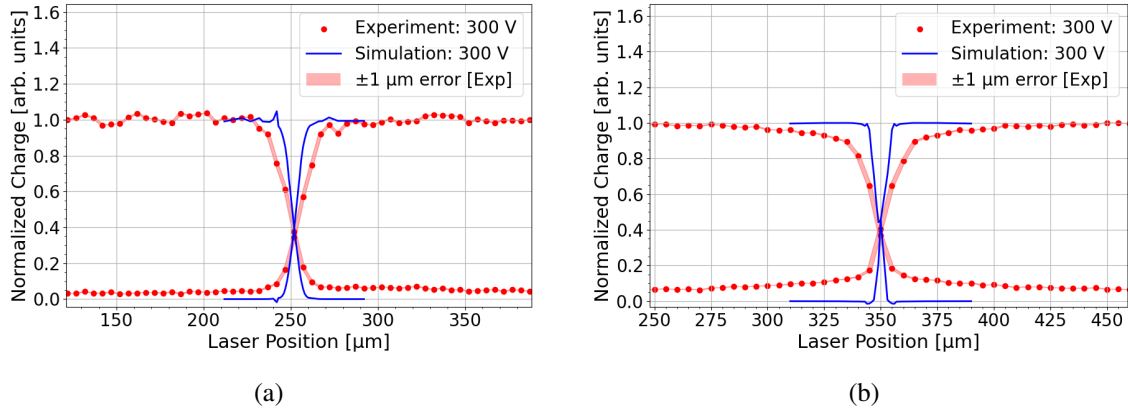


Figure 14. Comparison of the experimental and simulated 1-dimensional laser scan of the device using (a) infrared (1064 nm) and (b) red (660 nm) laser.

the above-mentioned configurations is shown in figure 15. The plot shows results for both red and infrared lasers illuminating from the front. The systematic uncertainty of $1 \mu\text{m}$ in experimentally obtained values is due to the stage movement. Figure 15 shows that the simulation underestimates IPD. At 300 V, the simulation predicts an IPD of $2.5 \mu\text{m}$, while the infrared laser measurements give an IPD of $\approx 6 \mu\text{m}$. Within the uncertainties, the IPD is not affected significantly by the applied bias voltage above V_{FD} , which is in agreement with the simulation. The measurements with the red laser illuminating the front side of the detector show a very similar response to the simulation.

The difference in the IR laser measurements and the simulation can be partly explained by the differences between simulation and reality. In the simulation, the laser profile is a $\sim 10 \mu\text{m}$ beam, which enters the detector exactly perpendicular to the surface and the beam profile remains constant throughout the full thickness of the device. In TCT measurements, although the laser is focused to approximately $\sim 10 \mu\text{m}$ at the detector surface, it spreads as it propagates through the silicon. This causes the resulting beam profile to form a cone-shaped induced charge cloud, leading to reduced spatial precision and an increased IPD. The angle of incidence can also be taken into account, which, due to the mounting of the detector on the PCB, may not be exactly perpendicular to the laser beam,

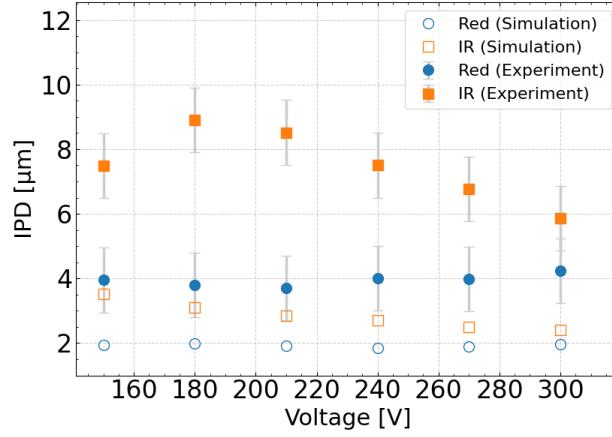


Figure 15. Experimental and simulated IPD value using Red (660 nm) and Infrared (1064) laser from the front side of the device.

resulting in an increased IPD. Considering only the results from the red laser, the device characteristics can be better understood. When the red laser illuminates the front side, the results match closely to those of the simulation. These differ from the results obtained by using the IR laser because the light penetrates only a few microns and thus produces a well-focused charge cloud, unlike the IR laser.

5 Conclusions and future work

The first batch of TI-LGADs produced by Micron Semiconductors Ltd. is characterized in this work. An extensive study of the 2×1 pixelated TI-LGADs is carried out to validate the quality of the pixel isolation and reduction of the no-gain region, referred to as the IPD.

IV measurements confirm that there is no premature breakdown of the devices due to trenches and no traces of breakdown are seen up to 1000 V. The leakage current is kept low and of the order of 10–100 nA for the operational voltages.

The gain of the standard- and TI-LGAD is similar, in the range of 2–3, which matches the transient simulations for the IR laser. Moreover, the 2D laser maps of the 2×1 TI-LGAD devices have shown remarkable isolation between the pixels. The 1D laser scans show that a fraction of charge is collected as the laser moves to the adjacent pixel, which may be referred to as crosstalk. However, the corresponding waveforms indicate an absence of signal when the laser is positioned directly on the adjacent pixel. Consequently, it can be reasonably inferred that the observed response likely arises from inadequate resolution of the bipolar signal, resulting in a non-zero integral despite the lack of actual charge collection. The reduction in IPD from 50–70 μm in standard LGADs to less than 10 μm in TI-LGADs represents a significant advancement. This achievement marks an important step toward enhancing the fill factor (FF), thereby enabling finer segmentation of pixelated devices. Future work will focus on characterizing additional wafers with increased doping levels in the gain layer to investigate the relationship between IPD and the gain layer doping concentration. The focus will be placed on understanding the IPD when the detectors are illuminated from the back side and improving the design to mitigate this change in response and ultimately improve the IPD. Additionally, plans are in place to irradiate the devices with both neutrons and soft X-rays. This approach will facilitate evaluations not only for HEP detectors but also those suitable for synchrotron and medical applications.

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References

- [1] G. Pellegrini et al., *Technology developments and first measurements of Low Gain Avalanche Detectors (LGAD) for high energy physics applications*, *Nucl. Instrum. Meth. A* **765** (2014) 12.
- [2] M.P. Casado, *A High-Granularity Timing Detector for the ATLAS Phase-II upgrade*, *Nucl. Instrum. Meth. A* **1032** (2022) 166628.
- [3] M. Carulla et al., *50 μm thin Low Gain Avalanche Detectors (LGAD) for timing applications*, *Nucl. Instrum. Meth. A* **924** (2019) 373.
- [4] V. Sola et al., *First FBK production of 50 μm ultra-fast silicon detectors*, *Nucl. Instrum. Meth. A* **924** (2019) 360 [[arXiv:1802.03988](#)].
- [5] N. Moffat, *Low gain avalanche detectors for particle physics and synchrotron applications*, Ph.D. thesis, Glasgow University, Glasgow, U.K. (2020).
- [6] N. Moffat et al., *Low Gain Avalanche Detectors (LGAD) for particle physics and synchrotron applications*, *2018 JINST* **13** C03014.
- [7] W. Krüger et al., *LGAD technology for HADES, accelerator and medical applications*, *Nucl. Instrum. Meth. A* **1039** (2022) 167046.
- [8] C. Royon and F. Gautier, *Fast timing detectors with applications in cosmic ray physics and medical science*, *Nucl. Instrum. Meth. A* **1058** (2024) 168886 [[arXiv:2311.04601](#)].
- [9] N. Cartiglia et al., *Tracking in 4 dimensions*, *Nucl. Instrum. Meth. A* **845** (2017) 47.
- [10] H.F.W. Sadrozinski, A. Seiden and N. Cartiglia, *4D tracking with ultra-fast silicon detectors*, *Rept. Prog. Phys.* **81** (2018) 026101 [[arXiv:1704.08666](#)].
- [11] P. Fernandez-Martinez et al., *Design and Fabrication of an Optimum Peripheral Region for Low Gain Avalanche Detectors*, *Nucl. Instrum. Meth. A* **821** (2016) 93 [[arXiv:1510.08626](#)].
- [12] N. Moffat and R. Bates, *Simulation of the small pixel effect contributing to a low fill factor for pixellated Low Gain Avalanche Detectors (LGAD)*, *Nucl. Instrum. Meth. A* **1018** (2021) 165746.
- [13] E. Currás et al., *Inverse Low Gain Avalanche Detectors (iLGADs) for precise tracking and timing applications*, *Nucl. Instrum. Meth. A* **958** (2020) 162545 [[arXiv:1904.02061](#)].
- [14] G. Giacomini, W. Chen, G. D’Amen and A. Tricoli, *Fabrication and performance of AC-coupled LGADs*, *2019 JINST* **14** P09004 [[arXiv:1906.11542](#)].
- [15] Y. Zhao et al., *A new approach to achieving high granularity for silicon diode detectors with impact ionization gain*, *J. Phys. Conf. Ser.* **2374** (2022) 012171 [[arXiv:2101.00511](#)].
- [16] A. Tournier et al., *Pixel-to-pixel isolation by deep trench technology: application to cmos image sensor*, in the proceedings of the *International Image Sensor Workshop*, Ōnuma Quasi-National Park, Hokkaido, Japan, June 8–11 (2011), pp. 12–15.

- [17] C. Piemonte et al., *Performance of NUV-HD Silicon Photomultiplier Technology*, *IEEE Trans. Electron Devices* **63** (2016) 1111.
- [18] G. Paternoster et al., *Trench-Isolated Low Gain Avalanche Diodes (TI-LGADs)*, *IEEE Electron. Dev. Lett.* **41** (2020) 884.
- [19] X. Cai et al., *Vertical 4H-SiC n-i-p-n APDs With Partial Trench Isolation*, *IEEE Photon. Technol. Lett.* **30** (2018) 805.
- [20] G. Paternoster et al., *Novel strategies for fine-segmented Low Gain Avalanche Diodes*, *Nucl. Instrum. Meth. A* **987** (2021) 164840.
- [21] M. Senger et al., *A Comprehensive Characterization of the TI-LGAD Technology*, *Sensors* **23** (2023) 6225.
- [22] A. Bisht et al., *Characterization of novel trench-isolated LGADs for 4D tracking*, *Nucl. Instrum. Meth. A* **1048** (2023) 167929.
- [23] E.H. Klaassen et al., *Silicon Fusion Bonding and Deep Reactive Ion Etching a New Technology for Microstructures*, in the proceedings of the *International Solid-State Sensors and Actuators Conference — TRANSDUCERS '95*, Stockholm, Sweden, June 25–29 (1995), pp. 556–559 [[DOI:10.1109/sensor.1995.717285](https://doi.org/10.1109/sensor.1995.717285)].
- [24] T.-E. Hansen et al., *First fabrication of full 3D-detectors at SINTEF*, *2009 JINST* **4** P03010.
- [25] T. Poikela et al., *Timepix3: a 65K channel hybrid pixel readout chip with simultaneous ToA/ToT and sparse readout*, *2014 JINST* **9** C05013.
- [26] Particulars, *Large scanning TCT*, <https://www.particulars.si/products.php?prod=LargeScanTCT.html>.
- [27] G. deGraaf and R.F. Wolffenbuttel, *Illumination Source Identification Using a CMOS Optical Microsystem*, *IEEE Trans. Instrum. Meas.* **53** (2004) 238.
- [28] M. Senger, *Chubut 2: Readout board for LGADs*, https://sengerm.github.io/Chubut_2/doc/testing/index.html.
- [29] E. Curras Rivera, A. La Rosa, M. Moll and F. Zareef, *Gain layer degradation study after neutron and proton irradiations in Low Gain Avalanche Diodes*, *2023 JINST* **18** P10020 [[arXiv:2306.11760](https://arxiv.org/abs/2306.11760)].
- [30] H. Spieler, *Semiconductor Detector Systems*, Oxford University Press (2005) [[DOI:10.1093/acprof:oso/9780198527848.001.0001](https://doi.org/10.1093/acprof:oso/9780198527848.001.0001)].