DEVELOPMENT OF A READ-OUT CHIP SUITABLE FOR THE LHCB EXPERIMENT

Martin Feuerstack-Raible, Ulrich Straumann
University of Heidelberg

Edgar Sexauer, Michael Schmelling, Ulrich Trunk
Max-Planck-Institute for Nuclear Physics, Heidelberg

Ruud Kluit
NIKHEF, Amsterdam

Jo van den Brand
Free University of Amsterdam

Abstract

For the LHCb experiment a dedicated analogue pipeline chip will be developed.To fulfill the time schedule of the LHCb experiment for detector prototyp testing but also to have a long-term solution, development will be made in two branches.

The already existing SCT128A design from CERN, which is implemented in the radiation hard DMILL process, will be adapted to the LHCb requirements.

In parallel, a new design will be made in a deep submicron process. These processes recently showed very good results concerning radiation hardness and their availability will grow in future.

Existing analog circuits from e. g. 0.8µm CMOS processes can not be ported easily to deep submicron processes. Also, to fully exploit the radiation hardness of this technology, special layout considerations must be taken into account. Thus existing digital standard cell libraries can no be used but must be constructed anew to be radiation hard. Such libraries would be interesting beyond the scope of the LHCb project.

THE ANALOGUE PIPELINE CHIP IN THE LHCB DATA ACQUISITION SYSTEM

As described in [1] the LHCb data acquistion system has four trigger levels. Here we discuss only the topics relevant to this subject. Electronics for level zero resides on the detectors and consist of pipeline buffers with a storage capacity of approx. 3µs. The buffers take data with the LHC bunch crossing clock of 40Mhz and are read out concurrently with the level zero trigger rate of 1Mhz, which makes it impossible to use existing LHC pipeline chips without changes. After a level zero trigger, data must be driven electrically to the next pipeline buffers, which reside in a distance of approx. 10m outside the detector.

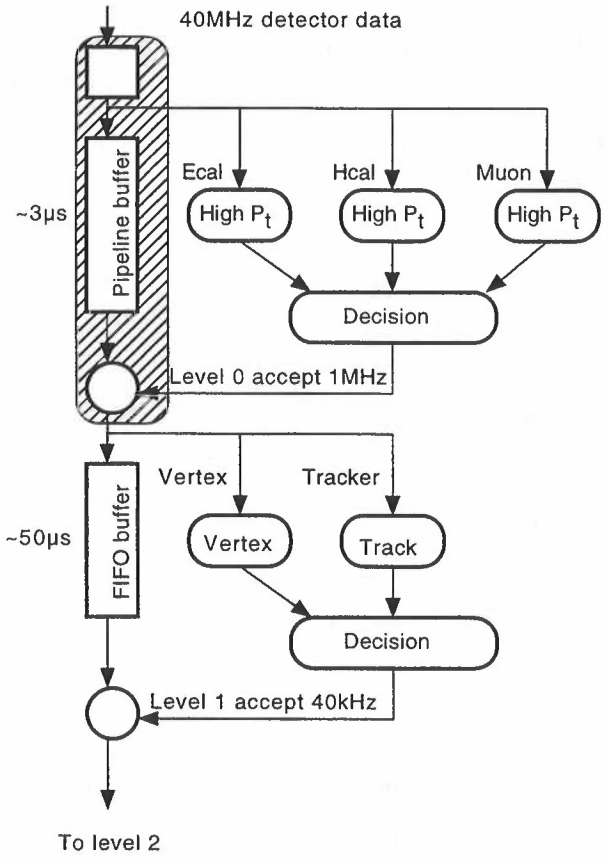

Fig. 1: The first two levels of the LHCb triggering architecture

Subdetector frontends

The Silicon Vertex Detector (SVD) [2], the Inner Tracker (IT), which most likely will be realized with Microstrip gaseous Counters (MSGCs)[2], and the RICH, in case it is implemented with Pad Hybrid Photo Detectors (Pad-HPDs) [2] or multianode Photo Multipliers, could make use of the same multi channel analogue pipeline chip. Table 1 summarizes the

requirements of the different detectors. For the RICH, only the Pad-HPD case is shown since the signal of the multianode PMT can easily be downscaled to a level comparable to the other cases.

Because of the large nunber of channels and because of space constraints in the SVD and the RICH, a 128 channel chip will be used.

The signal of the Inner Tracker's MSGC is a statistical distribution of charge pulses over a drift time which is longer than the LHC bunch crossing time. A detailed model of that process with parameters of a chamber suitable for LHCb has yet to be developed. Thus the preamplifier/shaper for the MSGC might differ from the one for the silicon microstrip detector and the Pad-HPD, which have similar characteristics.

Pipeline and read-out architecture

The maximum required latency is, as with any similar chips developed for LHC experiments, up to 3,2μs, including all signal delays and all trigger processor computation times. Thus a pipeline of 128 stages plus space for multi-event buffers is needed.

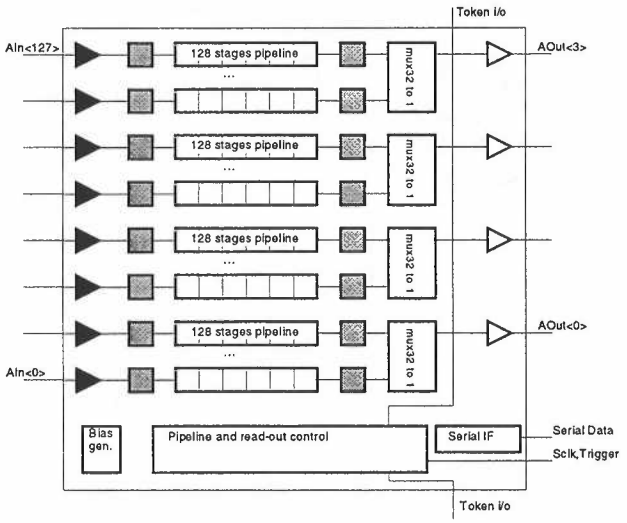

Fig. 2: Block diagram of the analogue pipeline chip

Because of the level zero trigger rate of 1Mhz the read-out speed is critical for the event loss rate. Hence a serial read-out of 32 channels at 40Mhz is foreseen. A 128 channel chip will then have four 32 channel ports running in parallel. To detect synchronisation errors, data will be prepended by a header of two clock cycle length. The four channels can then code the 8bit pipeline column number which was read out. In case of an internal error, numbers larger than the maximum column number can code information about the error condition.

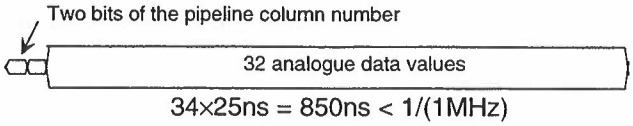

Fig. 3: The analogue output data format

Control interface

The chip will be programmable and monitorable via the standard I2C[3] interface. All clock and trigger signals are received via Low Voltage Differential Signal (LVDS) receivers.

IMPLEMENTATION

Due to the radiative environment of the Vertex Detector and the Inner Tracker „standard" CMOS technology, like 0.8μm CMOS processes, can not be used, though they were still interesting for the RICH detector. Thus it only remain two technolgy choices: the radiation hard DMILL technology from Temic or the newer deep submicron technologies from various suppliers.

Apart from the questionable future availability of the single vendor DMILL process, the cost disadvantage is especially evident for the RICH application, where essentially no radiation hard technology is needed.

Modern deep submicron processes have recently been shown to be radiation hard[4] (at least with respect to total dose effects) and their availability will grow in future. The main disadvantage is that few existing analogue CMOS designs can be ported to these processes, because the maximum supply voltage is typically limited to 2.5V and the process parameter spread is large. When radiation hardness is required,

	SVD	RICH	IT
Number of channels	233.000	500.000	70.000
Occupancy (%)	0,5	5	4
Min. signal (electrons)	12.000 for a MIP	5.000 for a photo electron	~30.000 for a MIP with large fluctuations
Detector capacity	4pF	4pF	12pF
Required S/N	> 8	> 8	> 15
Radiation	1Mrad/y	<100kRad/y	<1Mrad/y
Power consumption	<4mW/channel	<2mW/channel	<4mW/channel

Table 1: Detector requirements on the read-out chip

special layout techniques, like enclosed MOSFETs have to be used. Thus all analogue circuits have to be designed anew and even existing digital standard cell libraries can not be used for radiation hard designs.

Consequently, any read-out chip for LHCb in these technologies will be a complete new design, which is no short-term solution. To fulfill the time schedule of LHCb detector prototyping under theses circumstances a two-way strategy must be followed.

Implementation based on the SCT128A

For having a short-term solution for the radiative environment of the SVD, the SCT128A[5], which is a DMILL design from CERN, will be adapted to the LHCb specification. Since the SCT128A already fulfills the requirements on the frontend, solely the read-out multiplexer has to be splitted into four parts which run in parallel and which also output the header containing the column number, whic was read out. The output driver is already able to run at 40Mhz and the chip is also programmable via an I2C interface.

Implementation in deep submicron technology

The development of a new preamplifer/shaper in deep submicron technology which is suitable for the LHCb SVD is the first item to be addressed. First results on that are expected in the mid of next year.

In parallel, a digital standard cell library will be developed which obeys radiation hard design rules. This library will then be the basis for implementing all digital parts of the LHCb read-out chip, like the pipeline control logic or the I2C interface, for which well tested synthe-zisable Verilog code already exists from the Helix128[6][7] and the follow-on project CIPix.

THE RADIATION HARD DIGITAL STANDARD CELL LIBRARY

The digital standard cell library may be of interest beyond the scope of this project. A huge amount of digital designs are available as functional description or as netlist in a hardware description language like Verilog or VHDL. The description on this level of abstraction has several advantages:

- It is the prerequisite for simulation on a system level, which becomes inevitable for verification of large and complex systems.
- The portability of the designs is improved

To make maximum use of the standard cell library, there are two options. Either we agree on a process of a certain vendor so that the library for this process can be used in many projects, or the library is build in a para-meterized way, which simplifies porting it to different processes. The latter option is especially interesting, because technology is improving and processes will change often in future.

REFERENCES

[1] Jørgen Christiansen: „An overview of the LHC-B experiment and ist electronics", Proceedings of the third workshop on electronics for LHC experiments, CERN/LHCC/97-60

[2] LHCb Technical Proposal, CERN LHCC 98-4 LHCC/P4

[3] Philips semiconductors: „The I2C bus and how to use it (including specifications)

[4] G, Anelli et al.: „Total dose behavior of submicron and deep submicron CMOS technologies", Proceedings of the third workshop on electronics for LHC experiments, CERN/LHCC/97-60

[5] F. Anghinolfi et al.: „SCTA - A Rad-Hard BiCMOS Analogue Readout ASIC for the ATLAS Semiconductor Tracker", CERN-ECP-96-016

[6] W. Fallot-Burghardt et al.: „Helix128-2.1 - Design of a ReadoutChip for the Hera-B Microstrip Detectors", Proceedings of the third workshop on electronics for LHC experiments, CERN/LHCC/97-60

[7] W. Fallot-Burghardt: „A CMOS Mixed-Signal Readout Chip for the Microstrip Detectors of HERA-B", Ph.D. Thesis, Heidelberg 1998