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# Optical Readout and Control Interface for the BTeV Pixel Vertex Detector.*

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**Abstract**

*Optical links will be used for sending data back and forth from the counting room to the detector in the data acquisition systems for future high energy physics experiments, including ATLAS and CMS in the LHC at CERN (Switzerland) and BTeV at Fermilab (USA). This is because they can be ultra-high speed and are relatively immune to electro-magnetic interference (EMI). The baseline design for the BTeV Pixel Vertex Detector includes two types of optical link, one to control and monitor and the other to read out the hit data from the multi-chip modules on each half-plane of the detector. The design and performance of the first prototype of the Optical Readout and Control Interface for the BTeV Pixel Vertex Detector is described.*

## 1. Introduction

The goals of the BTeV experiment are to measure mixing, CP violation, and rare decays in charm and beauty particle decays at the Fermilab collider. The pixel vertex detector is crucial for achieving these goals. This is a multi-plane pixel device that sits inside the beam pipe. It is composed of 124 pixel half-planes of approximately 5x10cm each, divided in 31 double-stations perpendicular to the colliding beam and installed a few millimeters from the beam. Each half-plane is comprised of several multi-chip modules (MCMs). The detector will be employed for on-line track finding for the lowest level trigger. This means that the pixel readout chips bump-bonded to the sensors will have to read out all detected hits and input them to the trigger processors. To achieve the high bandwidth required for the readout, ultra-high-speed digital optical links of 1-2 Gbps will be employed on each detector half-plane. A second type of digital optical link, which will send the command and control signals to the FPIX chips from the counting room to each detector half-plane, can operate at lower speed (~100 Mbps). Both the emitters of the ultra-high-speed optical links and the receivers of the lower speed optical links will be about 7 cm from the beam if they are mounted on the detector planes as proposed in the baseline design. In this case, these devices will receive about 100 Krad of radiation per year of running and will suffer some radiation damage. A further, rather stringent requirement is that they must operate inside the beam pipe in vacuum at $\approx -5^0 C$ [1]. Other solutions, which place the optical circuits outside of the vacuum vessel about 25 cm from the detector, are also being studied.

The design and performance of the first prototype of the Optical Readout and Control Interface (ORCI) designed and built at Fermilab is detailed in this article. Features of note are the decision to operate PIN photodiodes in photovoltaic mode and the decision to drive VCSELs with voltage

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rather than current. The reasons for these choices are given in Sections 2.2 and 3, respectively. While not all components included in the present design are radiation hard, a completely radiation hard version is envisioned for the future.

## 2. First Prototype of the Optical Readout and Control Interface for the BTeV Pixel Vertex Detector

The first prototype of the ORCI for the BTeV pixel vertex detector contains two optical links. The first one operates at 104 Mbps and transmits commands to program and control the FPIX readout chips [2] contained on one multi-chip module (MCM) from the counting room to the detector. The second one operates at 1.04 Gbps and reads out all the detector hit data from the MCM and sends it to the counting room. A block diagram of the system is shown in Figure 1.

The MCM is an array of pixel readout chips (FPIX) mounted on a single sensor and connected in daisy chain using a flexible interconnect circuit [3]. The FPIX chips contain the front-end electronic cells and column-based readout circuitry for the pixel sensors. In order to achieve the needed resolution for tracking and vertexing, the pixel unit cell is very small, 50 microns by 400 microns in size. The FPIX chips contain cells of the same size, which will be bump-bonded to the sensors. The control and readout protocol of the current version of the FPIX chips, called FPIX1, requires that there be 13 control inputs to the MCM, 7 command lines to program the chips and 6 command lines to control the readout. It also contains 17 data output lines for readout of the hit information provided by the detector. We expect that the control and readout protocols of more advanced versions of the FPIX readout chips will be different.

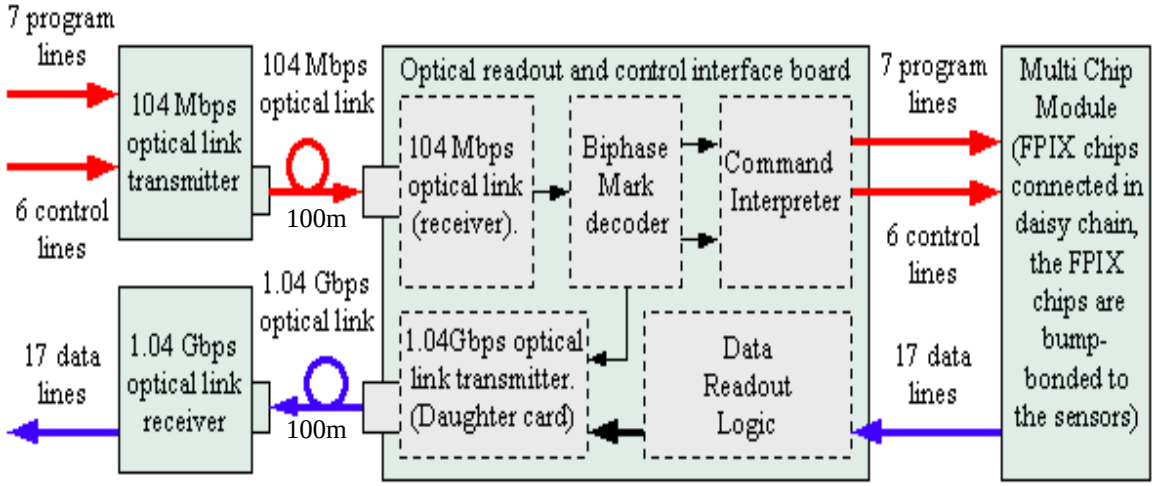



Figure 1: Block diagram of the first prototype of the ORCI for the BTeV pixel detector.

### 2.1 The command and control link transmitter

Figure 2 contains a block diagram showing the components of the 104 Mbps optical link transmitter, which receives the program and control lines from the data acquisition system and encodes the information into a 7-bit protocol. The first bit is always one to indicate the beginning of the data frame. The next five bits provide the unique identifier for the command and control line being sent. The seventh bit is the data (high or low) to be sent to the corresponding command and control line. The signal produced by the 7-bit protocol generator is non-return to zero (NRZ). In order to send both the NRZ signal and the clock in a single data stream they are converted to bi-phase mark code. The protocol generator and the bi-phase mark encoder are implemented in a Field Programmable Gate Array (FPGA). The 104 Mbps transmitter uses a VCSEL driver to

modulate the signal supplied to a Mitel 1A444 VCSEL. The VCSEL translates the bi-phase signal into an optical signal.

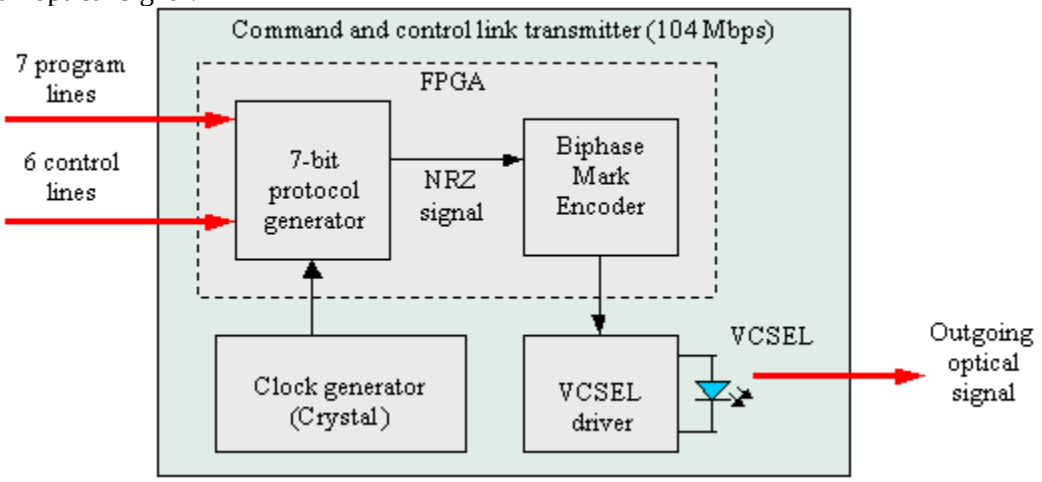



Figure 2: Block diagram of the 104 Mbps optical link transmitter.

**2.2 The command and control link receiver**

Figure 3 contains a block diagram of the command and control link receiver. The recovered signal must pass through a bi-phase mark decoder to separate the command signal and the clock signal. Following this, the command signal passes through an interpreter that identifies the data received and the corresponding command line. These functions have been implemented in an FPGA. Finally, the data are sent on the correct command line to the MCM.

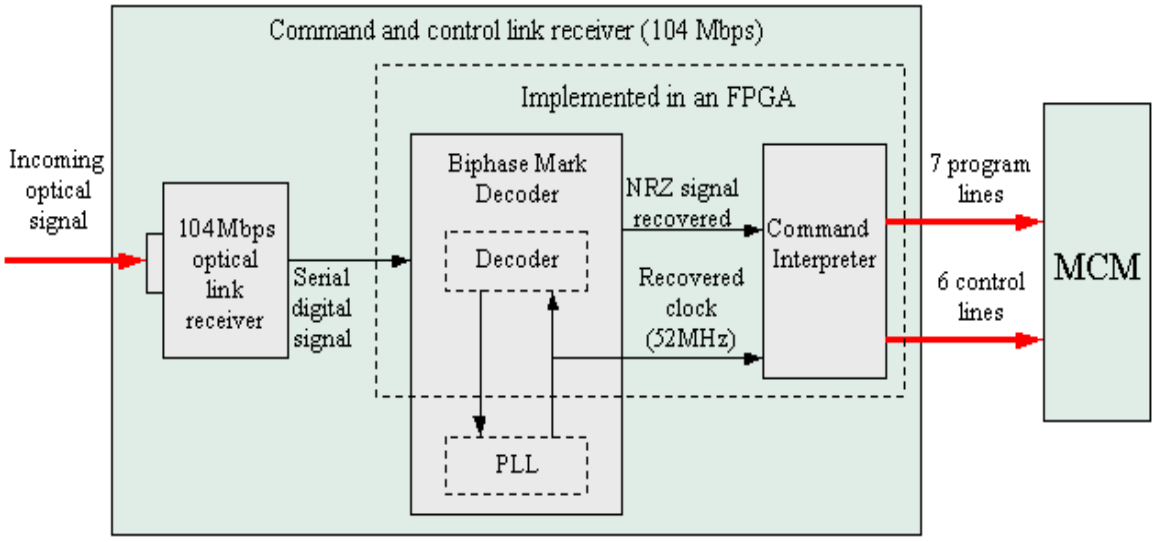



Figure 3: Block diagram of the command and control receiver section of the Optical Readout and Control Interface Board.

The 104 Mbps optical link receiver utilizes a Mitel 1A354 PIN photodiode or a Lasermate RST-M85A306 PIN photodiode operated in photovoltaic mode. This is connected to an amplifier; the output of the amplifier is connected to a discriminator that recovers the digital signal as shown in Figure 4. The discriminator has a threshold of 33mV, which is well above the noise level but still low enough to ensure that all data bits are received.

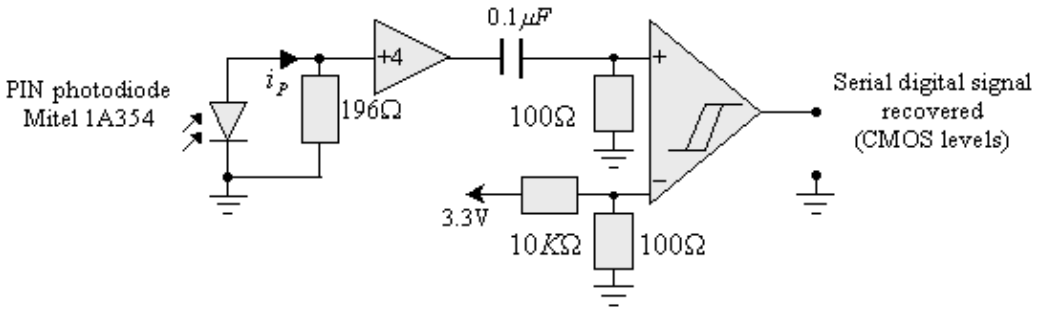



Figure 4: 104 Mbps optical link receiver.

The 104 Mbps optical link receiver is an inherently low noise circuit, because the PIN photodiode is being used in photovoltaic mode [4]. Since modern PIN photodiodes are fast enough to operate without a bias voltage being applied, both the dark current and the noise produced by a power supply used to do the biasing can be avoided. In the absence of an applied electric field, charge motion is caused only by the small electric field produced by the electron-hole pairs generated in the depletion region of the PIN photodiode [5]. Also, the depletion region is limited in size by the properties of the device, since there is no reverse bias voltage applied which would increase its size. We believe that this will reduce the impact of Single Event Upset (SEU) due to strong interactions in the PIN photodiodes and plan to carry out tests to demonstrate this in the near future.

The bi-phase mark decoder uses a 104 MHz square signal to separate the clock signal from the command signal. A phase-locked loop (PLL) is used to keep the receiver circuit synchronized with the incoming optical signal. The PLL uses a voltage controlled crystal oscillator (VCXO) to generate a 52 MHz clock signal and a phase and frequency detector that it is implemented in the FPGA. We synchronize the signal recovered with a 26 MHz square signal to get the best performance from the PLL.

**2.3 The readout optical link transmitter**

The data acquisition system sends the request to the MCM to read out the hit data using the 6 readout control lines. These are sent and received by means of the 104 Mbps optical link described above. The 17 data lines which output the hit data from the MCM are input to the FPGA, which delivers 16 of these data bits in parallel to the 1.04 Gbps optical link transmitter along with the corresponding 52 MHz clock, as shown in Figure 5. The 17th bit, data valid, is transmitted and received as one of the four G-link control bits.

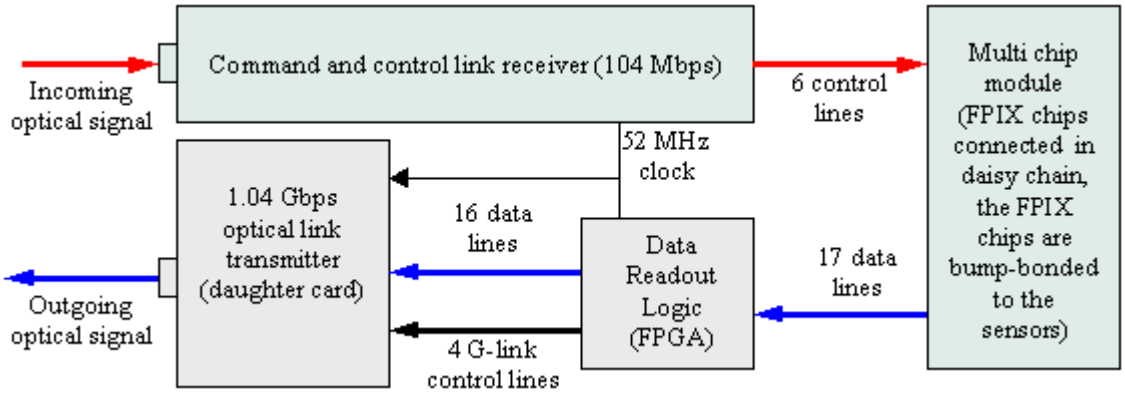



Figure 5: Block diagram of the circuit used to read out all the data generated by the detectors on the MCM.

The use of the data readout logic to input the data to the optical transmitter provides the possibility of checking out all the commands that are sent to the MCM. When we are transmitting commands to program the FPIX chips on the MCM, we need only to reroute the information in the control words to the FPGA and input them to the 1.04 Gbps optical link transmitter instead of the hit data generated in the MCM.

The 1.04 Gbps transmitter has been placed on a daughter card to allow the use of two versions of the 1.04 Gbps optical link transmitter. The first version, which is not radiation hard, is based on the HDMP-1032 G-Link transmitter [6], low power version, and the optoelectronic Finisar module FTM-8510 (See Figure 6.). The second option will be radiation hard. It will be built using a custom VLSI serializer in CHFET process [7]. Since this serializer includes a VCSEL driver, the serializer can be connected directly to the VCSEL as shown in Figure 7. Both the G-link transmitter and the CHFET serializer encode the information using the Conditional Invert Master Transition (CIMT) protocol [6]. Because the serializer is compatible with the HDMP-10X2 G-Link transmitter series, the daughter boards are interchangeable and both are fully compatible with the rest of the system. Thus, either daughter card can be used on the Optical Readout and Control Interface Board (ORCIB) without having to make any other changes. The function of the daughter card is to translate the parallel frame at 52MHz into a serial frame at 1.04 Gbps to send the MCM information to the counting room.

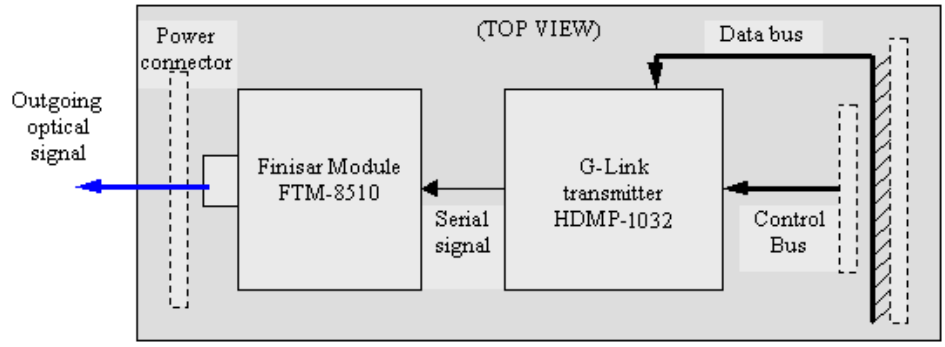


Figure 6: Block diagram of the Daughter board based on the G-link transmitter HDMP-1032.

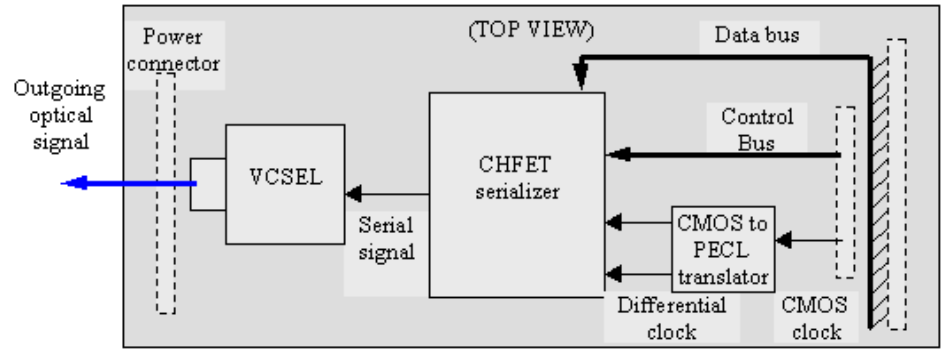


Figure 7: Block diagram of the Daughter board based on the CHFET serializer and a HFE4080 Honeywell VCSEL.

Tests of a preliminary version of the CHFET serializer show that it needs a differential clock signal with rise and fall times no more than 500ps and a jitter peak to peak of 100ps. This places rather stringent timing requirements on the bi-phase mark decoder, which supplies the clock signal to the daughter cards. On the CHFET serializer daughter card, we translate the CMOS

clock signal coming from the mother board into a differential PECL signal and provide it to the CHFET serializer. The translator delivers a PECL clock signal with 350 ps rise and fall times. The daughter card with the HDMP-1032 G-link transmitter needs a clock signal with less than 250 ps jitter peak to peak and less than 1.5 ns rise and fall time. Thus, the clock signal supplied by the mother board to the daughter cards must have less than 100 ps jitter peak to peak and less than 1.5 ns rise and fall times to work with either of the daughter cards.

### 2.4 The readout optical link receiver

The 1.04 Gbps optical link receiver uses a Finisar module FRM 8510, which translates the optical signal at 1.04 Gbps into an electrical signal. This electrical signal is supplied to an HDMP-1034 G-Link receiver, low power version. The chip translates the serial frames into parallel frames, recovers the 52 MHz clock, and synchronizes the recovered clock with the 52 MHz local clock as shown in Figure 8.

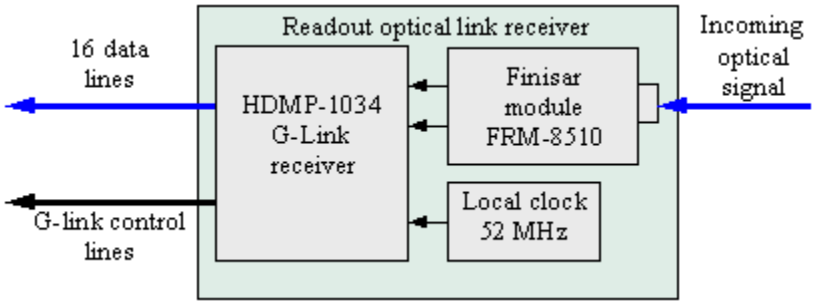



Figure 8: Block diagram of the readout optical link receiver.

## 3. Performance of the first prototype of the Optical Readout and Control Interface for the BTeV Pixel Vertex Detector

The VCSEL driver in the 104 Mbps optical link transmitter was designed to produce a minimum variation in optical power between different Mitel 1A444 VCSELs. Our measurements have shown that if we drive the VCSEL with current we get up to 80% optical power variation among the VCSELs under test. When we drive the VCSELs with voltage, we get a maximum variation of only 25%. This difference provides an important safety margin, especially when designing a driver for use in a high radiation environment where performance may be degraded progressively by radiation damage. In Figure 9 we show the optical power as a function of the forward current for two VCSELs, one of which emits the lowest optical power and the other of which emits the highest optical power of the six VCSELs of this type that we tested.

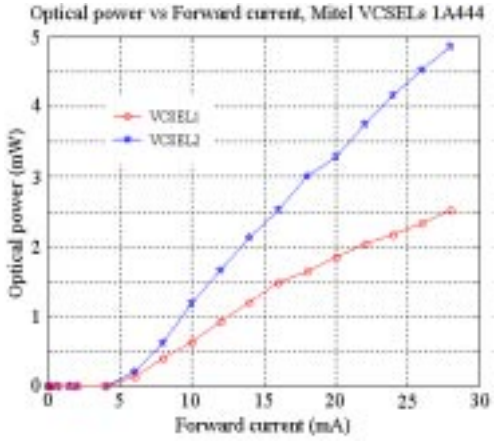
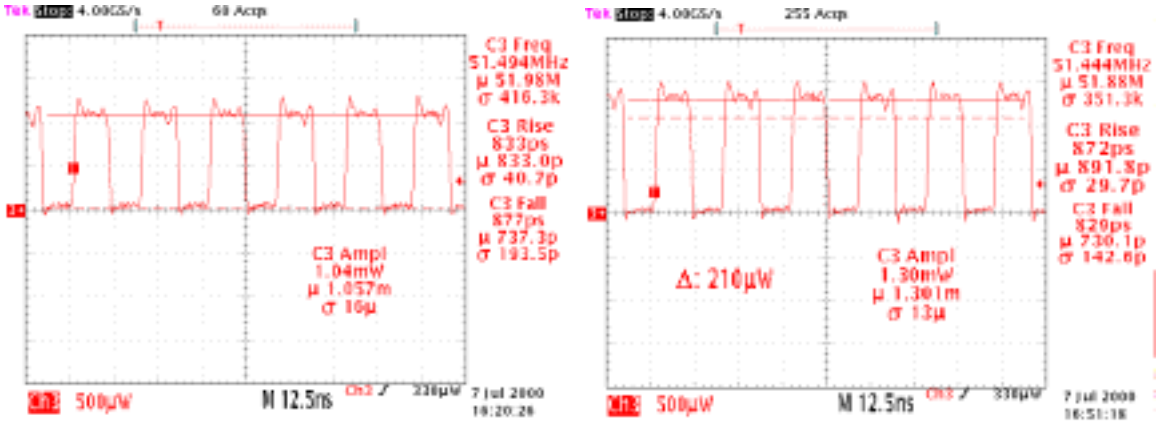



Figure 9: Optical power as a function of the forward current for two Mitel 1A444 VCSELs.

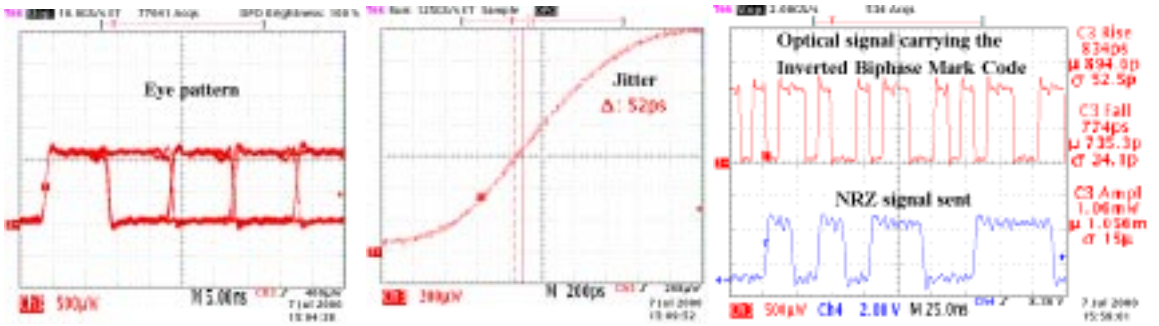
When we drive the VCSEL with a current bias of 5 mA and a modulation current of 7.5 mA, the maximum current driving the VCSEL is 12.5 mA. We can see from the figure that with this current we produce 1 mW of optical power from VCSEL1 and 1.8 mW from VCSEL2. This is an 80% optical power variation between them with respect to the lower optical power. But if we drive the VCSELs with voltage, for 1.99V maximum voltage applied, VCSEL1 emits 1.04 mW and VCSEL2 emits only 1.30 mW. This is a 25% optical power variation with respect to the lower optical power (See Figure 10.). This figure and the three that follow show the signals as seen on a Tektronix TDS 784D digital oscilloscope. The optical signals are input to the oscilloscope by means of the Tektronix P6701A optical probe.




(a) (b)

Figure 10: Optical signals when we drive the Mitel 1A444 VCSELs with voltage. (a) Optical signal from VCSEL1 at 103 Mbps and (b) Optical signal from VCSEL2 at 103Mbps.

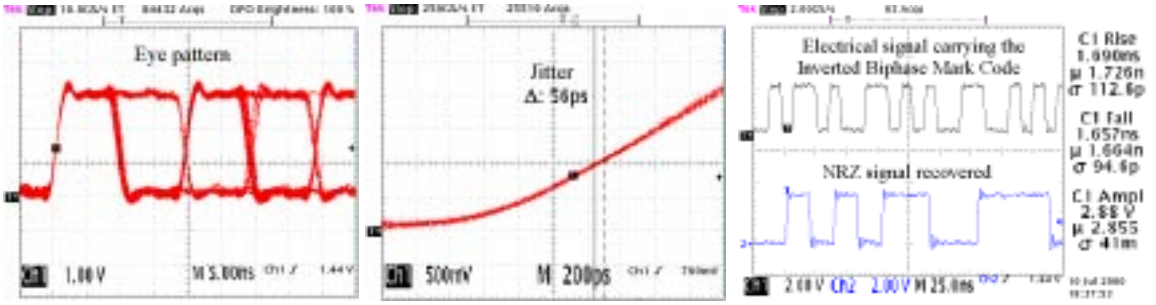
The characteristics of the optical signal output by the 104 Mbps optical link transmitter are very open-eye pattern, 52 ps of jitter peak to peak, and rise and fall times of about 800 ps. These are shown in Figure 11 along with the NRZ signal and the corresponding optical signal carrying the inverted bi-phase mark code.




(a) (b) (c)

Figure 11: Optical signal carrying the inverted bi-phase mark code. (a) Eye pattern, (b) Jitter and (c) Rise and fall times of the optical signal transmitted. Figure 11c also shows the NRZ signal sent.

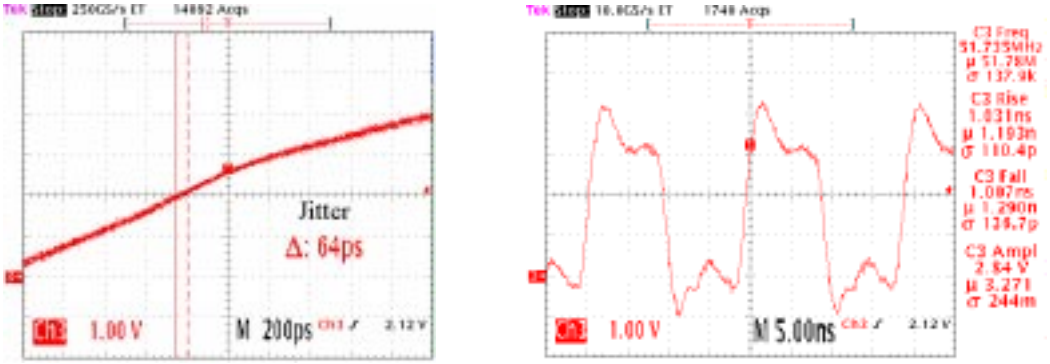
The 104 Mbps optical link receiver recovers the signal with very open-eye pattern, 56 ps of jitter peak to peak, and rise and fall times of 1.7 ns (See Figure 12.).




(a) (b) (c)

Figure 12: Electrical signal carrying the bi-phase mark code recovered. (a) Eye pattern, (b) Jitter and (c) Rise and fall times of the 104 Mbps optical link receiver. Figure 12c also shows the NRZ signal recovered.

The PLL designed and built for the ORCIB provides a clock signal with a jitter of only 64 ps peak to peak and rise and fall times of 1.2 ns to the G-Link daughter cards. The characteristics of this clock signal are shown in Figure 13.




(a) (b)

Figure 13: Clock signal supplied to the CHFET serializer or HDMP-1032 Glink receiver. (a) Jitter and (b) Rise and fall times.

The performance of the first prototype of the ORCI for the BTeV Pixel Vertex Detector is very good. The 104 Mbps optical link receiver recovers the signal with only a slight increase in jitter (about 4 ps) relative to the optical signal transmitted. The rise and fall times increase to 1.7 ns because of the performance limitations of the discriminator. The Bit Error Rate (BER) is another very good indicator of the performance of an optical link and can be calculated [8] as follows:

$$BER \approx \frac{e^{-(SNR^2/2)}}{SNR \times \sqrt{2\pi}} \qquad (1)$$

with *SNR* = Signal to Noise ratio.

We have measured a peak to peak noise of 5mV on the PIN photodiode's output terminal without any optical signal impinging on it. The responsivity of the PIN photodiode is 0.45A/W. Using these inputs we can calculate the SNR ratio as a function of the optical power impinging on the PIN photodiode to get the theoretical BER by means of Equation 1.

The experimental BER was measured using the 7-bit protocol generator as our pattern generator; this generates a long serial stream of bits. This signal is encoded by the bi-phase mark encoder. The bi-phase mark signal is input to the 104 Mbps optical link transmitter. The 104 Mbps optical link receiver recovers the signal. Afterwards, there is a comparison between the recovered signal and the original signal. If they are not equal, the error counter is incremented by one. A block diagram is shown as Figure 14.

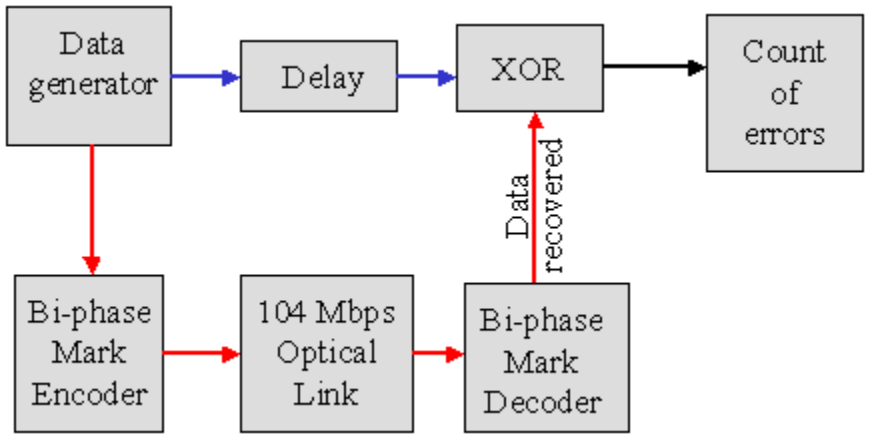



Figure 14: Block diagram of the BER test of the 104 Mbps optical link.

In Figure 15 we show the theoretical and experimental BER of the 104 Mbps optical link as a function of the optical power impinging on the PIN photodiode.

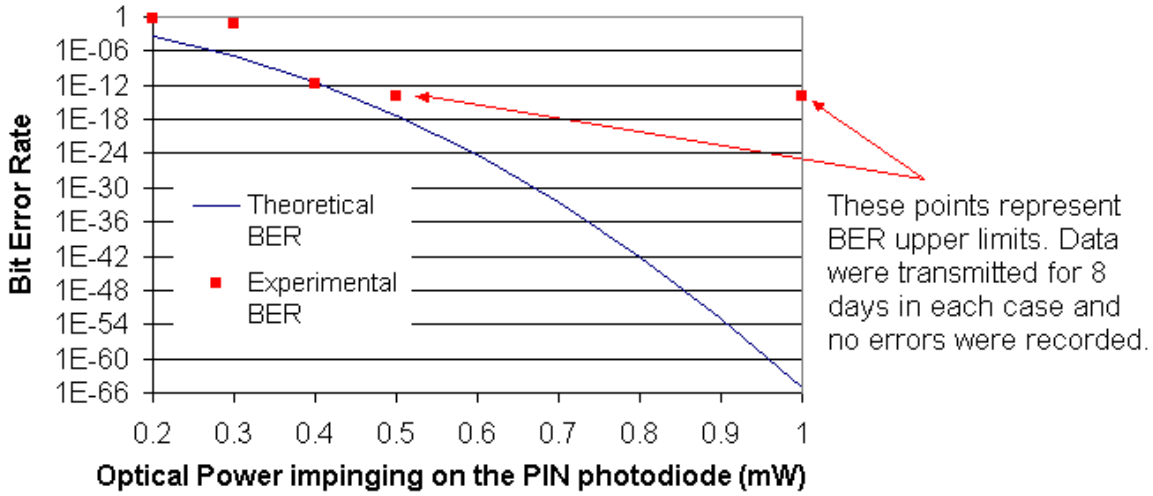



Figure 15: Theoretical and experimental BER of the 104 Mbps optical link.

The measured BER is very small, as expected, which indicates that the bi-phase mark decoder accurately reproduces the information sent from the counting room. The 1.04 Gbps optical link, which transmits the data generated in the MCM, has been shown by others to have a very low BER [9]. The FPGA is not radiation hard, but radiation hard FPGAs are available up to 300kRad [10]. Also, both the HFE-4080 VCSELs from Honeywell and the 1A444 VCSELs from Mitel have been shown to be radiation hard [7,11].

## 4. Tests of the Optical Readout and Control Interface

To verify that the ORCI provides the correct command and control signals to the MCM and performs the readout without introducing errors, we took advantage of an existing test stand at Fermilab, including software. We repeated the noise and threshold uniformity tests that had been carried out using the test stand without the ORCI, and thus were able to make a direct comparison between the two performances. The software developed runs under the LABVIEW framework and was designed to execute the threshold dispersion and noise measurements to characterize the FPIX1 chips on the MCM. Two computers running two different programs are used. One computer controls the test stand instruments and the data acquisition (DAQ); the second performs the data analysis. The DAQ program uses one data generator to send all the commands to configure the MCM and another data generator to send the commands to control the readout. The data acquired are input to a logic analyzer, which transfers them via a local area network (LAN) to the second computer for analysis. The analysis program first fits the threshold curve for each pixel to get the threshold and noise for the individual cells. It then fits a Gaussian to the threshold and noise distributions for the pixels on each chip to determine the mean threshold, threshold dispersion, mean noise, and noise dispersion for each of the five FPIX1 chips on the MCM. Full details are contained in reference 12.

We made the following modifications to the test stand to include the ORCI in the system. For the control path, instead of connecting the two data generators directly to the inputs of the MCM, we connected them to the inputs of the 104 Mbps optical link transmitter and connected the outputs of the 104 Mbps optical link receiver to the command and control lines of the MCM. For the readout path, instead of connecting the 17 data output lines of the MCM directly to the logic analyzer, we connected them to the inputs of the 1.04 Gbps optical link transmitter and the outputs of the 1.04 optical link receiver to the logic analyzer. No changes were needed to the software used to characterize the FPIX1 readout chips on the MCM. A picture of the setup is shown as Figure 16.

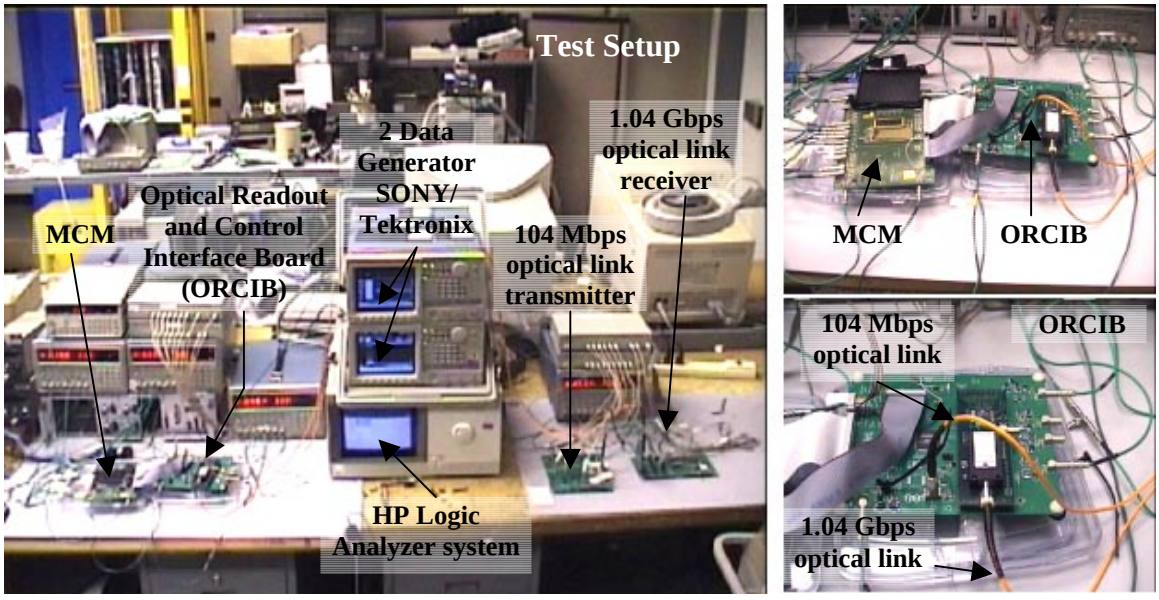
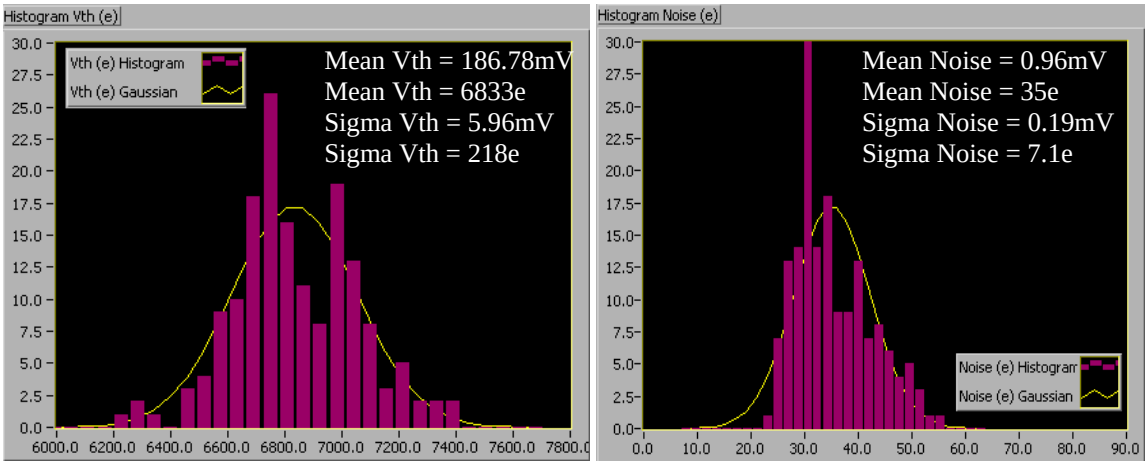



Figure 16: Setup used to characterize the MCM using the optical links to program, control and read out the MCM.

Table 1 shows the results of the threshold and noise uniformity tests of the MCM, obtained with and without the ORCI in the setup. Figure 17 shows the threshold and noise distribution of the first of the five FPIX1 chips on the MCM without using the ORCI. Figure 18 shows the threshold and noise distribution of the same FPIX1 chip using the ORCI. The results are seen to be the same within errors. The noise is slightly higher for the case with the ORCI, most likely because of the unshielded flat cables used to interface it to the MCM.

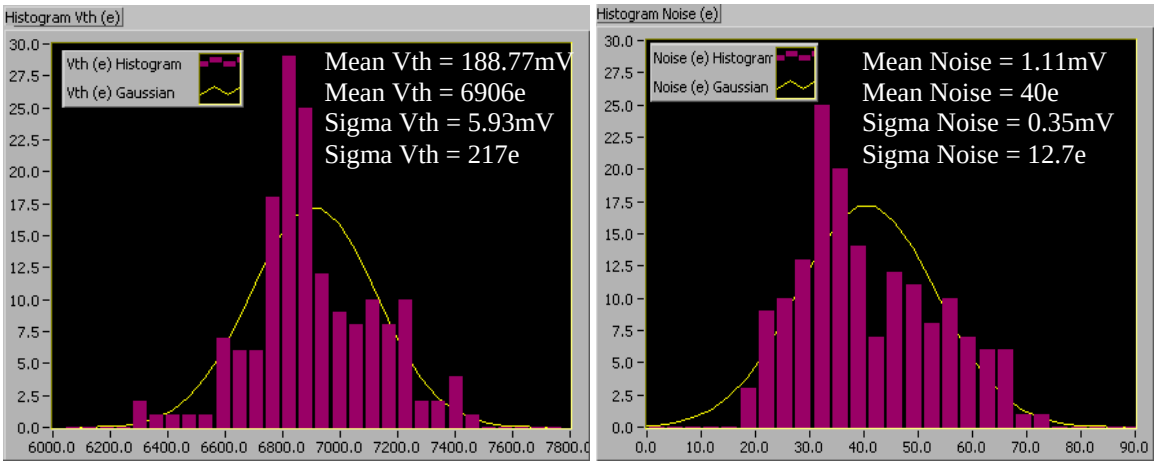
| Vth0 = 1.95V | Results of the characterization of the MCM when tested without the ORCI | | | | |
|---|---|---|---|---|---|
| | **Chip 1** | **Chip 2** | **Chip 3** | **Chip 4** | **Chip 5** |
| Mean threshold (e-) | 6833 | 6657 | 6581 | 6792 | 6956 |
| Threshold dispersion (e-) | 218 | 239 | 217 | 168 | 146 |
| Mean noise (e-) | 35 | 37 | 37 | 31 | 31 |
| Noise dispersion (e-) | 7.1 | 8.1 | 9.0 | 5.9 | 6.2 |
| **Vth0 = 1.95V** | **Results of the characterization of the MCM when tested with the ORCI** | | | | |
| | **Chip 1** | **Chip 2** | **Chip 3** | **Chip 4** | **Chip 5** |
| Mean threshold (e-) | 6906 | 6886 | 6820 | 6910 | 7051 |
| Threshold dispersion (e-) | 217 | 184 | 179 | 142 | 161 |
| Mean noise (e-) | 40 | 37 | 38 | 32 | 30 |
| Noise dispersion (e-) | 12.7 | 13.5 | 12.9 | 9.6 | 9.6 |

Table 1: Results of the threshold and noise uniformity of the MCM when tested with and without the ORCI.




(a) (b)

Figure 17: Distribution of the first of the five FPIX1 chips on the MCM when tested without the ORCI. a) Threshold distribution and b) Noise distribution.




(a) (b)

Figure 18: Distribution of the first of the five FPIX1 chips on the MCM when tested with the ORCI. a) Threshold distribution and b) Noise distribution.

## 5. Summary

The first prototype of the ORCI for the BTeV pixel vertex detector has been designed, built, and tested at Fermilab. The 104 Mbps optical link provides high accuracy transmission of information in a very wide renge of optical power as is evident from the low BERs measured. By driving the VCSELs with voltage we achieve better system uniformity. The decision to use the PIN photodiode in photovoltaic mode results in an improved SNR and is expected to make it less susceptible to SEU. Both of these design choices are expected to provide a larger margin of safety relative to potential radiation damage

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