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DEVELOPMENT OF DIGITAL BEAM POSITION MONITOR FOR HEPS*

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Abstract

High Energy Photon Source (HEPS) is a proposed new generation light source with a beam energy of 6 GeV, high brightness, and ultra-low beam emittance. An RF BPM electronic has been designed at IHEP as part of an R&D program to meet the requirements of both the injection system and storage ring. The RF BPM electronic architecture consists of an Analog Front-End (AFE) board and a Digital Front-End board (DFE) based on a custom platform. In this paper, we present the overall architecture of the RF BPM electronics system and the performance evaluation of the BPM processor, including position resolution and beam current dependence.

INTRODUCTION

High Energy Photon Source (HEPS) is a new 6 GeV synchrotron light source under construction in China. HEPS consists of a storage ring with a circumference of approximately 1360.4 m and energy of 6 GeV; a booster with a circumference of 454 m and energy range of 0.5 to 6 GeV; and a linear accelerator with a length of 49 m and energy of 0.5 GeV [1]. Figure 1 show the diagram of HEPS accelerator composition.

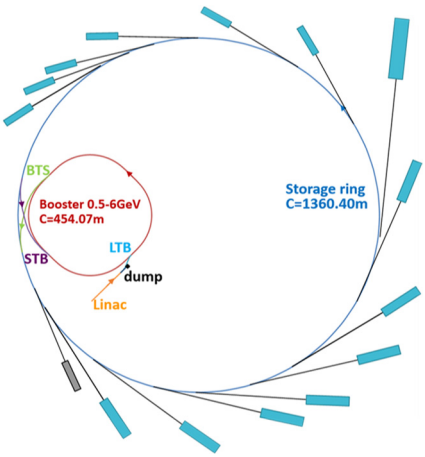

Figure 1: Layout of the HEPS accelerator.

With the HEPS storage ring to a multi-bend achromat lattice, about 700 digital Beam Position Monitors (DBPM) will be required, include LINAC BPM, booster BPM and storage ring BPM. The required numbers of DBPM are gathered in Table 1. And the HEPS beam sizes are below 10 microns in both horizontal and vertical planes, putting stringent requirements on the BPM electronics resolution, long-term stability, beam current dependency and instrument reproducibility.

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Table 1: HEPS BPM Number Requirements List

HEPS Accelerator	BPM Number
LINAC	8
LTB	8
BTS	12
STB	12
Booster	78
Storage Ring	578

SYSTEM ARCHITECTURE

The system architecture of the HEPS RF BPM electronics is shown in Figure 2. The hardware system is primarily divided into Analog front-end (AFE) electronics and digital Front-end (DFE) electronics, while the software system consists of signal processing algorithms, signal logic control, and EPICS driver design [2, 3].

The AFE electronics mainly consist of components such as RF conditioning modules for beam signal RF filtering, amplification, and attenuation, high-speed high-precision digital sampling modules, clock management and distribution modules, and pilot signal output modules.

The DFE electronics primarily utilizes the Xilinx ZYNQ FPGA as the core control unit to implement digital signal processing functions and signal control functions. The board can boot programs using a 32 Gbyte TF-Card and runs a custom Debian system embedded with an EPICS IOC on the ARM system within the FPGA chip. Data caching is performed using 2 Gbyte DDR3 Memory, and data transmission is carried out through a Gigabit Ethernet (GbE).

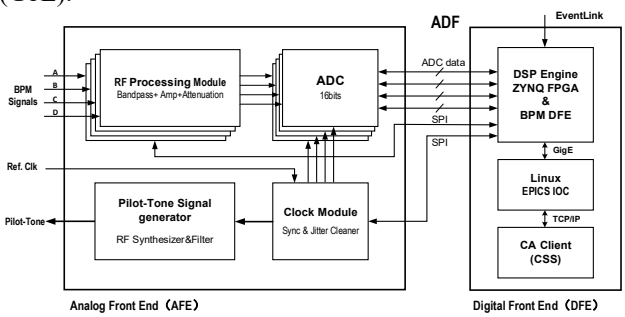

Figure 2: The diagram of HEPS BPM electronic.

Analog Front End (AFE)

The performance of the AFE electronics is a key factor in determining the quality of the entire digital BPM processor, affecting the measurement resolution, sensitivity, and long-term stability of the BPM processor. The beam signal spectrum at HEPS is broad, and the signal at 499.8 MHz is selected to represent the beam position information. In the RF front-end conditioning circuit of the digital BPM signal

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processor, the signal at 499.8 MHz is extracted from the raw BPM signal primarily through a band pass filter and then amplified and attenuated to adjust the raw signal to fit within the effective input range of the ADC for subsequent data acquisition and digital signal processing. The basic architecture schematic of the digital BPM front-end RF conditioning module is shown in Figure 3.

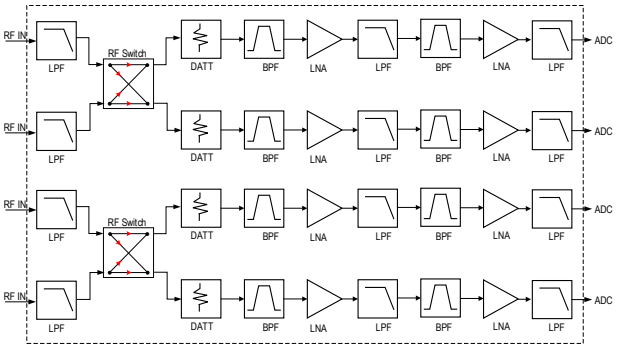

Figure 3: The diagram of AFE module.

The AFE module has been adapted with proper amplification and attenuation stages, as well as with design of the RF switch and A/D converters. The AFE module includes two RF switches designed to minimize the impact of channel variations and temperature changes on test results [4]. These switches help adjust signal paths to ensure more accurate and consistent measurements in the BPM signal processor.

In addition, optimization has been done in the filter section by replacing the SAW filter with a ceramic filter. Ceramic filters offer better temperature stability and improved passband flatness performance. Within the range of 499.8 MHz ± 5 MHz, the flatness is less than 0.1 dB, which will greatly benefit the implementation of the PT function and enhance long-term stability performance.

Digital Front End (DFE)

The digital processing electronics serve as the control unit of the entire digital BPM signal processor, managing the operation of all peripherals and digital signal processing. As shown in Figure 4, the architecture diagram of the digital processing electronics is illustrated. The most crucial component in the digital processing electronics is the Xilinx ZYNQ FPGA module, which provides powerful data processing capabilities, enabling high-performance data processing for real-time control tasks and complex algorithm calculations [5]. The ZYNQ FPGA also offers flexibility in programmability, highly integrated system-level design, low power consumption, high performance, and various interfaces and communication capabilities.

Internally embedded within the digital processing electronics is a dual-core ARM A9 processor, running a Linux-based Debian system and hosting the EPICS control platform. Hardware peripherals include a 2Gbyte DDR3 memory for storing large amounts of data. A gigabit Ethernet program runs on the ZYNQ FPGA for real-time data network transmission. Additionally, the digital electronics incorporate an SFP+ fiber optic data transmission module.

The ZYNQ FPGA is internally divided into the Programmable Logic (PL) side and Processing System (PS) side. The PL side primarily handles data signal processing,

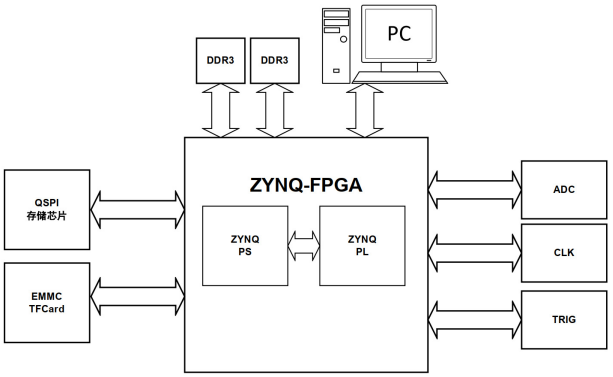

Figure 4: The diagram of HEPS BPM DFE module

Software System

The core of the BPM signal processor lies in the design of the digital signal processing module, and the success of this section's design determines the reliability and stability of the final output results. The digital signal processing section is mainly completed by an FPGA chip, which includes modules for custom functions and digital down-conversion data processing algorithms [6]. The architecture of the digital signal processing module is shown in Figure 5.

The digital down-conversion algorithm module mainly consists of parts such as DDS Compiler, Complex Multiplier, CORDIC, CIC Compiler, FIR Compiler, and others. This algorithm processes the intermediate frequency band digital signal obtained through high-precision ADC bandpass sampling, down-converting the digital signal to baseband for the second time to obtain DC IQ signals [7, 8]. Through CORDIC calculations, the amplitude of the ADC input down-converted signal is determined, and the signal is then extracted and filtered using digital filters to obtain beam position information at different rates and bandwidths.

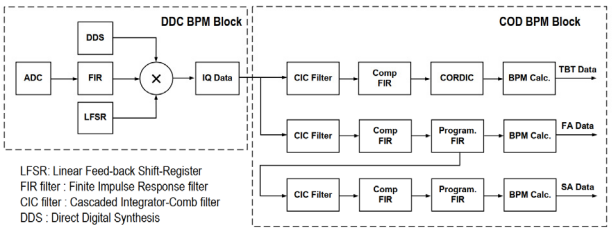

Figure 5: The architecture of the DSP module.

EPICS Driver

In the ZYNQ FPGA design platform, a significant advantage is the inclusion of a dual-core ARM-A9 series processor, which is embedded and runs a Linux-based Debian system. This greatly enhances the integration and reliability of the BPM signal processor. The design of the embedded EPICS driver based on this Debian system is an important and challenging part of the BPM signal processor.

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On the ZYNQ FPGA design platform of the BPM signal processor, a cross-data transfer method based on Linux Kernel Driver has been designed to facilitate data acquisition through different transmission methods. For instance, the original ADC data, which has a large volume, utilizes DMA data transfer, while other TBT, FA, and SA data employ FIFO for data transfer [9]. The architecture of the embedded EPICS driver design is illustrated in Figure 6.

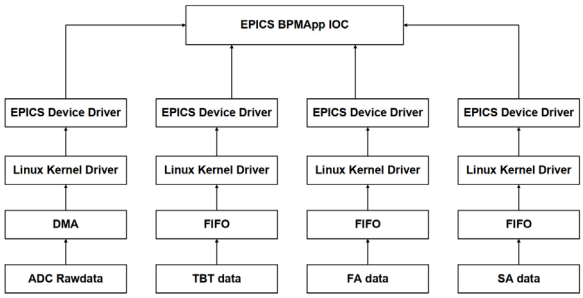

Figure 6: The architecture of the embedded EPICS driver.

PERFORMANCE TEST

Based on the detailed design and testing described above, a comprehensive performance evaluation test was conducted on the BPM signal processor in a laboratory environment. The laboratory primarily tested the data performance of TBT, FA and SA [10].

Turn by Turn (TBT)

In the laboratory setting, a signal of 499.8 MHz with a power level of -20 dBm was input into the four-channel input signal port of the BPM signal processor for testing the resolution of TBT data. TBT frequency of HEPS is 220 kHz, a total of 2000 points of TBT data were collected in the laboratory for resolution testing. The results showed that the STD of TBT-X direction is approximately 393 nm, and the STD of TBT-Y direction is approximately 390 nm. The resolution test results for TBT are shown in Figure 7, meeting the design requirements.

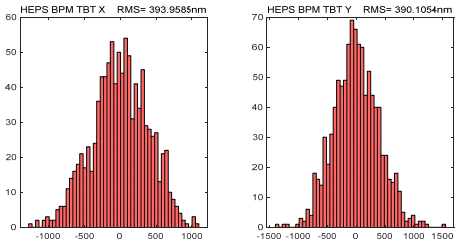

Figure 7: The resolution test results for TBT.

Fast Acquire (FA)

In the laboratory setting, a signal of 499.8 MHz with a power level of -20 dBm was input into the four-channel input signal port of the BPM signal processor for testing the resolution of FA data. FA frequency of HEPS is 22 kHz, a total of 2000 points of FA data were collected in the laboratory for resolution testing. The results showed that the resolution of FA-X direction is approximately 162 nm, and the resolution of FA-Y direction is approximately 165 nm. The resolution test results for FA are shown in Figure 8.

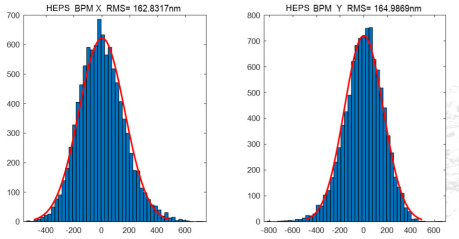

Figure 8: The resolution test results for FA.

Slow Acquire (SA)

In the laboratory setting, a signal of 499.8 MHz with a power level of -20 dBm was input into the four-channel input signal port of the BPM signal processor for testing the resolution of FA data. A total of 1000 points of SA data were collected in the laboratory for resolution testing. The results showed that the resolution of SA-X direction is approximately 48 nm, and the resolution of SA-Y direction is about 65 nm. When the RF switch is ON, the resolution of SA-X and SA-Y are all less than 5 nm. The resolution test results for SA are shown in Figure 9.

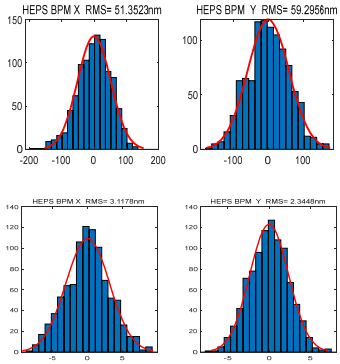

Figure 9: The resolution test results for SA.

Beam Current Dependence (BCD)

Beam Current Dependence (BCD) is also a key performance indicator of the BPM during operation [11, 12]. We conducted detailed testing in the laboratory, using an R&S SMA100A signal source to test the BCD from -54 dBm to -14 dBm. As shown in Figure 10, the BCD of both X and Y directions is about 2 μm, meeting the system requirements. When the RF Switch is on, the BCD value drops to less than 1 μm.

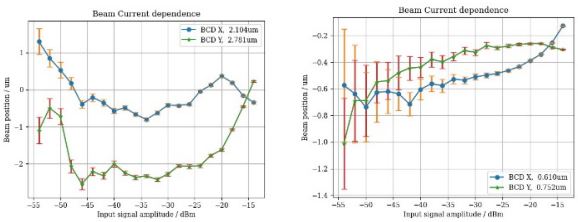

Figure 10: The BCD test results.

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CONCLUSION

The development of a BPM processor for the HEPS has successfully demonstrated performance and stability, and the BPM processor has been successfully applied in the LINAC, injector, booster, and storage ring of HEPS. This BPM processor not only monitors the closed orbit signals but also captures TBT signals, FA signals and monitors the first-turn injection mode. The entire HEPS accelerator is equipped with about 700 BPM signal processors, covering the entire HEPS facility, and meeting the requirements for beam tuning and operation at HEPS.

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