**Design and first test results of the CMS HGCAL on-detector ECON-T ASIC with a reconfigurable encoder algorithm for data compression**

Cristina Mantilla Suarez¹ and Jim Hoff¹ on behalf of the CMS Collaboration

**Huge data challenge:** HGCAL is a 6M channel “imaging calorimeter” with good precision over wide dynamic range for amplitude and time of arrival.

- 4 selectable trigger data compression algorithms: variable and fixed-latency options.
- Includes formatter and smart buffer.
- PLL and 1.28GHz phase-aligners from lpGBT.

**ECON-T:** sums, selects and compresses trigger charge data @ 40 MHz

**Eye diagram measured on one of the 13 outputs 1.28Gbps 4Tx channels.**

**Phase value selected at the center of the eye diagram to minimize the error rate.**

**Phase value selected at the center of the**

- **Bench Tests and Radiation Tolerance SEE Tests**

  - SEE Tests with 200 MeV protons with fluence: 5.4E+12 p/cm² H-L-LHC fluence: 1E+14 p/cm²

  - ECON-T has triplication for SEE protection.

  - Chose not to replicate clocks for simplicity and power, I²C configuration protected with dedicated Hamming correction.

  - Observed serializer SEU in radiation tests. Serializer design improved for v2.

  - 1.28 Gbps outputs agree perfectly with simulation/emulation run on FPGA.

  - Verified functionality of power-up-state-machine, PLL, eRx, eTx, formatter, serializer and buffer.

**Results**

- Chip functionality has been verified.
- Few verilog bugs found, fixed for v2.
- SEE tests: no observed I²C errors or errors requiring chip reset.

**Overview**

- **AI on Chip: Reconfigurable Encoder**

  - Input (48x7bit)
  - Encoded 16 x 3bit outputs, 48 bits
  - Decode off-detector to 336 bits

  - Quantization Aware Training of Encoder algorithm based on LHC simulation.

  - Optimization of CNN architecture for physics performance and area and power requirements.

  - Reconfigurable weights and biases via I²C.

  - Full triplication of clocks, logic, and resets for I²C configuration.

**Latency**

<table>
<thead>
<tr>
<th>Buffer Latency</th>
<th>Target</th>
<th>Achieved</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-12 BX</td>
<td>0-12 BX</td>
<td></td>
</tr>
<tr>
<td>Other Latency</td>
<td></td>
<td>7 BX</td>
</tr>
<tr>
<td>Power consumption</td>
<td>500 mW</td>
<td>Most of detector: 385 mW Max 420 mW</td>
</tr>
<tr>
<td>TID</td>
<td>200 Mrad</td>
<td>In progress</td>
</tr>
</tbody>
</table>

**SEE tolerance**

- Cross section results:
  - IPC configuration: 0
  - Error requiring reset: <1err/30s on whole detector
  - eRx single bit error: 1.7E-11 cm²

**ECON-T Testing Results**