Journal of Applied Physics

RESEARCH ARTICLE | JUNE 03 2025

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J. Appl. Phys. 137, 215702 (2025)
https://doi.org/10.1063/5.0267235

Journal of Applied Physics ARTICLE pubs.aip.org/aip/jap

Modeling total ionizing dose effects in fully-depleted silicon-on-insulator technology: Bridging device degradation to radiation-hardened circuit design

Cite as: J. Appl. Phys. **137**, 215702 (2025); doi: 10.1063/5.0267235
Submitted: 23 February 2025 · Accepted: 14 May 2025 ·
Published Online: 3 June 2025

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ABSTRACT

While a fully depleted silicon-on-insulator (FDSOI) metal–oxide–semiconductor field-effect transistor (MOSFET) exhibits superior immunity to single event effects through buried oxide layer isolation, its vulnerability to total ionizing dose (TID) effects poses significant reliability challenges in radiation-intensive applications. This work aims to bridge device-level performance degradation mechanisms to circuit-level reliability prediction through modeling TID effects in FDSOI technology. A physics-based TID effects model is developed to quantify the dependence of radiation-induced trapped charge density on cumulative dose and bias condition. The model is then integrated into the industry-standard FDSOI compact model BSIM-IMG through modified surface potential equations, enabling accurate prediction of a TID-induced threshold voltage shift and leakage current elevation. Credibility of the proposed model is verified through comparative analysis with the experimental current–voltage characteristics of devices measured at varying radiation doses. Key radiation-related parameters, including radiation-induced trapped charge density and a mobility degradation parameter, are extracted, enabling predictive simulation of FDSOI ring oscillator circuit performance degradation under ionizing radiation conditions. The feasibility of back-gate biasing to mitigate TID effects in the ring oscillator circuit is demonstrated, underscoring its potential as a circuit-level solution for radiation-hardened designs.

I. INTRODUCTION

Over the last two decades, with the rapid acceleration of the space industry, human's enthusiasm for the outer space exploration is tremendously stimulated. Just recently NASA's Europa Clipper, which is the largest spacecraft ever built, has successfully embarked on its long voyage to Europa for the purpose of studying the Jovian moon's potential to support life. As missions to space become more ambitious, radiation hardening techniques have to evolve considering the harsh space environment. Outer space that generally portrayed as "vacuum" is actually filled with an interstellar medium. The interstellar medium contains cosmic rays that will cause damage to microelectronic components. A silicon-on-insulator (SOI) is one of the radiation hardening technologies that designed to inhibit a kind of radiation damage called single event effects (SEEs). Specifically, SOI technology dielectrically isolates the channel and the substrate by introducing a buried oxide (BOX) layer, which improves the latch-up immunity and suppresses the SEE failures by dramatically reducing the charge collection volume.[1,2] Despite the great advantages mentioned above, the introduction of a BOX layer is not entirely free of drawbacks. The current literature has verified that the SOI technology is more vulnerable to total ionizing dose (TID) effects compared to their bulk silicon counterparts.[3,4] The phenomena of device performance deterioration caused by radiation-induced charge generation/trapping in the isolation oxides are referred as the TID effects.

This work focuses on the fully depleted SOI metal–oxide–semiconductor field-effect transistor (FDSOI MOSFET), which possesses a thin channel layer where the floating body is not present, thus effectively eliminating the kink effect compared to the

partially depleted SOI (PDSOI) MOSFET. Much effort has been spent on studying the TID effects of FDSOI MOSFETs by experimental investigation and TCAD simulation.[5–7] While device-level TID characterization provides fundamental insights, circuit-level analysis is imperative for modern integrated circuits containing billions of nanoscale transistors, where localized degradation can cascade into system-level failures. During circuit analysis and design, compact models are commonly adopted to describe the device characteristics by solving a set of physics-based analytical expressions with technology-dependent device model parameters. Therefore, analyzing the influence of TID effects on FDSOI-based circuits requires the incorporation of TID effects into a standard compact model. Esqueda *et al.*[8] presented a physics-based compact modeling approach for TID effects in SOI technology; yet, discussions on the compatibility of this approach with the standard compact model that is dedicated to FDSOI MOSFETs are not involved in their work. Rostand *et al.*[9] proposed an incorporation of TID effects into an Leti-UTSOI compact model for FDSOI devices, while their modeling of TID effects lacks discussion of key radiation-related parameters. Note that the radiation-induced trapped charge density is highly related to the cumulative dose and the bias condition, which are not taken into account in their work.

This work proposes a novel methodology to integrate TID effects into the BSIM-IMG compact model, ensuring compatibility with industry-standard tools and direct applicability to FDSOI MOSFETs. The methodology develops a physics-based TID degradation model that quantitatively captures the radiation-induced performance degradation mechanisms, including a threshold voltage shift and elevated leakage current. Through detailed analysis of charge trapping dynamics in the BOX layer, the model establishes explicit correlations among the trapped charge density, the cumulative dose, and the bias condition. This is crucial for predicting device performance under diverse irradiation scenarios. By reformulating the back-gate surface potential equations, the TID effect model is embedded into BSIM-IMG, enabling the derivation of an analytical drain current expression that incorporates radiation-induced mobility degradation and oxide/interface trap effects. These methodological improvements yield higher accuracy compared to existing approaches.

II. EXPERIMENTAL DETAILS

Three sets of ultra-thin body and BOX (UTBB) FDSOI MOSFETs based on a 22-nm process node with different channel widths ($W = 170$ nm, 1 μm, and 10 μm) were selected in this work. In the device configuration, there are four external biases, which are a front-gate bias (V_{gf}), a back-gate bias (V_{gb}), a drain bias (V_d), and a source bias (V_s). Thicknesses of the silicon channel, the gate oxide, and BOX layers are 6, 1, and 20 nm, respectively. TID experiments were conducted under gamma-ray exposure provided by a ^{60}Co radiation source at the Xinjiang Technical Institute of Physics & Chemistry of the Chinese Academy of Sciences. The dose rate was 100 rad(Si) per second. TID responses of devices were measured prior to irradiation and after irradiation up to 100, 300, and 500 krad(Si) at ambient temperature. During gamma-ray irradiation, devices were mounted on the test card under a transmission gate (TG) bias of $V_{gf} = V_{gb} = 0$ and $V_d = V_s = 0.8$ V. A schematic diagram of an UTBB FDSOI MOSFET irradiated with gamma rays is displayed in Fig. 1(a), and a schematic cross-sectional view of an n-type UTBB FDSOI MOSFET is shown in Fig. 1(b).

III. MODEL FORMULATION

A. TID effect model

As pointed out in the previous literature studies,[6,10,11] oxide traps and interface traps are two main causes responsible for the reduced TID tolerance of SOI technology. Below is an elaboration on the modeling of TID effects in UTBB FDSOI MOSFETs based

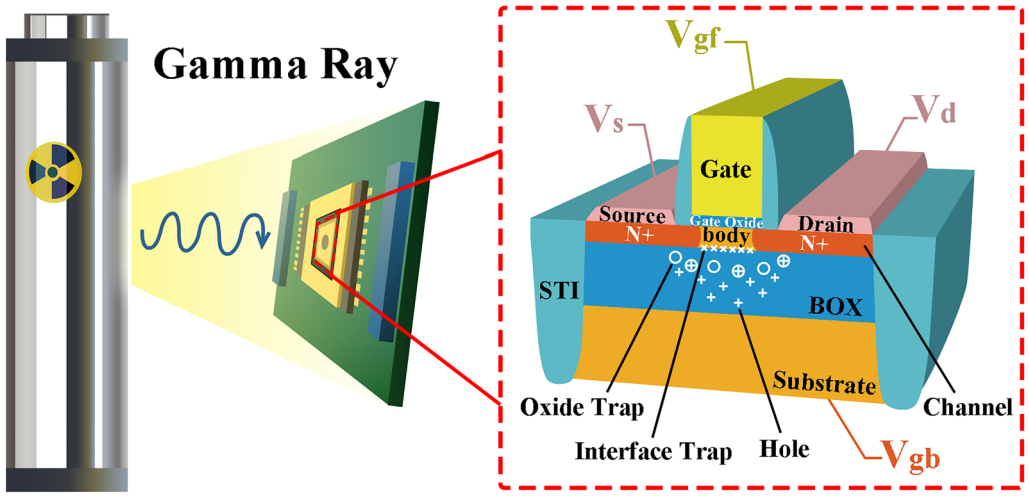

FIG. 1. Schematic diagram of an UTBB FDSOI MOSFET irradiated with gamma rays.

on the systematic analysis of radiation-generated charge trapping dynamics.

First and foremost, the 1 nm-thick gate oxide layer is so thin that can be ignored in the TID effect modeling. In other words, neither gate oxide traps nor front interface traps are considered. On one hand, this is because the number of oxide traps within the gate oxide layer is negligible compared to that within the BOX layer. On the other hand, the back interface trap density far exceeds the front interface trap density, which is supported by the work of Cheng *et al.*[12] where the back and front interface trap densities of FDSOI MOSFETs are extracted using an experimental technique and the ratio of the former to the latter is approximately 25.

Under gamma-ray exposure, high-energy photons pass through the BOX layer and lose energy in the form of Compton scattering. The scattering reaction produces a scattered photon and a free recoil electron that can interact with other electrons and nuclei. The subsequent impact ionization of free electrons with other target atoms produces a large number of electron–hole pairs (ehps). Producing each ehp requires approximately 17 eV of energy in SiO_2 on the femtosecond timescale.[13] Thus, the initial ehp density generated in SiO_2 per rad that is typically denoted by the conversion factor g_0 is estimated to be 8.1×10^{12} pairs cm^{-3} rad^{-1}. A fraction of ehps will recombine immediately after their production, and the others begin to transport within the BOX layer. The fraction of holes that escape initial recombination is defined as the hole yield (f_y), which is reported to depend on the electric field within the BOX layer and the stopping power of the incident radiation particle.[14] For ^{60}Co gamma rays, dependence of the hole yield (f_y) on the magnitude of the electric field (E) can be empirically approximated by $f_y(E) = (0.5/|E| + 1)^{-0.7}$ (Ref. 15), where E is in units of MV/cm. The number of holes that escape initial recombination per unit area (N_h) then could be expressed by the product of the cumulative dose (D), the conversion factor (g_0), the hole yield (f_y), and the BOX layer thickness (t_{box}),

$$N_h = D g_0 f_y t_{box}. \tag{1}$$

For the TG bias condition, both the front gate and the back gate are grounded. In addition, both the drain and the source are connected to the supply voltage. Consequently, two reverse-biased P–N junctions (drain–body and source–body junctions) are formed in NMOS. Under the circumstance, holes that escape initial recombination are attracted toward the back interface of the channel driven by the electric field. The transport behavior of holes is described as "hopping" through localized states in the valence band. As long as these holes approach the back interface, some of them will be captured by deep-level hole traps. Note that the hole trapping will be confined under the body region by the symmetric electric field distribution, which explains why the TG state is the worst bias condition for FDSOI MOSFETs as reported by Ferlet-Cavrois *et al.*[16]

The dominant defects responsible for the deep-level hole traps are oxygen vacancies accumulated in the strained transition region.[11,17] An oxygen vacancy serves as a non-activated donor center, which can capture a hole and, therefore, form a positive oxide trapped charge. The number of positive oxide trapped charges per unit area (N_{botc}) is directly related to the saturation density of oxide traps ($N_{bot,sat}$) and the density of radiation-generated holes that escapes recombination (N_h), which can be expressed by

$$N_{botc} = \frac{K_{bot} N_h}{\sqrt{1 + (K_{bot} N_h / N_{bot,sat})^2}}, \tag{2}$$

where K_{bot} is a proportionality coefficient and the term $K_{bot}N_h$ represents the density of holes captured by oxide traps that approach the back interface of the channel. Note that $N_{botc} \approx K_{bot}N_h$ when $K_{bot}N_h << N_{bot,sat}$ and $N_{botc} \approx N_{bot,sat}$ when $K_{bot}N_h >> N_{bot,sat}$. The former corresponds to what will happen at the beginning of irradiation, and the latter corresponds to the situation when oxide traps are filled up with holes captured.

Meanwhile, protons (H^+) are released during the transport of holes, which will also drift toward the back interface of the channel and react with the passivated dangling bonds, thus facilitating the formation of back interface traps under the body region ultimately.[18] These localized interface traps are electrically active states that can exchange charges with the adjacent silicon channel layer. The occupancy of interface traps is determined by the Fermi level position, and hence, the number of interface trapped charges per unit area (N_{bitc}) is given by

$$N_{bitc} = D_{bitc}(\psi_{sb} - \phi_n) = \frac{K_{bit} N_h}{\sqrt{1 + (K_{bit} N_h / D_{bit,sat})^2}} (\psi_{sb} - \phi_n), \tag{3}$$

where ψ_{sb} is the back surface potential and ϕ_n is the quasi-Fermi potential of the channel ($\phi_n = V_s$ at the source end and $\phi_n = V_d$ at the drain end). D_{bitc} represents the back interface trapped charges per unit area per unit volt, which is positively correlated with $K_{bit}N_h$ and $D_{bit,sat}$. Herein, $D_{bit,sat}$ is the saturation density of back interface traps per unit volt. The term $K_{bit}N_h$ denotes the density of protons released following hole capture. The dependence of D_{bitc} on N_h is built on the consensus that the capture of holes during the transport process leads to the release of protons and contributes to the subsequent formation of interface traps.[19–21]

B. Drain current model

To probe into the influence of TID effects on FDSOI-based circuits, (2) and (3) should be incorporated into an industry-standard compact model. In this work, the physical surface-potential-based Independent Multi-Gate (BSIM-IMG) model that is developed to capture the electrical characteristics of UTBB FDSOI MOSFETs is utilized.[22,23] The derivation of drain current in the BSIM-IMG model relies on the calculation of front and back surface potentials. To incorporate the TID effects into the BSIM-IMG compact model, additional terms representing the contributions of N_{botc} and N_{bitc} are introduced into the surface potential expressions. To start with, the one-dimensional Poisson equation for an UTBB FDSOI MOSFET is shown below:

$$\frac{d^2\psi}{dy^2} = \frac{q n_i}{\varepsilon_{ch}} \exp\left(\frac{\psi - \phi_n}{V_t}\right), \tag{4}$$

where y stands for the vertical direction across the channel, ψ for the channel electrostatic potential, q for the elementary charge, n_i

for the intrinsic carrier density in the channel, ε_{ch} for the channel permittivity, and V_t for the thermal voltage with $V_t = k_B T/q$ (k_B is the Boltzmann constant and T the device temperature). Replacing $d^2\psi/dy^2$ by $(1/2)dE^2/d\psi$ in the left side of (4), then moving $d\psi$ to the right side and integrating it from the back surface to the front surface of the silicon channel, (5) is obtained,

$$E_{sf}^2 - E_{sb}^2 = \frac{2qn_i V_t}{\varepsilon_{ch}} e^{-\phi_n/V_t}\left(e^{\psi_{sf}/V_t} - e^{\psi_{sb}/V_t}\right), \tag{5}$$

where $E_{sf,b}$ and $\psi_{sf,b}$ are electric fields and electrostatic potentials at the front or back surface, respectively. E_{sf} and E_{sb} are in relation to the front- and back-gate voltages as given by

$$E_{sf}^2 = \left[C_{\rm ox}(V_{gf} - \Phi_{mf} - \psi_{sf})/\varepsilon_{ch}\right]^2, \tag{6a}$$

$$E_{sb}^2 = \left(\frac{C_{\rm box}}{\varepsilon_{ch}}\right)^2\left[V_{gb} - \Phi_{mb} - \frac{-qN_{\rm botc}}{C_{\rm box}} - \frac{qD_{\rm bitc}(\psi_{sb} - \phi_n)}{C_{\rm box}} - \psi_{sb}\right]^2, \tag{6b}$$

where $\Phi_{mf,b}$ is the front or back gate-to-semiconductor work function difference. C_{ox} stands for the gate oxide capacitance with $C_{ox} = \varepsilon_{ox}/t_{ox}$ (ε_{ox}: is the gate oxide permittivity and t_{ox} the gate oxide layer thickness) and $C_{\rm box}$ for the buried oxide capacitance with $C_{\rm box} = \varepsilon_{\rm box}/t_{\rm box}$ ($\varepsilon_{\rm box}$ is the buried oxide permittivity). The term $(-qN_{\rm boxc}/C_{\rm box})$ denotes the defect potential arising from oxide trapped charges within the BOX layer, and $qD_{\rm bitc}(\psi_{sb} - \phi_n)/C_{\rm box}$ represents the defect potential stemming from back interface trapped charges. Note that the oxide trapped charges are positive, whereas the interface trapped charges are negative for NMOS. Positive trapped charges favor the inversion regime by repulsing holes in the back channel, thus resulting in the negative shift of the threshold voltage. On the contrary, negative trapped charges give rise to the positive shift of the threshold voltage. Substituting E_{sf} and E_{sb} in (5) with (6) leads to the following relation in a normalized fashion:

$$k_1^2(x_{gf} - x_{sf})^2 - k_2^2(x_{gb} - x_{sb})^2 = A_0 e^{-x_n}(e^{x_{sf}} - e^{x_{sb}}), \tag{7}$$

where $x_n = \phi_n/V_t$, $x_{sf} = \psi_{sf}/V_t$, $x_{sb} = \psi_{sb}/V_t$, $k_1 = C_{ox}/C_{ch}$, $k_2 = C_{\rm box}(1 + qD_{\rm bitc}/C_{\rm box})/C_{ch}$, $C_{ch} = \varepsilon_{ch}/t_{ch}$, and $t_{\rm ch}$ is the channel thickness. x_{gf}, x_{gb}, and A_0 are expressed by

$$x_{gf} = (V_{gf} - \Phi_{mf})/V_t, \tag{8a}$$

$$x_{gb} = \frac{V_{gb} - \Phi_{mb} + qN_{\rm botc}/C_{\rm box} + \phi_n C_{\rm bit}/C_{\rm box}}{(1 + C_{\rm bit}/C_{\rm box})V_t}, \tag{8b}$$

$$A_0 = 2qn_i t_{ch}^2/(\varepsilon_{ch} V_t), \tag{8c}$$

where $C_{\rm bit}$ represents the back interface capacitance with $C_{\rm bit} = qD_{\rm bitc}$. Note that (7) is a binary quadratic equation with two unknowns x_{sf} and x_{sb} that await being solved. Considering the capacitive coupling between the front and back interfaces, the front and back surface potentials (ψ_{sf} and ψ_{sb}) with respect to the applied front- and back-gate voltages could be given by

$$V_{gb} - \Phi_{mb} + \frac{qN_{\rm botc}}{C_{\rm box}} + \frac{\phi_n C_{\rm bit}}{C_{\rm box}} = \left(1 + \frac{C_{ch}}{C_{\rm box}} + \frac{C_{\rm bit}}{C_{\rm box}}\right)\psi_{sb} - \frac{C_{ch}}{C_{\rm box}}\psi_{sf}. \tag{9}$$

According to (9), x_{sb} could be expressed as a function of x_{sf} in the form of

$$x_{sb} = \frac{C_{ch}}{C_{ch} + C_{\rm box} + C_{\rm bit}} x_{sf} + \frac{C_{\rm box} + C_{\rm bit}}{C_{ch} + C_{\rm box} + C_{\rm bit}} x_{gb}. \tag{10}$$

Finally, ψ_{sf} and ψ_{sb} are derived by solving (7) and (10) simultaneously, based on which the drain current can be readily obtained by

$$I_d = \frac{\mu_{\rm total}(\mu_{\rm efff}, \mu_{\rm effb})W}{D_{\rm vsat}L} i_{\rm ds0}(q_{\rm fronts}, q_{\rm frontd}, q_{\rm backs}, q_{\rm backd}), \tag{11}$$

where $i_{\rm ds0}$ represents the normalized drain current, which is dependent on $q_{\rm fronts,d}$ and $q_{\rm backs,d}$. Herein, $q_{\rm fronts}$ and $q_{\rm frontd}$ stand for the front charge at the source and drain ends and $q_{\rm backs}$ and $q_{\rm backd}$ for the back charge at the source and drain ends. The former two are functions of ψ_{sf} and the latter two are functions of ψ_{sb}.[24] $D_{\rm vsat}$ denotes the drain current degradation factor resulted from the velocity saturation in the linear region.[25] $\mu_{\rm total}$ is the total channel mobility, which is determined by the effective front side mobility ($\mu_{\rm efff}$) and the effective back side mobility ($\mu_{\rm effb}$); see the work of Lin *et al.*[26] for explicit expressions. Note that both oxide trapped charges and interface trapped charges will cause the degradation of $\mu_{\rm effb}$ due to the enhanced Coulomb scattering. In view of this, the radiation-induced back-channel mobility degradation can be modeled by

$$\mu_{\rm effb,tid} = \mu_{\rm effb}/(1 + \alpha_{\rm bot}N_{\rm botc} + \alpha_{\rm bit}N_{\rm bitc}), \tag{12}$$

where $\alpha_{\rm bot}$ and $\alpha_{\rm bit}$ are model parameters that characterize the effects of oxide and interface trapped charges, respectively.

IV. MODEL VERIFICATION

The proposed drain current model considering the TID effects is then verified by fitting the experimentally measured I_d–V_{gf} characteristics of UTBB FDSOI MOSFETs at different radiation doses. Seven radiation-related model parameters (f_y, $N_{\rm bot,sat}$, $D_{\rm bit,sat}$, $K_{\rm bot}$, $K_{\rm bit}$, $\alpha_{\rm bot}$, and $\alpha_{\rm bit}$) await being extracted during the fitting procedure.

First, fitting range of f_y that is associated with the electric field within the BOX layer under a TG bias is determined by means of Silvaco TCAD tools. The structure of an n-type UTBB FDSOI MOSFET is created using Atlas syntax. The pre-radiation front gate transfer characteristic (I_d–V_{gf}) is simulated as shown in Fig. 2, where the drain current (I_d) remains insignificant until the front-gate voltage (V_{gf}) reaches the threshold voltage. The threshold voltage is defined as the gate voltage at which the device starts to switch on. Moreover, it is observed that the simulated I_d–V_{gf} data

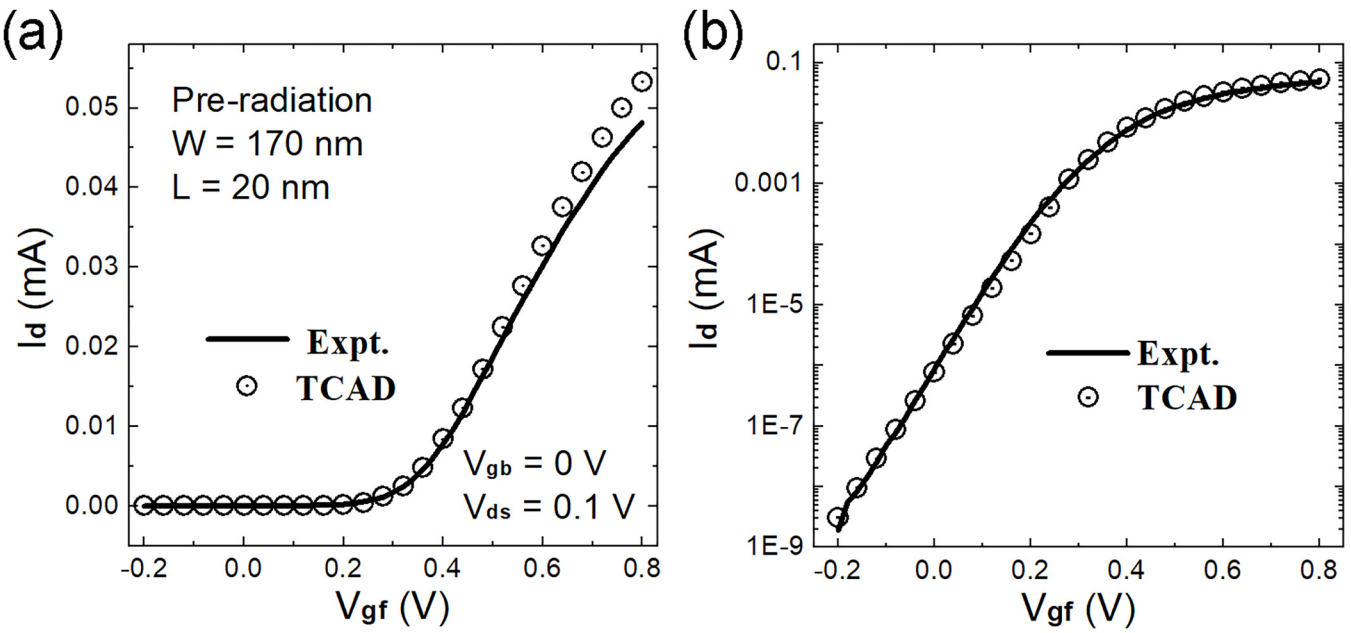

FIG. 2. Pre-radiation front-gate transfer characteristic (I_d–V_{gf}) of an n-type UTBB FDSOI MOSFET, experimentally measured and simulated using Silvaco TCAD tools. (a) Data are plotted on a linear scale representation. (b) Data are plotted on a logarithmic scale representation.

basically agree with the measured ones, which confirms the credibility of the follow-up simulation results.

On this basis, an electric field distribution within the BOX layer under a TG bias is simulated. The electric potential contours and electric field lines are displayed in Figs. 3(a) and 3(b). During the initial phase of voltage application ($V_s = V_d = 0.1$ V), all the electric field lines are directed from the drain and source regions toward the body region. As the drain and source voltages rise to the supply voltage, a fraction of the electric field lines extend to the rear surface of the BOX layer, whereas the majority remain terminate under the body region. Therefore, hole trapping mainly occurs under the body region, and any spreading is prohibited by the symmetric electric field distribution. Note that the overall electric field distribution consists of two parts: one is produced by the doping difference between the body and the drain or source regions, and the other is resulted from the applied drain or source bias. In Figs. 3(a) and 3(b), the insets illustrate the simulated energy band diagrams along the cutline, which demonstrate that the transport direction of holes is mainly toward the back interface of the channel, coinciding with the above analysis. Figure 3(c) exhibits the vertical electric field component (E_y) along the cutline under a TG bias. The corresponding f_y that varies with the magnitude of the electric field is calculated as shown in Fig. 3(d), where an average value of 0.3 is observed and the fitting range for f_y is confirmed from 0 to 0.6.

Next, I_d–V_{gf} characteristics of UTBB FDSOI MOSFETs experimentally measured at different radiation doses are fitted. Comparisons between the experimental data and the modeled ones are displayed in Fig. 4, where black hollow circles stand for the measured data and colorful solid circles for the modeled results at different radiation doses. For three sets of devices with channel widths ranging from 170 nm and 10 μm, comparisons between modeled and measured results demonstrate consistency in the above-threshold region but reveal minor discrepancies in the subthreshold region. These discrepancies may arise from several factors. First, the drain current (I_d) in the subthreshold region is exponentially dependent on the front-gate bias (V_{gf}) due to carrier diffusion. Carrier mobility, which governs the transport behavior of carriers, is significantly affected by radiation-enhanced Coulomb scattering. This work considers mobility degradation with a cumulative dose, as modeled in (12). However, the relationship between the carrier mobility and the radiation dose in UTBB FDSOI MOSFETs may be more complex than captured by (12). This can lead to minor mismatches between modeled and measured results. Second, experimental uncertainties not fully reflected in the model contribute to these discrepancies, including variability in the radiation dose delivery (e.g., a non-uniform dose distribution or calibration errors in the gamma-ray source), environmental factors (e.g., temperature fluctuations during irradiation), and measurement system limitations (e.g., noise in low-current measurements). These factors explain the observed discrepancies and highlight areas for further model refinement.

The extracted radiation-related model parameters for three sets of devices are listed in Table I. It is observed that the hole yield (f_y) decreases as the channel width (W) gets wider owing to the declined electric field strength within the BOX layer as shown in Fig. 5(a). In addition, saturation densities of both oxide traps ($N_{bot,sat}$) and interface traps ($D_{bit,sat}$) are seen to increase with W.

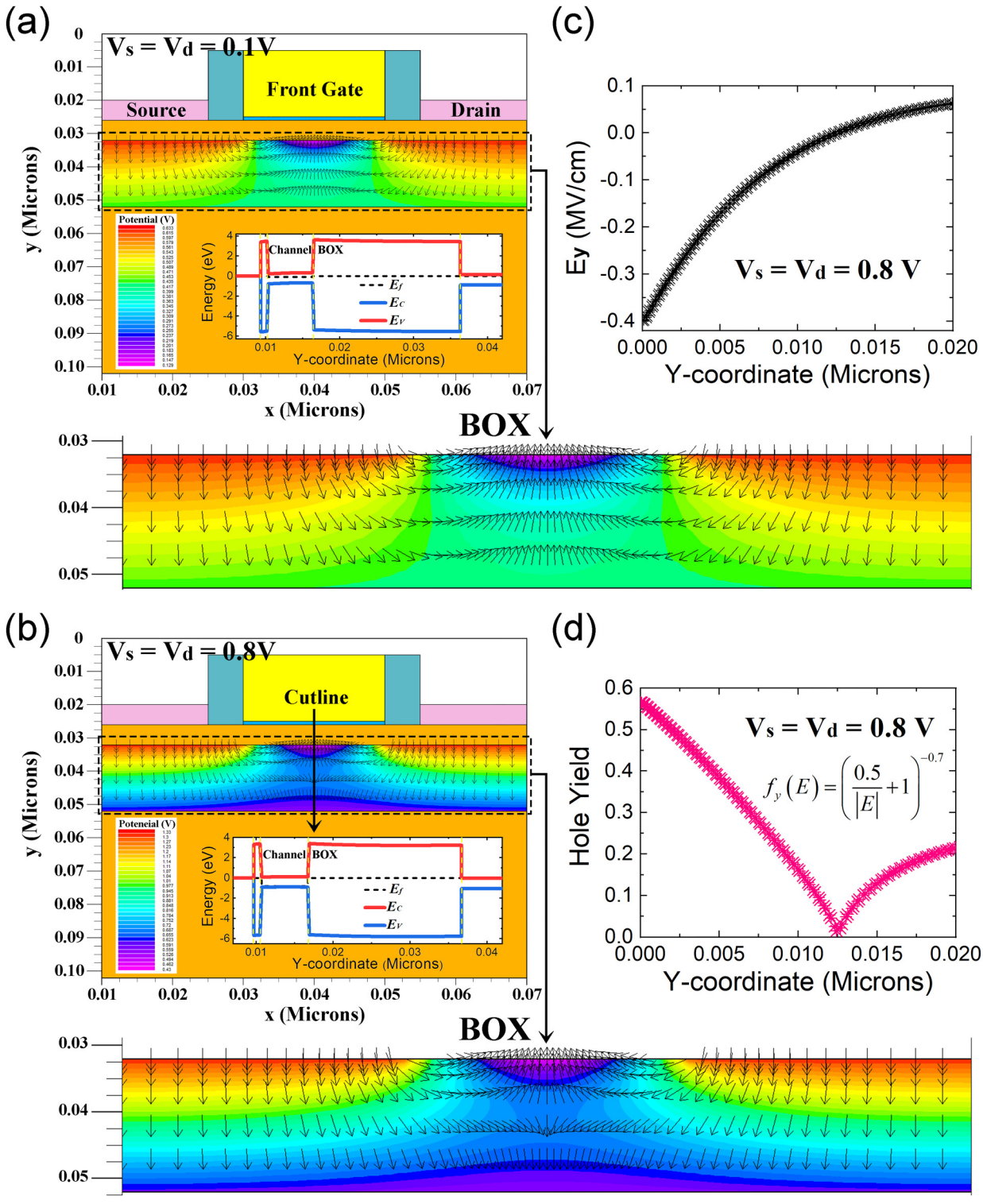

FIG. 3. Electric potential contours and field lines within the BOX layer under bias conditions of (a) $V_s = V_d = 0.1$ V and (b) $V_s = V_d = 0.8$ V with insets displaying simulated energy band diagrams along the cutline. (c) Vertical electric field component (E_y) along the cutline under a TG bias. (d) Hole yield (f_y) along the cutline under a TG bias.

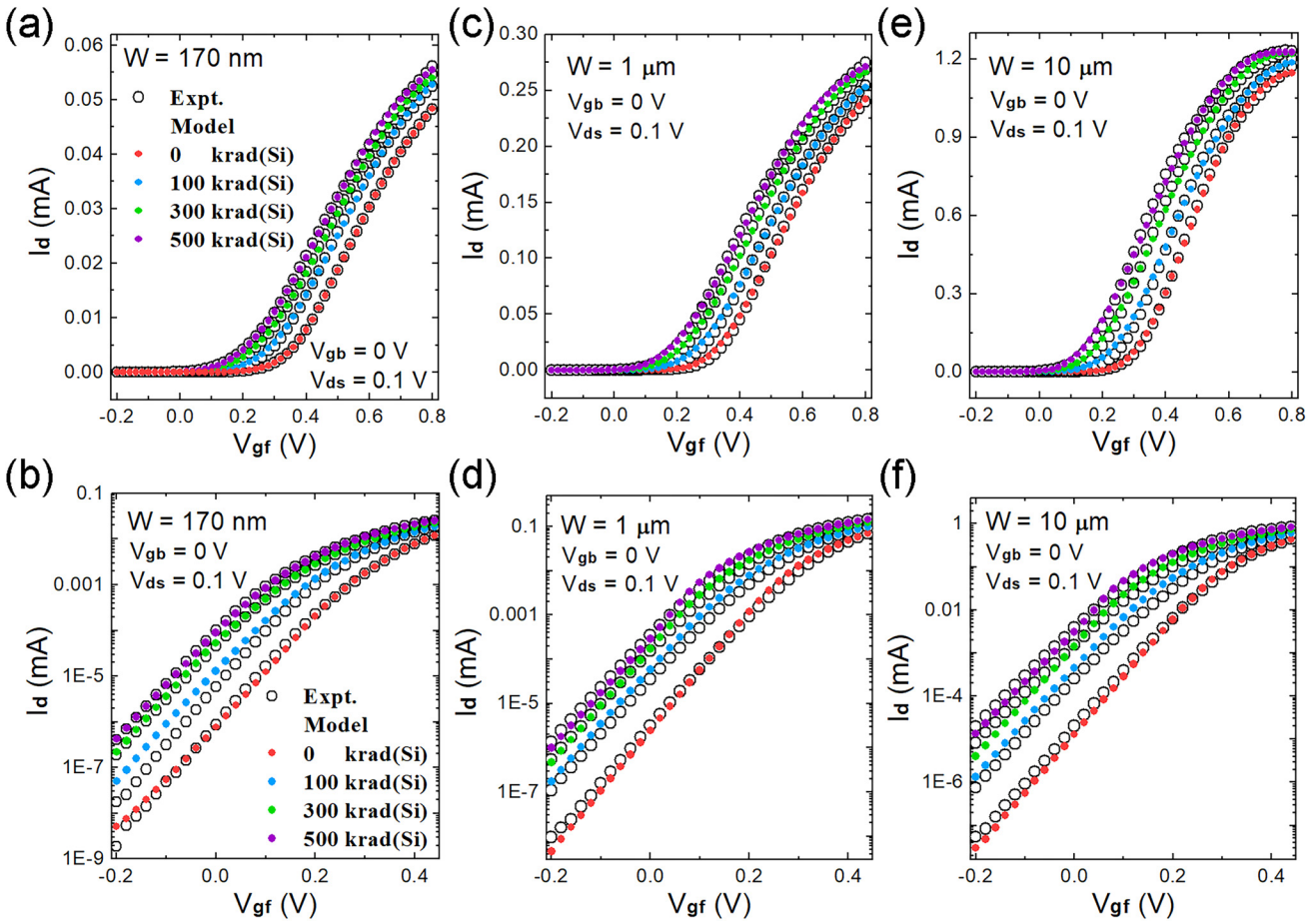

FIG. 4. Comparisons of I_d–V_{gf} characteristics between model predictions and experimental measurements at different radiation doses for n-type UTBB FDSOI MOSFETs. (a) and (b) $L = 20$ nm, $W = 170$ nm. (c) and (d) $L = 20$ nm, $W = 1\,\mu$m. (e) and (f) $L = 20$ nm, $W = 10\,\mu$m. (b), (d), and (f) depict the subthreshold region of I_d–V_{gf} characteristics on a logarithmic scale.

Figure 5(b) depicts the variations of the threshold voltage (V_{th}) with the radiation dose (D) for three sets of devices, where V_{th} is obtained from the measured I_d–V_{gf} characteristics using the constant-current method. It is found that V_{th} fluctuates during irradiation, which embodies as a negative shift with the increasing radiation dose. As analyzed above, this negative shift is ascribed to the positive oxide trapped charges accumulated under the body region. Figures 5(c) and 5(e) illustrate that the densities of oxide

TABLE I. Extracted radiation-related model parameters for three sets of UTBB FDSOI MOSFETs with different channel widths.

Parameter	$W = 170$ nm	$W = 1\,\mu$m	$W = 10\,\mu$m
Hole yield (f_y)	0.34	0.32	0.28
Saturation density of oxide traps ($N_{bot,sat}$)	2.59×10^{16} m^{-2}	3.32×10^{16} m^{-2}	7.44×10^{16} m^{-2}
Saturation density of back interface traps per volt ($D_{bit,sat}$)	5.04×10^{16} m^{-2} V^{-1}	8.41×10^{16} m^{-2} V^{-1}	4.53×10^{17} m^{-2} V^{-1}
Proportionality coefficient with respect to hole capture (K_{bot})	0.44	0.47	0.45
Proportionality coefficient with respect to proton release (K_{bit})	0.89	0.95	0.94
Parameter characterizing the effect of oxide trapped charges on back-channel mobility degradation (α_{bot})	1.85×10^{-16} m^2	4.95×10^{-16} m^2	7.20×10^{-16} m^2
Parameter characterizing the effect of interface trapped charges on back-channel mobility degradation (α_{bit})	1.78×10^{-15} m^2	4.93×10^{-15} m^2	6.49×10^{-15} m^2

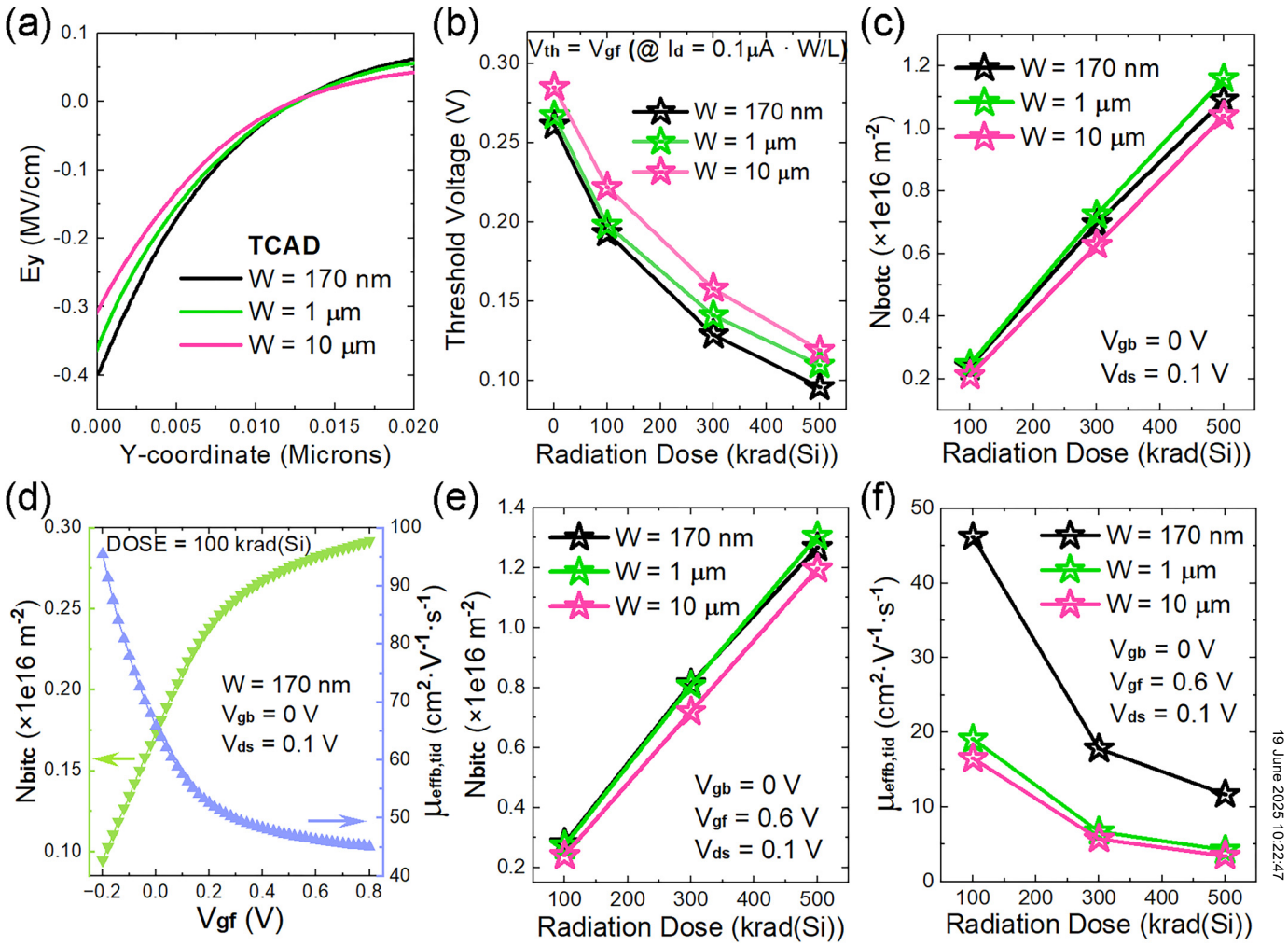

FIG. 5. (a) Vertical electric field component (E_y) along the cutline under a TG bias for three sets of UTBB FDSOI MOSFETs with $W = 170$ nm, 1 μm, and 10 μm. (b) Threshold voltage (V_{th}) vs radiation dose (D) for the three sets of devices. (c) Oxide trapped charge density (N_{botc}) vs D for the three sets of devices. (d) Interface trapped charge density (N_{bitc}) and effective back-channel mobility ($\mu_{effb,tid}$) vs a front-gate bias (V_{gf}) for devices with $W = 170$ nm. (e) N_{bitc} vs D for the three sets of devices. (f) $\mu_{effb,tid}$ vs D for the three sets of devices.

trapped charges (N_{botc}) and interface trapped charges (N_{bitc}) increase with the radiation dose, while maintaining comparable values across devices with varying channel widths. This suggests that widening the channel has a negligible impact on the charge density but increases the total number of trapped charges due to the expanded device area. Notably, more oxide trapped charges exacerbate the negative shift of V_{th}, whereas more interface trapped charges counteract this trend, explaining the similar variation trends of V_{th} with D across the three sets of devices shown in Fig. 5(b). As derived from (3), N_{bitc} is proportional to the back surface potential (ψ_{sb}), which is modulated by the front-gate bias (V_{gf}), as depicted in Fig. 5(d). The increase in N_{bitc} consequently reduces the effective back-channel mobility ($\mu_{effb,tid}$), which is consistent with the aggravated mobility degradation observed at higher radiation doses in Fig. 5(f). Furthermore, devices with narrower channels exhibit higher back-channel mobility, which is attributed to reduced Coulomb scattering from interface traps and suppressed surface roughness scattering. In contrast, devices with wider channels exhibit enhanced carrier interactions with interfacial traps near the channel edges, leading to pronounced mobility degradation. This underscores the complex interplay between geometric scaling and radiation-induced performance deterioration.

One of the most intuitive and detrimental effects induced by gamma-ray irradiation is that NMOS fails to turn off at the nominal voltage, coupled with an undesirable increase in static power consumption. In this case, applying a negative back-gate bias (V_{gb}) is proven as an effective TID hardening strategy.[27,28] Figures 6(a) and 6(b) display the measured I_d–V_{gf} characteristics

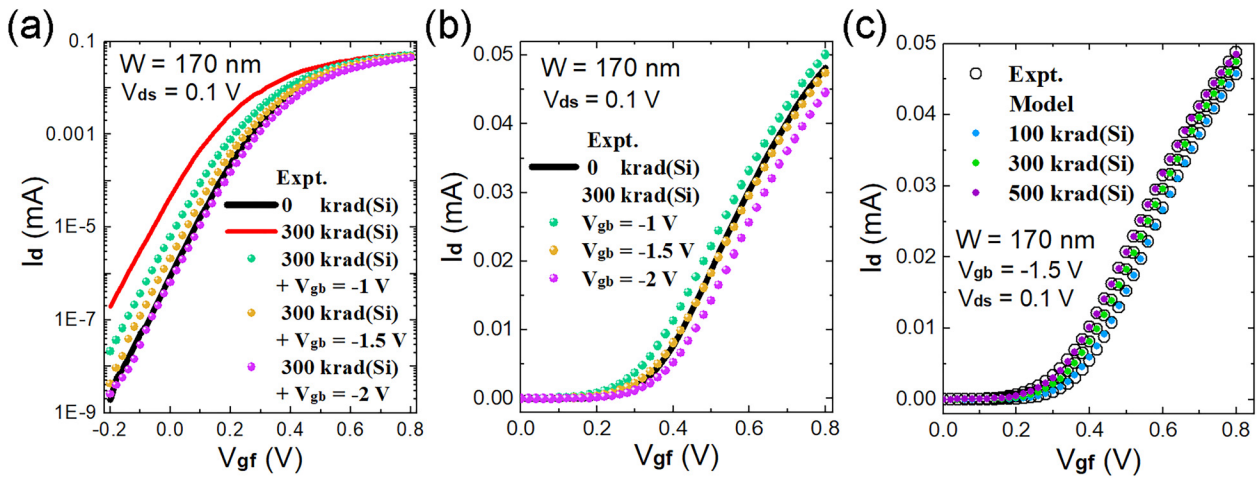

FIG. 6. (a) Measured I_d–V_{gf} characteristics for an UTBB FDSOI MOSFET prior to irradiation and after irradiation up to 300 krad(Si) with different back-gate biases, plotted on a logarithmic scale. (b) Same I_d–V_{gf} characteristics as in (a), plotted on a linear scale. (c) Comparison of I_d–V_{gf} characteristics between model predictions and experimental measurements at different radiation doses with a fixed back-gate bias of −1.5 V.

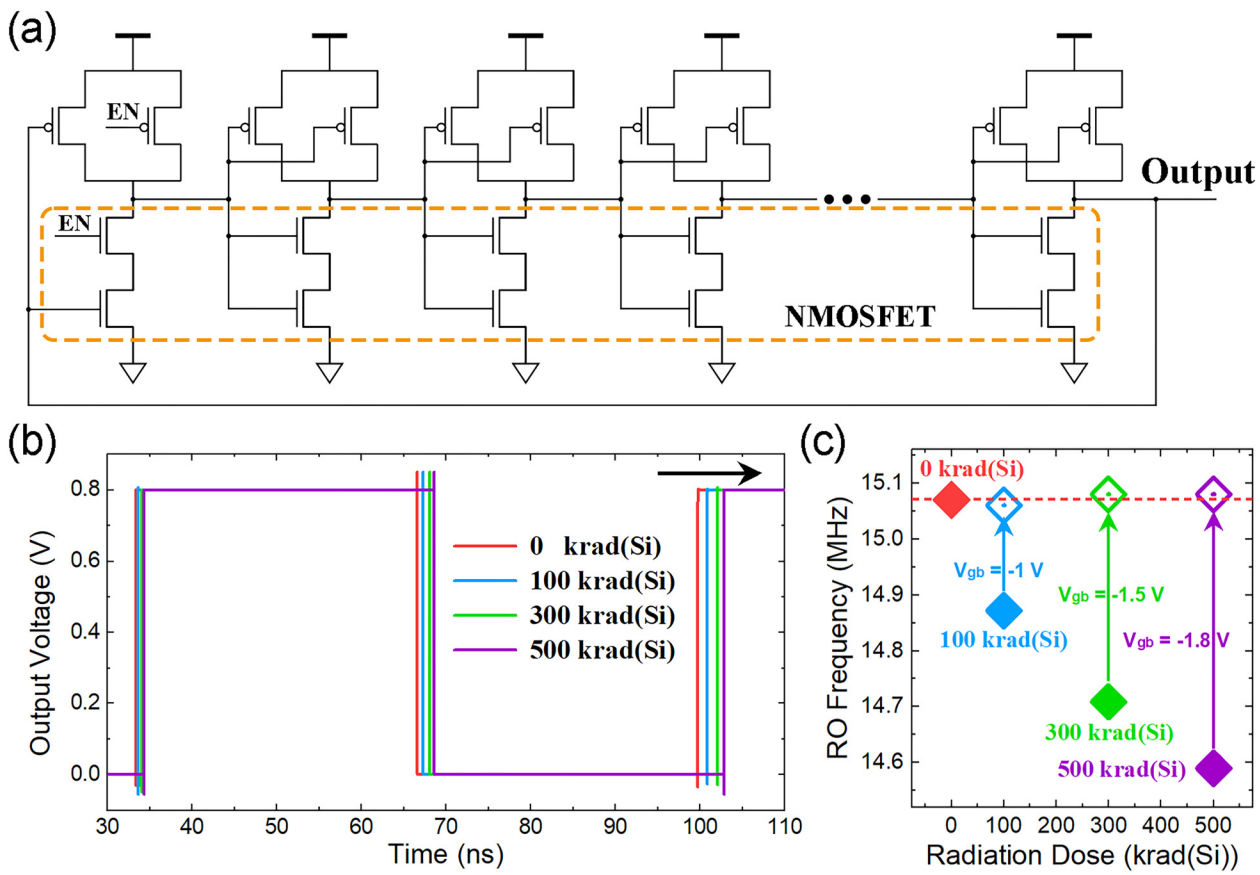

FIG. 7. (a) Schematic of a ring oscillator circuit. (b) Output waveforms of the ring oscillator circuit at varying radiation doses. (c) Oscillating frequency vs radiation dose: solid diamonds represent simulated results without applying back-gate biasing, while hollow diamonds indicate the effect of back-gate biasing in mitigating frequency reduction.

for a UTBB FDSOI MOSFET prior to irradiation and after irradiation up to 300 krad(Si) with different back-gate biases ($V_{gb} = 0$, -1, -1.5, and -2 V). It is observed that a V_{gb} of -1.5 V effectively restores the pre-radiation electrical characteristics of the UTBB FDSOI MOSFET. As shown in Fig. 6(c), the negative shift trend of I_d–V_{gf} characteristics with the increasing W is significantly inhibited with $V_{gb} = -1.5$ V compared to that with $V_{gb} = 0$. By fitting the experimental data with our model, it is revealed that the values of K_{bot} and K_{bit} drop from 0.44 to 0.35 and 0.89 to 0.86 with $V_{gb} = -1.5$ V, respectively. The reduction in K_{bot} suggests that fewer holes are captured by oxide traps near the back interface of the channel, leading to fewer protons being released and, thus, a decrease in K_{bit}. Notably, values of $N_{\text{bot,sat}}$ and $D_{\text{bit,sat}}$ remain unchanged.

V. CIRCUIT SIMULATION

TID effects pose significant challenges for electronic circuits operating in radiation-intensive environments. Therefore, this work evaluates the impact of TID effects at the circuit level, extending device-level analyses to practical circuit performance. Figure 7(a) depicts the schematic of a ring oscillator (RO) circuit implemented in 22 nm FDSOI technology. The RO circuit consists of a trigger NAND gate and an even number of cascaded NAND gates, forming a closed-loop configuration. The trigger NAND gate with enabled inputs allows control over oscillation, while subsequent NAND gates serve as inverting stages. To evaluate TID effects on circuit performance, the BSIM-IMG compact model, incorporating radiation-related parameters from Table I, is employed within the Spectre simulator. Notably, this work systematically investigates TID effects on NMOSFET characteristics and their impact on RO circuit performance. The adoption of NAND-based architecture emphasizes the role of NMOSFETs, each featuring a channel width of 170 nm.

Simulation results indicate that the oscillating frequency is 15 MHz at 0 krad(Si), which decreases with increasing radiation dose. This trend is consistent with prior works.[4,29,30] At 500 krad (Si), a maximum frequency reduction of 3.2% is observed, as shown in Fig. 7(c). This frequency reduction originates from TID-induced leakage current elevation in NMOSFETs, which subsequently prolongs propagation delays in the NAND gates. To mitigate TID-induced frequency degradation, a dynamic back-gate bias (V_{gb}) adjustment is adopted. This strategy leverages the inherent coupling between front and back gates in FDSOI technology, allowing precise control over transistor characteristics. By adjusting V_{gb}, the RO circuit maintains stable performance across varying radiation doses. Figure 7(c) demonstrates that an appropriate V_{gb} could restore the oscillating frequency to its pre-irradiation level, effectively counteracting TID effects. The feasibility of back-gate biasing to mitigate TID effects in the RO circuit underscores its potential as a circuit-level solution for radiation-hardened designs.

VI. CONCLUSION

This work systematically investigates the vulnerability of UTBB FDSOI MOSFETs to TID effects. A novel TID effect model is developed to quantify radiation-induced trapped charge density, linking it to cumulative dose and bias condition. By incorporating this model into the BSIM-IMG compact model, an analytical drain current expression incorporating TID effects is established, enabling direct evaluation of radiation impacts on device behavior. Experimental validation through current–voltage measurements across varying radiation doses confirms the model's accuracy, while extracted radiation-related parameters offer a pathway to predict circuit-level performance degradation in irradiated environments. This work bridges the gap between device-level TID characterization and circuit reliability assessment, providing a foundational tool for radiation-hardened FDSOI circuit design in aerospace, nuclear, and high-reliability applications.

ACKNOWLEDGMENTS

The authors acknowledge the support of the fund of the Innovation Center of Radiation Application under Grant No. KFZC2021010202.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Lili Zhang: Conceptualization (lead); Data curation (equal); Methodology (lead); Software (equal); Writing – original draft (lead); Writing – review & editing (equal). **Tao Wang:** Software (equal). **Yanan Yin:** Data curation (equal). **Lei Dong:** Software (equal). **Xinjie Zhou:** Funding acquisition (equal); Project administration (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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